Application Report
SBAA431–March 2020

ADS1018-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for ADS1018-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

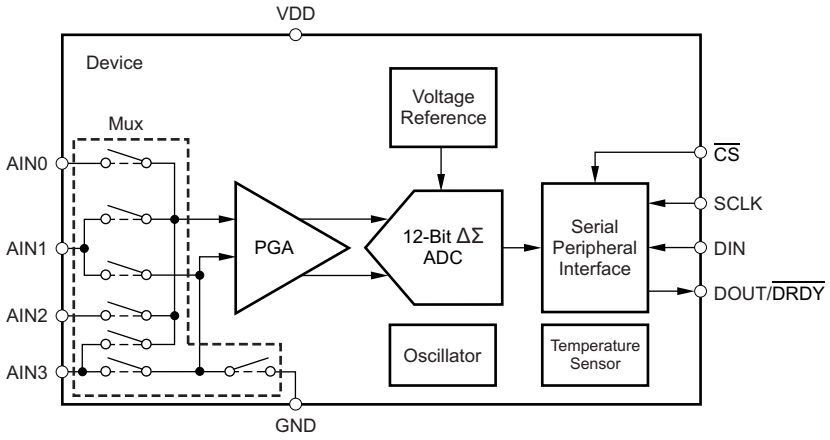

Figure 1. Functional Block Diagram

ADS1018-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for ADS1018-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.0 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ADS1018-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Channel-channel short	10%
Incorrect channel selected	15%
ADC output code bit error	15%
ADC gain out of specification	20%
ADC offset out of specification	20%
Communication error	20%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ADS1018-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VDD (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the ADS1018-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the ADS1018-Q1 datasheet.

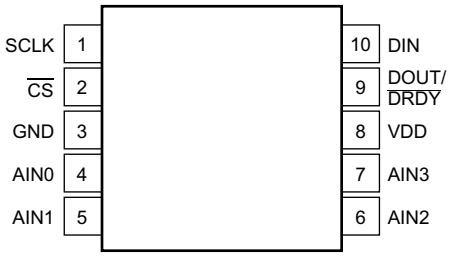

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pull-up resistor on $\overline{CS}$ to VDD.
- RC filters on every analog input, AINx.
  Series resistors are sized to limit the input currents into the analog inputs to <10mA in all circumstances, e.g. also in case device is unpowered and input signal is applied.
- Device is the only slave on the SPI bus.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	1	SCLK stuck low. No SPI communication with device possible.	B
$\overline{CS}$	2	$\overline{CS}$ stuck low. Normal operation. SPI communication still functional. However SPI of device cannot be actively reset anymore by taking $\overline{CS}$ high and low again.	C
GND	3	No effect. Normal operation.	D
AIN0	4	AIN0 stuck low. Conversion results for multiplexer channel combinations using AIN0 corrupted, unless AIN0 is tied to GND anyway.	B
AIN1	5	AIN1 stuck low. Conversion results for multiplexer channel combinations using AIN1 corrupted, unless AIN1 is tied to GND anyway.	B
AIN2	6	AIN2 stuck low. Conversion results for multiplexer channel combinations using AIN2 corrupted, unless AIN2 is tied to GND anyway.	B
AIN3	7	AIN3 stuck low. Conversion results for multiplexer channel combinations using AIN3 corrupted, unless AIN3 is tied to GND anyway.	B
VDD	8	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DOUT/$\overline{DRDY}$	9	DOUT/$\overline{DRDY}$ stuck low. No SPI communication back to SPI master possible. No data ready indication possible. Increase in supply current when DOUT/$\overline{DRDY}$ tries to drive high. Device damage plausible if DOUT/$\overline{DRDY}$ drives high for extended period of time.	A
DIN	10	DIN stuck low. No SPI communication with device possible.	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	1	State of SCLK input undetermined. No SPI communication with device possible.	B
$\overline{CS}$	2	State of $\overline{CS}$ input undetermined. SPI communication corrupted.	B
GND	3	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
AIN0	4	State of AIN0 input undetermined. Conversion results for multiplexer channel combinations using AIN0 undetermined.	B
AIN1	5	State of AIN1 input undetermined. Conversion results for multiplexer channel combinations using AIN1 undetermined.	B
AIN2	6	State of AIN2 input undetermined. Conversion results for multiplexer channel combinations using AIN2 undetermined.	B
AIN3	7	State of AIN3 input undetermined. Conversion results for multiplexer channel combinations using AIN3 undetermined.	B
VDD	8	Device functionality undetermined. Device unpowered if all external analog and digital pins are held low. Device may power up through internal ESD diodes to VDD if voltages above the device's power-on reset threshold are present on any of the analog or digital pins.	B
DOUT/$\overline{DRDY}$	9	State of DOUT/$\overline{DRDY}$ output undetermined. No SPI communication back to SPI master possible. No data ready indication possible.	B
DIN	10	State of DIN input undetermined. No SPI communication with device possible.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	1	$\overline{CS}$	SPI communication corrupted. No SPI communication with device possible.	B
$\overline{CS}$	2	GND	$\overline{CS}$ stuck low. Normal operation. SPI communication still functional. However SPI of device cannot be actively reset anymore by taking $\overline{CS}$ high and low again.	C
GND	3	AIN0	AIN0 stuck low. Conversion results for multiplexer channel combinations using AIN0 corrupted, unless AIN0 is tied to GND anyway.	B
AIN0	4	AIN1	Conversion results for multiplexer channel combinations using AIN0 or AIN1 undetermined.	B
AIN1	5	AIN2	Not considered. Corner pin.	D
AIN2	6	AIN3	Conversion results for multiplexer channel combinations using AIN2 or AIN3 undetermined.	B
AIN3	7	VDD	AIN3 stuck high. Conversion results for multiplexer channel combinations using AIN3 corrupted, unless AIN3 is tied to VDD anyway.	B
VDD	8	DOUT/$\overline{DRDY}$	DOUT/$\overline{DRDY}$ stuck high. No SPI communication back to SPI master possible. No data ready indication possible. Increase in supply current when DOUT/$\overline{DRDY}$ tries to drive low. Device damage plausible if DOUT/$\overline{DRDY}$ drives low for extended period of time.	A
DOUT/$\overline{DRDY}$	9	DIN	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DOUT/$\overline{DRDY}$ tries to drive low while DIN drives high or vice versa. Device damage plausible if this condition exists for extended period of time.	A
DIN	10	SCLK	Not considered. Corner pin.	D

Table 8. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	1	SCLK stuck high. No SPI communication with device possible.	B
$\overline{CS}$	2	$\overline{CS}$ stuck high. No SPI communication with device possible.	B
GND	3	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AIN0	4	AIN0 stuck high. Conversion results for multiplexer channel combinations using AIN0 corrupted, unless AIN0 is tied to VDD anyway.	B
AIN1	5	AIN1 stuck high. Conversion results for multiplexer channel combinations using AIN1 corrupted, unless AIN1 is tied to VDD anyway.	B
AIN2	6	AIN2 stuck high. Conversion results for multiplexer channel combinations using AIN2 corrupted, unless AIN2 is tied to VDD anyway.	B
AIN3	7	AIN3 stuck high. Conversion results for multiplexer channel combinations using AIN3 corrupted, unless AIN3 is tied to VDD anyway.	B
VDD	8	No effect. Normal operation.	D
DOUT/$\overline{DRDY}$	9	DOUT/$\overline{DRDY}$ stuck high. No SPI communication back to SPI master possible. No data ready indication possible. Increase in supply current when DOUT/$\overline{DRDY}$ tries to drive low. Device damage plausible if DOUT/$\overline{DRDY}$ drives low for extended period of time.	A
DIN	10	DIN stuck high. No SPI communication with device possible.	B

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