Application Report

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Data Converters for Industrial Power Measurements

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ABSTRACT

Sources of noise generation are pervasive in contemporary industrial applications. Unwanted noise presents one of the major problems in measuring power or protecting circuits in such an environment. Knowing the characteristics and understanding the behavior of noise sources are valuable to designers and users of electronic circuits. This application report discusses both of these topics. The first part of this report defines some fundamental concepts of electronic noise; the latter portion addresses the selection and design of filters used in conjunction with analog-to-digital converters (ADCs). A design example for measuring voltage and current with dedicated transformers, using the ADS8364, is provided along with equations and experimental results.

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1 Types of Noise

Noise in electronic circuits is most frequently caused by electromagnetic interference (EMI), radio frequency interference (RFI), and ground loops.

In terms of ac power, common-mode noise is the noise signal between the neutral and the ground conductor. This type of signal interference differs from normal-mode (or differential) noise, which is referenced from the line (hot) and the neutral conductor.

Common-mode noise impulses tend to be higher in frequency than the associated normal-mode noise signal. This characteristic is to be expected, since the majority of common-mode signals originate from capacitive-coupled normal-mode signals. More coupling among the line, conductors, neutral and ground occur as operating frequency increases. Electronic equipment is 10 to 100 times more sensitive to common-mode noise than it is to normal-mode noise.

The amount of noise present on the power line can be surprising at any given time. The source of this noise typically arises from the electrical distribution system external to the building as well as the distribution system within the building. The noise itself is the result of the power line's dynamic nature because of the ever-changing loads carried on the line. Figure 1 shows the typical noise found on a power line.

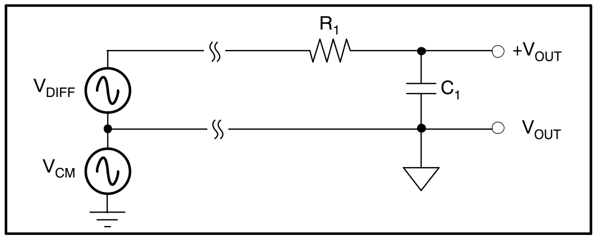

Figure 1. Typical Noise Sources

Conventional power transformers and isolation transformers will not block normal-mode noise impulses. However, if the secondaries of these transformers steer the neutral bonded to ground, they will convert normal-mode noise to common-mode. From the standpoint of microelectronic circuits, common-mode noise is potentially more harmful than normal-mode.

In a data acquisition system (such as power measurement), noise effects can be reduced by taking advantage of an ADC with differential inputs. Balancing the impedances allows one to convert noise sources into common-mode signals that can be rejected by an ADC with differential inputs.

Differential signals are more suitable for use in most industrial applications. Common-mode noise is dramatically reduced, if not completely eliminated, when measuring differential signals. For industrial or high-noise environment applications, several Burr-Brown products from Texas Instruments are intended to give designers maximum advantage by using fully-differential signal paths.

2 Noise Filter Design for Differential Signals

One such ADC specifically designed for applications in a noisy environment is the ADS8364. The input signal is ±2.5V around 2.5V. In industrial power metering, for example, the output of the voltage measurement transformer is typically ±10V. Before applying the meter outputs to the ADC, the signal needs to be scaled and offset to fit the differential input range of the converter.

The resistors R_{2A} and R_{2B} from Figure 2 will offset the output signal from the transformer Tr_1 around the reference voltage (V_{REF}) of the ADC. The resistor network of R_{1A} and R_{2A}, along with R_{1B} and R_{2B}, will scale the differential input signal to the full-scale range (FSR) of the ADC. The scaling factor or gain of this resistor network is presented in Equation 1. To have this circuit work properly, resistors R_{1A} and R_{1B} must be equal in value; R_{2A} and R_{2B}, as well, must be of equal value. The attenuation of the differential and the common-mode signal is the same.

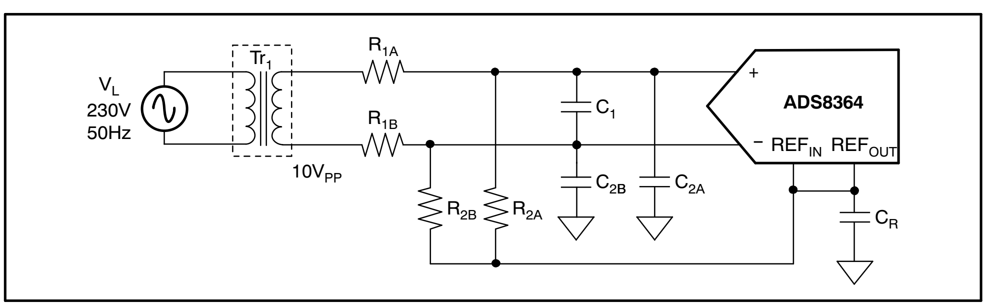

Figure 2. Typical Power Measurement Application Circuit (Differential Signal) of the ADS8364

$$G_{DIFF} = G_{CM} = \frac{R_{2A}}{R_{1A} + R_{2A}} = \frac{R_{2B}}{R_{1B} + R_{2B}} \tag{1}$$

The resistors R_{1A} and R_{1B} need to have a high enough impedance to avoid loading the signal source. They also provide additional input-overload protection, isolating the ADC input from extreme external signal sources.

The next step is to implement a low-pass filter, to filter the noise from the differential signal applied to the ADC. Adding capacitor C_1 between the (+) and (–) inputs of the ADC will create the differential filter.

Finally, the common-mode signal that occurs is first attenuated by the resistor divider, then further attenuated by the implemented RC filter. The cutoff frequency of the common-mode signal can be calculated by Equation 2.

$$BW_{CM} = \frac{1}{2 \cdot \pi \cdot \frac{R_{1A} \cdot R_{2A}}{R_{1A} + R_{2A}} \cdot C_{2A}} = \frac{1}{2 \cdot \pi \cdot \frac{R_{1B} \cdot R_{2B}}{R_{1B} + R_{2B}} \cdot C_{2B}} \tag{2}$$

The –3dB differential bandwidth of this filter can be expressed by Equation 3.

$$BW_{DIFF} = \frac{1}{2 \cdot \pi \cdot \frac{2 \cdot R_{1A} \cdot R_{2A}}{R_{1A} + R_{2A}} \cdot \left(C_1 + \frac{C_{2A}}{2}\right)} \tag{3}$$

Any mismatch between the time constants of corresponding common-mode filters will unbalance the input bridge and reduce high-frequency common-mode rejection. Capacitor C_1 connected across the bridge output effectively reduces any ac common-mode rejection errors from component mismatch.

For example, making C_1 ten times larger than C_{2A} or C_{2B} provides a 20x reduction in the common-mode rejection error arising from a C_{2A}/C_{2B} mismatch. Figure 3 shows the frequency response of the differential filter and mismatched common-mode filters. From the previous example, the differential filter had an attenuation of –26dB for the cutoff frequency of the first common-mode filter. The difference in the –3dB bandwidth between these two common-mode filters, which is presented as a differential signal, will be attenuated by –26dB.

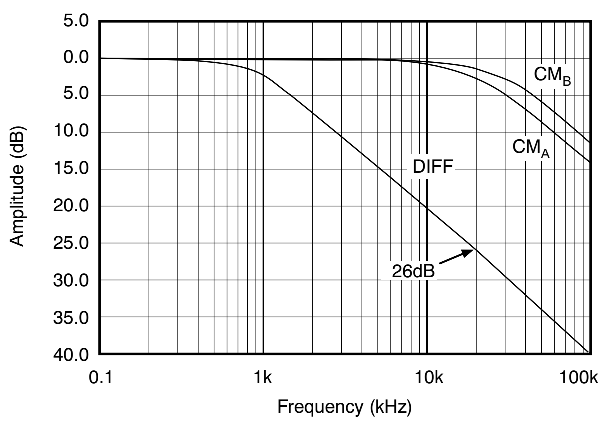

Figure 3. Frequency Response of the Equivalent Differential and Common-Mode Filters

3 Noise Filter Design for Single-Ended Signals

In cases where the common-mode noise is not a concern, the differential signal is replaced with a single-ended signal. In this configuration, one side of the transformer is tied to ground. Another side acts as a signal source. As in the previous example, the output signal from the transformer is ±10V and needs to be scaled to match the differential input of the ADS8364. The resistor network from Figure 4 will scale the input signal and offset so that the full-scale range (FSR) will be from 0V to 5V.

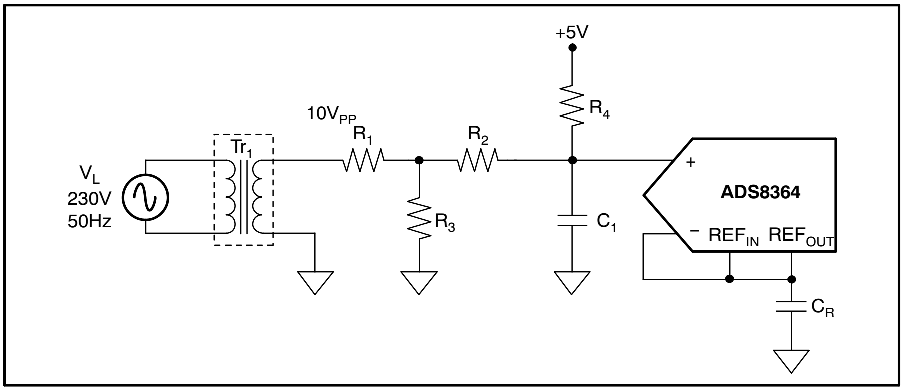

Figure 4. Typical Power Measurement Application Circuit (Single-Ended Signal) of the ADS8364

The resistor network of R_1, R_2, R_3 and R_4 will scale the single-ended input signal to the FSR of the ADC. The scaling factor (or gain) of this resistor network must be the same as in the previous example. In order to have this circuit work properly, resistors R_1, R_3 and R_4 must be equal and each have twice the value of resistor R_2.

The next step is to implement a low-pass filter, in order to filter the noise from the single-ended signal applied to the ADC. Adding capacitor C_1 between the (+) input and the ground of the ADC creates the filter.

4 Measurement Results

Measurements were made with the ADS8364 operating with a clock of 3.8MHz. The sampling rate was 38kHz. These conditions resulted in a conversion time of 4.47µs and an acquisition time of 21.84µs. In the case of the differential signal, the choice of resistor values for R_{1A} and R_{1B} was 4kΩ, and 1.3kΩ for R_{2A} and R_{2B}. These resistor values provide a gain of 0.245. For the transformer output voltage of ±10V, the full-scale ADC input is 4.9V. The value of capacitor C_1 was changed from 0 to 3.3nF.

Keeping the operating conditions the same for the ADC as those of the single-ended signal, the resistor values for R_1, R_3 and R_4 were 6.48kΩ, and 3.24kΩ for R_2. These resistor values provide a gain of 0.25. For the transformer output voltage of ±10V, the full-scale ADC input will be 5V. The value of capacitor C_1 was changed from 0 to 1.8nF.

It is essential to realize that the input filter time constant, from equivalent R and C_1, must not exceed one-fifth of the ADC sampling time. For greater time constants, performance degradation can be expected.

Measurements were taken and the results were analyzed. Table 1 presents the measurement results for the differential signal. Figure 5 and Figure 6 present graphical representations of the measurement data from Table 1.

Table 1. Experimental Measurement Data for Differential Signal in Figure 2 2

Capacitor (nF)			AC Performance				Harmonics			
C_1	C_{2A}	C_{2B}	SNR	SINAD	SFDR	THD	3rd	5th	7th	9th
0.00	0.00	0.00	84.8	83.7	90.6	–90.0	–90.6	–102.3	–102.4	–114.1
0.56	0.00	0.00	85.3	84.8	98.2	–94.3	–98.2	–98.5	–101.0	–122.0
1.00	0.00	0.00	85.3	84.9	98.1	–94.8	–98.1	–99.8	–101.6	–122.8
1.20	0.00	0.00	85.5	85.0	98.4	–94.7	–98.7	–99.2	–101.1	–115.5
1.50	0.00	0.00	85.3	84.9	98.2	–95.4	–99.6	–99.7	–101.8	–124.3
1.80	0.00	0.00	85.3	85.0	98.1	–96.3	–101.4	–100.4	–102.4	–110.1
2.20	0.00	0.00	85.3	84.9	97.9	–95.6	–103.1	–100.1	–100.5	–105.1
3.30	0.00	0.00	84.2	81.8	88.4	–85.6	–88.4	–92.3	–93.8	–96.7
1.80	0.18	0.18	86.0	85.6	100.4	–96.2	–101.6	–100.4	–101.6	–113.8

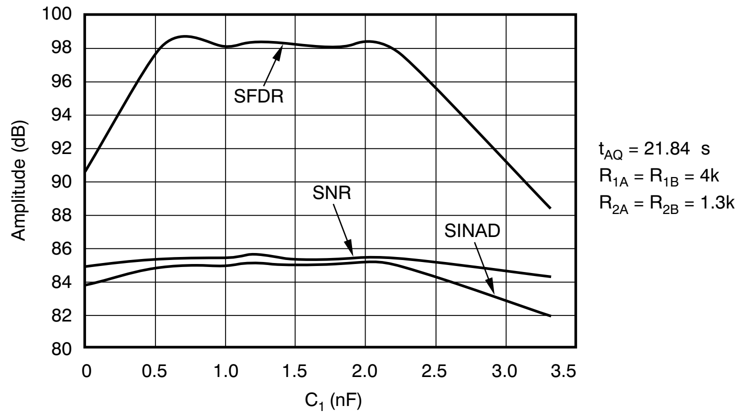

Figure 5. AC Performance Curves as Function of Filter Capacitor C_1 from Table 1

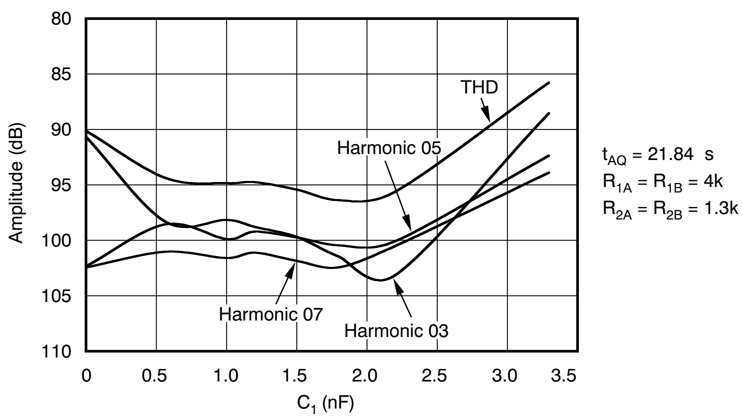

Figure 6. THD and Harmonics as Function of Filter Capacitor C_1 from Table 1

After preliminary measurement, capacitors C_{2A} and C_{2B} were added. The lowest measured THD was for a value of C_1 around 2nF. Choosing 1.8nF for C_1 and 0.18nF for C_{2A} and C_{2B} will give an equivalent capacitance of 1.9nF.

Adding common-mode filter capacitors C_{2A} and C_{2B} will improve SNR. The FFT results of the final circuit are presented in Figure 7.

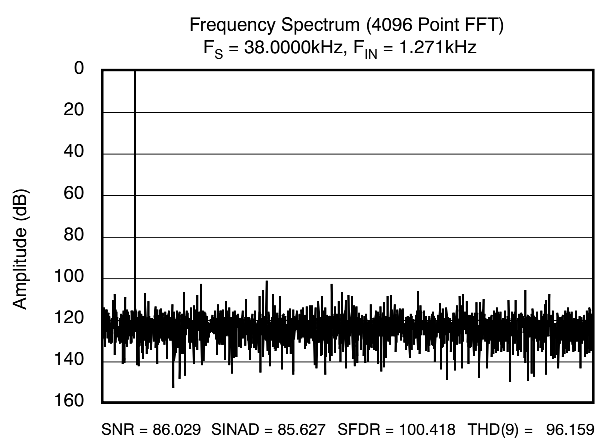

Figure 7. 4096 Point FFT of ADS8364 with Optimized Differential Input Filter Circuit from Figure 2 2

The same measurements are done using the schematic from Figure 4. Table 2 presents the measurement results for the single-ended signal. Figure 8 and Figure 9 present graphical representations of the measurement data from Table 2.

Table 2. Experimental Measurement Data for Single-Ended Signal in Figure 4 4

Capacitor (nF)	AC Performance				Harmonics			
C_1	SNR	SINAD	SFDR	THD	2nd	3rd	5th	7th
0.00	83.37	82.26	92.55	–88.74	–92.55	–108.11	–92.91	–97.49
0.15	85.67	84.67	95.93	–91.57	–95.93	–100.81	–96.42	–100.82
0.33	85.96	84.86	95.65	–91.35	–95.65	–100.10	–96.36	–100.65
0.51	85.77	84.66	95.57	–91.12	–95.57	–99.42	–96.50	–100.27
0.68	86.09	85.00	95.64	–91.51	–95.64	–100.33	–96.83	–100.60
0.82	86.36	85.27	95.78	–91.83	–95.78	–102.92	–97.05	–99.91
1.00	86.35	85.05	95.00	–90.92	–95.00	–98.98	–96.65	–99.95
1.20	85.69	82.97	90.56	–86.30	–92.31	–90.56	–93.09	–96.16
1.50	83.50	77.94	81.92	–79.35	–88.49	–81.92	–86.76	–89.76
1.80	81.04	74.34	77.72	–75.39	–85.42	–77.72	–83.00	–85.76

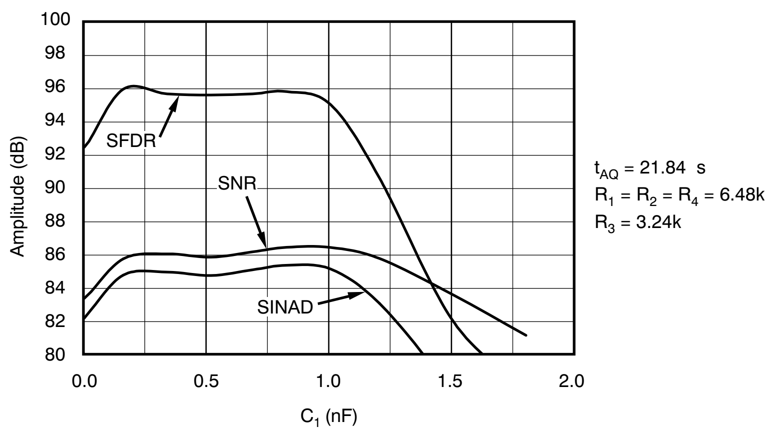

Figure 8. AC Performance Curves as Function of Filter Capacitor C_1 from Table 2

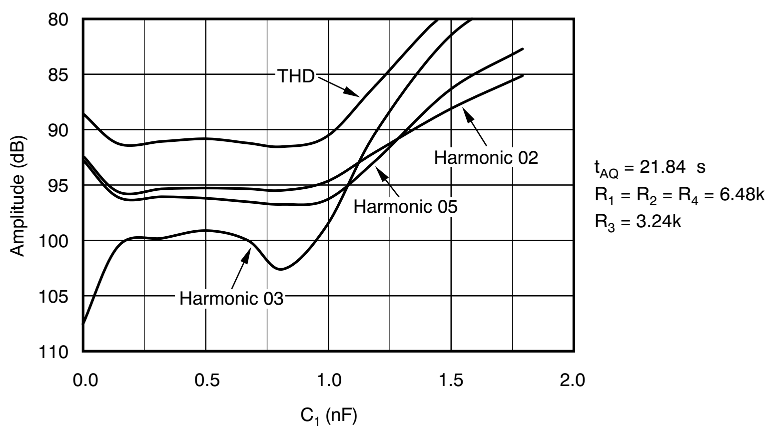

Figure 9. THD and Harmonics as Function of Filter Capacitor C_1 from Table 2

The FFT results of the single-ended circuit are presented in Figure 10.

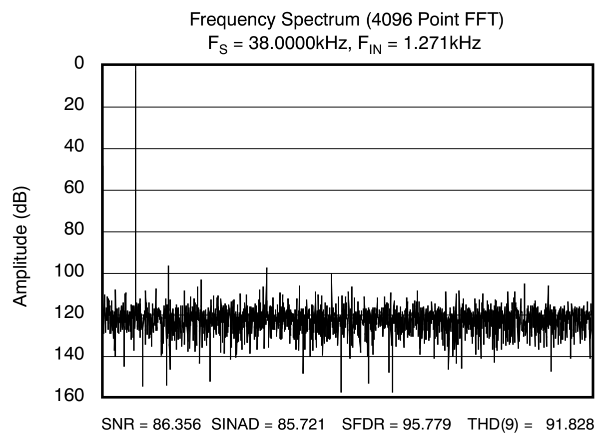

Figure 10. 4096 Point FFT of ADS8364 with Optimized Single-Ended Input Filter Circuit from Figure 2 2

5 Conclusion

The preceding analysis shows a simple and effective way to implement a high-performance ADC for industrial power measurement. Understanding noise sources and propagation through the measurement circuit is essential in determining the final design. Proper filtering will not only reduce harmful differential and common-mode noise; it will also permit the ADC to operate at its maximum performance. After choosing an input resistor divider that will properly scale and offset the input signal (as well as protect the input of the ADC), it is necessary to make several measurements with different capacitors. These capacitors will reduce input bandwidth of the ADC, increasing the SNR performance and the effective number of bits. The value of these capacitors is directly proportional to the value of the input resistors as well as to the sampling time of the ADC. This application report shows that an ADC operating with relatively high source impedance and a properly designed differential filter can provide measurements with an SFDR greater than 98dB as well as THD better than –96dB with SNR over 85dB.