Application Report
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Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN

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ABSTRACT

Gallium Nitride (GaN) FETs are providing designers with a viable alternative to Si MOSFETs in high power density applications. This is due to their significant advantages over Si, including small junction capacitance, lack of body diode, and no reverse recovery loss. These advantages enable more efficient and compact power converter designs, driven by a higher switching frequency. Nowadays, the major commercial GaN FETs are lateral high-electron-mobility transistors (HEMT). Without the p-n-doping drift region in the structure, GaN illustrates unique characteristics in the third quadrant operation. This application report provides a detailed explanation of the diode-like behavior of GaN in reverse current conduction, based on the study on its lateral structure. The third quadrant operation naturally happens when GaN is applied as rectifiers. This application report also shows how to minimize the third quadrant loss of GaN FETs used as rectifiers by leveraging a short dead time or adaptive dead time control.

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Trademarks

1 Introduction

GaN is enabling higher power density and higher efficiency power converters. In contrast to Si MOSFETs, GaN offers faster switching speed, smaller output charge, and lower switching losses. Unlike a MOSFET, there is no p-n junction within the lateral structure of a GaN FET and no body-diode and no reverse recovery charge (Q_{rr}). By eliminating the reverse recovery losses, GaN enables efficient high switching frequency operation in the hard-switched topologies. For example, in the bridgeless totem-pole power factor correction (PFC) under continuous conduction mode (CCM), using superjunction MOSFETs are not

practical due to their high reverse recovery losses. As shown in Figure 1, by using GaN FETs as the high-frequency switches, the reverse recovery loss is fully eliminated and the switching-related loss is significantly reduced. The inverter for AC drive is another beneficial topology, where the low switching loss and lack of reverse recovery loss downsize the heat sink in the compact servo drives and integrated motor drives.

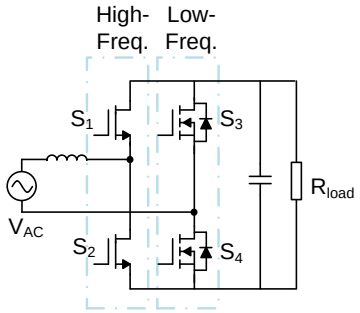

Figure 1. Bridgeless Totem-Pole PFC Using GaN as the High-Frequency Switching and Si MOSFET as the Rectifier

Third quadrant operation occurs for a power MOSFET when the current flows from the source to the drain terminal through the body diode or the channel. Although GaN FETs have no body diode, the symmetry of the device helps conduct in the third quadrant with diode-like behavior. Similar to the situation with the Si MOSFET, it is recommended not to add an antiparallel diode with the GaN FET to conduct the reverse current. Adding an antiparallel diode adds output capacitance to the switch node and increases switching losses. Instead, the third quadrant losses can be minimized by optimizing the dead time.

2 Mechanism of Reverse Conduction in GaN FETs

The lateral GaN structure is comprised of a Source and Drain connected by a two-dimensional electron gas (2DEG) channel. The gate voltage controls the conductivity of the channel. Figure 2 shows the simplified cross-section of the lateral GaN structure, illustrating the symmetry of the channel region between the source and the drain. In third quadrant operation, the drain and the source switch positions. The drain potential is lower than the gate turning on the GaN device and allows the reverse conduction without a body diode.

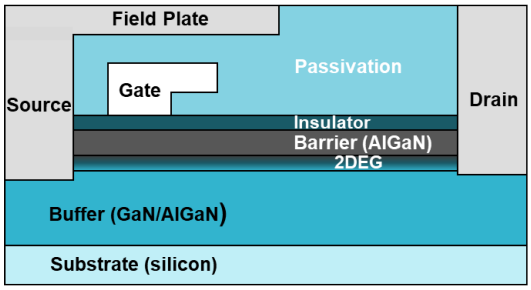

Figure 2. Cross Section of the Lateral Structure of GaN FETs

The condition to turn on the channel in the forward conduction (the drain to the source) is that the gate-to-source voltage, V_{gs}, is higher than the threshold voltage V_{th}, as Figure 3 illustrates. With the channel on, V_{ds} can be calculated using Equation 1.

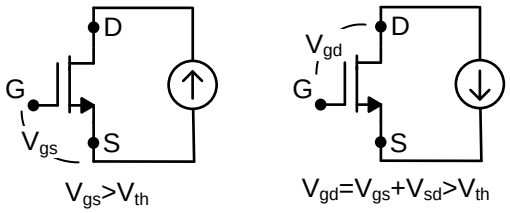

Figure 3. Conditions to Turn on the Channel in the Forward and Reverse Conduction

$V_{ds} = I_{ds}R_{on}$

where

- R_{on} is the on-resistance of the channel in the first quadrant (1)

When V_{gs} is smaller than V_{th}, the current cannot conduct in the first quadrant, but can flow in the third quadrant. When the current flows in the reverse direction (third quadrant), the drain and source terminal can swap termination. The condition to turn on the channel for reverse conduction is the gate-to-drain voltage V_{gd} is higher than the threshold voltage, V_{th}. Like a diode, the channel in GaN FET self-commutates and V_{sd} is self-biased so that V_{gd} can reach V_{th} and the channel conducts the reverse current. Under this operation, V_{sd} is biased by V_{th}- V_{gs} and increases with the reverse current, I_{sd} as Equation 2 illustrates. In Equation 2, $R_{on\_reverse}$, the equivalent on-resistance in the third quadrant with the off gate is dependent on I_{sd} as the device operates in the saturation region. It is recommended to refer to IV-curve in the datasheet to estimate V_{sd} in the third quadrant. When the gate is on during reverse conduction, V_{gd}, equals to (V_{gs} + V_{sd}), which is higher than V_{th}, enabling the channel fully on with the same on-resistance as R_{on} in the first quadrant.

$V_{sd} \approx (V_{th} - V_{gs}) + I_{sd}R_{on\_reverse}$

where

- $R_{on\_reverse}$ is the equivalent on-resistance in third quadrant with the off gate (2)

Compared with a Si MOSFET body diode, GaN FETs have higher V_{sd} drop as V_{th} - V_{gs} is usually higher than 0.7 V when the gate is off. This may induce a higher third quadrant loss of GaN over Si MOSFET.

Figure 4 shows the simplified behavior of the GaN FET in the first and the third quadrant. The analysis above is true for both enhancement and depletion mode GaN FETs.

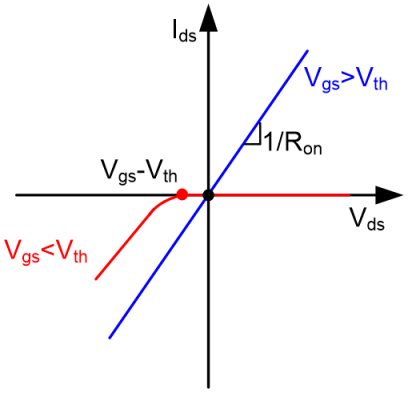

Figure 4. Simplified Behavior of GaN in the First and Third Quadrant

3 Operation and Loss Estimation in the Third Quadrant

To further explain the operation, a synchronous boost converter using GaN is shown inFigure 5 as an example. When S_1 turns off, S_2 goes into the third quadrant operation. Before S_2 turns on, S_2 operates like a diode, following the behavior in the red curve in Figure 4 in the third quadrant. After the dead time, t_{d2}, the S_2 channel is on and S_2 behaves following the blue curve in Figure 4 in the third quadrant. After S_2 turns off, S_2 returns to the diode behavior in the duration of t_{d1}.

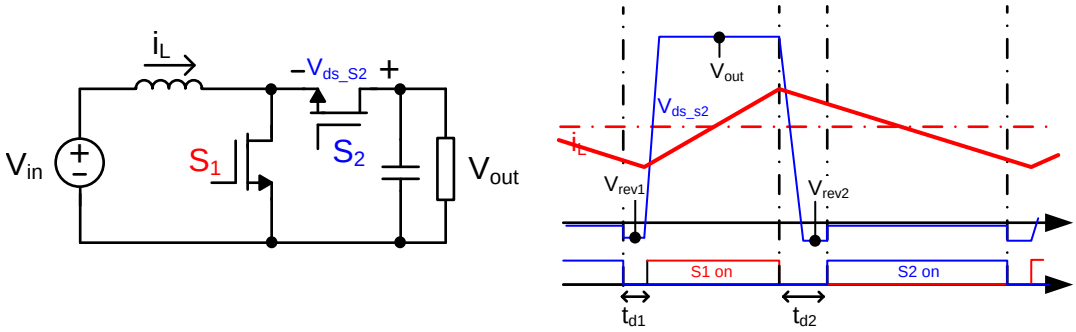

Figure 5. The Third Quadrant Operation in the Boost Converter

The difference of the behavior above from Si MOSFET is a high V_{ds} drop, V_{rev1}, and V_{rev2} during the dead time t_{d1}, t_{d2}. Use Equation 3 to calculate the dead time loss.

$$P_{dt} = f_{sw}t_{d1}V_{rev1}i_{L\_vl} + f_{sw}(t_{d2} - t_r)V_{rev2}i_{L\_pk}$$

where

- f_{sw} is the switching frequency
- t_r is the rising time for S_1 V_{ds}
- i_{L_pk}, i_{L_vl} are the peak and valley inductor current respectively
- V_{rev1} and V_{rev2} are the corresponding third quadrant voltage drop under i_{L_vl}, i_{L_pk} (3)

For the hard-switched edge, the dead time is determined by the input charge, the gate driver propagation delay and mismatch. For the soft-switched edge, the dv/dt slew rate is another main constraint.

4 How to Minimize the Dead Time Losses

Designers have a number of options to minimize the dead-time losses of GaN.

- Select a Proper Turn-Off Gate Voltage for GaN.

  Section 2 explains that V_{sd} during dead time is a function of the turn-off gate voltage. The turn-off gate voltage can be optimized between the dead-time loss and the turn-off speed. In the hard-switched half bridge, the turn-off gate voltage must be low enough to avoid a false turn-on when the opposite switch turns on. This is internally optimized for the designers for integrated GaN solutions such as the *LMG3410R070*.

- Minimize the Dead Time.

  Minimizing the dead time is the most straightforward solution. The dead time can always be well-tuned based on the maximum dead time needed. For example, in the reference design of *1 MHz 1 kW High Efficiency and High Power Density Resonant Converter* using TI GaN LMG3410R070, the dead time is 100 ns and the dead time loss on GaN under full power is only 0.2 W, taking only 0.7% of total loss.

- Adaptive Dead-Time Control

  For the topologies like PFC, adaptive dead-time control is more beneficial. In PFC, the inductor peak current varies and the turn-off dv/dt slew rate is not constant in each switching cycle. The fixed dead time is determined by the worst case with the lowest dv/dt slew rate, resulting in higher dead-time losses in the operation with a higher dv/dt slew rate.

  The principle of the adaptive dead-time control is demonstrated in Figure 6 where the optimum dead time is almost equal to the switch-node capacitor charging time. The optimum dead time is dependent on the inductor current and switch node capacitance and requires real-time correction in each switching cycle. By doing so, the 'diode' operation period, shown as t_{diode} in Figure 6, can almost be eliminated.

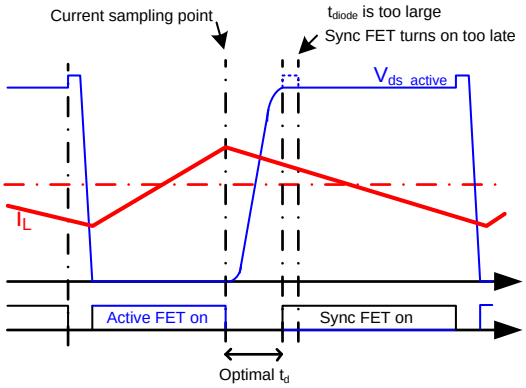

Figure 6. Illustration of Adaptive Dead-Time Control

Generally, there are two types of implementation. With digital control, the dead time for the next switch event can be calculated based on the operating conditions. For example, in the 3.3 kW GaN-based totem-pole CCM PFC *TIDM-1007* with C2000TM MCU, the dead time is calculated using Equation 4 before the synchronous rectifier GaN FET turns on. Figure 7 shows the diagram of its implementation. In *TIDM-1007*, at high line 230 Vrms, the power loss savings using the adaptive control compared with a fixed dead time is shown in Figure 8.

$$t_d = C_{sw} V_o / i_{L,AVG} \quad (4)$$

where

- t_d is the minimal dead time for the next switching event
- C_{sw} is the total parasitic capacitor from the switching node to ground
- V_o is the output voltage
- $i_{L,AVG}$ is the sampled inductor current in the current cycle

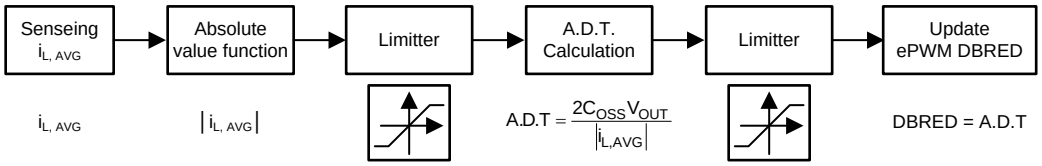

Figure 7. Implementation of Adaptive Dead Time Control in *TIDM-1007*

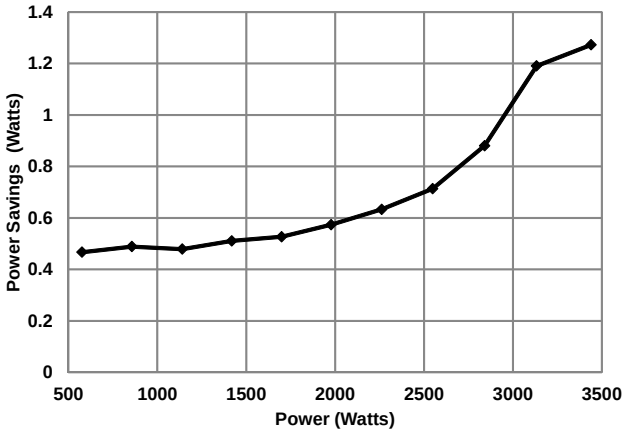

Figure 8. Power Saving with Adaptive Dead Time in *TIDM-1007*

With analog control, the adaptive dead-time control is implemented in some controllers for synchronized rectifiers. The switching mode voltage V_{sw} is monitored and compared with a predetermined threshold voltage to provide a detection signal to turn on the synchronized rectifier. A short period, like 12 ns to 15 ns, may be needed between the detection signal and the turn-on signal to leave enough dead time. See the *UCC24612 High Frequency Synchronous Datasheet* for a design example.

5 Summary

The lack of p-n junction of the GaN HEMT in the lateral structure eliminates the body diode and reverse recovery loss, which significantly reduces the switching loss in the hard switched topologies, such as the bridgeless totem-pole CCM PFC. To conduct current in the reverse direction, GaN FET self-commutates and behaves like a diode due to the symmetry of the lateral structure, but tends to have a large V_{sd}. With a short dead time, the dead-time losses can be minimized. Adaptive dead-time control is an effective way to further reduce the loss by correcting the dead time based on the operating condition.

6 References

- E. A. Jones, F. Wang, and B. Ozpineci. (2014) *Application-based review of GaN HFETs.* IEEE Workshop on Wide Bandgap Power Devices and Applications, pp. 24-29. https://ieeexplore.ieee.org/document/6964617
- Edward Andrew Jones. (2016) *Review and Characterization of Gallium Nitride Power Devices.* University of Tennessee. https://trace.tennessee.edu/utk_gradthes/4048/

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