Application Report
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Using the ADS1202 Reference Design

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ABSTRACT

This application report describes the characteristics, operation, and use of the ADS1202 reference design. It includes two isolated ADS1202 circuits for a variety of applications and a $Sinc^3$ filter implemented in a Xilinx® XC2S150 field-programmable gate array (FPGA). Optional optocouplers provide additional isolation. A complete circuit description and schematic diagram are included.

Related Documentation from Texas Instruments

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Data Sheets:	**Literature Number:**
ADS1202	SBAS275
TPS70358	SLVS285
Users Guides:	**Literature Number:**
5-6K Interface Card	SLAU104
Application Notes:	**Literature Number:**
ADS1202 Traffo	SBAA096
ADS1202 Opto Selection	SBAA088
ADS1202 Digital Filter	SBAA094
Clock Divider Circuit	SBAA105

Application Overview

Features

- Xilinx 150,000 Gate Spartan II FPGA – XC2S150
- Two analog channels, with independent ADS1202 circuits
- JTAG interface, ISP capable
- SPI or McBSP operation

Introduction

The ADS1202 reference design provides two isolated ADS1202 circuits for a variety of applications. It includes a $Sinc^3$ filter implemented in a Xilinx XC2S150 FPGA. Optional optocouplers can be used to provide electrical isolation.

The modular form factor of the reference design allows direct evaluation of ADS1202 performance and operating characteristics. This reference design is compatible with the 5-6K interface board from Texas Instruments. See the *5-6K Interface Board User's Guide* (literature number SLAU104) for more information.

Analog Interface

The ADS1202 reference design easily interfaces to multiple analog sources. Two-position screw terminals J11 and J12 provide convenient access to the ADS1202 input pins. Each channel has socketed components to easily implement input-filter options.

Each analog channel is electrically isolated for high-voltage applications when used with optional optocouplers. Two-position screw terminals J13 and J16 provide convenient individual access to each ADS1202 power connection.

Digital Interface

The ADS1202 reference design easily interfaces to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual-row header/socket combination at J2 and J8. This header/socket provides access to the digital control and serial data pins of the ADS1202 reference design. The signals and pin assignments are given in Table 1.

Table 1. Digital-Interface Connector

Pin Number		Signal	Description
J2.1	J8.1	Unused	
J2.3	J8.3	SCLK	Serial clock; used in SPI mode
J2.5	J8.5	CLKR	Serial clock; used in McBSP mode
J2.7	J8.7	/SS	Slave select; used in SPI mode
J2.9	J8.9	FS(R)	Frame sync; used in McBSP mode
J2.11	J8.11	Unused	
J2.13	J8.13	SDO	Serial data output from FPGA ($Sinc^3$ filter output)
J2.15	J8.15	Unused	
J2.17	J8.17	Unused	
J2.19	J8.19	SPARE	

Power Supplies

The ADS1202 reference design board requires separate 5-V dc supplies for each ADS1202 circuit and for the digital section. When used in combination with the 5-6K interface board, J17 (located on the bottom side of the board) provides connection to the common power bus described in the *5-6K Interface Board User's Guide* (literature number SLAU104) for use with the digital portion of the board. U1 provides 3.3 V and 2.5 V for the FPGA and optional optocoupler circuits. The analog sections must be powered through J13 and J16.

When the reference design is used as a stand-alone module, the 5-V digital power is applied to J1. Although filters are provided for all power supply inputs, optimal performance of the board requires a clean, well-regulated power source.

Reference Design Operation

Analog input sources connect directly to J14 and J15. Note the polarity on the silkscreen for proper signal connections. Two-pin headers J11 and J12 provide grounding options to the (–) input of the ADS1202 device. Closing the jumper shorts the (–) input to ground through R24 and R27 (refer to the schematic for additional details).

Digital control signals can be applied directly to J2 and J8 (top or bottom side). The ADS1202 reference design can also be connected directly to a DSP interface board. Connector J6 is provided for mechanical stability only. No signals are applied to this connector.

The four-position dipswitch S2 selects decimation ratios and selects between McBSP or SPI operation. When an S2 switch is in the ON position, a logic level 0 is applied to the respective FPGA input pin.

Switch 2 position 1 selects the operating mode.

The ON position selects SPI mode. In this case, a burst clock is applied to the host processor, and the host processor is to be set as an SPI slave device with CPOL = 0 and CPHA = 0.

The OFF position selects McBSP mode and a continuous clock is applied to the host processor. A frame sync pulse is provided via FSR to the DSP in this mode. The McBSP port must be set to accept an active high FS with 0-bit data delay. In either mode, a periodic burst of eight 16-bit words is supplied to the host, and the data rate depends on the decimation ratio.

Switch 2 positions 2, 3, and 4 select the decimation ratio. Table 2 describes the settings.

Table 2. Decimation-Ratio Switch Settings

Switch 2 Position (ON = 0)			Decimation Ratio - Effective Resolution
2	3	4	
0	0	0	4–6 bits
0	0	1	8–9 bits
0	1	0	16–12 bits
0	1	1	32–15 bits
1	0	0	64–18 bits
1	0	1	128–21 bits
1	1	0	256–24 bits

A 20-MHz crystal is supplied at position U3. This crystal can be replaced with a lower frequency crystal to provide alternate clocks to the ADS1202. As configured, the ADS1202 reference design is set for Mode 3 operation. The VHDL code for the FPGA can be modified for alternate modes of operation. Jumpers J18 through J21 control the operating mode of the installed ADS1202 devices. Opening the jumper applies a logic 1 on the ADS1202 mode pins. The clock-configuration modes are described in Table 3.

Table 3. Clock Configuration

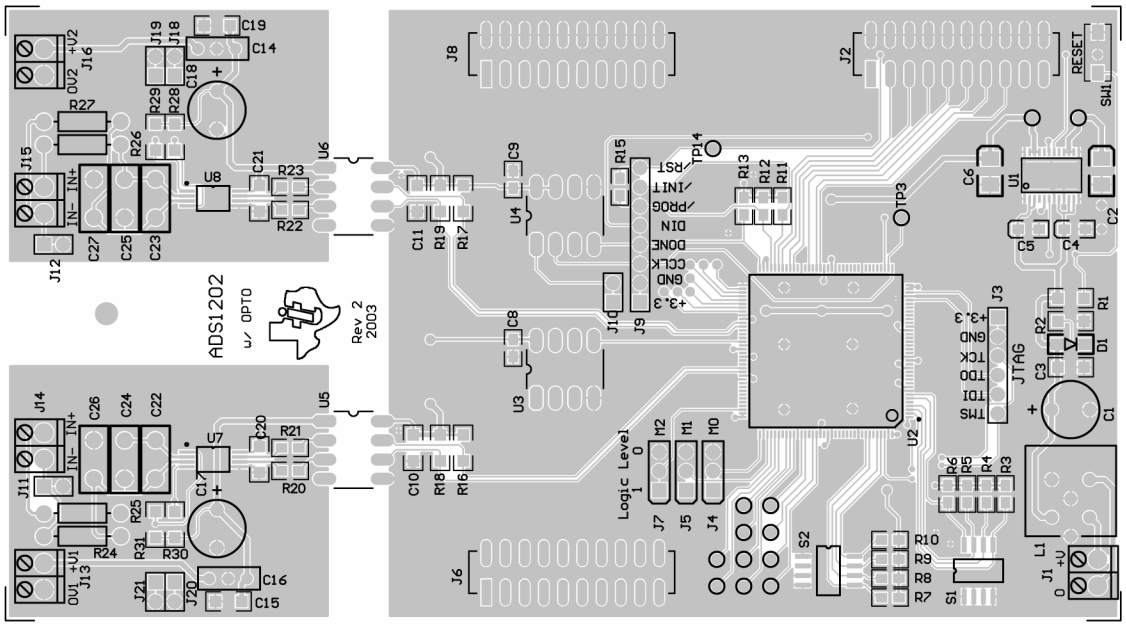
Jumper		Description
J19/J21	J18/J20	
Closed	Closed	Mode 0 operation; processor reads MDAT on rising clock edge only
Open	Closed	Mode 1 operation; processor reads MDAT on every clock edge
Closed	Open	Mode 2 operation; Manchester decoding required
Open	Open	Mode 3 operation; requires external clock (default condition)

ADS1202 Reference Design Schematic and BOM

Table 4 provides the ADS1202 reference design bill of materials. The PC-board layers are shown in Figure 1. The schematic for the ADS1202 reference design is included at the end of this document. The Gerber files and VHDL code are available for download from the Texas Instruments web site at www.ti.com. Use the keyword search and follow the links for document number SLAA186.

Table 4. Bill of Materials

Designator	Description	Manufacturer	Mfg. Part Number
C1 C17 C18	TANT 100 µF 20V 10% RAD	AVX	TAP107K020CCS
C2	TANT 47 µF 10V 20% SMD	Kemet	T491B476M010AS
C6	TANT 22 µF 10V 20% SMD	Kemet	T491B226M010AS
C3 C8 C9 C10 C11 C15 C19 C20 C21	0.1uF, 1206, ceramic, X7R, 50V, 10%	Panasonic	ECJ-3VB1H104K
C4 C5	20VDC .22 µF TES-series SMD	Panasonic	ECS-T1DP224R
C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44	0.1 µF, 0805, ceramic, X7R, 50V, 10%	Panasonic	ECJ-2YB1H104K
C14 C16	EXC-EMT/EMI filter 2200 pF	Panasonic	EXC-EMT222DT
C22 C23 C24 C25 C26 C27	CK05-style ceramic, radial, value TBD	Various	Various
D1	1206-size SMT LED, amber	Chicago Miniature	7010X7
J1 J13 J14 J15 J16	2-terminal screw connector	Off Shore Technologies	ED1514
J2 J6 J8 (top side)	10-pin, dual-row, SMT header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
J2 J6 J8 (bottom side)	10-pin, dual-row, SMT socket (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
J3	6-pin , .1” header	Samtec	TSW-106-07-L-S
J5 J6 J7	3-pin , .1” header	Samtec	TSW-103-07-L-S
J9	8-pin , .1” header	Samtec	TSW-108-07-L-S
J10 J11 J12 J18 J19 J20 J21	2-pin , .1” header	Samtec	TSW-102-07-L-S
J17 (bottom side)	5-pin, dual-row, SMT socket (10 pos.)	Samtec	SSW-105-22-F-D-VS-K
L1	EMI filter	Murata	BNX002-01
R1	1206-size, 5%, 3.3 KΩ	Yageo America	9C12063A3301JLHFT
R2	1206-size, 5%, 560 Ω	Yageo America	9C12063A5600JLHFT
R3 R4 R5 R6 R7 R8 R9 R10 R28 R29 R30 R31	0805-size, 5%, 10 KΩ	Yageo America	9C08052A1002JLHFT
R11 R12 R13	0805-size, 5%, 4.7 KΩ	Yageo America	9C08052A4701JLHFT
R15	0805-size, 5%, 0.0 Ω	Yageo America	9C08052A0R00JLHFT
R16 R17 R18 R19	1206-size, 5%, 330 Ω	Yageo America	9C12063A3300JLHFT
R20 R21 R22 R23	0805-size, 5%, 470 Ω	Yageo America	9C12063A4700JLHFT
R24 R25 R26 R27	1/4W axial lead, value TBD	Various	Various
S1 S2	Switch, DIP, half-pitch, 4-position	CTS	218-4LPST
SW1	Switch, momentary pushbutton, NO	Panasonic	EVQ-PJ
U1	TPS70358	TI	TPS70358PWP
U2	XC2S100	Xilinx	XC2S100-5TQ144C
U3	20-MHz, half-size oscillator	CTS	MXO45HS-20.0000
U4	SRL CONFIG EEPROM 1M	Atmel	AT17LV010-10PC
U5 U6	Wire shunts, 2 ea., pins 2-7 and pins 3-6	NA	NA
U7 U8	ADS1202	TI	ADS1202IPWT
Various	Red test-point loop	Keystone	5000
Various	Black test-point loop	Keystone	5001



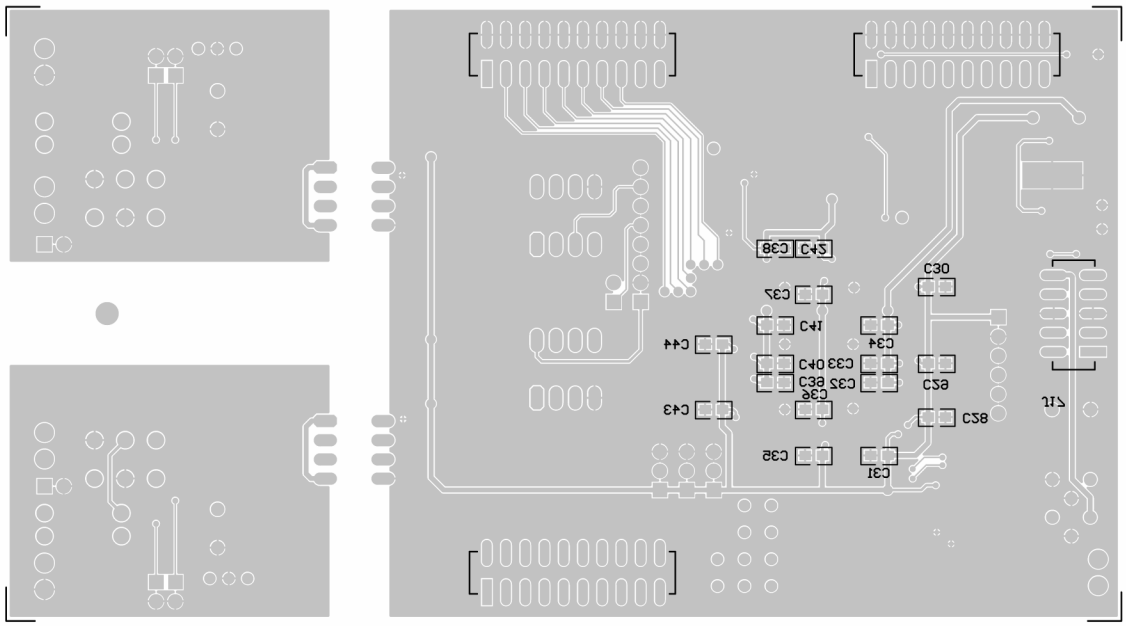
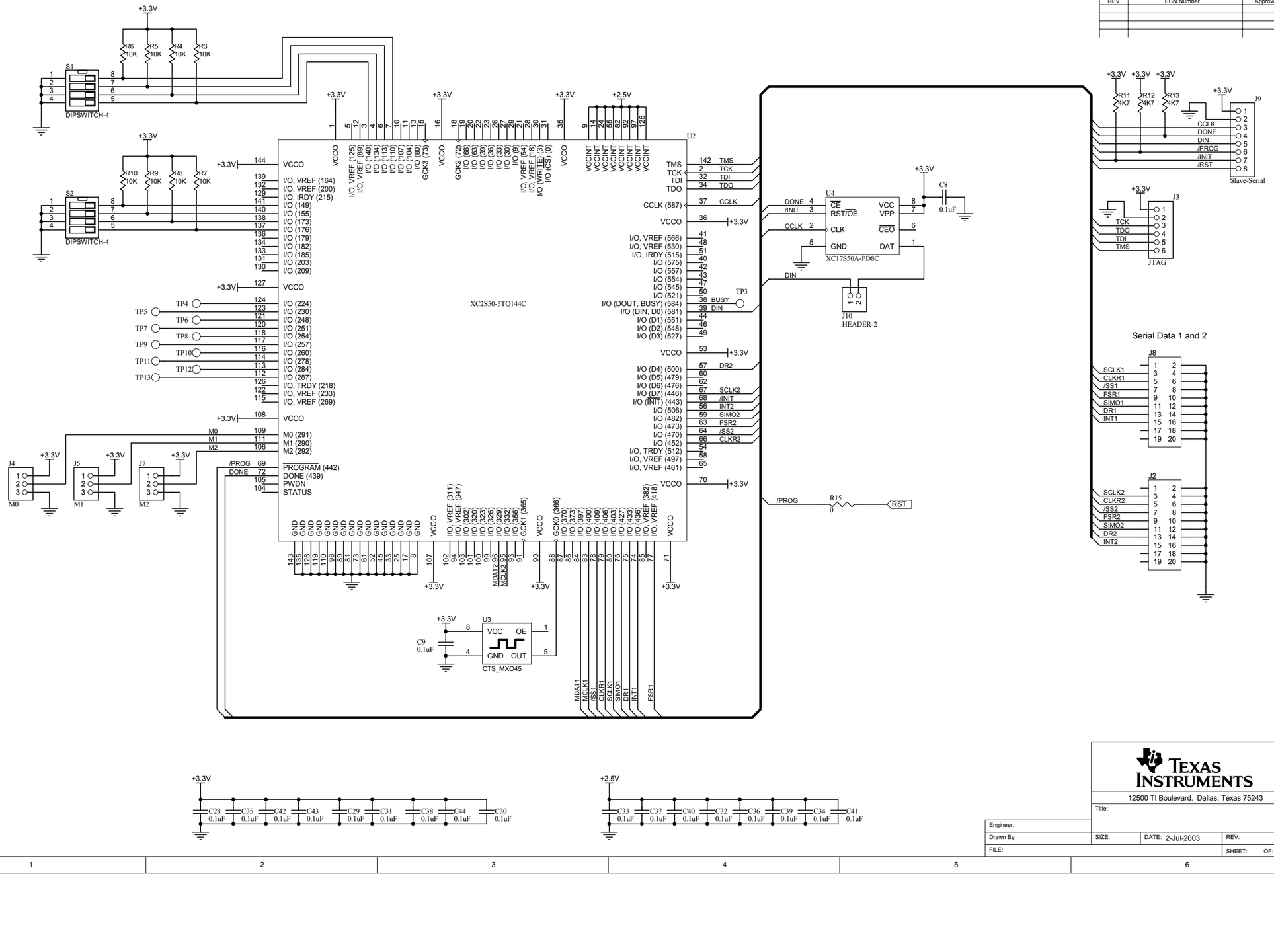


Figure 1. PC Board Layers and Silkscreens


Revision History
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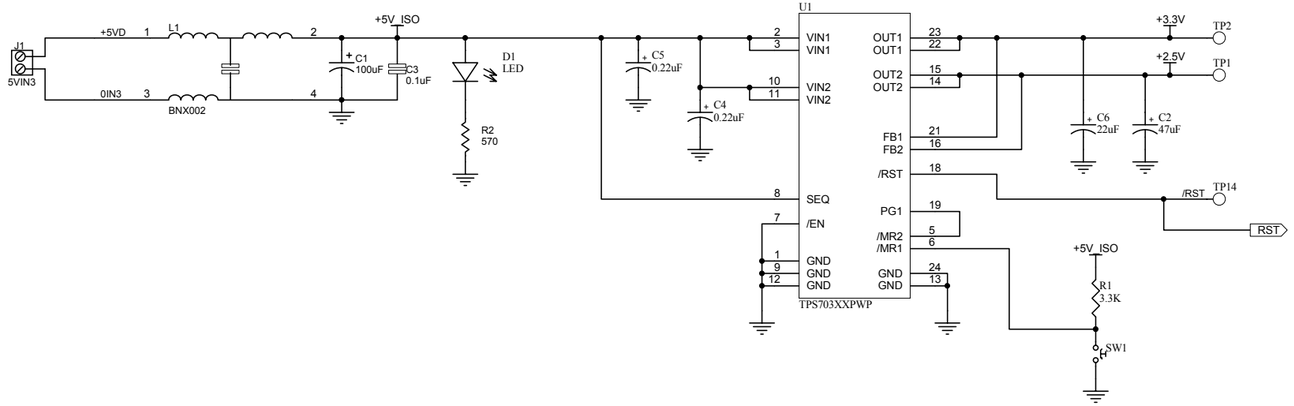
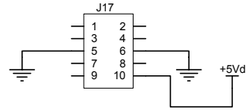
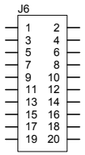
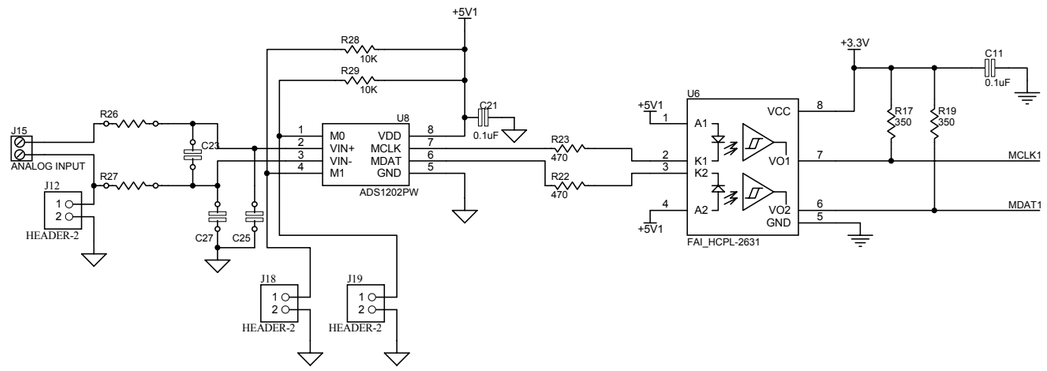
ECN Number
Approved
DIPSWITCH-4
XC2S50-5TQ144C
XC17S50A-PD8C
JTAG
Slave-Serial
HEADER-2
Serial Data 1 and 2
CTS_MXO45
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title:
Engineer:
Drawn By:
SIZE:
DATE: 2-Jul-2003
REV:
FILE:
SHEET:
OF:

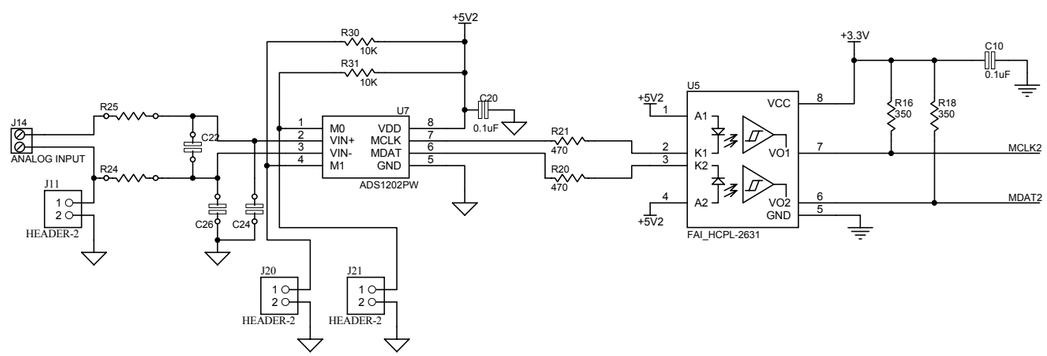
Revision History		
REV	ECN Number	Approved

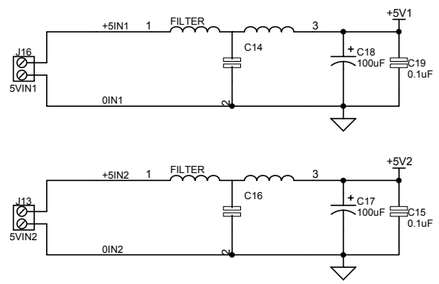












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