Analog Engineer's Circuit

Integrator Circuit

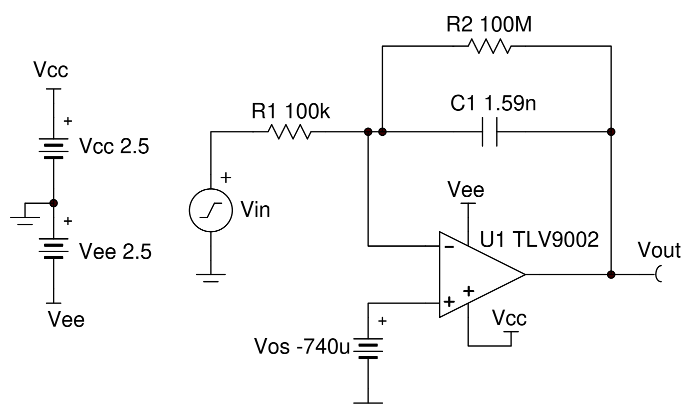
Pete Semig

Design Goals

Input			Output		Supply	
f_{Min}	f_{0dB}	f_{Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
100 Hz	1 kHz	100 kHz	–2.45V	2.45V	2.5V	–2.5V

Design Description

The integrator circuit outputs the integral of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal integrator circuit saturates to the supply rails depending on the polarity of the input offset voltage and requires the addition of a feedback resistor, R_2, to provide a stable DC operating point. The feedback resistor limits the lower frequency range over which the integration function is performed. This circuit is most commonly used as part of a larger feedback/servo loop which provides the DC feedback path, thus removing the requirement for a feedback resistor.



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Design Notes

1. Use as large of a value as practical for the feedback resistor.
2. Select a CMOS op amp to minimize the errors from the input bias current.
3. The gain bandwidth product (GBP) of the amplifier will set the upper frequency range of the integrator function. The effectiveness of the integration function is usually reduced starting about one decade away from the amplifier bandwidth.
4. An adjustable reference needs to be connected to the non-inverting input of the op amp to cancel the input offset voltage or the large DC noise gain will cause the circuit to saturate. Op amps with very low offset voltage may not require this.

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Design Steps

The ideal circuit transfer function is given below.

$$V_{out} \quad = \quad -\frac{1}{R_1 \times C_1}\int_0^t V_{in}\left(t\right)\,d\,t$$

1. Set R_1 to a standard value.

   $$R_1 = 100k\Omega$$

2. Calculate C_1 to set the unity-gain integration frequency.

   $$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_{0dB}} = \frac{1}{2 \times \pi \times 100k\Omega \times 1\ \ kHz} = 1.59nF$$

3. Calculate R_2 to set the lower cutoff frequency a decade less than the minimum operating frequency.

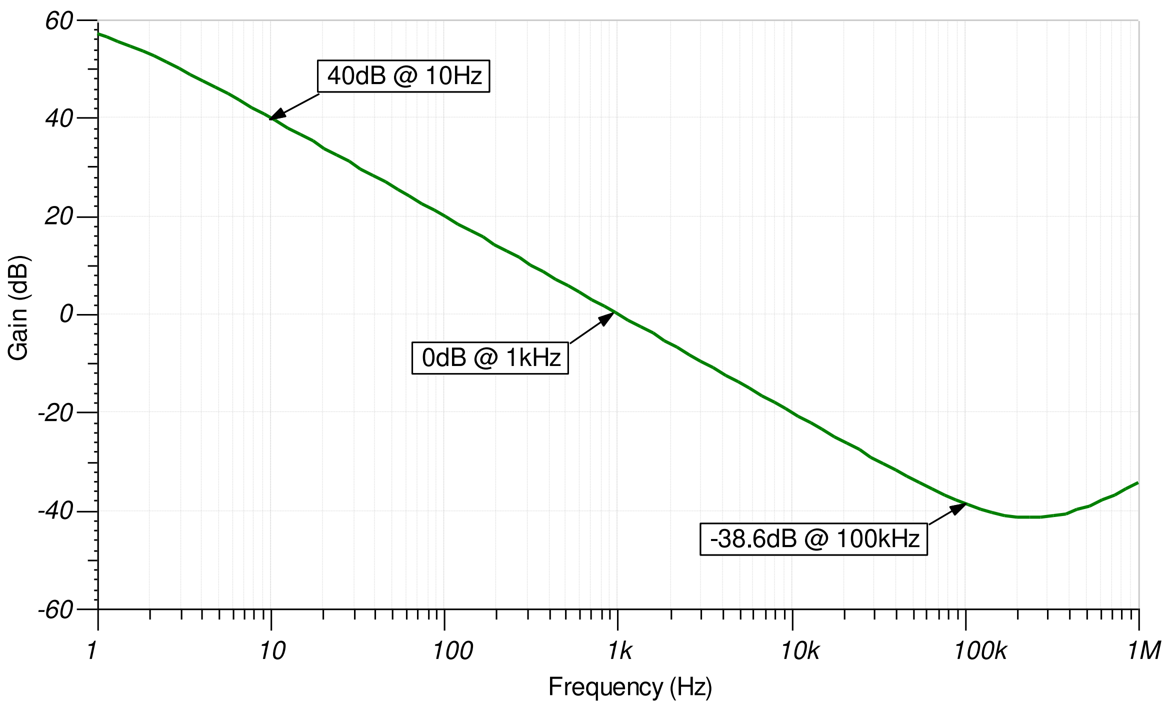
   $$R_2 \geq \frac{10}{2 \times \pi \times C_1 \times f_{Min}} \geq \frac{10}{2 \times \pi \times 1.59nF \times 10Hz} \geq 100M\Omega$$

4. Select an amplifier with a gain bandwidth at least 10 times the desired maximum operating frequency.

   $$GBP \geq 10 \times f_{Max} \geq 10 \times 100kHz \geq 1\ \ MHz$$

Design Simulations

AC Simulation Results



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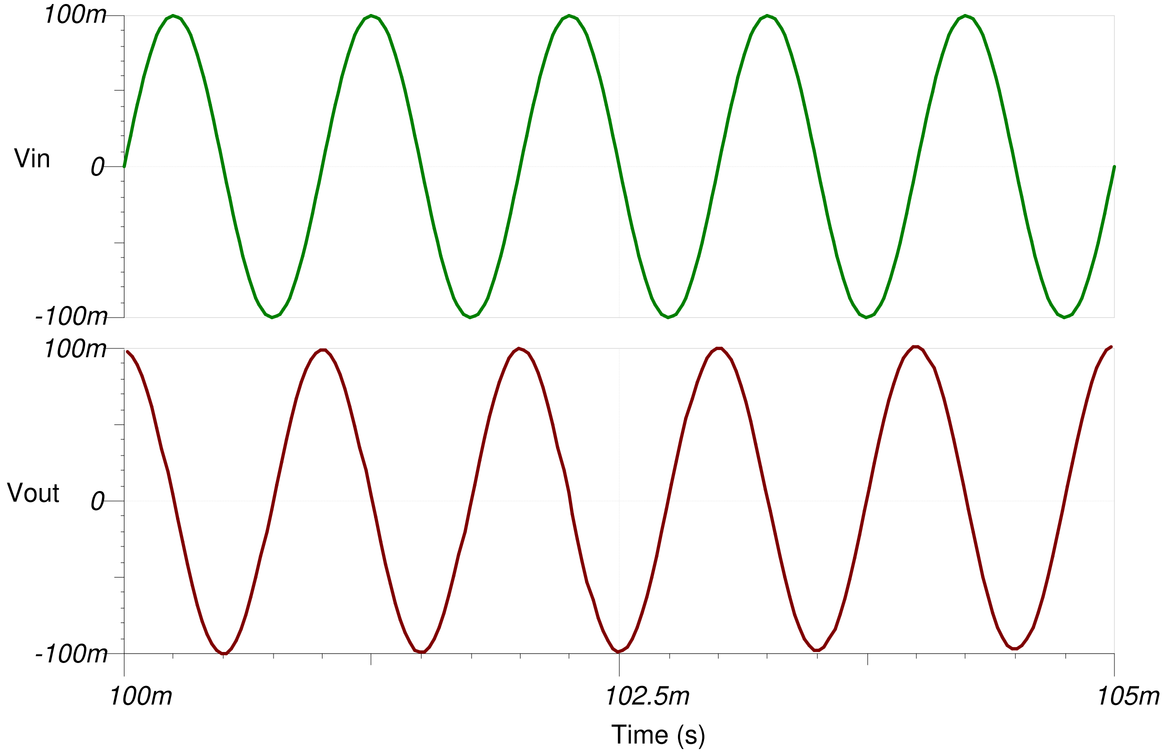
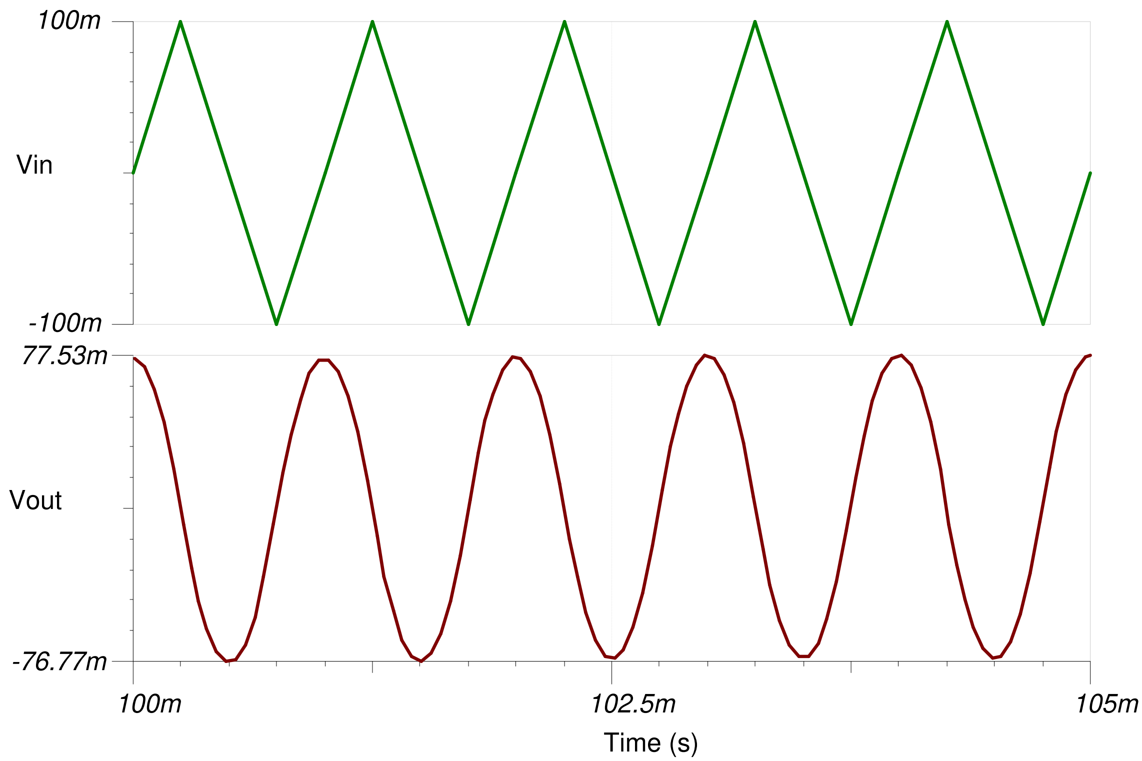
Transient Simulation Results

A 1kHz sine wave input yields a 1kHz cosine output.



A 1kHz triangle wave input yields a 1kHz sine wave output.



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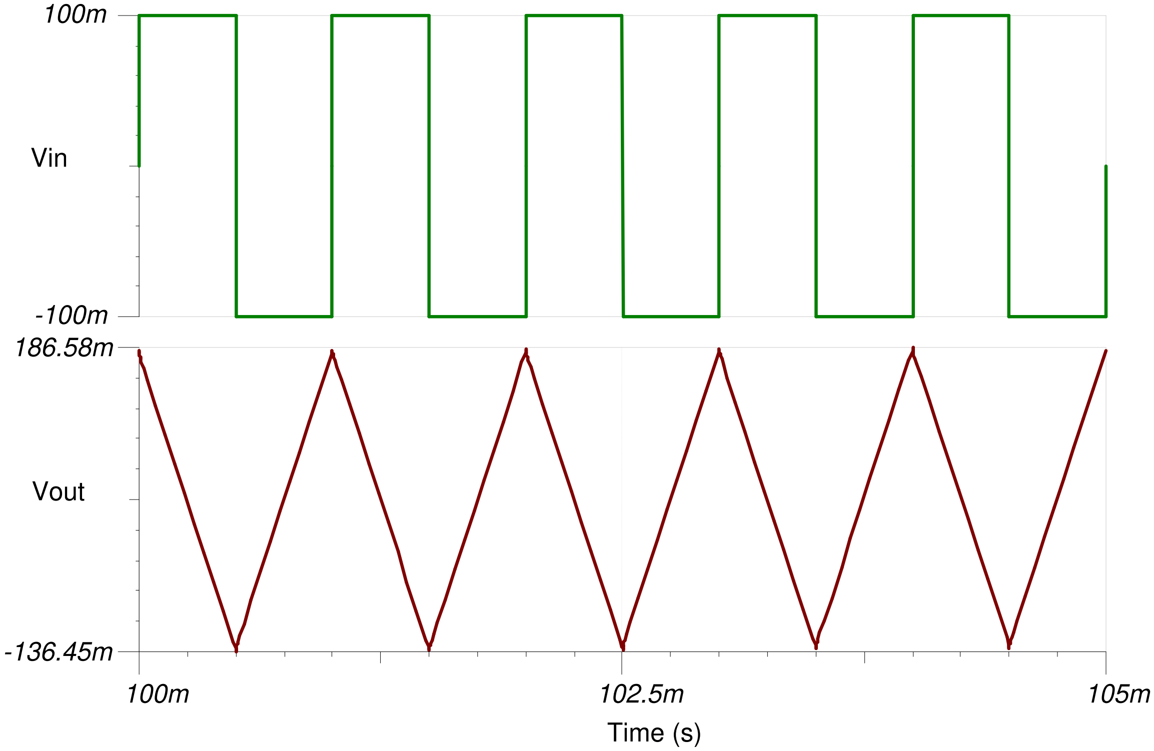
A 1kHz square wave input yields a 1kHz triangle wave output.



Design References

Texas Instruments, *Simulation for Integrator Circuit*, SBOC496 tool

Texas Instruments, *Instrumentation Amplifier with DC Rejection*, TIPD191 reference design

Design Featured Op Amp

TLV9002	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	0.06mA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, and 4
TLV9002	

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Design Alternate Op Amp

OPA376	
V_{cc}	2.2V to 5.5V
V_{inCM}	(V_{ee}-0.1V) to (V_{cc}-1.3V)
V_{out}	Rail-to-rail
V_{os}	0.005mV
I_q	0.76mA
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1, 2, and 4
OPA376	

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B (September 2024)	**Page**
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (January 2019)	**Page**
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page	1

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