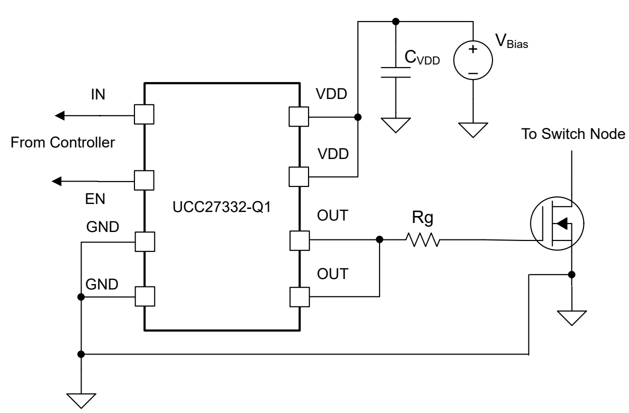
UCC27332-Q1 20-V, 9-A Single Channel Low Side Gate Driver with –5-V Input Capability For Automotive Application

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  – Device temperature grade 1: –40°C to +125°C ambient Operating Temperature Range
  – Device HBM ESD classification level H2
  – Device CDM ESD classification level C4B
- Industry-standard pin-out
- Typical 9-A sink, 9-A source output currents
- Input pin capable of withstanding up to –5 V
- Absolute maximum VDD voltage: 20 V
- Wide VDD operating range from 4.5 V to 18 V
- Available in 3-mm x 3-mm MSOP8 package
- Typical 25-ns propagation delay
- TTL compatible input thresholds
- Operating junction temperature range of –40°C to 125°C

2 Applications

- Automotive DC/DC converter
- Automotive on-board charger (OBC)
- Telecom switch mode power supplies
- Power factor correction (PFC) circuits
- Solar power supplies
- Motor drives
- High frequency line drivers
- Pulse transformer drivers
- High power buffers



Simplified Application Diagram

3 Description

The UCC27332-Q1 is a single channel, high-speed, low-side gate driver capable of effectively driving MOSFET and GaN power switches. UCC27332-Q1 has a typical peak drive strength of 9-A, which reduces the rise and fall times of the power switches, lowering switching losses and increasing efficiency. The UCC27332-Q1 device's small propagation delay yields better power stage efficiency by improving the dead time optimization, pulse width utilization, control loop response, and transient performance of the system.

UCC27332-Q1 can handle –5-V on its input, which improves robustness in systems with moderate ground bouncing. An independent enable signal allows the power stage to be controlled independent of the main control logic. The gate driver can quickly shut off the power stage if there is a fault in the system (which requires the power train to be turned-off). The enable function also improves system robustness. Many high-frequency switching power supplies exhibit high frequency noise at the gate of the power device, which can get injected into the output pin of the gate driver and can cause the driver to malfunction. The UCC27332-Q1 performs well in such conditions due to its transient reverse current and reverse voltage capability.

The strong internal pulldown MOSFET holds the output low if the VDD voltage is below the specified power on reset threshold. This active pulldown feature further improves system robustness. The small 3-mm×3mm MSOP package enables optimum gate driver placement and inproved layout. This small package also enables optimum gate driver placement and improved layout.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
UCC27332-Q1	DGN (VSSOP-PowerPAD, 8)	3.0 mm × 4.9 mm	3.0 mm x 3.0 mm

(1) For all available packages, see the orderable addendum at the end of this data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial release

5 Pin Configuration and Functions

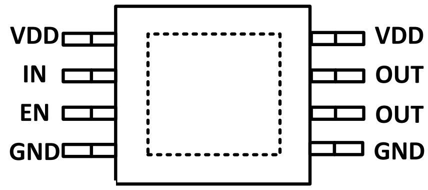


Figure 5-1. 8-Pin MSOP DGN Package Top View

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
EN	3	I	Enable or disable control pin. If not used, connect to VDD.
GND	4,5	G	Device ground or reference
IN	2	I	Non-inverting PWM input
OUT	6,7	O	Output of the driver
VDD	1,8	P	Driver bias supply. Connect the positive node of the voltage source to this pin through an impedance for high common mode noise rejection. Bypass this pin with two ceramic capacitors, generally >=1 μF and 0.1 μF, which are referenced to GND pin of this device.
	Thermal Pad	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I/O = Digital input/output, IA = Analog input, AO= Analog output, P = Power connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)] [(3)]

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
Output Voltage (DC)	VOUT	–0.3	VDD +0.3	V
Output Voltage (100-ns Pulse)	VOUT	–2	VDD +0.3	V
Input Voltage IN		–5	VDD +0.3	V
Input Voltage EN		-0.3	VDD +0.3	
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 s		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *Section 6.4* of the data sheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)] HBM ESD classification level H2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	18	V
Input voltage, IN	–2		VDD	V
Input voltage, EN	0		VDD	V
Output Voltage, OUT	0		VDD	V
Operating junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		UCC27332-Q1 DGN (MSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.1	°C/W

6.5 Electrical Characteristics

Unless otherwise noted, VDD = 4.5 V to 18 V, $T_A = T_J$ = –40°C to 125°C, 1-µF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDD}	VDD static supply current	V_{IN} = 3.3V, EN = VDD		150	380	uA
I_{VDD}	VDD static supply current	V_{IN} = 0 V, EN = VDD		107	180	uA
I_{VDDO}	VDD dynamic operating current	C_{LOAD} = 1.8 nF, f_{SW} = 100 kHz, EN = VDD, V_{IN} = 0 V to 3.3 V PWM		3.9	4.5	mA
I_{DIS}	VDD disable current	V_{IN} = 3.3 V, EN = 0 V		280	380	uA
POWER ON RESET (POR)						
V_{VDD_ON}	VDD POR rising threshold		2.1	3.0	4.0	V
V_{VDD_OFF}	VDD POR falling threshold		1.8	2.7	3.5	V
V_{VDD_HYS}	VDD POR hysteresis			0.3		V
INPUT (IN)						
V_{IN_H}	Input signal high threshold,	Output High, EN=HIGH	1.6	2.2	2.5	V
V_{IN_L}	Input signal low threshold	Output Low, EN=HIGH	0.8	1.2	1.5	V
V_{IN_HYS}	Input signal hysteresis			1.0		V
ENABLE (EN)						
V_{EN_H}	Enable signal high threshold	Output high, IN=HIGH	1.7	2.3	2.7	V
V_{EN_L}	Enable signal low threshold	Output low, IN=HIGH	1.1	1.8	2.0	V
V_{EN_HYS}	Enable signal hysteresis			0.7		V
R_{EN}	EN pin pullup resistance	EN = 0 V		100		kΩ
OUTPUT (OUT)						
I_{SRC} (1)	Peak output source current	VDD = 14V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		9		A
I_{SNK} (1)	Peak output sink current	VDD = 14V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–9		A
R_{OH} (2)	OUTH, pullup resistance	I_{OUT} = –10 mA See: Section 7.3.4		0.6	1.5	Ω
R_{OL}	OUTL, pulldown resistance	I_{OUT} = 10 mA		0.4	1	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

6.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 4.5 V to 18 V, T_A = T_J = –40°C to 125°C, 1-μF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C [(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	C_{LOAD} = 10 nF, 20% to 80%, V_{IN} = 0 V to 5V		16	30	ns
t_F	Fall time	C_{LOAD} = 10 nF, 80% to 20%, V_{IN} = 0 V to 5V		11	28	ns
t_{D1}	Turnon propagation delay	C_{LOAD} = 10 nF, V_{IN_H} of the input rise to 20% of output rise, V_{IN} =0 V to 5V, Fsw=500kHz, 50% duty cycle		25	60	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 10 nF, V_{IN_L} of the input fall to 80% of output fall, V_{IN} =0 V to 5V, Fsw=500kHz, 50% duty cycle		34	65	ns
t_{PD_EN}	Enable propagation delay	C_{LOAD} = 10 nF, V_{EN_H} of the enable rise to 20% of output rise, V_{IN} =0 V to 5V, Fsw=500kHz, 50% duty cycle		27	40	ns
t_{PD_DIS}	Disable propagation delay	C_{LOAD} = 10 nF, V_{EN_L} of the enable fall to 80% of output fall, V_{IN} =0 V to V, Fsw=500kHz, 50% duty cycle		28	64	ns
t_{PWmin}	Minimum input pulse width that passes to the output	C_{LOAD} = 10 nF, V_{IN} =0 V to 5V, Fsw=500kHz, Vo > 1.5 V			30.5	ns

(1) Switching parameters are not tested in production.

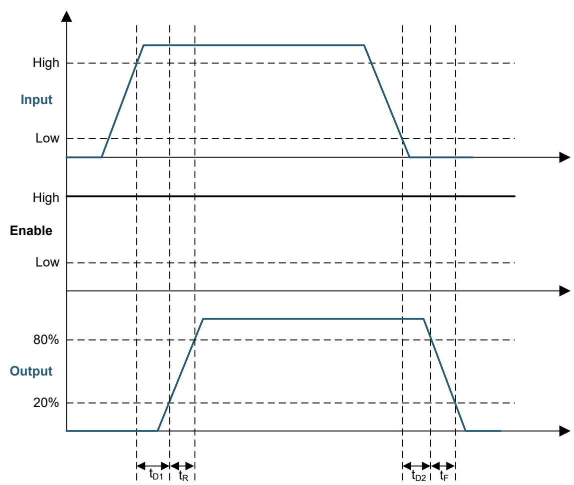


Figure 6-1. Input-Output Operation

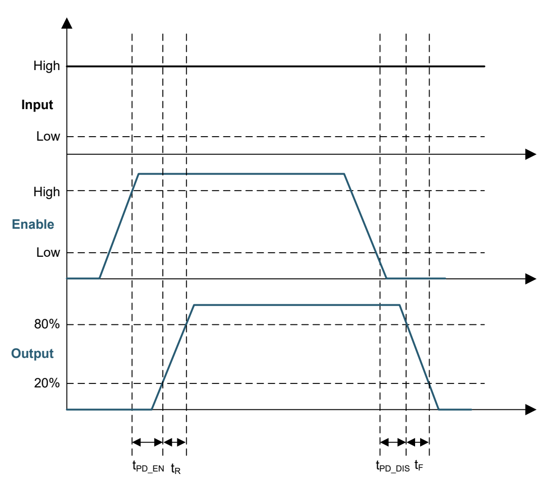


Figure 6-2. Enable Function

6.8 Typical Characteristics

Unless otherwise specified, VDD=12V, IN+=3.3V, IN-=GND, T_J = 25 °C, no load

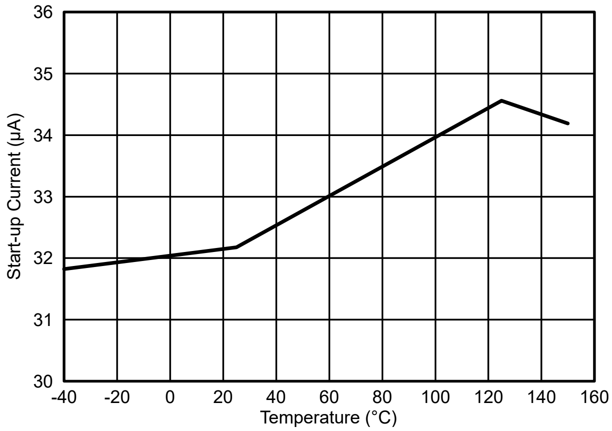


Figure 6-3. Start-Up and Quiescent Current

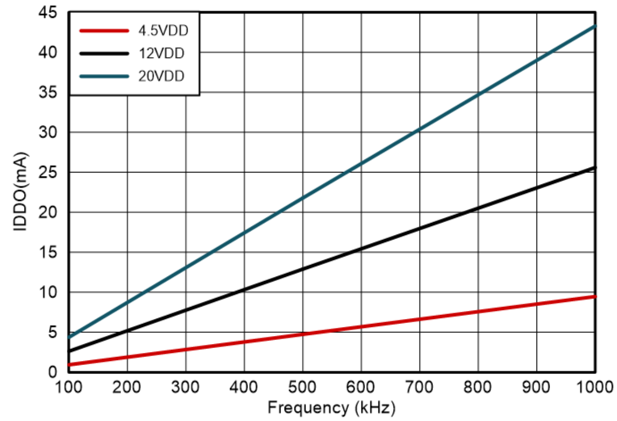


Figure 6-4. Operating Supply Current

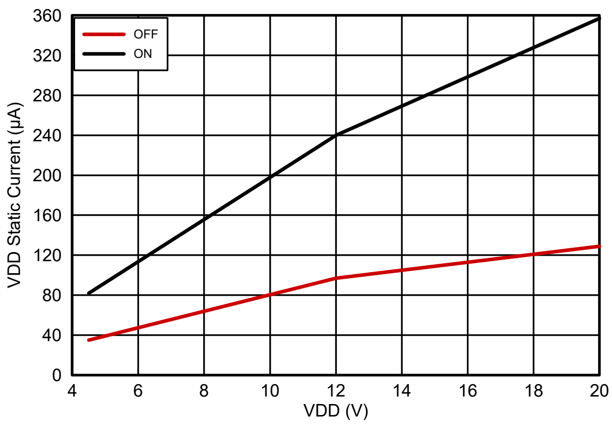


Figure 6-5. Static Supply Current

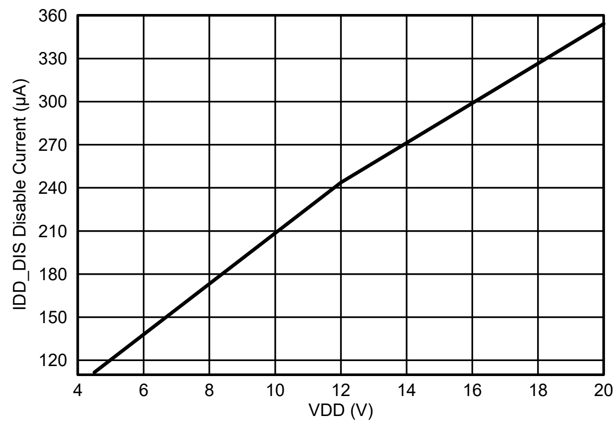


Figure 6-6. Disable Current

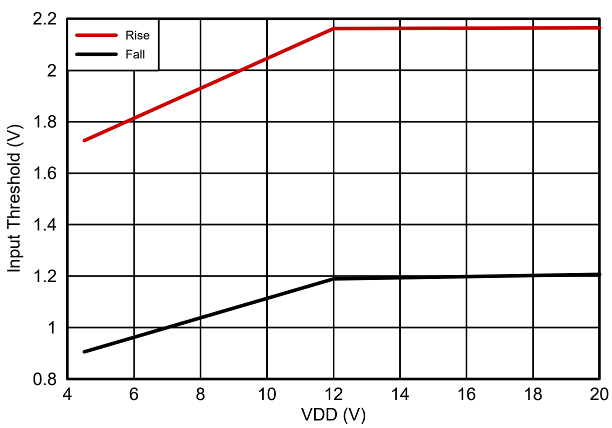


Figure 6-7. Input Thresholds

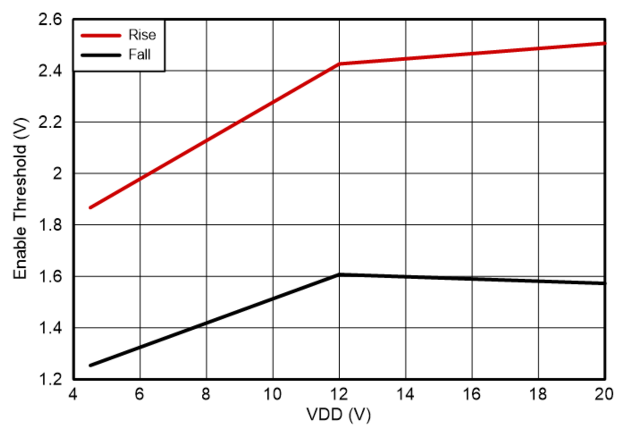


Figure 6-8. Enable Threshold

6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, IN+=3.3V, IN-=GND, T_J = 25 °C, no load

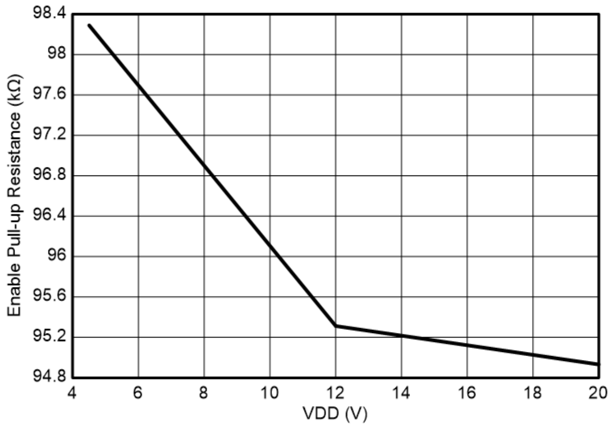


Figure 6-9. Enable Pullup Resistance

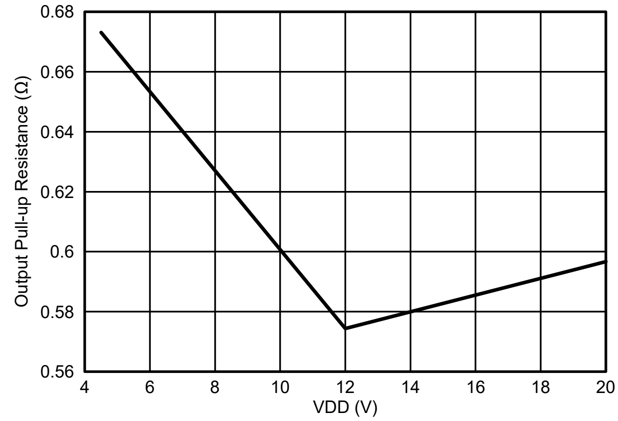


Figure 6-10. Output Pullup Resistance

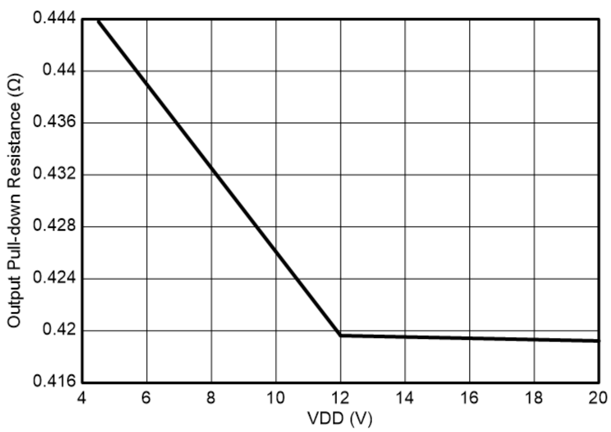
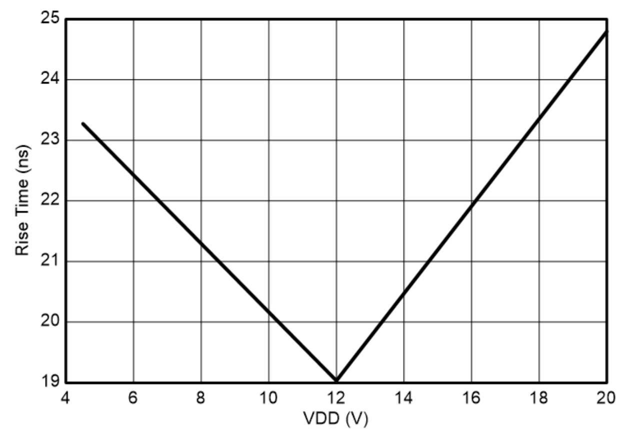
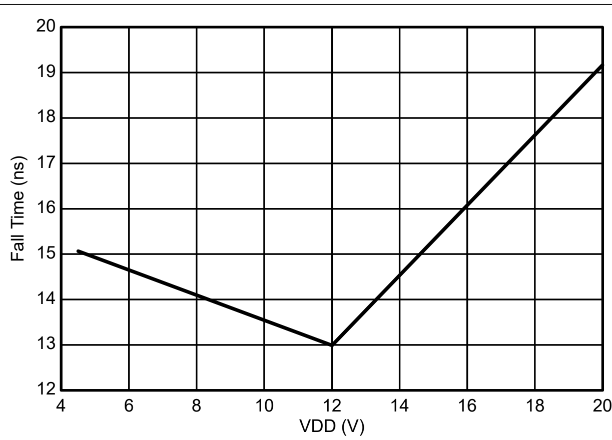


Figure 6-11. Output Pulldown Resistance



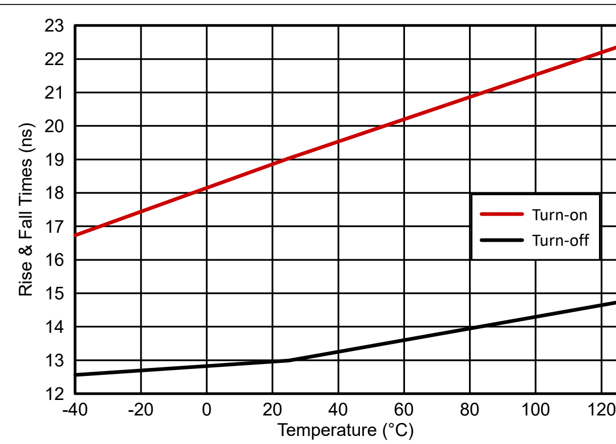
C_{LOAD} = 10 nF

Figure 6-12. Output Rise Time vs VDD



C_{LOAD} = 10 nF

Figure 6-13. Output Fall Time vs VDD

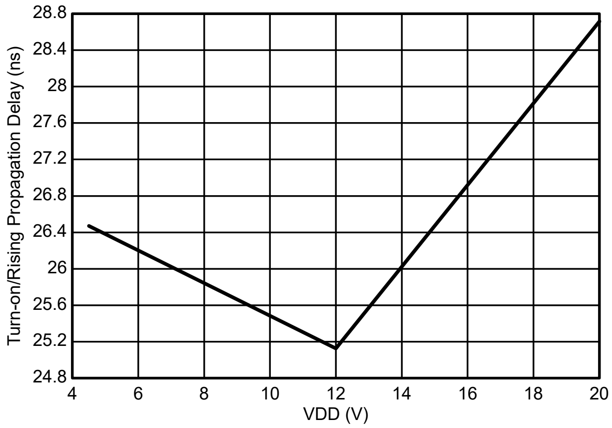


C_{LOAD} = 10 nF

Figure 6-14. Output Rise and Fall Time vs Temperature

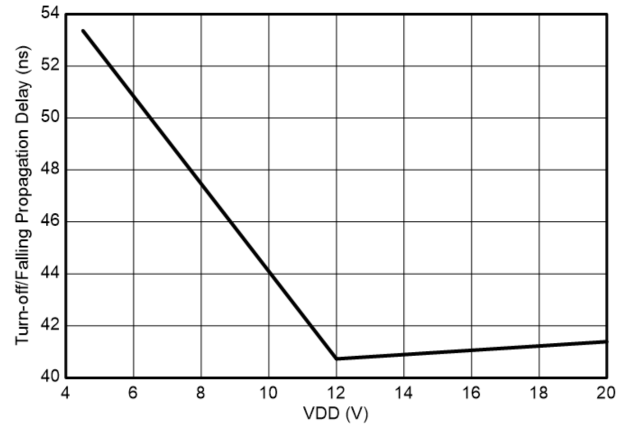
6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, IN+=3.3V, IN-=GND, T_J = 25 °C, no load



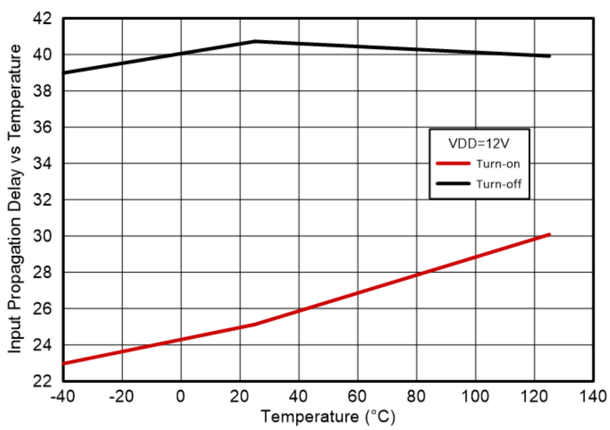
C_{LOAD} = 10 nF

Figure 6-15. Input to Output Rising (turn-on) Propagation Delay vs VDD



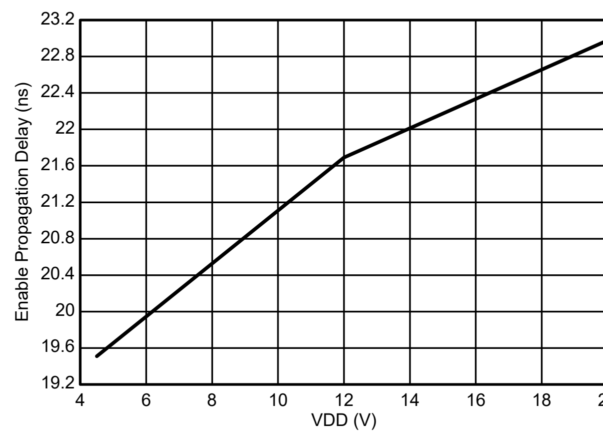
C_{LOAD} = 10 nF

Figure 6-16. Input to Output Falling (turn-off) Propagation Delay vs VDD



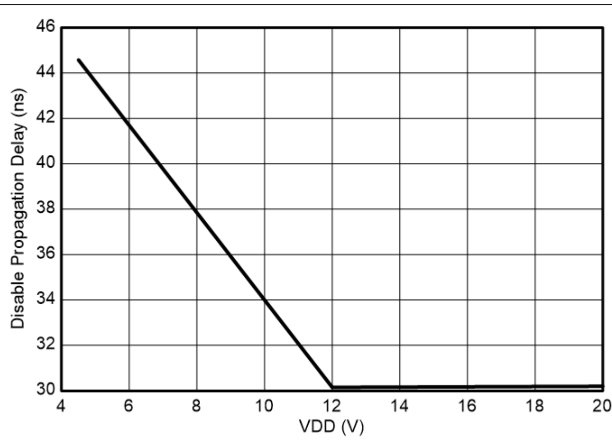
C_{LOAD} = 10 nF

Figure 6-17. Input Propagation Delay vs Temperature



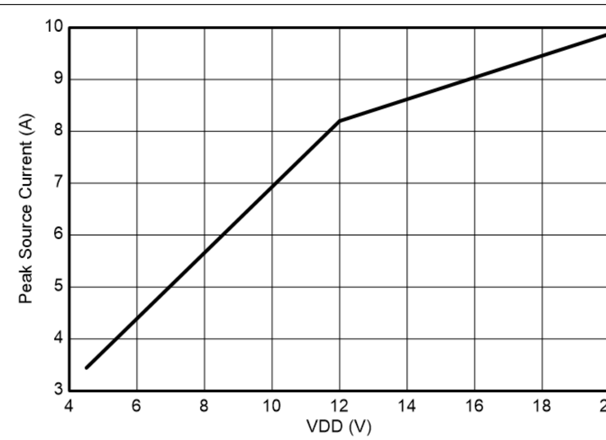
C_{LOAD} = 10 nF

Figure 6-18. Enable to Output Rising Propagation Delay



C_{LOAD} = 10 nF

Figure 6-19. Enable to Output Falling Propagation Delay

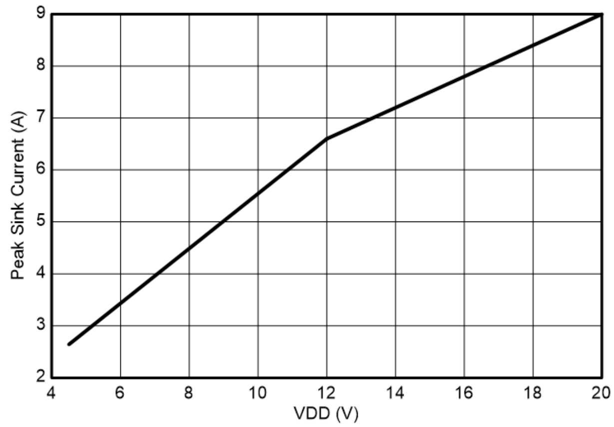


C_{LOAD} = 10 nF

Figure 6-20. Peak Source Current vs VDD

6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, IN+=3.3V, IN-=GND, T_J = 25 °C, no load



C_{LOAD} = 10 nF

Figure 6-21. Peak Sink Current vs VDD

7 Detailed Description

7.1 Overview

The UCC27332-Q1 deviceis a single-channel, high-speed, gate drivers capable of effectively driving MOSFET, and GaN power switches with 9-A source and 9-A sink (symmetrical drive) peak current. A strong source and sink capability boost immunity against a parasitic Miller turnon effect. The UCC27332-Q1 device can be directly connected to the gate driver transformer or line driver transformer as the inputs of UCC27332-Q1 can handle –5V. The driver has a good transient handling capability on its output due to reverse currents, as well as rail-to-rail drive capability and small propagation delay, typically 23 ns.

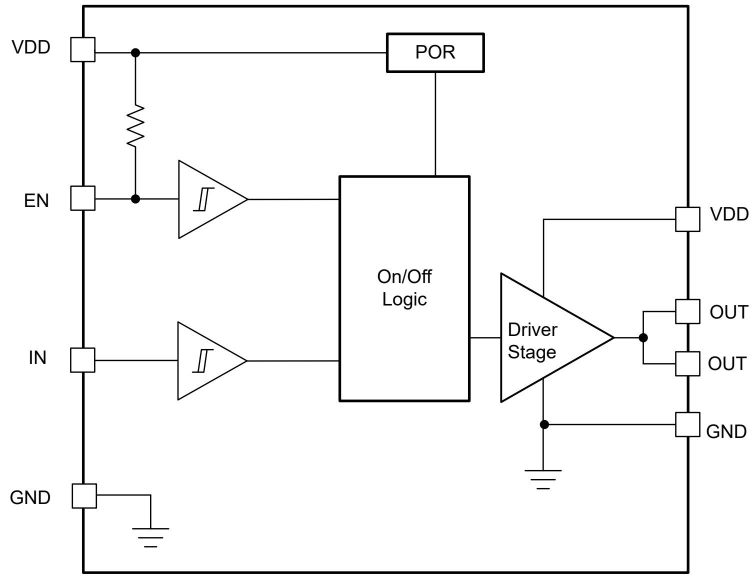
The input threshold of UCC27332-Q1 is compatible to TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

The driver has an EN pin with fixed TTL compatible threshold. EN is internally pulled up; pulling EN low disables the driver, while leaving EN open provides normal operation. The EN pin can be used as an additional input with similar performance as the IN pin.

Table 7-1. UCC27332-Q1 Features and Benefits

FEATURE	BENEFIT
–5 V IN and EN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver.
High source and sink current capability 9 A	High current capability helps drive large gate charge loads to minimize switching losses.
Low 25 ns (typ) propagation delay.	Extremely low pulse transmission distortion
Wide VDD operating range of 4.5 V to 18 V	Flexibility in system design
EN can float	Safe operation when the output of the controller ties to the EN pin in tristate
Strong sink current (9 A) and low pulldown impedance (0.4Ω)	High immunity to high dV/dt Miller turnon events
TTL compatible input threshold logic with wide hysteresis	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power

7.2 Functional Block Diagram



Typical EN pullup resistance is 100 kΩ.

7.3 Feature Description

7.3.1 VDD Power On Reset

The UCC27332-Q1 device offers an power on reset lockout threshold of 3.0 V (rising). The device's hysteresis range helps to avoid any chattering due to the presence of noise on the bias supply. 0.3 V of typical POR hysteresis is expected for 4-V devices. There is no significant driver output turnon delay due to the POR feature. The POR turn-off delay is also minimized as much as possible. The POR delay is designed to minimize chattering that may occur due to very fast transients that may appear on VDD. When the bias supply is below POR thresholds, the outputs are held actively low irrespective of the state of input pins and enable pin. The device accepts a wide range of slew rates on its VDD pin.

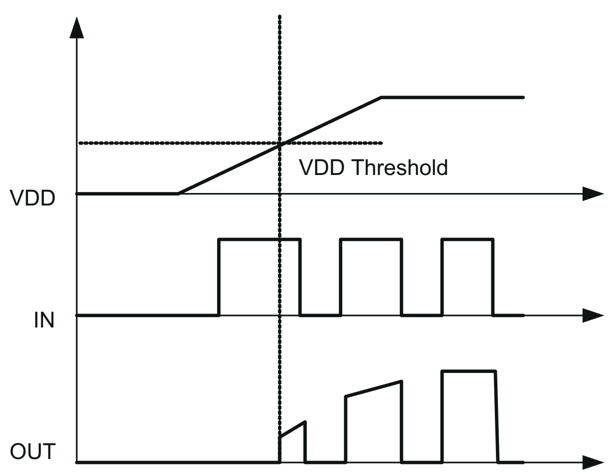


Figure 7-1. Power Up

7.3.2 Input Stage

The inputs of the UCC27332-Q1 device are compatible with TTL based threshold logic andthe inputs are independent of the VDD supply voltage. With typical high threshold of 2.2 V and typical low threshold of 1.2 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or

5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V.

The device high resistance driver input (IN) reduces leakage currents in the input pin. The driver input signals are expected to be in a defined high or low state to control the driver outputs. If a controller is used which may have undefined or tri-state conditions on the driver control signals, it is recommeded to have an external pull down resistance from the IN pin to ground.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 25-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

An external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This also limits the rise or fall times to the power device which reduces the EMI. The external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

7.3.3 Enable Function

The Enable (EN) pin of the UCC27332-Q1 device also has TTL compatible input thresholds with wide hysteresis. The typical turnon threshold is 2.3V and the typical turn-off threshold is 1.8V with typical hysteresis of 0.7V. The Enable (EN) pin of the UCC27332-Q1 has an internal pullup resistor to an internal reference voltage. Thus, leaving the Enable pin floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver. There is minimum delay from the enable block to the output for fast system response time.

7.3.4 Output Stage

The output stage of the UCC27332-Q1 device is illustrated in Figure 7-2. The UCC27332-Q1 device features a P-Channel on the pull up structure, which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain/collector voltage experiences dV/dt). This pull up architecture closely emulates the behavior of the popular industry driver devices UCC2732x. One characteristic of this pull up driver stage architecture is relatively consistent driver output rise and fall times over a wide VDD range.

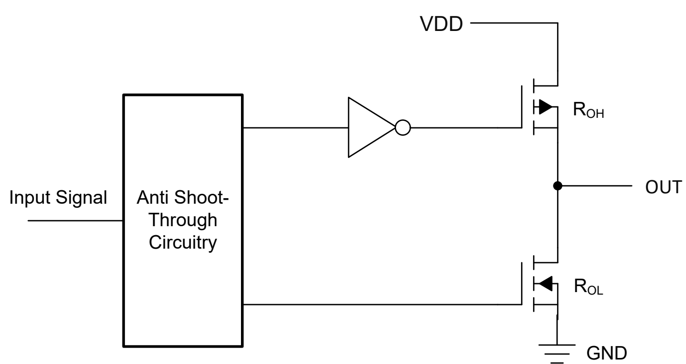


Figure 7-2. UCC27332-Q1 Gate Driver Output Stage

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device on the pull up stage of the driver output. The pulldown structure is composed of a

N-channel MOSFET only. The R_{OL} is also a DC measurement, and it is representative of true impedance of the pulldown stage in the device.

The UCC27332-Q1 can deliver 9-A source, and up to 9-A sink at VDD = 14 V. Strong sink capability results in a very low pulldown impedance in the driver output stage which boosts immunity against the parasitic Miller turnon (high slew rate dV/dt turnon) effect that is seen in FET power switches.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in OFF state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in Figure 7-3.

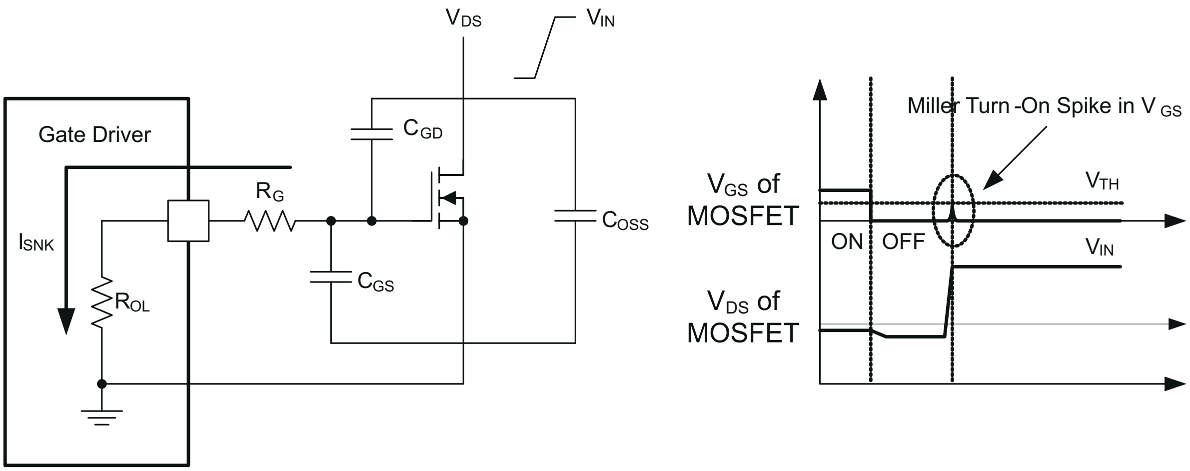


Figure 7-3. Low Pull-Down Impedance in UCC27332-Q1 (Output Stage Mitigates Miller Turnon Effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation because of the low dropout of the output stage. In most applications, the external Schottky diode clamps may be eliminated because the presence of the MOSFET body diodes offers low impedance to switching overshoots and undershoots. The output stage of the UCC27332-Q1 devices can handle significant transient reverse current. The two OUT pins of the device should be shorted on the application board. The application may use resistor and parallel diode-resistor combination at the gate of the MOSFET to program different rise (pullup current) time and fall (pulldown) time.

7.4 Device Functional Modes

The UCC27332-Q1 devices operate in normal mode and POR mode (see Section 7.3.1 for information on POR operation). In normal mode, the output state is dependent on the states of the device, and the input pins.

The UCC27332-Q1 features a single, non-inverting input, but also contains enable and disable functionality through the EN pin. Setting the EN pin to logic HIGH will enable the non-inverting input to output on the IN pin. The two OUT pins are internally shorted and shall be shorted on the application board as well.

Table 7-2. UCC27332-Q1 Truth Table

IN	EN	OUT
H	L	L
H	H	H
L	H	L
L	L	L
Float	L	L
Float	H	X

Table 7-2. UCC27332-Q1 Truth Table (continued)

IN	EN	OUT
Any	Float	IN

Note

The IN pin does not have an internal pulldown resistance, TI recommends an external pulldown resistor if the IN signal can be high impedance. X indicates a possible high or low state.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27332-Q1 is very flexible in this role with a strong drive current capability and wide recommended supply voltage range of 4.5V to 18 V. This allows the driver to be used in 5-V bias logic level very high frequency MOSFET applications and 12-V MOSFET applications. As a single-channel driver, the UCC27332-Q1 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as a bias supply that is referenced to the UCC27332-Q1 ground pin. Alternatively, in a high-side drive configuration the UCC27332-Q1 can be tied directly to the controller signal and biased with a nonisolated supply. However, in this configuration the output of the UCC27332-Q1 must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch.

These requirements, coupled with the need for low propagation delays and availability in compact, and low-inductance packages with good thermal capability, make gate driver devices such as the UCC27332-Q1 extremely important components in switching power combining benefits of high-performance, low cost, low component count, board space reduction and simplified system design.

8.2 Typical Application

8.2.1 Driving MOSFET

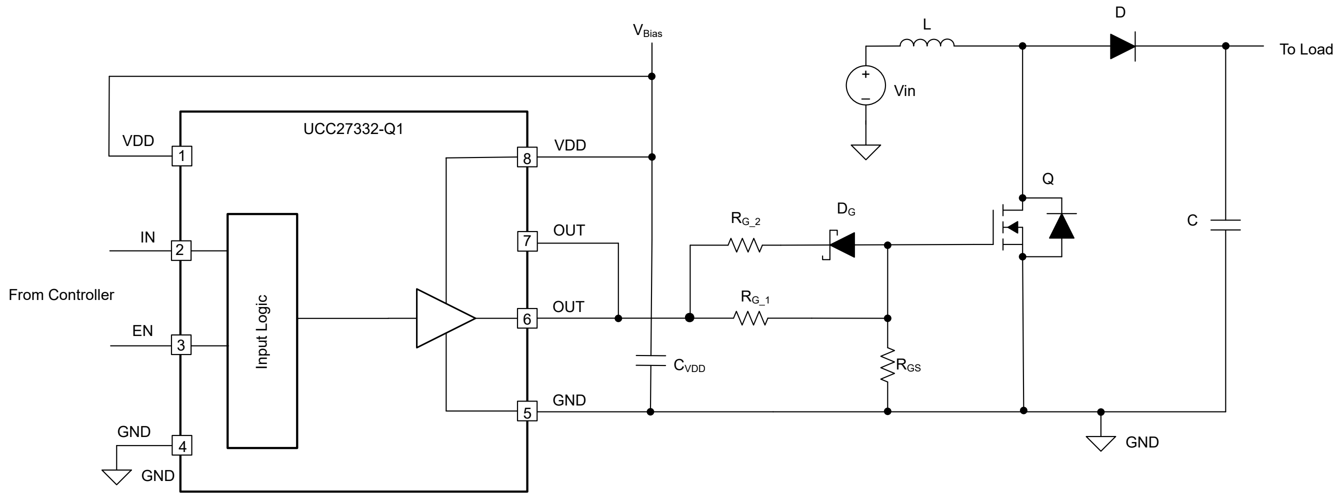


Figure 8-1. Driving a MOSFET in a Boost Converter

8.2.1.1 Design Requirements

When selecting the gate driver device for an end application, some design considerations must be evaluated in order to make the most appropriate selection. Following are some of the design parameters that should be used when selecting the gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input to output logic	Non-inverting
Input threshold type	TTL
Bias supply voltage levels	+18 V
Negative output low voltage	N/A
dV_{DS}/dt[1]	100 V/ns
Enable function	Yes
Disable function	N/A
Propagation delay	<30 ns
Power dissipation	<1 W
Package type	MSOP8

(1) dV_{DS}/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in Section 8.2.1.2.4.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input-to-Output Configuration

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET when the input signal is in high state is preferred, then a device capable of the non-inverting configuration must be selected. If turning off the power MOSFET when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen.

If ground-bouncing is a potential issue, a gate driver with negative voltage handling capability should be chosen. UCC27332-Q1 devices can handle -5-V at its input and -2-V on its output. The input of the UCC27332-Q1 devices can handle wide range of slew rate at its input and the inputs have wide hysteresis.

8.2.1.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC27332-Q1 devices feature a TTL compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the Electrical Characteristics table for the actual input threshold voltage levels and hysteresis specifications for the UCC27332-Q1 devices.

8.2.1.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should not exceed the values listed in the Recommended Conditions table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turn-off. With an operating range from 4.5 V to 18 V, the UCC27332-Q1 devices can be used to drive a power switches such as logic level MOSFETs, power MOSFETS, and GaN devices.

8.2.1.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turn-off should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power switching devices such as logic level MOSFETs, power MOSFETs, and GaN.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a 600V power MOSFET must be turned on with a dV_{DS}/dt of 100 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 4 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{GD} parameter of the 600V power MOSFET, let us say, is 32 nC) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(th)}$.

To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 4 ns or less. In other words a peak current of 8 A (= 32 nC / 4 ns) or higher must be provided by the gate driver. The UCC27332-Q1 series of gate drivers can provide 9-A peak sourcing current, and 9A peak sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The significantly high drive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ($\frac{1}{2} \times I_{Peak} \times$ time) would equal the total gate charge of the 600V power MOSFET (Q_G parameter in the power MOSFET datasheet). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_G of the switching power MOSFET. In other words, the time parameter in the above equation would dominate and the I_{Peak} value of the current pulse would be much less than the true peak current capability of the driver, while the required Q_G is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed.

Thus, placing the gate driver device very close to the power MOSFET and designing a very small gate drive-loop with minimal PCB trace inductance is important to realize fast switching.

8.2.1.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input PWM signal. A pin which offers an enable and disable function achieves this requirement. For these applications, the UCC27332-Q1 is suitable as it features an input pin (IN) and an Enable pin (EN). Both of these pins are independent of each other .

8.2.1.2.6 Propagation Delay and Minimum Input Pulse Width

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27332-Q1 devices feature 25-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high frequencies. Very high switching frequency applications also need the gate driver to satisfactorily produce the output pulse when the input pulse width is very small. The UCC27332-Q1 devices can typically handle 20ns at its input and produce satisfactory output depending on the load. See Switching Characteristics table for the propagation and other timing specifications of the UCC27332-Q1 devices.

8.2.1.2.7 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \tag{1}$$

The DC portion of the power dissipation is P_{DC} = I_Q × VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections,and so on, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of internal parasitic capacitances, parasitic shoot-through). The UCC27332-Q1 features low quiescent currents (less than 1 mA) and contains internal logic to minimize any shoot-through (PMOS to NMOS and vice versa) in the output driver stage. Thus, the effect of the P_{DC} on the total power dissipation within the gate driver can be assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

As explained in earlier sections, the output stage of the gate driver is based on PMOS and NMOS. These NMOS and PMOS are designed in such a way that they offer very low resistance during switching. And therefore they have very low drop-out. The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OUT} drop-out)
- Switching frequency
- Power MOSFET internal and external gate resistor

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. During turnoff the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} \tag{3}$$

where

- f_{SW} is the switching frequency

The switching load presented by a power FET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD}V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver IC and MOSFET, this power is completely dissipated inside the driver IC. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as shown in following equation. This primarily applies to those applications where total external gate resistor is significantly large to limit the peak current of the gate driver.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \tag{5}$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pullup structure)

8.2.1.3 Application Curves

The figures below show the switching characteristic for the UCC27332-Q1. The test condion: load capacitance is 1.8 nF, gate resistor is 0 Ω, driver supply voltage is 12 V, switching frequency is 100 kHz.

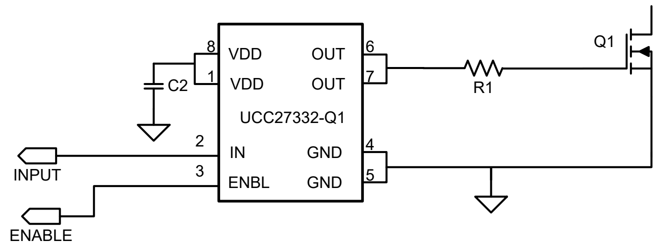
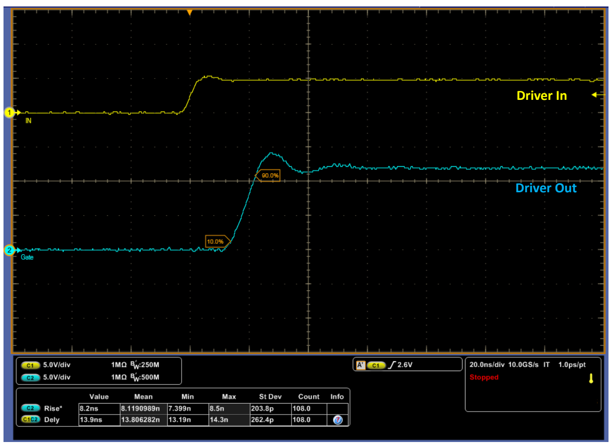
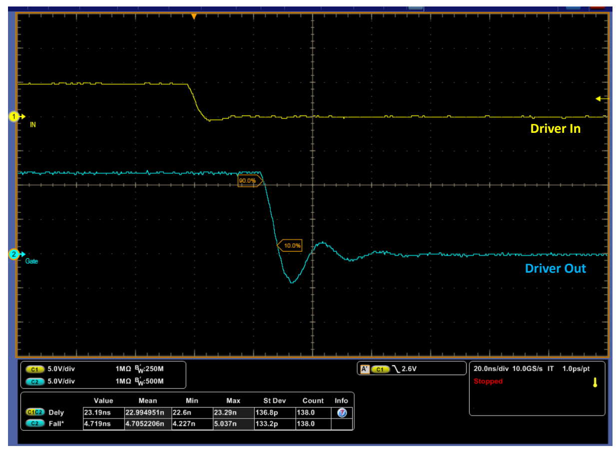


Figure 8-2. Typical Application Diagram of UCC27332-Q1



Cload = 1.8 nF Fsw = 100 kHz, driver supply voltage = 12 V, gate resistor = 0 Ω

Figure 8-3. UCC27332-Q1 Rise Time and Turn-On Propagation Delay



Cload = 1.8 nF, Fsw = 100 kHz, driver supply voltage = 12 V, gate resistor =0 Ω

Figure 8-4. UCC27332-Q1 Fall Time and Turn-Off Propagation Delay

8.3 Power Supply Recommendations

The bias supply voltage range for which the UCC27332-Q1 devices are recommended to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal POR protection feature on the VDD pin supply circuit blocks. Whenever the driver is in POR condition when the VDD pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 18-V recommended maximum voltage rating of the VDD pin of the device. The absolute maximum voltage for the VDD pin is 20 V.

The POR protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, ensuring that, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD POR falling threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up, the device does not begin operation until the VDD pin voltage has exceeded above the VDD POR rising threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUT pin is also supplied through the same VDD pin is important. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is needed. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitorplaced less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel.

UCC27332-Q1 is a high current gate driver. If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. Large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

8.4 Layout

8.4.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27332-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver device as close as possible to power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place the bypass capacitors between VDD pin and the GND pin as close to the driver pins as possible to minimize trace length for improved noise filtering. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another ceramic surface-mount capacitor of few microfarads added in parallel. These capacitors support high peak current being drawn from VDD during turnon of power switch. The use of low inductance surface-mount components such as chip capacitors is highly recommended.
- The turnon and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turnon and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at a single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin may corrupt the input signals during transitions. The ground plane must not be a conduction path for any current loop. Instead the ground plane should be connected to the star-point with one trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

8.4.2 Layout Example

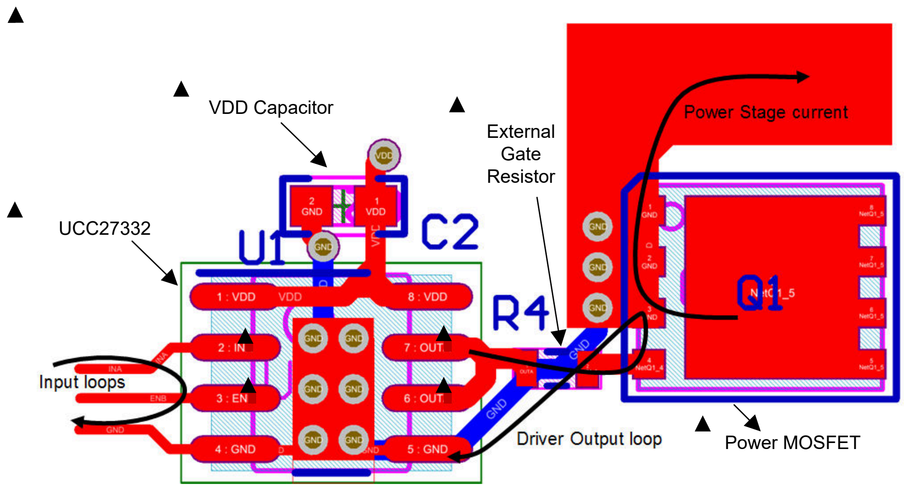


Figure 8-5. Layout Example: UCC27332-Q1

8.4.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the Thermal Characteristics section of the datasheet. For detailed information regarding the thermal information table, refer to *IC Package Thermal Metrics Application Note* (SPRA953).

9 Device and Documentation Support

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27332QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	332Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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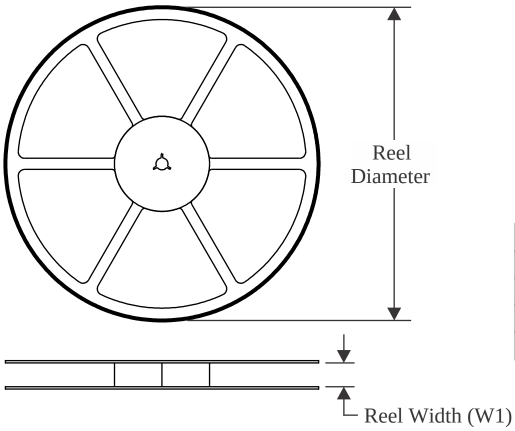
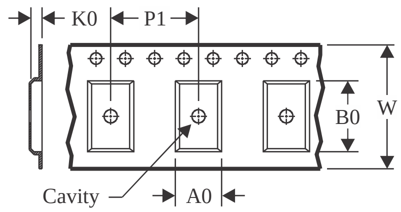
TAPE AND REEL INFORMATION

REEL DIMENSIONS

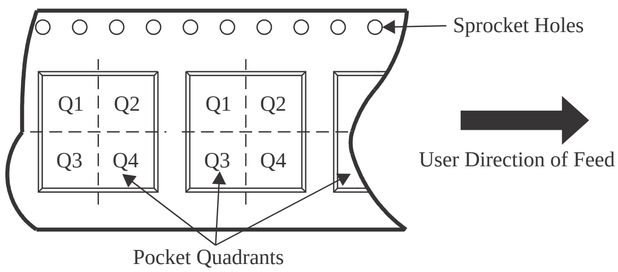


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

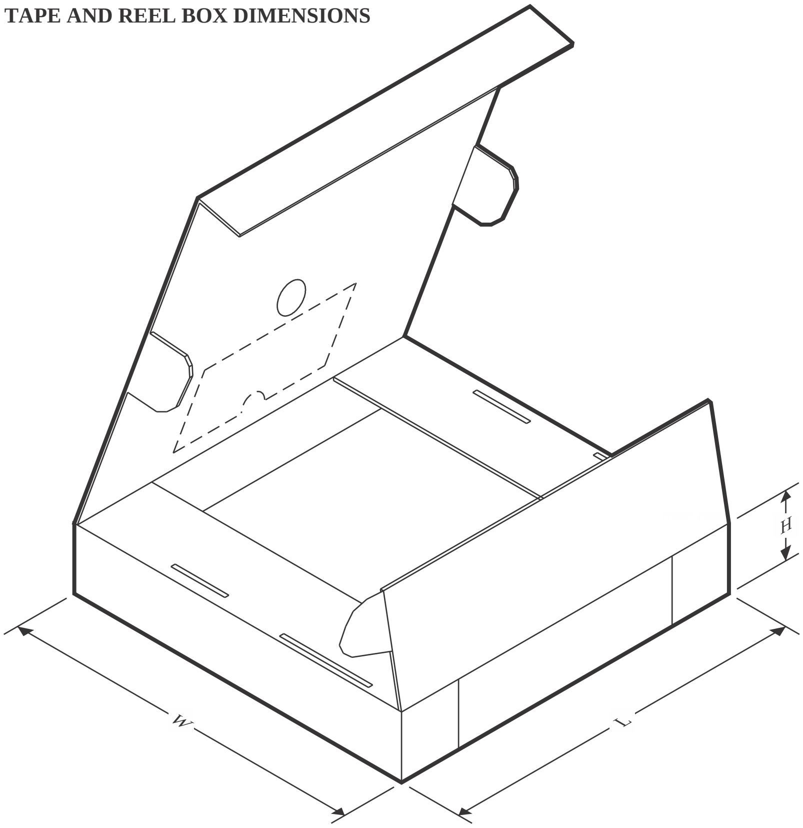
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27332QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

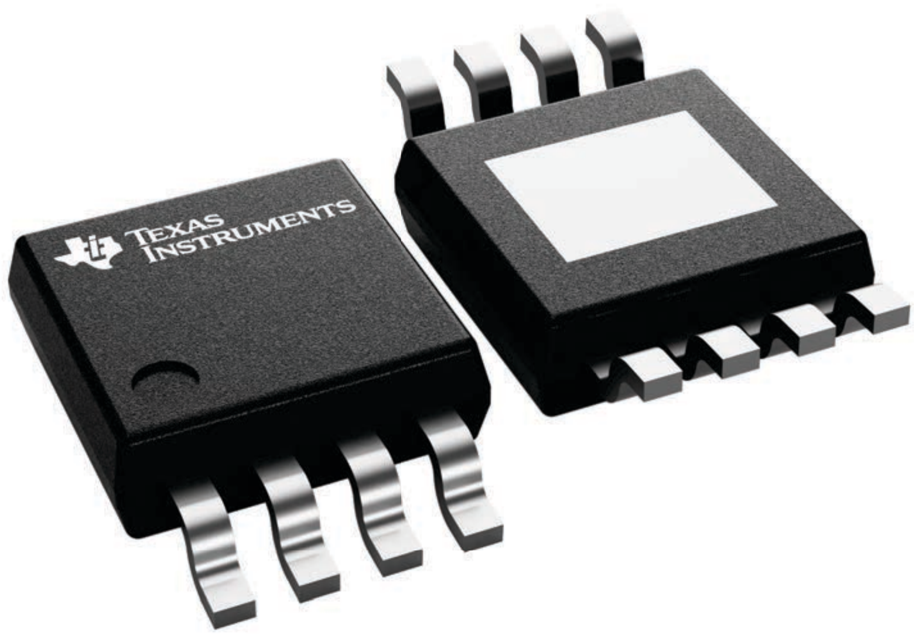
TAPE AND REEL BOX DIMENSIONS

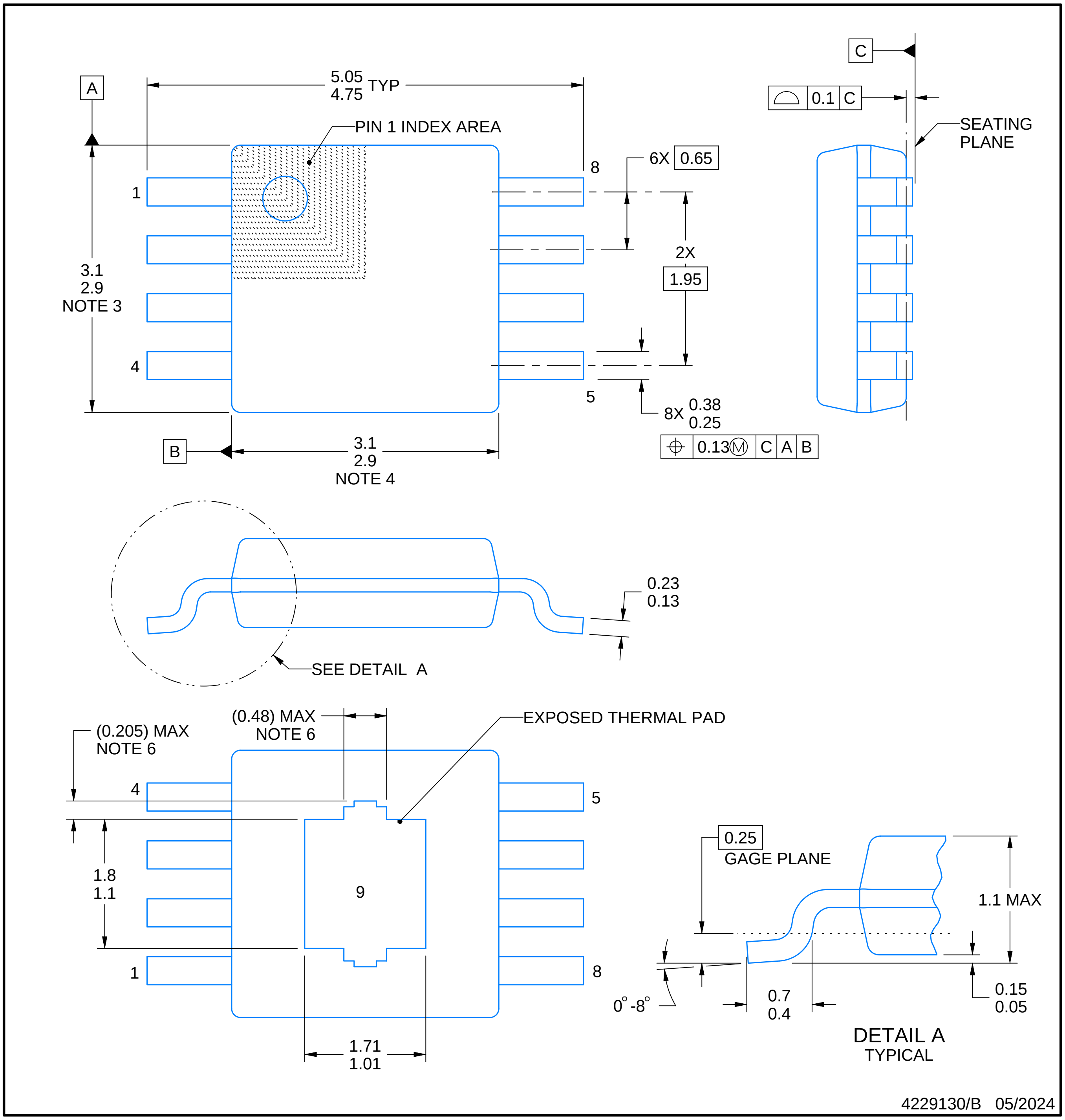


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27332QDGNRQ1	HVSSOP	DGN	8	2500	356.0	356.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



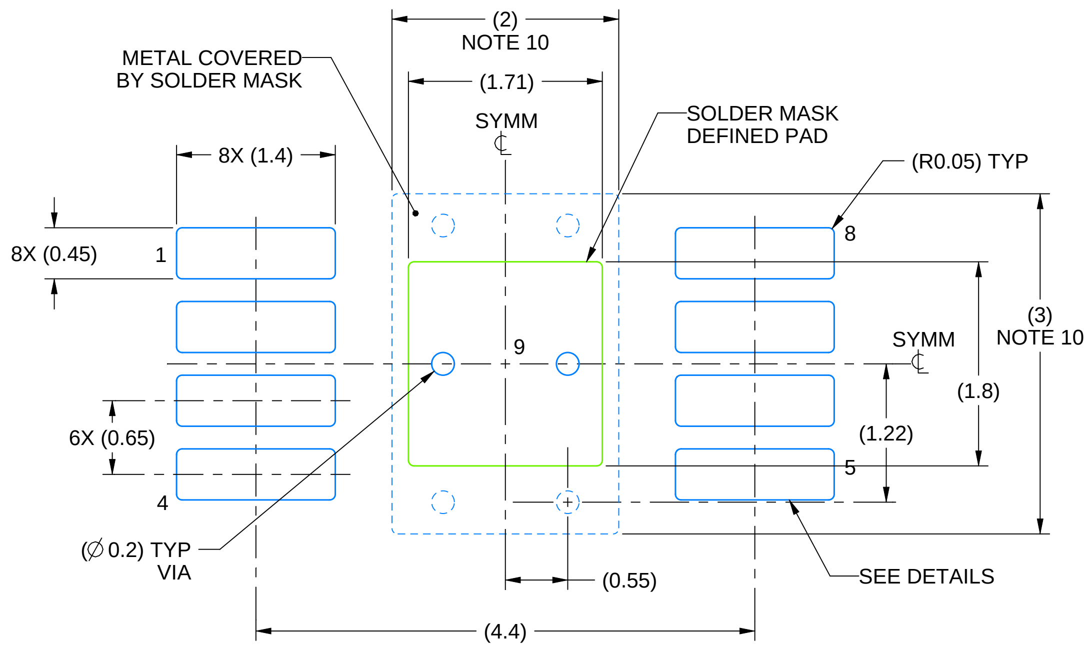


4229130/B 05/2024

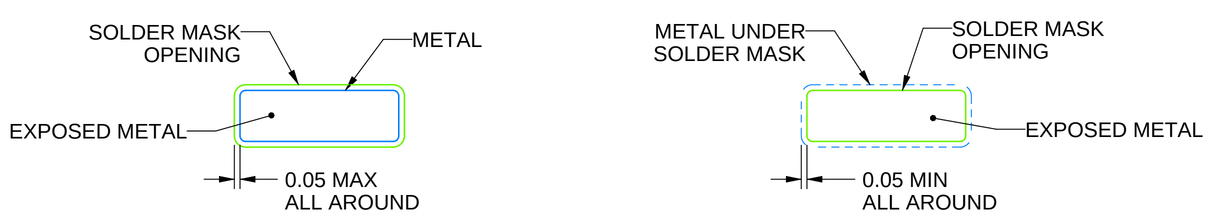
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

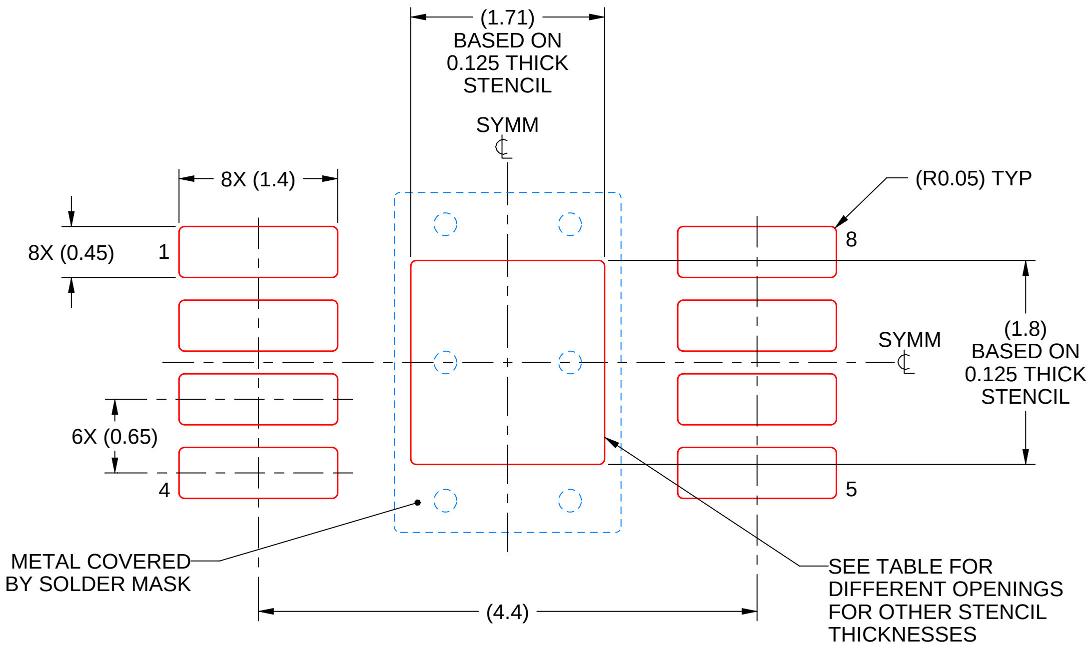
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

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