RAD-TOLERANT, HIGH-SPEED PWM CONTROLLER

Check for Samples: UC1825-DIE

FEATURES

- **Rad-Tolerant: 30 kRad (Si) TID** (1)
- **Compatible With Voltage- or Current-Mode Topologies**
- **Practical Operation Switching Frequencies**
- **50-ns Propagation Delay-to-Output**
- **High-Current Dual Totem Pole Outputs**
- **Wide Bandwidth Error Amplifier**
- **Fully Latched Logic With Double-Pulse Suppression**
- **Pulse-by-Pulse Current Limiting**
- **Soft Start/Maximum Duty-Cycle Control**
- **Undervoltage Lockout With Hysteresis**
- **Low Start-Up Current**

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

DESCRIPTION

The UC1825-DIE PWM control device is optimized for high-frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty-cycle clamp. The logic is fully latched to provide jitter-free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start up current. During undervoltage lockout, the outputs are high impedance.

This device features totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
UC1825	TD	Bare die in waffle pack(2)	UC1825VTD1	88
			UC1825VTD2	10

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	AlCu2%	2000 nm

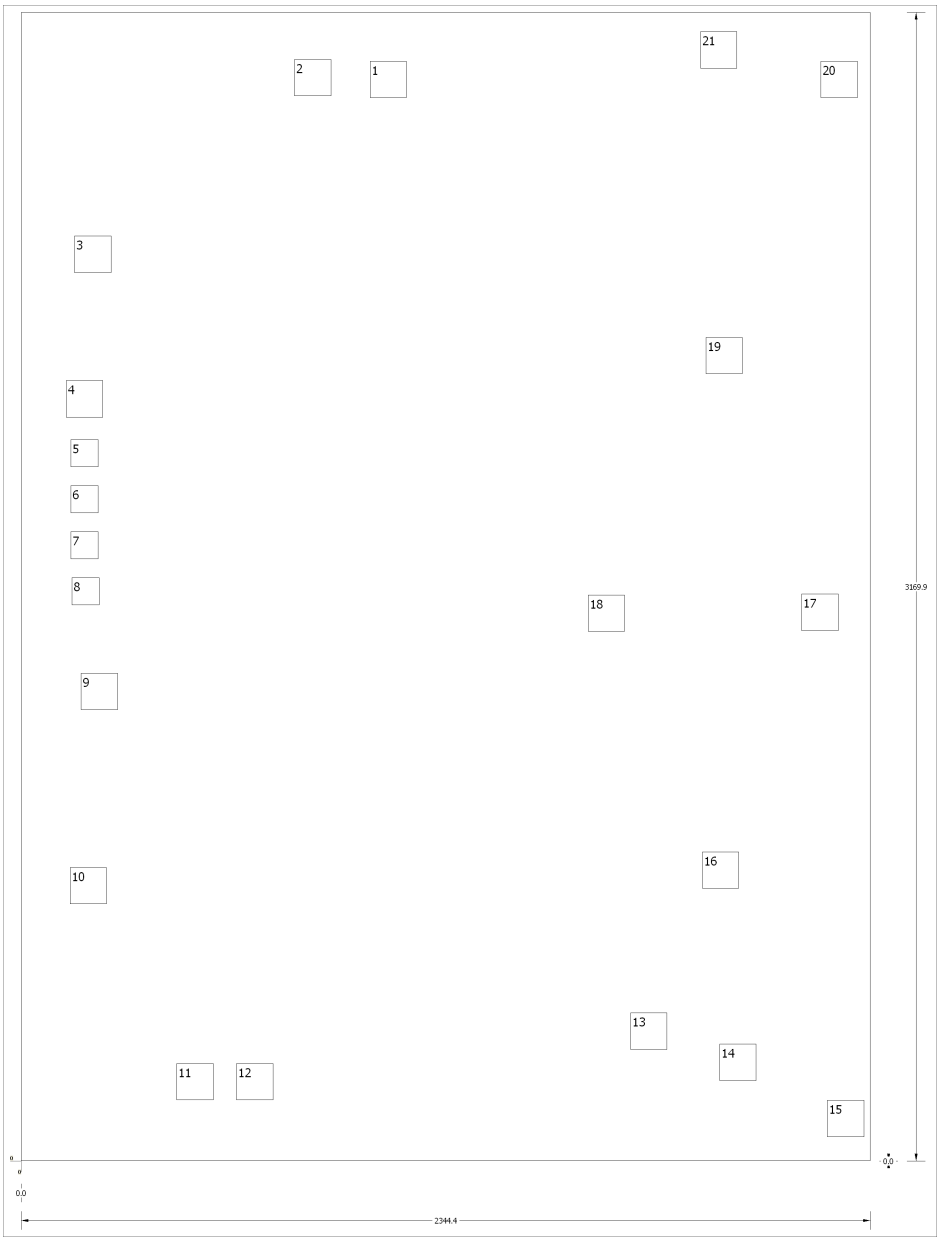

Table 1. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
INV	1	962.685	2933.725	1064.285	3035.325
NI	2	754.405	2938.805	856.005	3040.405
E/A OUT	3	147.345	2451.125	248.945	2552.725
CLOCK	4	124.485	2052.345	226.085	2153.945
N/C	5	137.185	1915.185	213.385	1991.385
N/C	6	137.185	1788.185	213.385	1864.385
N/C	7	137.185	1661.185	213.385	1737.385
N/C	8	139.725	1534.185	215.925	1610.385
RT	9	165.125	1244.625	266.725	1346.225
CT	10	134.645	708.685	236.245	810.285
RAMP	11	429.285	167.665	530.885	269.265
SOFT START	12	594.385	167.665	695.985	269.265
ILIM/SD	13	1681.505	307.365	1783.105	408.965
N/C	14	1927.885	221.005	2029.485	322.605
GND	15	2225.065	66.065	2326.665	167.665
OUT A	16	1879.625	751.865	1981.225	853.465
PWR GND	17	2153.945	1463.065	2255.545	1564.665
VC	18	1564.665	1460.525	1666.265	1562.125
OUT B	19	1889.785	2171.725	1991.385	2273.325
VCC	20	2207.285	2933.725	2308.885	3035.325
VREF	21	1874.545	3015.005	1976.145	3116.605

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1825VTD1	ACTIVE			0	88	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples
UC1825VTD2	ACTIVE			0	10	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1825-DIE :

- Space : UC1825-SP

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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