TUSB217-Q1 USB High Speed Signal Conditioner

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 2: –40°C to 105°C T_A
- Wide Supply Voltage Range: 2.3 - 6.5 V
- Ultra-low USB Disconnect and Shutdown Power Consumption
- Provides USB 2.0 High Speed Signal Conditioning
- Compatible with USB 2.0, OTG 2.0 and BC 1.2
- Support for Low Speed, Full Speed, High Speed Signaling
- Host/Device Agnostic
- Supports up to 5m Cable Length
  - Four Selectable Signal Boost (Edge Boost Along with DC Boost) Setting via External Pull Down Resistor
  - Three Selectable RX Sensitivity via Pull Up or Down Configurable Pin to Compensate ISI Jitter for High Loss Applications
- Scalable Solution - Daisy Chain Devices for High Loss Applications
- Pin Compatible with TUSB213 (5V)

2 Applications

- Automotive Infotainment
- Automotive Head Unit
- Automotive Media Hub
- Laptop/Desktop/Docking Stations
- Tablets/Cell Phones
- Televisions
- Active Cable, Cable Extenders
- Backplane

3 Description

The TUSB217-Q1 is a third generation USB 2.0 high speed signal conditioner designed to compensate both AC loss (due to capacitive load) and DC loss (due to resistive loss) in the transmission channel.

The TUSB217-Q1 has a patented design that speeds up transition edges of USB 2.0 high speed signal with an edge booster and increases static levels with a DC boost function. In addition, the TUSB217-Q1 includes a pre-equalization function to improve the receiver sensitivity and compensate the ISI jitter in application with longer cable length. USB low speed and full speed signal characteristics are unaffected by the TUSB217-Q1.

The TUSB217-Q1 improves signal quality without altering packet timing or adding propagation delay, making it ideal for applications that require low latency.

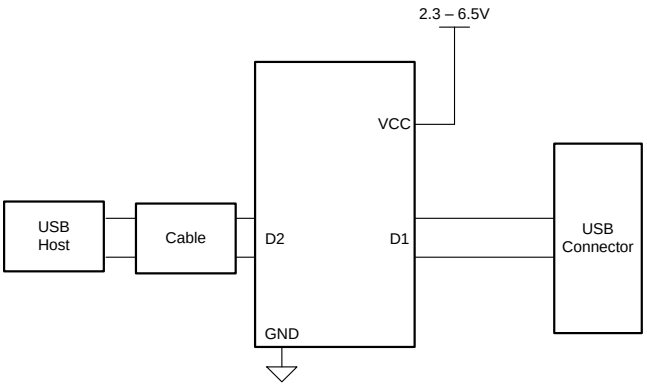
The TUSB217-Q1 helps a system to pass the USB 2.0 high speed electrical near end eye compliance tests with a cable as long as 5 meters.

The TUSB217-Q1 is compatible with the USB On-The-Go (OTG) and Battery Charging (BC 1.2) protocols.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB217-Q1	VQFN (14)	3.50 mm x 3.50 mm

Simplified Schematic



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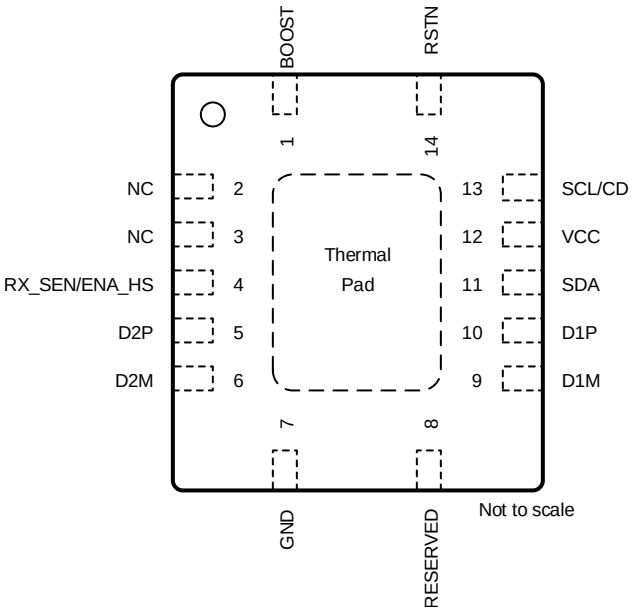
4 Revision History

Changes from Original (September 2018) to Revision A	Page
• Changed the document status From: *Advanced Information* To: *Production* data	1

5 Pin Configuration and Functions

RGY Package
14 Pin (VQFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
BOOST	1	I	N/A	USB High Speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
NC	2,3	I		Leave unconnected
RESERVED	8	O		Leave unconnected or connect a decoupling cap 0.1μF
RX_SEN(1)/ENA_HS	4	I/O	N/A	In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High Speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) – high RX sensitivity (high loss channel) M (pin is left floating) – medium RX sensitivity (medium loss channel) L (pin is pulled low) – low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 μs – 128 μs].
D2P	5	I/O	N/A	USB High Speed positive port.
D2M	6	I/O	N/A	USB High Speed negative port.
GND	7	P	N/A	Ground
D1M	9	I/O	N/A	USB High Speed negative port..
D1P	10	I/O	N/A	USB High Speed positive port.

(1) Pull-down and pull-up resistors for RX_SEN pin must follow R_{RXSEN1} and R_{RXSEN2} resistor recommendations in non I^2C mode.

Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
SDA[2]	11	I/O	500 kΩ PU 1.8 MΩ PD	I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
VCC	12	P	N/A	Supply power
RSTN	14	I	500 kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
SCL[2]/CD	13	I/O	When RSTN asserted there is a 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
Thermal Pad	TPAD	N/A	N/A	Thermal Pad is electrically not connected to device ground. Connection to board ground is optional.

(2) Pull-up resistors for SDA and SCL pins in I^2C mode should be $R_{Pull-up}$ (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I^2C mode.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	7	V
Voltage range USB data	DxP, DxM	–0.3	5.5	V
Voltage range on BOOST pin	BOOST	-0.3	1.98	V
Voltage range other pins	SCL, SDA, RX_SEN, RSTN	-0.3	5	V
Storage temperature, T_{stg}		–65	150	°C
Maximum junction temperature, $T_{J\ (max)}$			125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100- 011 CDM ESD Classification Level C4A	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.3	5	6.5	V
T_A	Operating free-air temperature (AEC-Q100)	–40		105	°C
T_J	Junction temperature (AEC-Q100)			115	°C
V_{I2C_BUS}	I2C Bus Voltage	1.62		3.6	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
SCL, SDA, RX_SEN, RSTN	Voltage range other pins (SCL, SDA, RX_SEN, RSTN)	0		3.6	V

6.4 Thermal Information

THERMAL METRIC (1)		RGY (VQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable, with Boost = Max		22	36	mA
I_{IDLE_HS}	High Speed Idle Current	USB channel = HS mode, no traffic. V_{CC} supply stable, Boost = Max		22	36	mA
$I_{HS\_SUPSPEND}$	High Speed Suspend Current	USB channel = HS Suspend mode. V_{CC} supply stable		0.75	1.4	mA
I_{FS}	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V_{cc} supply stable		0.75	1.4	mA
$I_{DISCONN}$	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I_{SHUTDN}	Shutdown Power	RSTN driven low, V_{CC} supply stable		35	95	µA
CONTROL PIN LEAKAGE						
I_{LKG_FS}	Pin failsafe leakage current for SDA, RSTN	V_{CC} = 0 V, pin at $V_{IH,\ max}$		10	15	µA
I_{LKG_FS}	Pin failsafe leakage current for BOOST, RX_SEN	V_{CC} = 0 V, pin at $V_{IH,\ max}$		6	10	µA
I_{LKG_FS}	Pin failsafe leakage current for SCL	V_{CC} = 0 V, pin at $V_{IH,\ max}$			70	nA
INPUT RSTN						
V_{IH}	High level input voltage		1.5		3.6	V
V_{IL}	Low-level input voltage		0		0.5	V
I_{IH}	High level input current	V_{IH} = 3.6 V, R_{PU} enabled			±15	µA
I_{IL}	Low level input current	V_{IL} = 0V, R_{PU} enabled			±20	µA
INPUT RX_SEN (3-level input, for mid level leave pin floating)						
V_{IH}	High level input voltage R_{RXSEN1}=47kΩ, R_{RXSEN2}=10kΩ	VCC<=4.3V	1.8		3.6	V
V_{IH}	High level input voltage R_{RXSEN1}=37kΩ, R_{RXSEN2}=47kΩ	VCC>4.3V	2.0		3.6	V

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{IL}	Low level input voltage 22kΩ <= R_{RXSEN1} <= 33kΩ				0.4	V
INPUT BOOST						
R_{BOOST_LVL0}	External pulldown resistor for BOOST Level 0				160	Ω
R_{BOOST_LVL1}	External pulldown resistor for BOOST Level 1		1.5	1.8	2	kΩ
R_{BOOST_LVL2}	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	kΩ
R_{BOOST_LVL3}	External pulldown resistor for BOOST Level 3		7.5			kΩ
OUTPUTS CD, ENA_HS						
V_{OH}	High level output voltage	I_O = –50 µA, VCC >= 3.0V	2.5			V
V_{OH}	High level output voltage	I_O = –50 µA, VCC = 2.3V	1.8			V
V_{OL}	Low level output voltage	I_O = 50 µA			0.3	V
I2C						
C_{I2C_BUS}	I^2C Bus Capacitance		4		150	pF
I_{OL}	I^2C open drain output current	V_{OL} = 0.4V	1.5			mA
V_{IL}	V_{I2C_BUS} = 1.8V +/-10%	$R_{Pull-up}$ =1.6kΩ to 2.5kΩ, % of V_{I2C_BUS}			25	%
V_{IL}	V_{I2C_BUS} = 3.3V +/-10%	$R_{Pull-up}$ =2.8kΩ to 7kΩ, % of V_{I2C_BUS}			25	%
V_{IH}	V_{I2C_BUS} = 1.8V +/-10%	$R_{Pull-up}$ =1.6kΩ to 2.5kΩ, % of V_{I2C_BUS}	75			%
V_{IH}	V_{I2C_BUS} = 3.3V +/-10%	$R_{Pull-up}$ =2.8kΩ to 7kΩ, % of V_{I2C_BUS}	75			%
$R_{Pull-up}$	V_{I2C_BUS} = 1.8V +/-10%		1.6	2	2.5	kΩ
$R_{Pull-up}$	V_{I2C_BUS} = 3.3V +/-10%		2.8	4.7	7	kΩ
SCL Frequency					100	kHz
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with VNA at 240 MHz, V_{CC} supply stable, Redriver off		2.5		pF

6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DxP, DxM USB Signals						
F_{BR_DXX}	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable			480	Mbps
t_{R/F_DXX}	Rise/Fall time		100			ps

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER UP TIMING					
T_{RSTN_PW}	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			µs
T_{STABLE}	VCC must be stable before RSTN de-assertion	300			µs
T_{READY}	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	µs
T_{RAMP}	V_{CC} ramp time	0.2		100	ms
I2C (STD)					
t_{SUSTO}	Stop setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	4			µs
t_{HDSTA}	Start hold time, SCL (Tr=600ns-1000ns), SDA (Tf=6.5ns-106.5ns), 100kHz STD	4			µs
t_{SUSTA}	Start setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	4.7			µs
t_{SUDAT}	Data input or False start/stop, setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	250			ns
t_{HDDAT}	Data input or False start/stop, hold time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	5			µs
t_{BUF}	Bus free time between START and STOP conditions	4.7			µs
t_{LOW}	Low period of the I_{2C} clock	4.7			µs
t_{HIGH}	High period of the I_{2C} clock	4			µs
t_F	Fall time of both SDA and SCL signals			300	ns
t_R	Rise time of both SDA and SCL signals			1000	ns

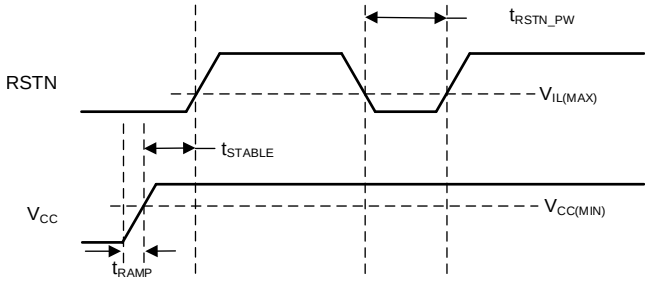


Figure 1. Power On and Reset Timing

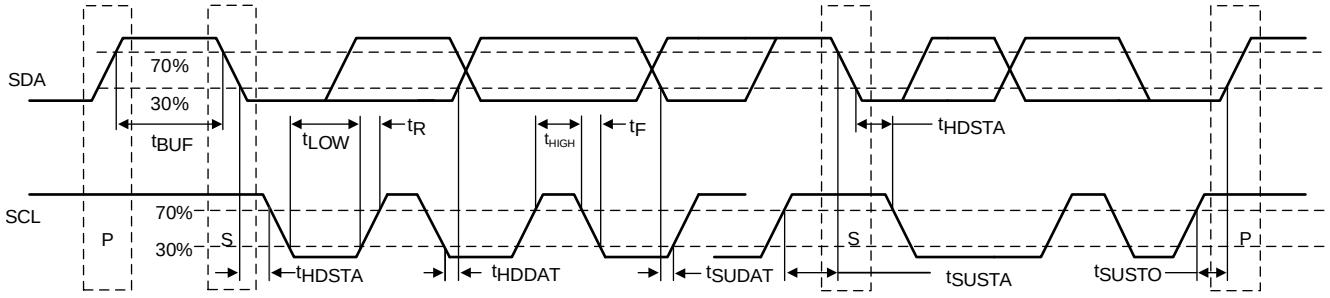


Figure 2. I2C Timing

7 Detailed Description

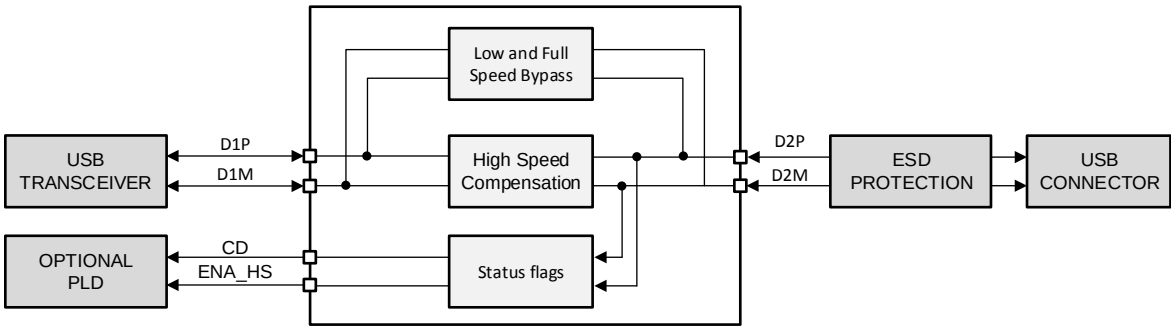
7.1 Overview

The TUSB217-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB217-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB217-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

7.2 Functional Block Diagram

Functional Block Diagram



7.3 Feature Description

7.3.1 High speed boost

The high speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set via I2C register according to I^2C mode. Internal circuitry of the signal conditioner reduces possible overshoot.

7.3.2 RX Sensitivity

The RX_SEN pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

7.4 Device Functional Modes

7.4.1 Low Speed (LS) mode

TUSB217-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

7.4.2 Full Speed (FS) mode

TUSB217-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low

Device Functional Modes (continued)

7.4.3 High Speed (HS) mode

TUSB217-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA_HS pin are asserted high when high speed boost is active.

7.4.4 High Speed downstream port electrical compliance test mode

TUSB217-Q1 will detect HS compliance test fixture and enter downstream port high speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB217-Q1 is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB217-Q1 is operating in HS functional mode, TUSB217-Q1 will transition to HS eye compliance test mode and CD asserts low and ENA_HS remains high. When this occurs signal compensation is enabled.

7.4.5 Shutdown mode

TUSB217-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

Table 1. CD and ENA_HS Pins in Different Modes

MODE	CD	ENA_HS
Low speed	HIGH	LOW
Full speed	HIGH	LOW
High speed	HIGH	HIGH
High speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

7.4.6 I^2C mode

TUSB217-Q1 supports 100 KHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification 2.1, 2001 – STANDARD MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high speed mode.

7.5 TUSB217 Registers

Table 2 lists the memory-mapped registers for the TUSB217 registers. All register offset addresses not listed in Table 2 should be considered as reserved locations and the register contents should not be modified.

Table 2. TUSB217 Registers

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	Go
0x3	CONFIGURATION	This register is selecting device mode.	Go
0xE	DC_BOOST	This register is setting DC BOOST level.	Go
0x25	RX_SEN	This register is setting RX Sensitivity level.	Go

Complex bit access types are encoded to fit into small table cells. Table 3 shows the codes that are used for access types in this section.

Table 3. TUSB217 Access Type Codes

Access Type	Code	Description
Read Type		
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1 EDGE_BOOST Register (Offset = 0x1) [reset = X]

EDGE_BOOST is shown in Figure 3 and described in Table 4.

Return to Summary Table.

This register is setting EDGE BOOST level.

Figure 3. EDGE_BOOST Register

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

Table 4. EDGE_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting) 0x3 = BOOST PIN LEVEL 1 0x6 = BOOST PIN LEVEL 2 0x8 = BOOST PIN LEVEL 3 0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in Figure 4 and described in Table 5.

Return to Summary Table.

This register is selecting device mode.

Figure 4. CONFIGURATION Register

7	6	5	4	3	2	1	0
RESERVED							CFG_ACTIVE
RH/W-X							RH/W-0x1

Table 5. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

Table 5. CONFIGURATION Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode. 0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

7.5.3 DC_BOOST Register (Offset = 0xE) [reset = X]

DC_BOOST is shown in Figure 5 and described in Table 6.

Return to Summary Table.

This register is setting DC BOOST level.

Figure 5. DC_BOOST Register

7	6	5	4	3	2	1	0
RESERVED				DCB_LVL			
RH/W-X				RH/W-X			

Table 6. DC_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting) 0x2 = BOOST PIN LEVEL 1 and 2 0x6 = BOOST PIN LEVEL 3 0xF = (highest dc boost setting)

7.5.4 RX_SEN Register (Offset = 0x25) [reset = X]

RX_SEN is shown in Figure 6 and described in Table 7.

Return to Summary Table.

This register is setting RX Sensitivity level.

Figure 6. RX_SEN Register

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

Table 7. RX_SEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range 0x0 = RX_SEN LEVEL LOW 0x44 = RX_SEN LEVEL MID 0x77 = RX_SEN LEVEL HIGH 0xFF = (highest setting)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The purpose of the TUSB217-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB217-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB217-Q1 to control other blocks on the customer platform, if so desired.

8.2 Typical Application

A typical application is shown in Figure 7. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

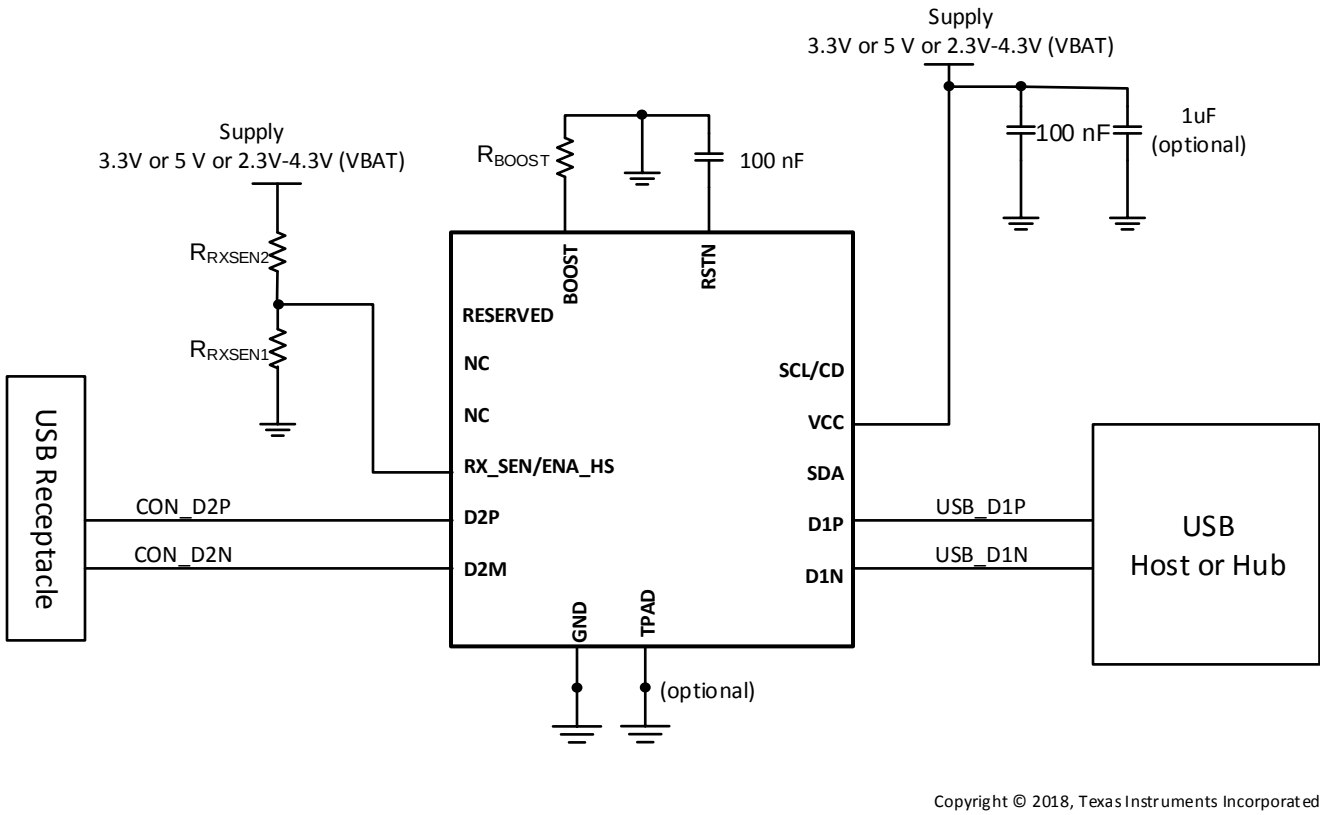


Figure 7. Reference Schematic (design example)

Typical Application (continued)

8.2.1 Design Requirements

TUSB217-Q1 requires a valid reset signal as described in the *power supply recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in Table 8, Table 9 and Table 10

Table 8. Design Parameters for 5 V Supply with High Loss System

PARAMETER				VALUE(1)
V_{CC}				5 V ±10%
I^2C support required in system (Yes/No)				No
Edge and DC Boost		R_{BOOST}	BOOST Level	Boost Level 1: R_{BOOST} = 1.8 kΩ
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ± 1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	R_{RXSEN1}	R_{RXSEN2}	RX_SEN Level	High RX Sensitivity Level: R_{RXSEN1} = 37 kΩ R_{RXSEN2} = 47 kΩ
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 kΩ(2)	47 kΩ	High	

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 5V supply system could be applicable to 3.3V supply system as well.
(2) This resistor is needed for a 5V supply to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

Table 9. Design Parameters for 3.3 V Supply with Low to Medium Loss System

PARAMETER				VALUE(1)
V_{CC}				3.3 V ±10%
I^2C support required in system (Yes/No)				No
Edge and DC Boost		R_{BOOST}	BOOST Level	Boost Level 0: R_{BOOST} = 0-Ω
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	R_{RXSEN1}	R_{RXSEN2}	RX_SEN Level	Medium RX Sensitivity Level: R_{RXSEN1} = DNI R_{RXSEN2} = DNI
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ - 33 kΩ (27 kΩ typical)	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system could be applicable to 5V supply system as well.

Table 10. Design Parameters for 2.3V - 4.3V VBAT Supply with Low to Medium Loss System

PARAMETER				VALUE(1)
V_{CC}				2.3 V to 4.3V
I^2C support required in system (Yes/No)				No
Edge and DC Boost		R_{BOOST}	BOOST Level	Boost Level 0: R_{BOOST} = 0-Ω
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	R_{RXSEN1}	R_{RXSEN2}	RX_SEN Level	Medium RX Sensitivity Level: R_{RXSEN1} = DNI R_{RXSEN2} = DNI
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 kΩ(2)	10 kΩ	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 2.3V-4.3V supply system could be applicable to 5V supply system as well.
(2) This resistor is needed for a VBAT supply (2.3V - 4.3V) to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. if permissible. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level 1.

In order for the TUSB217-Q1 to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

NOTE

The TUSB217-Q1 compensates for extra attenuation in the signal path according to the configuration of the RX_SEN pin. This pin is not 5 V tolerant and therefore when selecting the highest RX sensitivity level, the voltage level at RX_SEN pin must be less than 3.6V.

Placement of the device is also dependent on the application goal. Table 11 summarizes our recommendations.

Table 11. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB217-Q1 PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB217s to improve device enumeration	Midway between each USB interconnect

Table 12. Table of Recommended Settings

BOOST and RX_SEN settings (1)for channel loss		
Pre-channel cable length (Between USB PHY and TUSB217-Q1)	**BOOST**	**RX_SEN**
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB217-Q1 and inter-connect)	**BOOST**	**RX_SEN**
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host and/or device as well as cable length and loss profile.

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

NOTE

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB217-Q1
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB217-Q1. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

8.2.3 Application Curves

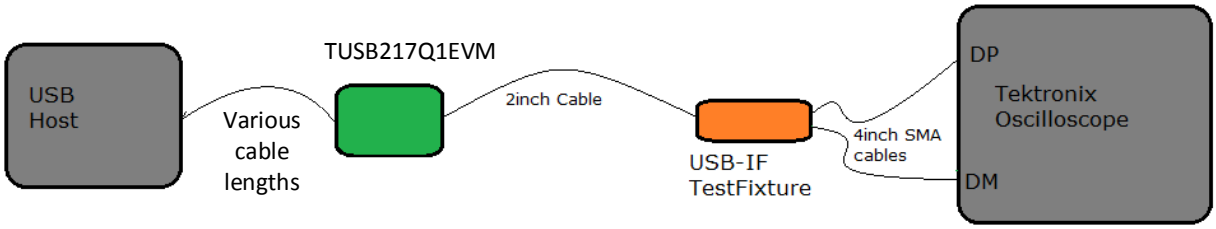


Figure 8. Near End Eye Measurement Set up With Pre-channel Cable

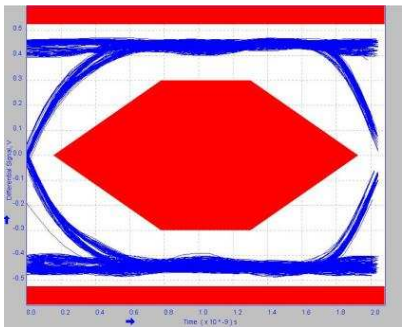


Figure 9. 6 inches without TUSB217-Q1

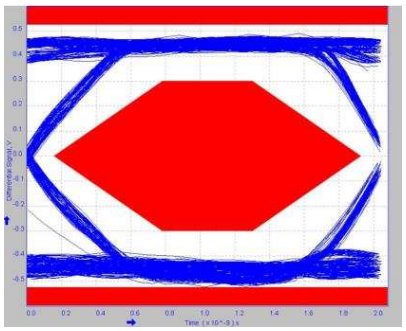


Figure 10. 6 inches pre-channel with TUSB217-Q1 BOOST=0 RX_SEN=MED

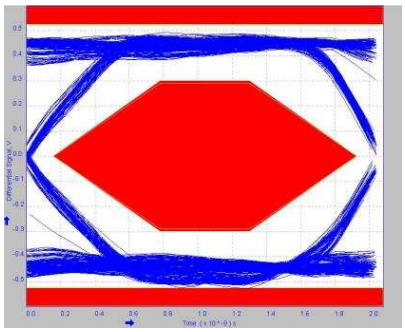


Figure 11. 6 inches pre-channel with TUSB217-Q1 BOOST=0 RX_SEN=HIGH

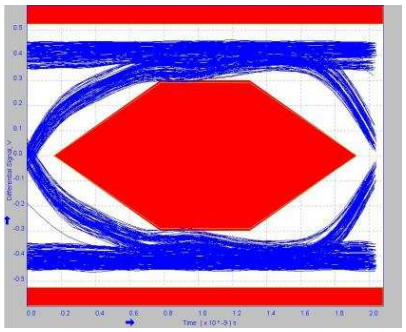


Figure 12. 3 meter without TUSB217-Q1

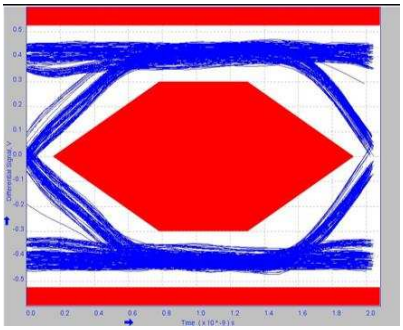


Figure 13. 3 meter pre-channel with TUSB217-Q1 BOOST=0 RX_SEN=MED

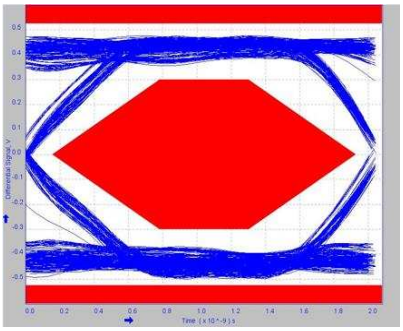


Figure 14. 3 meter pre-channel with TUSB217-Q1 BOOST=0 RX_SEN=HIGH

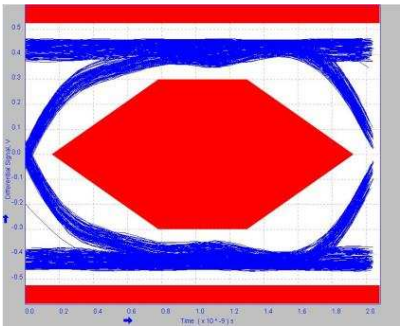


Figure 15. 2 meter without TUSB217-Q1

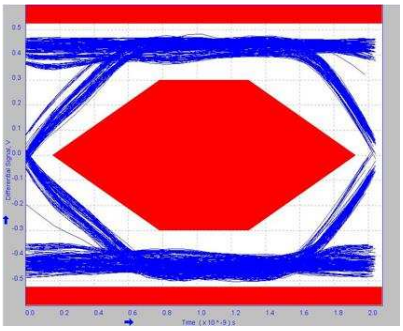


Figure 16. 2 meter pre-channel with TUSB217-Q1 BOOST=1 RX_SEN=MED

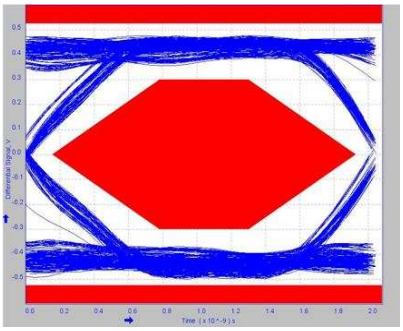


Figure 17. 2 meter pre-channel with TUSB217-Q1 BOOST=1 RX_SEN=HIGH

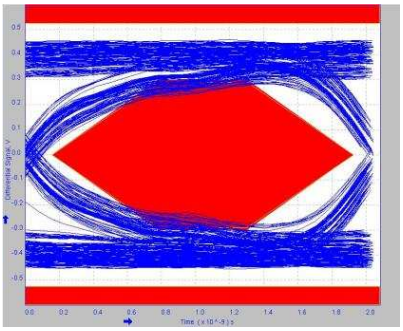


Figure 18. 5 meter without TUSB217-Q1

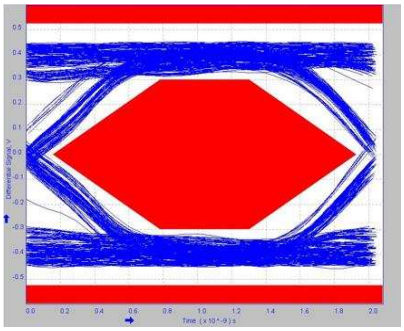


Figure 19. 5 meter pre-channel with TUSB217-Q1 BOOST=1 RX_SEN=MED

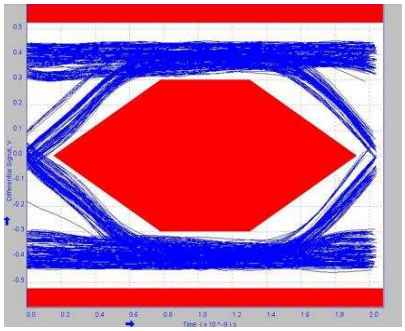


Figure 20. 5 meter pre-channel with TUSB217-Q1 BOOST=1 RX_SEN=HIGH

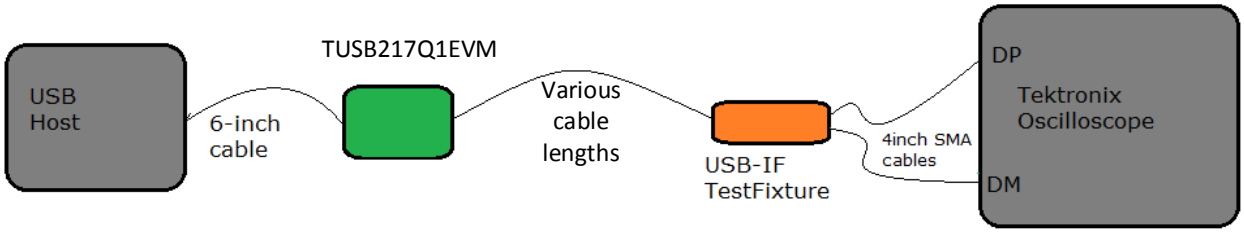


Figure 21. Near end eye measurement set up with post-channel cable

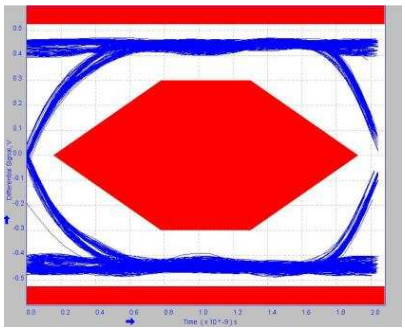


Figure 22. 6 inches without TUSB217-Q1

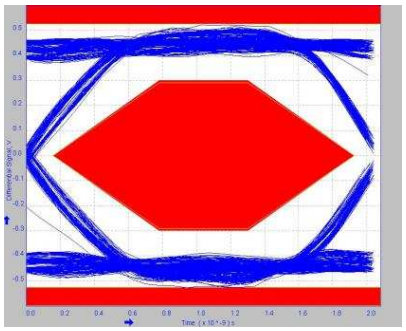


Figure 23. 6 inches post-channel with TUSB217-Q1 BOOST=0 RX_SEN=MED

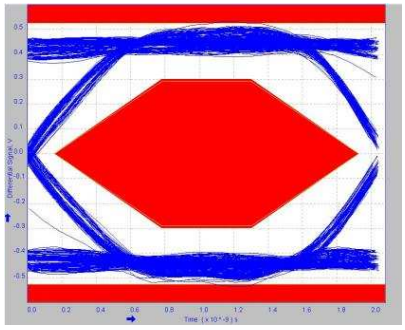


Figure 24. 6 inches post-channel with TUSB217-Q1 BOOST=0 RX_SEN=HIGH

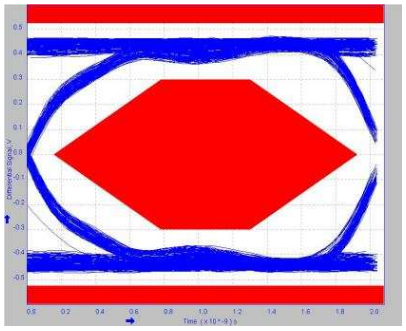


Figure 25. 1 meter without TUSB217-Q1

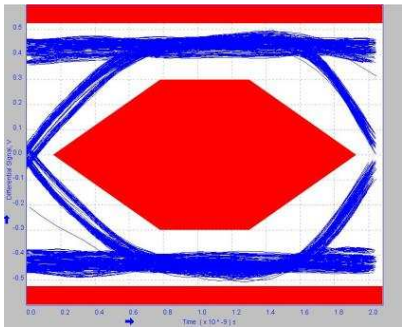


Figure 26. 1 meter post-channel with TUSB217-Q1 BOOST=0 RX_SEN=MED

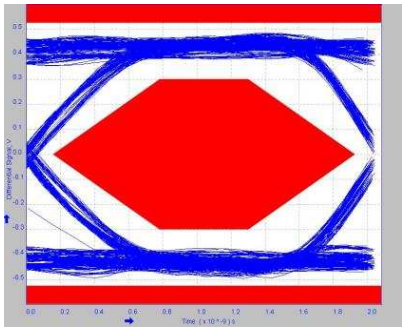


Figure 27. 1 meter post-channel with TUSB217-Q1 BOOST=0 RX_SEN=HIGH

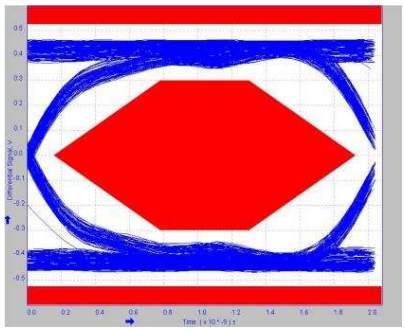


Figure 28. 2 meter without TUSB217-Q1

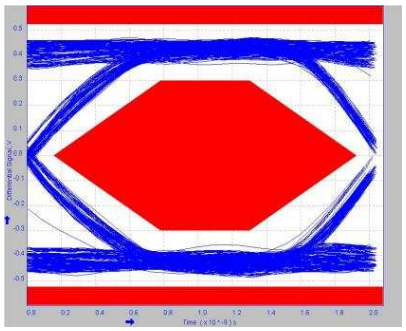


Figure 29. 2 meter post-channel with TUSB217-Q1 BOOST=1 RX_SEN=MED

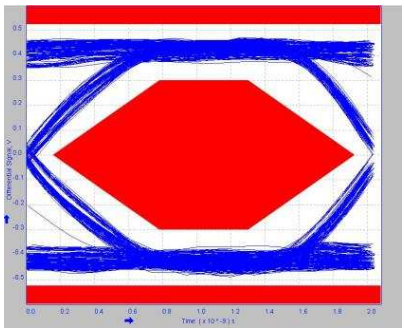


Figure 30. 2 meter post-channel with TUSB217-Q1 BOOST=1 RX_SEN=HIGH

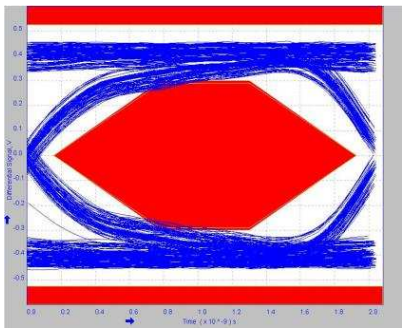


Figure 31. 4 meter without TUSB217-Q1

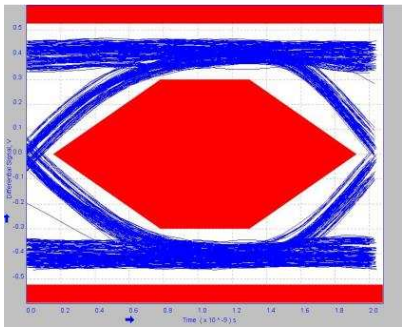


Figure 32. 4 meter post-channel with TUSB217-Q1 BOOST=1 RX_SEN=MED

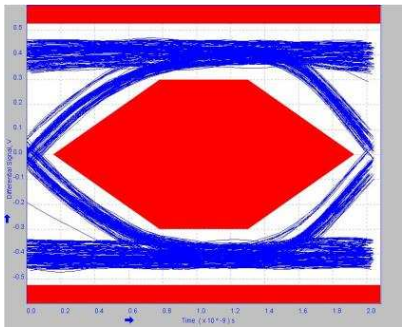


Figure 33. 4 meter post-channel with TUSB217-Q1 BOOST=1 RX_SEN=HIGH

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

[Ramp Time x 5] ÷ [500 kΩ] (1)

10 Layout

10.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

All dimensions are in millimetres (mm).

10.2 Layout Example

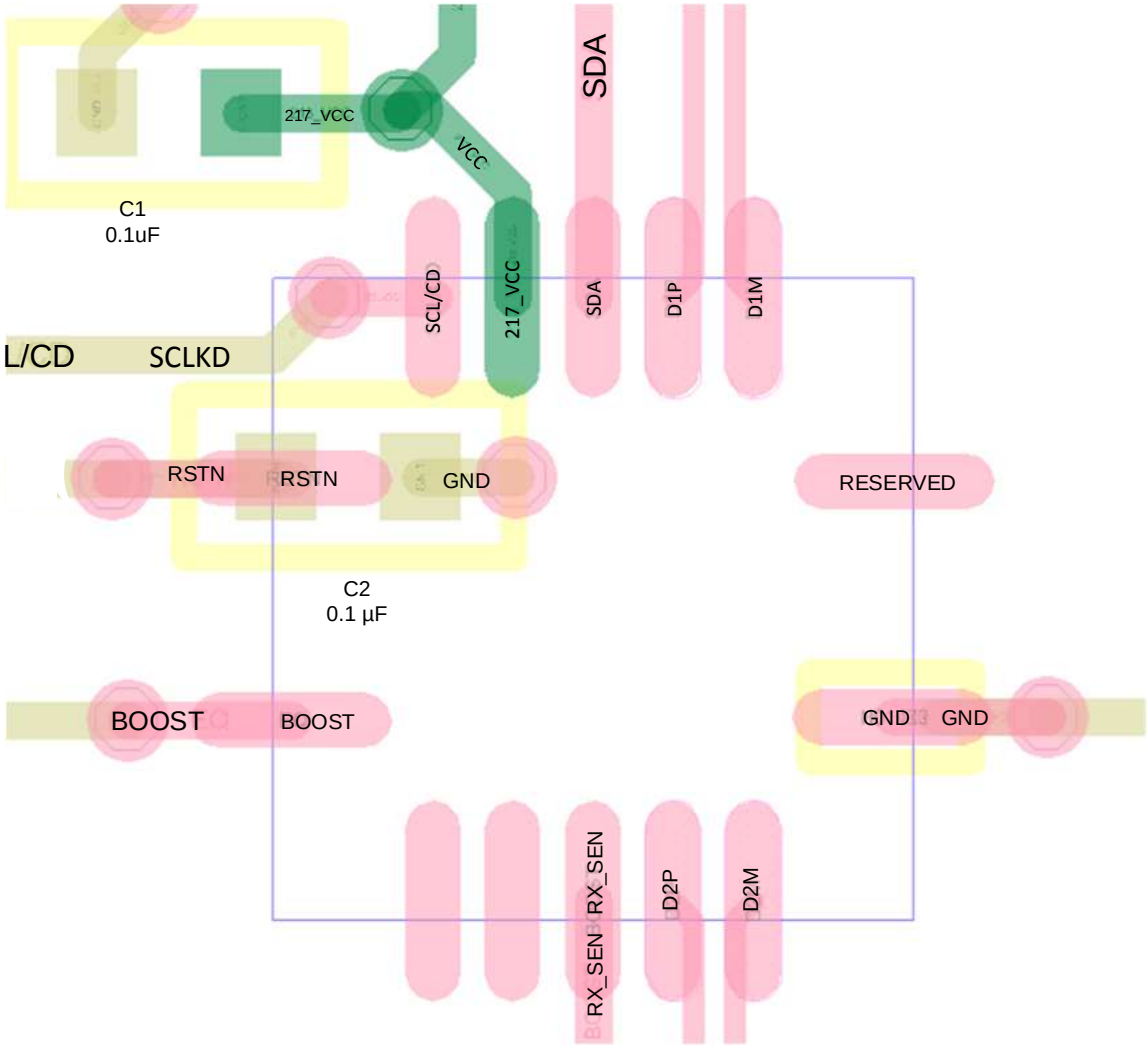


Figure 34. Layout Example (thermal pad grounding is optional)

11 Device and Documentation Support

11.1 Documentation Support

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

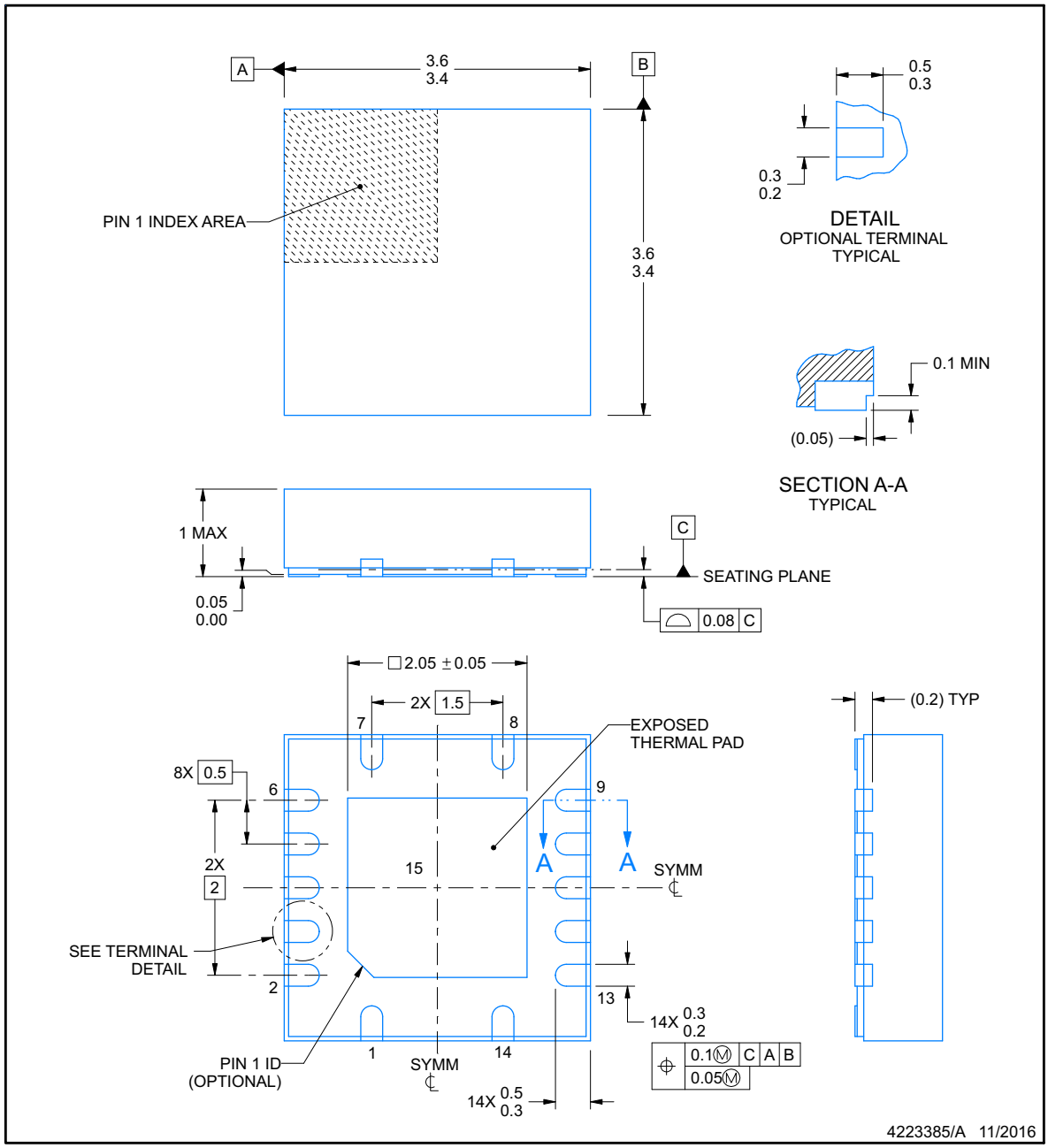
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RGY0014B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

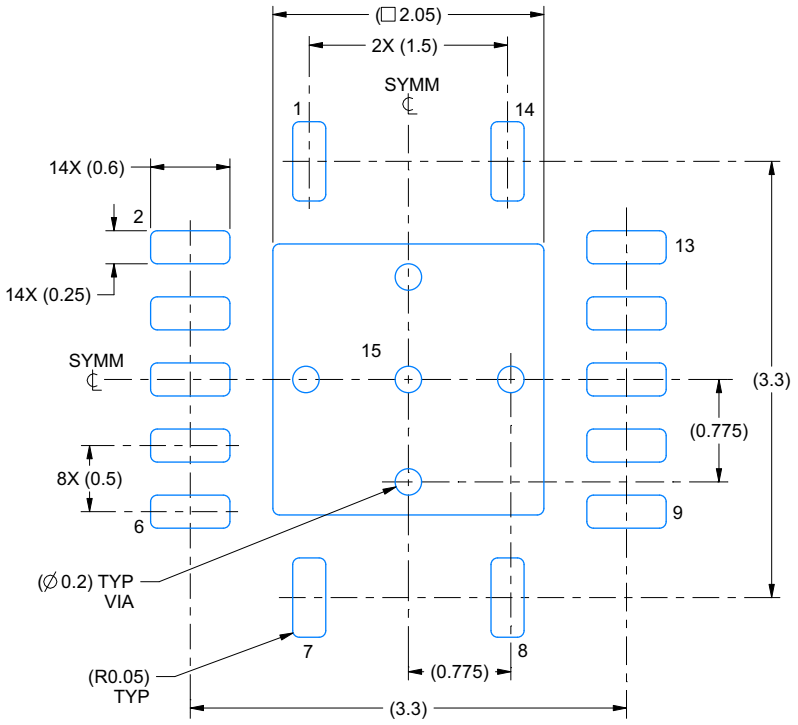
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

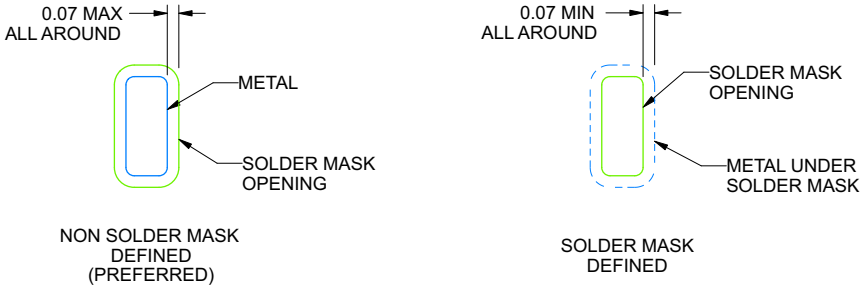
RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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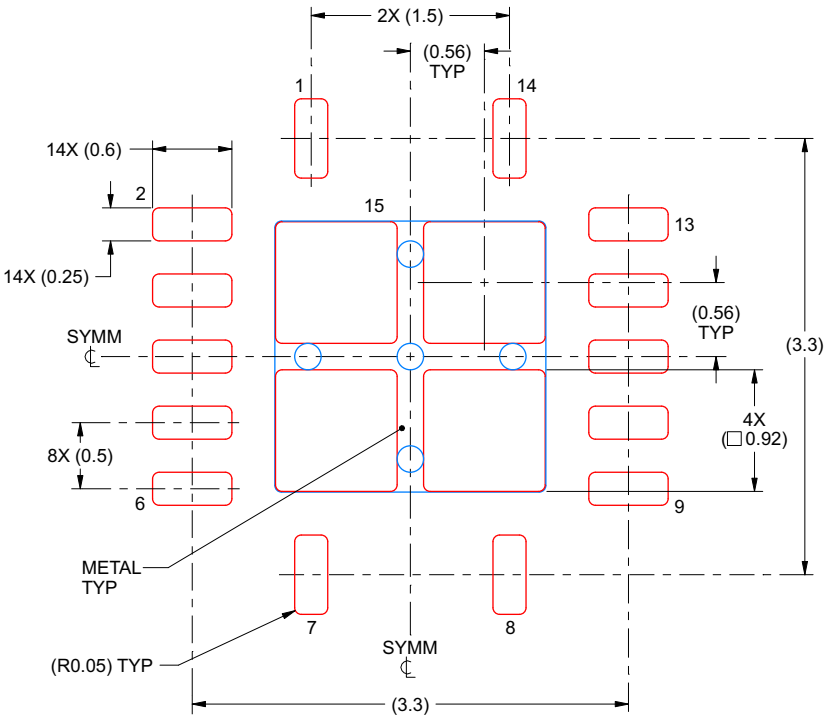
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0014B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223385/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB217RGYRQ1	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1	Samples
TUSB217RGYTQ1	ACTIVE	VQFN	RGY	14	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

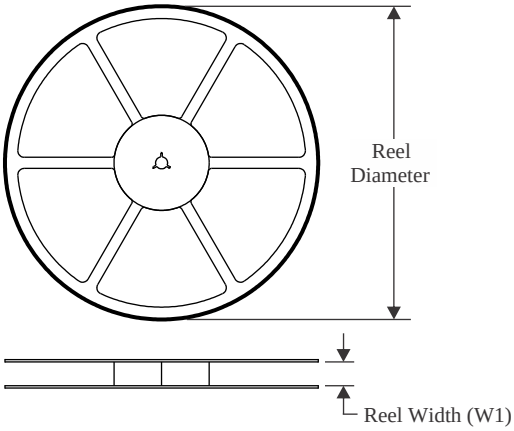
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

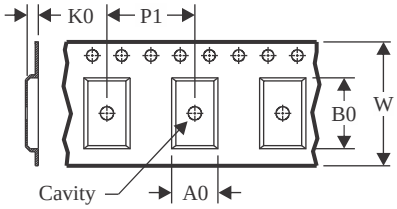
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

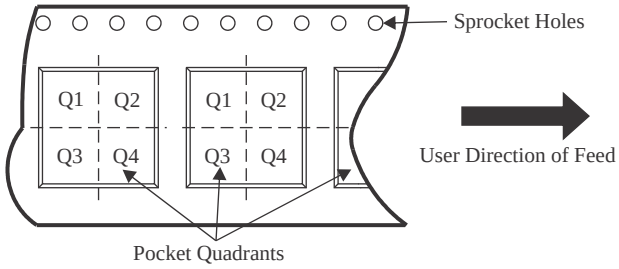


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

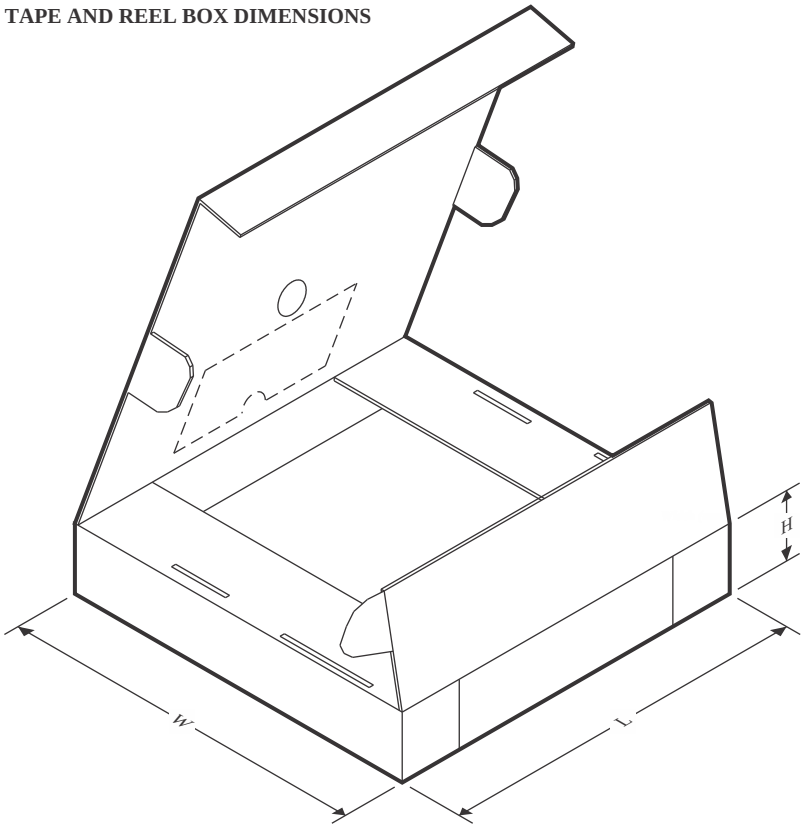
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB217RGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB217RGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB217RGYTQ1	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB217RGYRQ1	VQFN	RGY	14	3000	367.0	367.0	35.0
TUSB217RGYRQ1	VQFN	RGY	14	3000	367.0	367.0	38.0
TUSB217RGYTQ1	VQFN	RGY	14	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

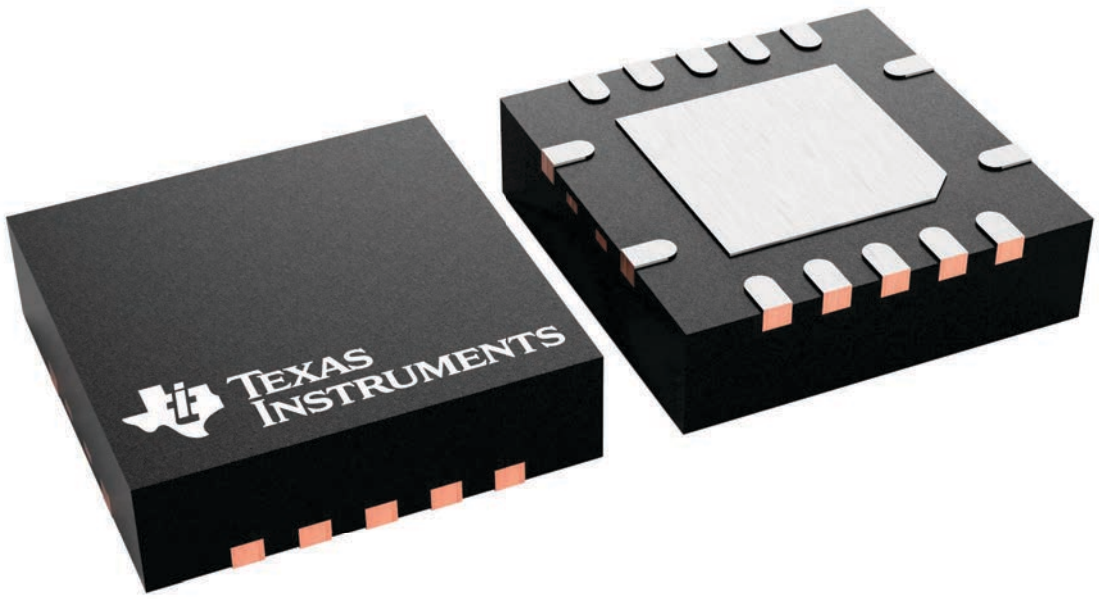
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



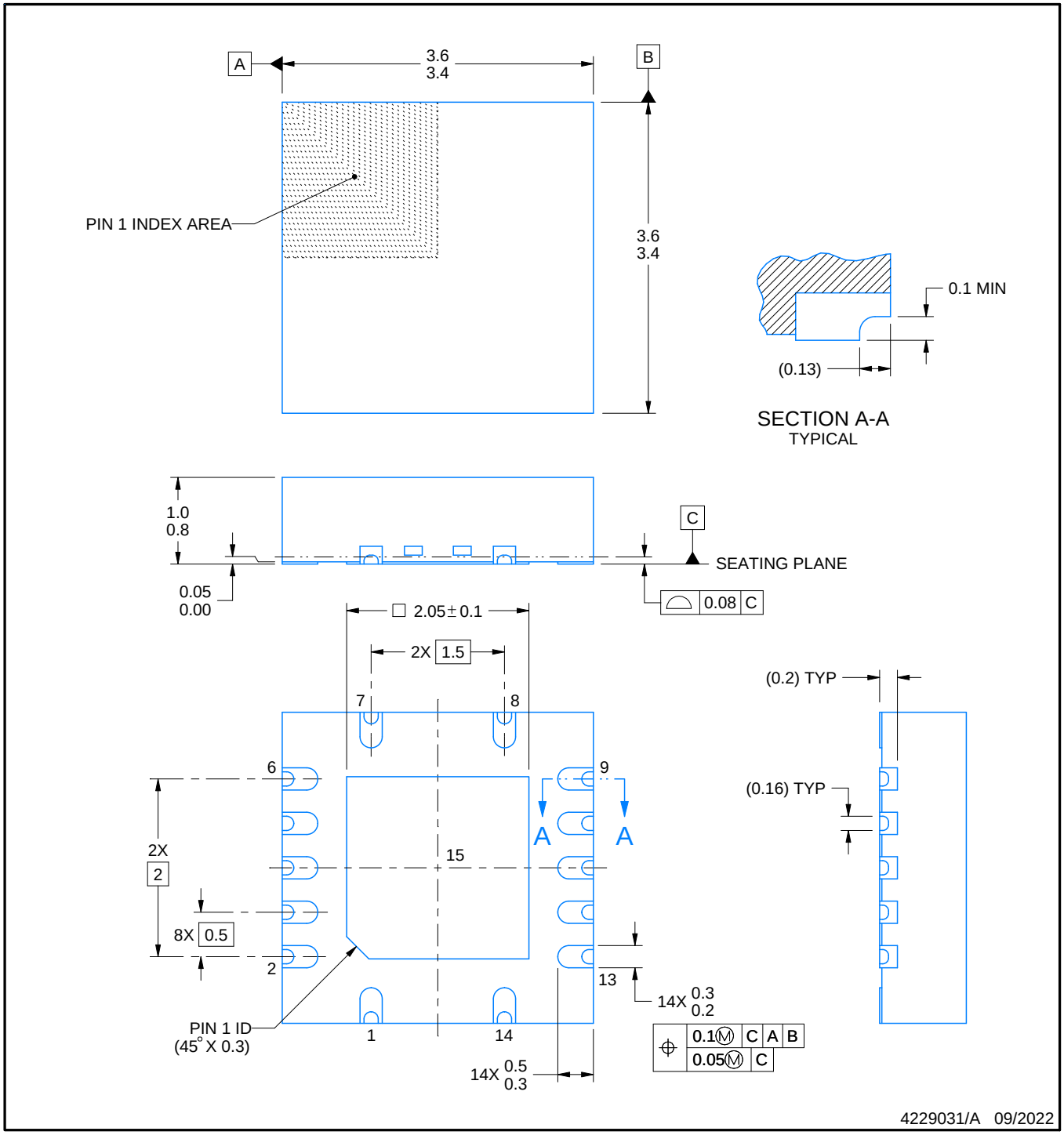
4231541/A

RGY0014C

PACKAGE OUTLINE

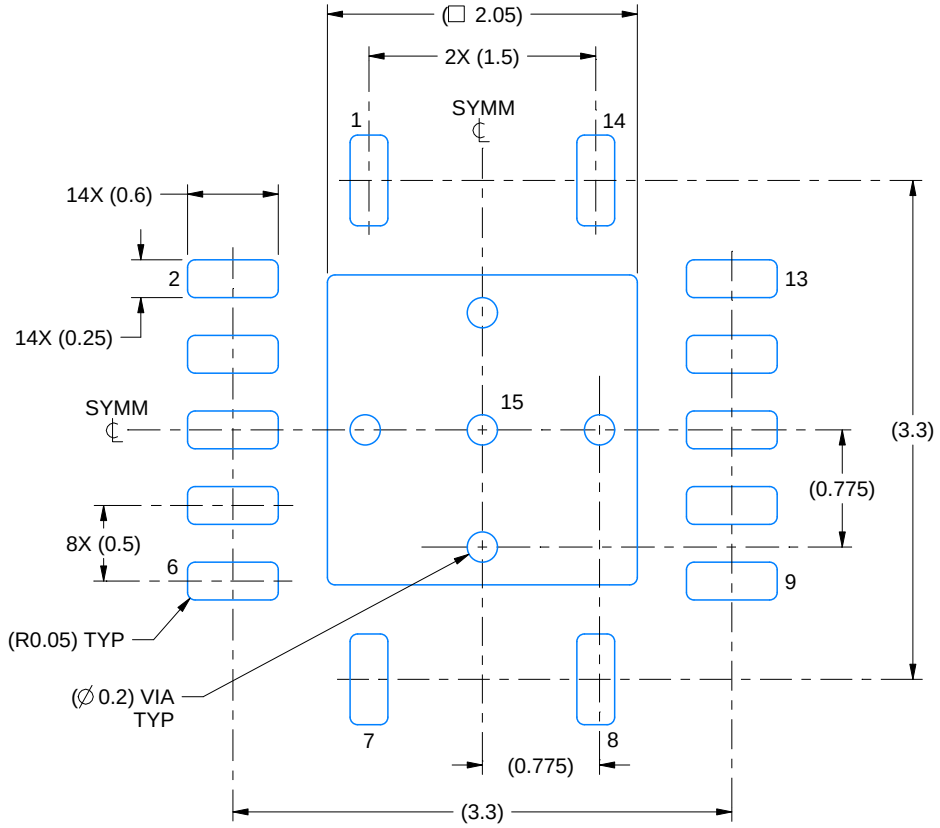
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

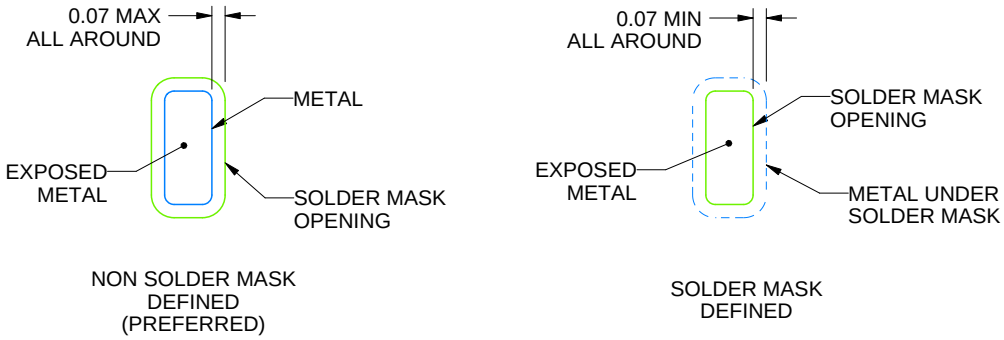


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

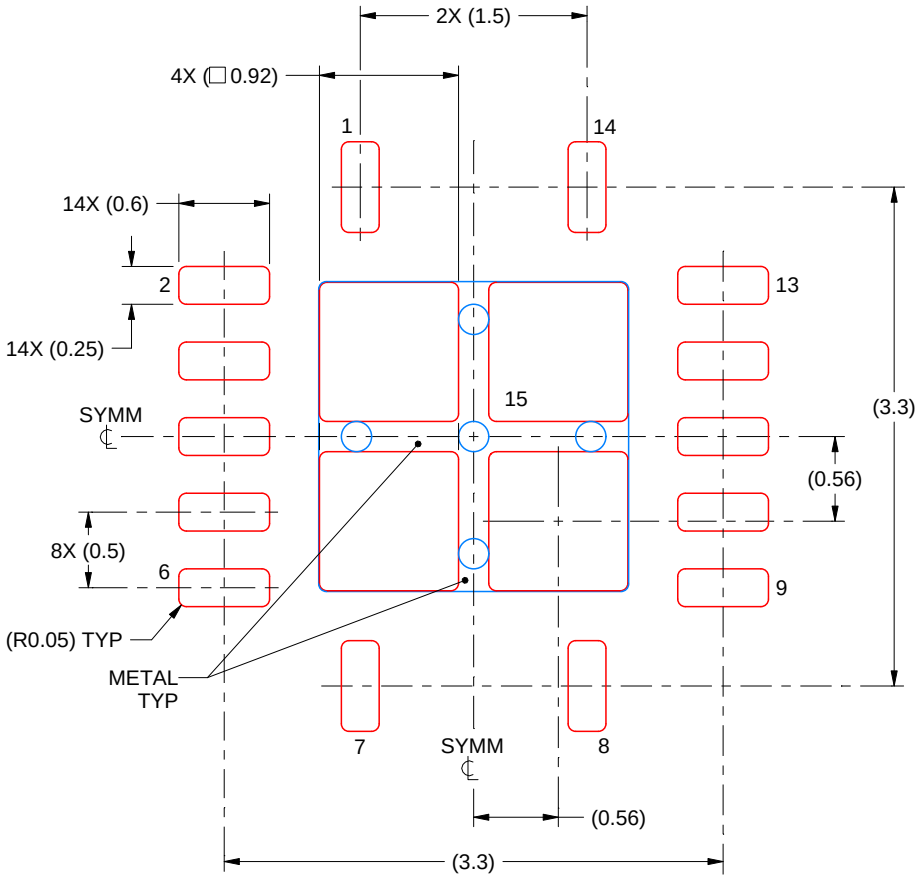


SOLDER MASK DETAILS

4229031/A 09/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4229031/A 09/2022

NOTES: (continued)

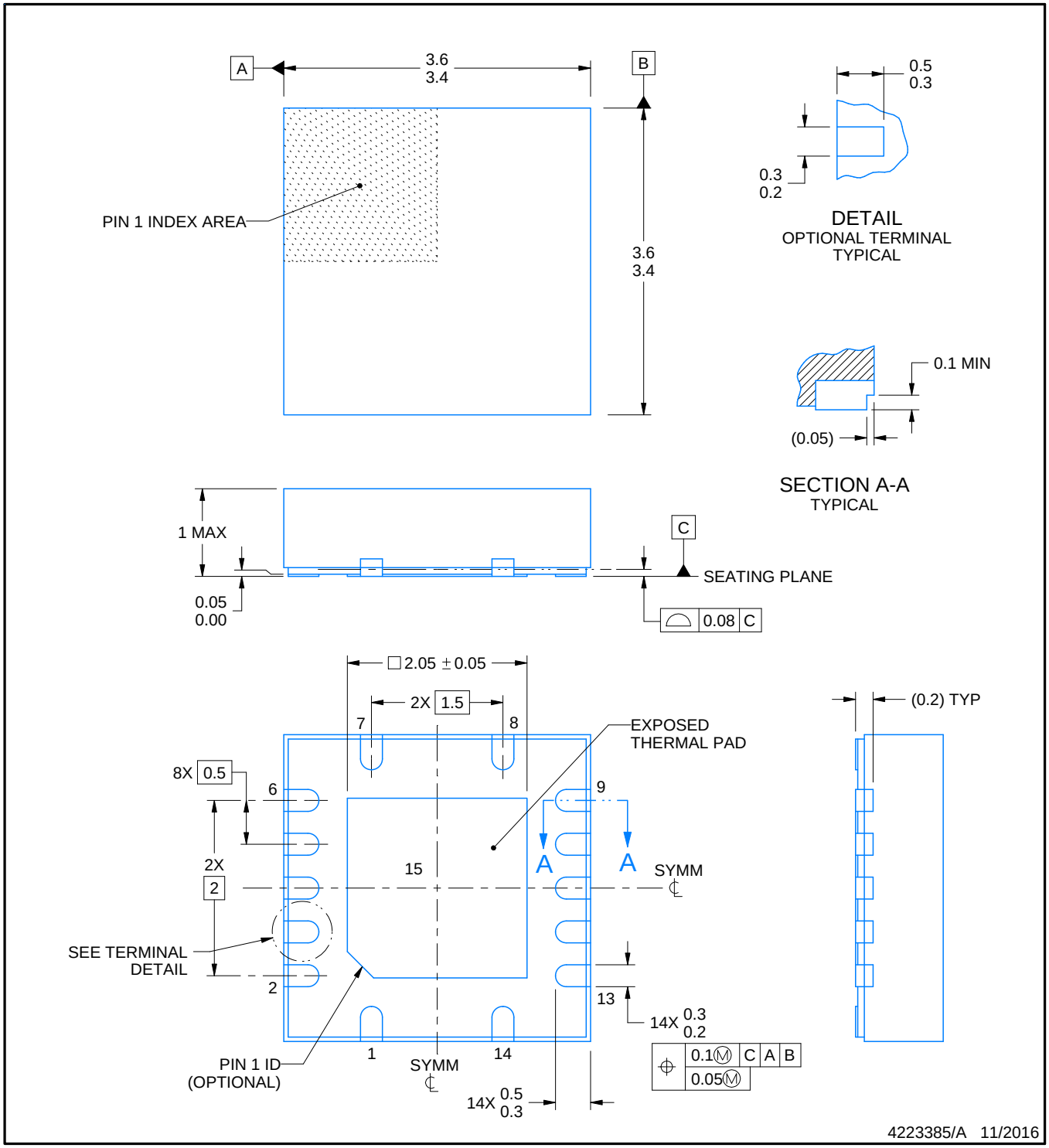
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

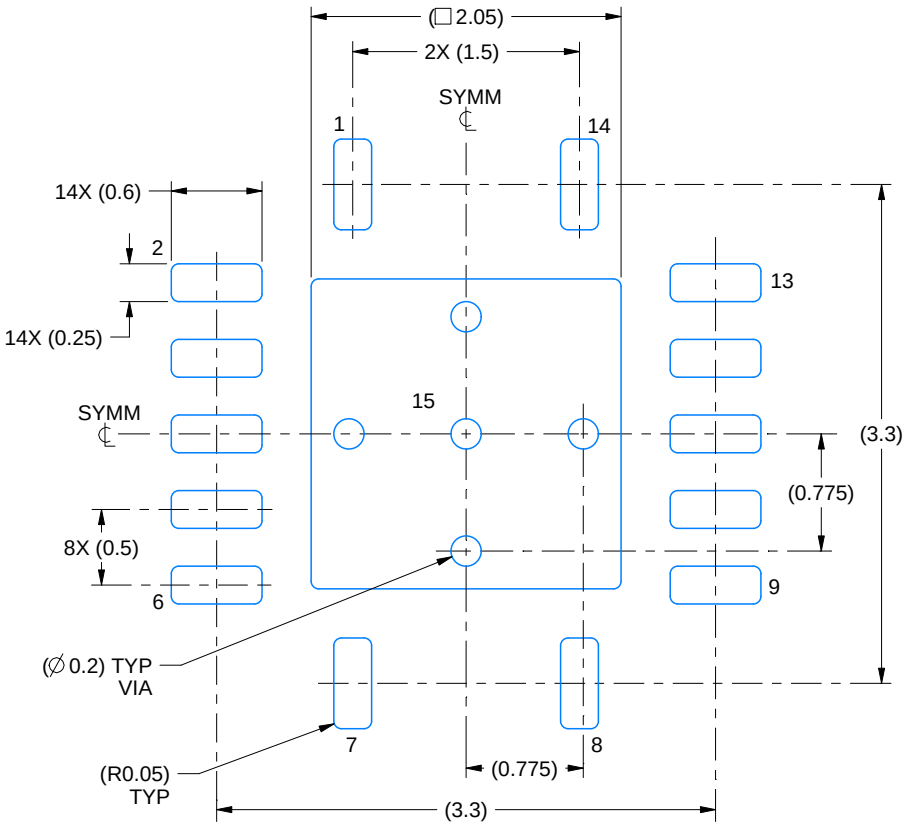
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

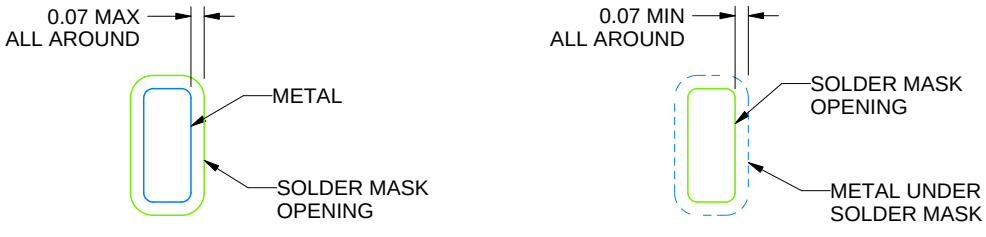
RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

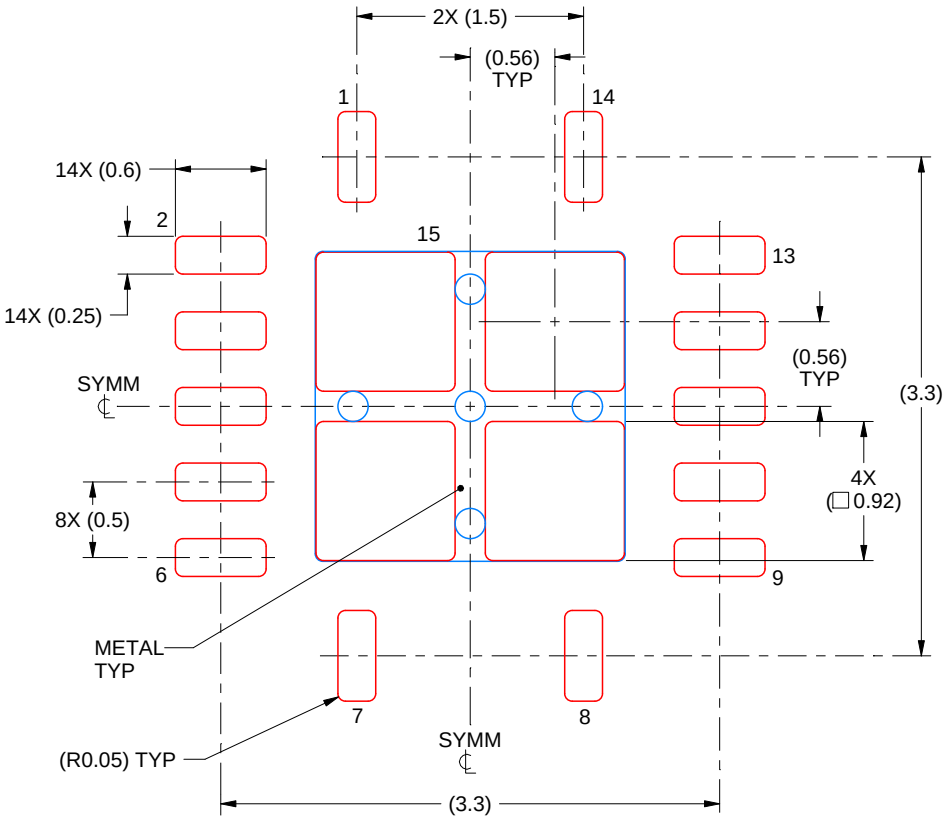
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223385/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223385/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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