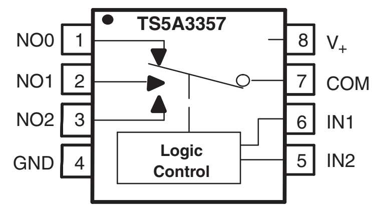
SINGLE 5-Ω SP3T ANALOG SWITCH 5-V/3.3-V 3:1 MULTIPLEXER/DEMULTIPLEXER

Check for Samples: TS5A3357-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance**
- **High Bandwidth**
- **Control Inputs Are 5.5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch Up Exceeds 100 mA per JESD78B, Class I**

SC-70 (DCU) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5A3357 is a high-performance, single-pole triple throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and low input/output capacitance and, thus, causes a very low signal distortion. The break-before-make feature allows transferring of a signal from one port to another, with a minimal signal distortion. This device also offers a low charge injection which makes this device suitable for high-performance audio and data acquisition systems.

Table 1. Summary of Characteristics(1)

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	5 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	6.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	6.5 ns/3.7 ns
Break-before-make time (t_{BBM})(2)	0.5 ns
Charge injection (Q_C)	3.4 pC
Bandwidth (BW)	334 MHz
OFF isolation (O_{ISO})	–82 dB at 10 MHz
Crosstalk (X_{TALK})	–62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Leakage current ($I_{COM(OFF)}$)	±1 μA
Package option	8-pin DCU (US8)

(1) $V_+ = 5$ V, $T_A = 25°C$
(2) Specified by designed. Not production tested.

Table 2. FUNCTION TABLE

IN1	IN2	COM TO NO0	COM TO NO1	COM TO NO2
L	L	OFF	OFF	OFF
H	L	ON	OFF	OFF
L	H	OFF	ON	OFF
H	H	OFF	OFF	ON

Table 3. ORDERING INFORMATION(1)

T_A	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT – DCU	Reel of 3000	TS5A3357QDCURQ1	JAVR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(3) (4) (5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–100	100	mA
V_I	Digital input voltage range(3) (4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.

PACKAGE THERMAL IMPEDANCE

		MAX	UNIT
θ_{JA}	Package thermal impedance(1)	165	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA, Switch ON, See Figure 13	Full	4.5 V			15	Ω
ON-state resistance	r_{on}	V_{NO} = 0, I_{COM} = 30 mA, Switch ON, See Figure 13	25°C	4.5 V		5	7	Ω
			Full				7	
		V_{NO} = 2.4 V, I_{COM} = –30 mA, Switch ON, See Figure 13	25°C			6	12	
			Full				12	
		V_{NO} = 4.5 V, I_{COM} = –30 mA, Switch ON, See Figure 13	25°C			7	15	
			Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 3.15 V, I_{COM} = –30 mA, Switch ON, See Figure 13	25°C	4.5 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA, Switch ON, See Figure 13	25°C	5 V		6.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0, Switch OFF, See Figure 14	25°C	5.5 V	–0.2		0.2	µA
			Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0, Switch OFF, See Figure 14	25°C	0	–0.2		0.2	µA
			Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = Open, Switch ON, See Figure 14	25°C	5.5 V	–0.2		0.2	µA
			Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+, Switch ON, See Figure 14	25°C	5.5 V	–0.2		0.2	µA
			Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)								
Input logic high	V_{IH}		Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}		Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0	25°C	5.5 V			0.1	µA
			Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	1.5		10	ns
				Full	4.5 V to 5.5 V	1.5		10	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	0.8		6.5	ns
				Full	4.5 V to 5.5 V	0.8		7	
Break-before-make time (3)	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	5 V	0.5			ns
				Full	4.5 V to 5.5 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	5 V		3.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	4.5 V to 5.5 V		334		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	4.5 V to 5.5 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	4.5 V to 5.5 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	

(3) Specified by designed. Not production tested.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	Full	3 V			25	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 24 mA	Switch ON, See Figure 13	25°C	3 V		6.5	9	Ω
				Full				9	
		V_{NO} = 3 V, I_{COM} = –24 mA		25°C			9	20	
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3.3 V		13.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	3.6 V	–0.2		0.2	μA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	3.6 V	–0.2		0.2	μA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	3.6 V	–0.2		0.2	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	3.6 V	–0.2		0.2	μA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–1		0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	2		12	ns
				Full	3 V to 3.6 V	2		12.9	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	1.3		8	ns
				Full	3 V to 3.6 V	1.5		8	
Break-before-make time (3)	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	3.3 V	0.5			ns
				Full	3 V to 3.6 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	3.3 V		1.75		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3 V to 3.6 V		327		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3 V to 3.6 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3 V to 3.6 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	μA
				Full				10	

(3) Specified by designed. Not production tested.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –8 mA,	Switch ON, See Figure 13	Full	2.3 V			50	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 8 mA	Switch ON, See Figure 13	25°C	2.3 V		8	12	Ω
				Full				12	
		V_{NO} = 2.3 V, I_{COM} = –8 mA		25°C			11	30	
				Full				30	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.5 V		39		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	2.7 V	–0.2		0.2	μA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	2.7 V	–0.2		0.2	μA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	2.7 V	–0.2		0.2	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	2.7 V	–0.2		0.2	μA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.75$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.25$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V			0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{NO} = V_+$ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V	3		15	ns
				Full	2.3 V to 2.7 V	3		19.4	
Turn-off time	t_{OFF}	$V_{NO} = V_+$ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V	2		8.1	ns
				Full	2.3 V to 2.7 V	2		10	
Break-before-make time (3)	t_{BBM}	$V_{NO} = V_+$, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	2.5 V	0.5			ns
				Full	2.3 V to 2.7 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	2.5 V		1.15		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 15	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.3 V to 2.7 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.3 V to 2.7 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.3 V to 2.7 V		–61		dB
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
				Full				10	

(3) Specified by designed. Not production tested.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY[(1)]

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –4 mA,	Switch ON, See Figure 13	Full	1.65 V			150	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 4 mA	Switch ON, See Figure 13	25°C	1.65 V		10	20	Ω
				Full				20	
		V_{NO} = 1.8 V, I_{COM} = –4 mA		25°C			17	50	
				Full				50	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.8 V		140		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	1.95 V	–0.2		0.2	μA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	1.95 V	–0.2		0.2	μA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	1.95 V	–0.2		0.2	μA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	1.95 V	–0.2		0.2	μA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)[(2)]									
Input logic high	V_{IH}			Full		$V_+ \times 0.75$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.25$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V			0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{NO} = V_+$ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	5		32	ns
				Full	1.65 V to 1.95 V	5		40	
Turn-off time	t_{OFF}	$V_{NO} = V_+$ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	3		14	ns
				Full	1.65 V to 1.95 V	3		17.6	
Break-before-make time (3)	t_{BBM}	$V_{NO} = V_+$, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	1.8 V	0.5			ns
				Full	1.65 V to 1.95 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	1.8 V		0.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 15	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.65 V to 1.95 V		341		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	1.65 V to 1.95 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	1.65 V to 1.95 V		–61		dB
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V			1	μA
				Full				10	

(3) Specified by designed. Not production tested.

TYPICAL PERFORMANCE

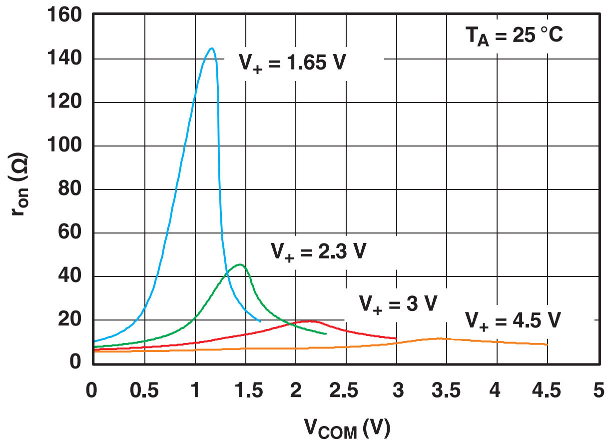


Figure 1. r_{on} vs V_{COM}

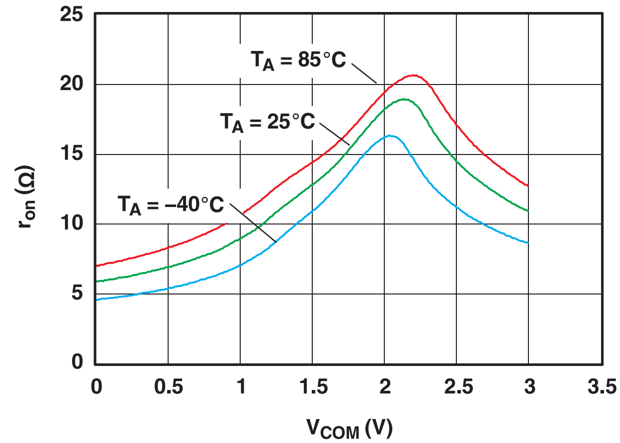


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

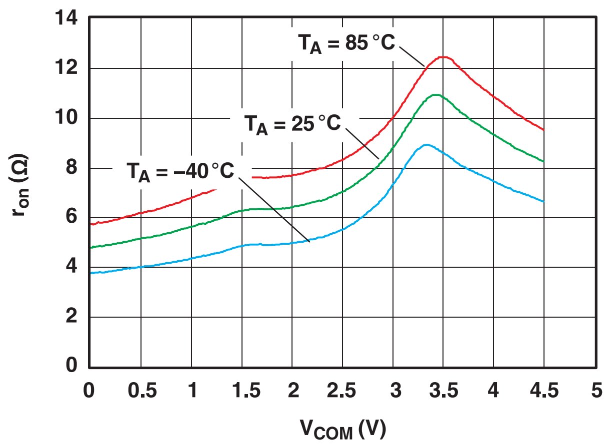


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

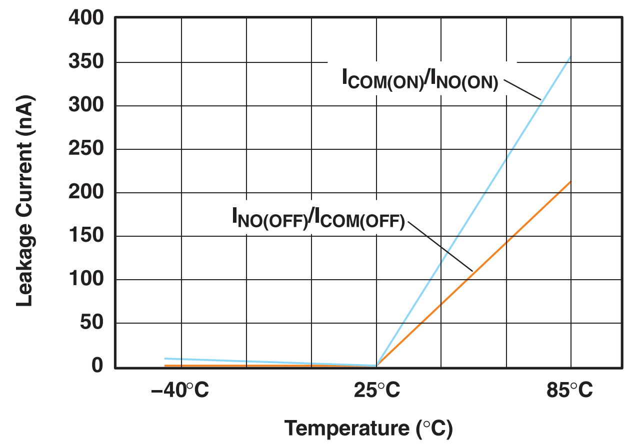


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

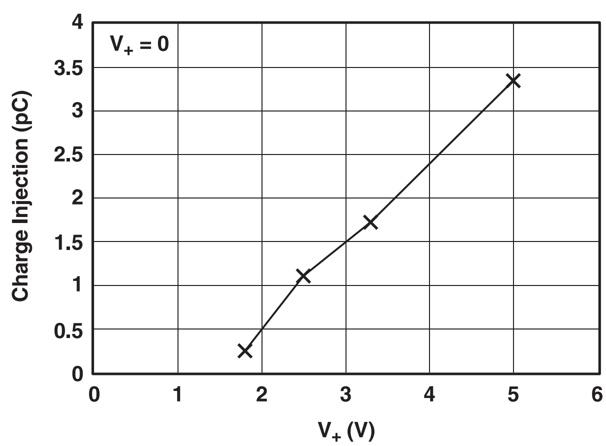


Figure 5. Charge Injection (Q_C) vs V_{COM}

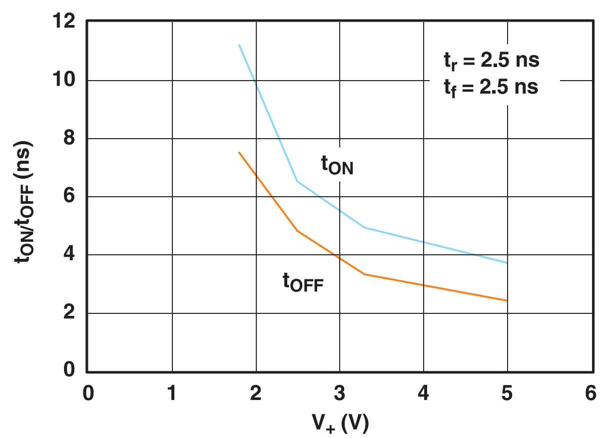


Figure 6. t_{ON} and t_{OFF} vs V_+

TYPICAL PERFORMANCE (continued)

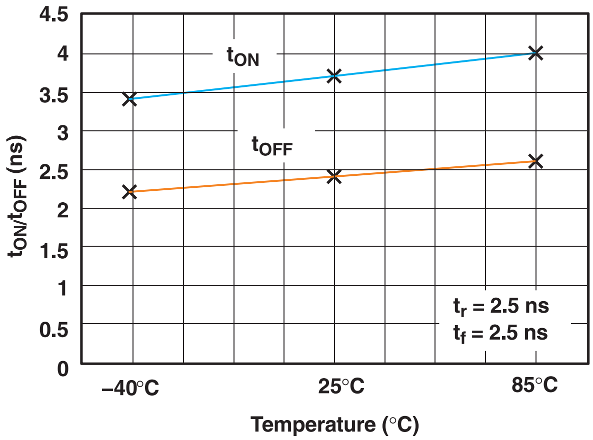


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

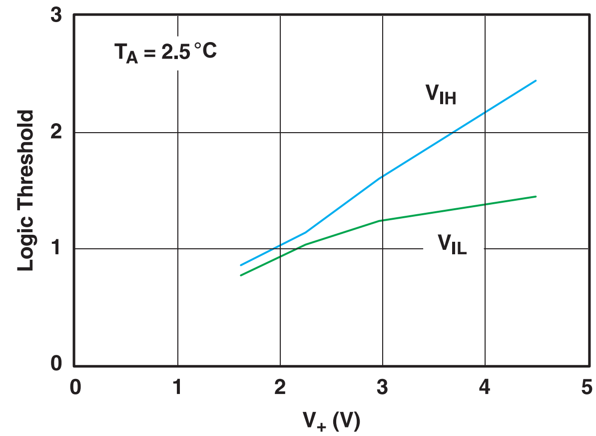


Figure 8. Logic-Level Threshold vs V_+

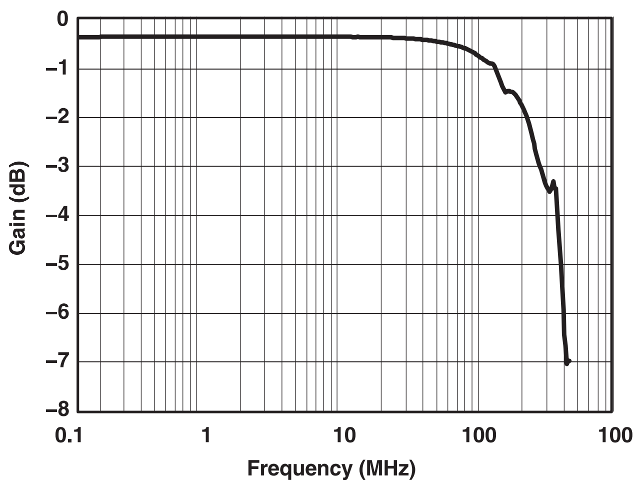


Figure 9. Frequency Response (V_+ = 3 V)

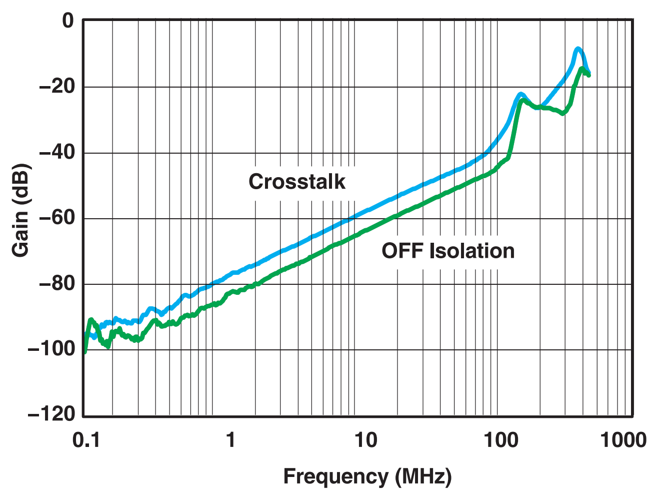


Figure 10. OFF Isolation and Crosstalk vs Frequency (V_+ = 3 V)

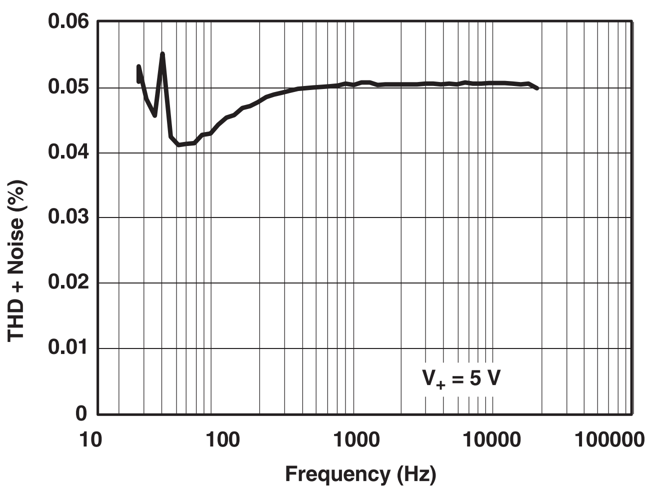


Figure 11. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

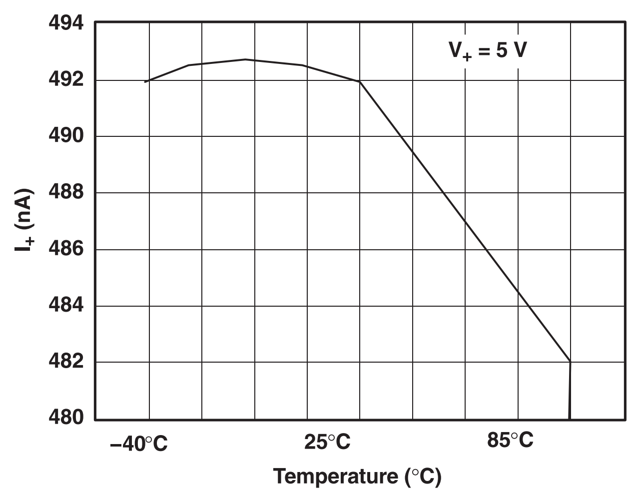


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

Table 4. PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NO0	Normally open
2	NO1	Normally open
3	NO2	Normally open
4	GND	Digital ground
5	IN2	Digital control to connect COM to NO
6	IN1	Digital control to connect COM to NO
7	COM	Common
8	V_+	Power supply

Table 5. PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(OFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

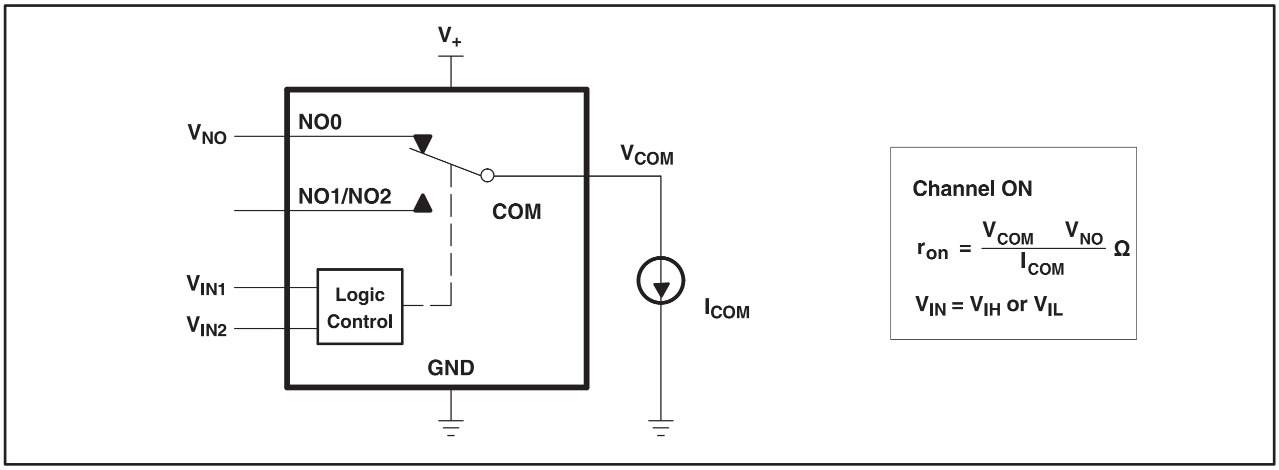


Figure 13. ON-State Resistance (r_{on})

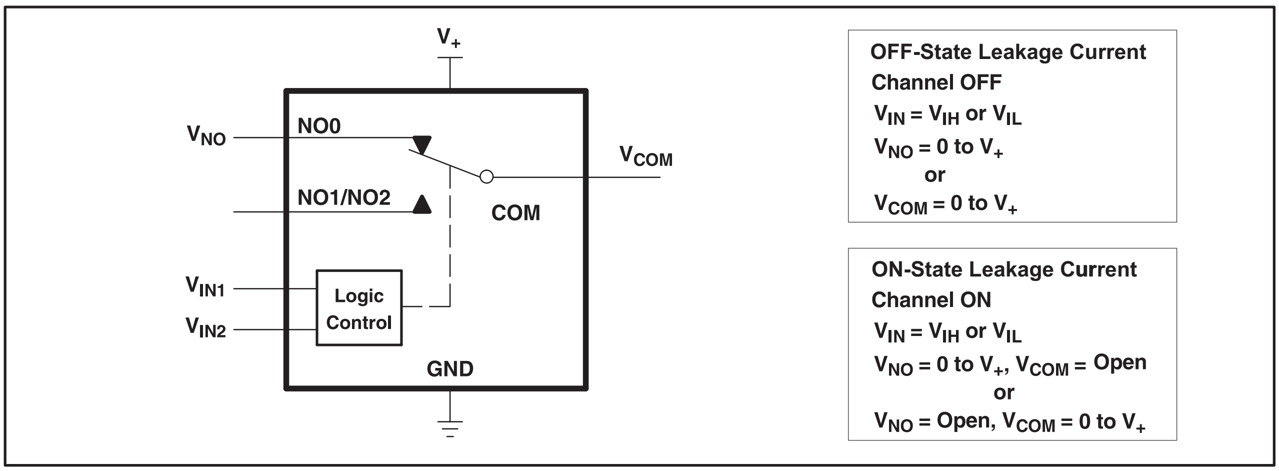


Figure 14. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{COM(OFF)}$, $I_{NO(ON)}$, $I_{NO(OFF)}$)

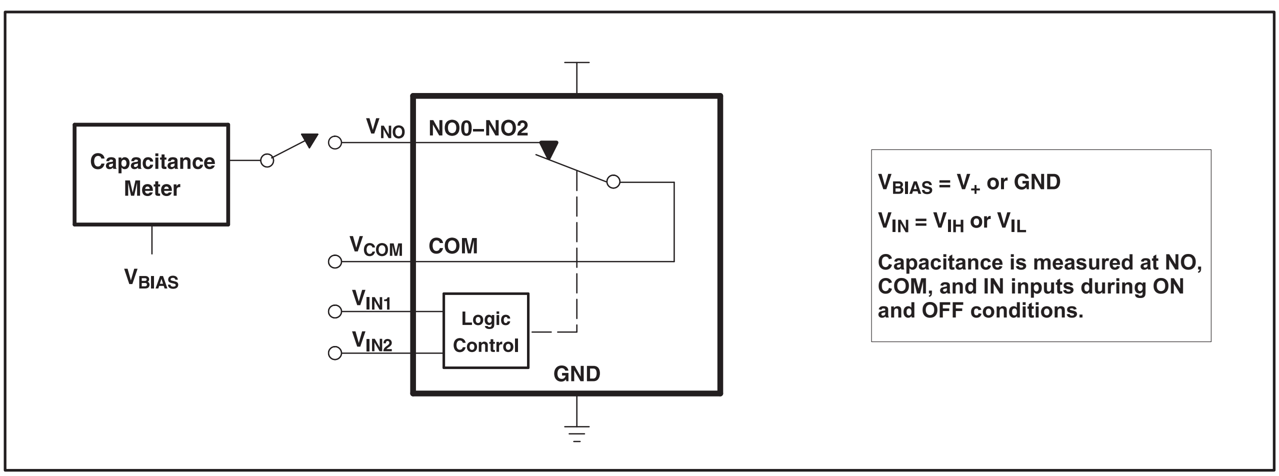
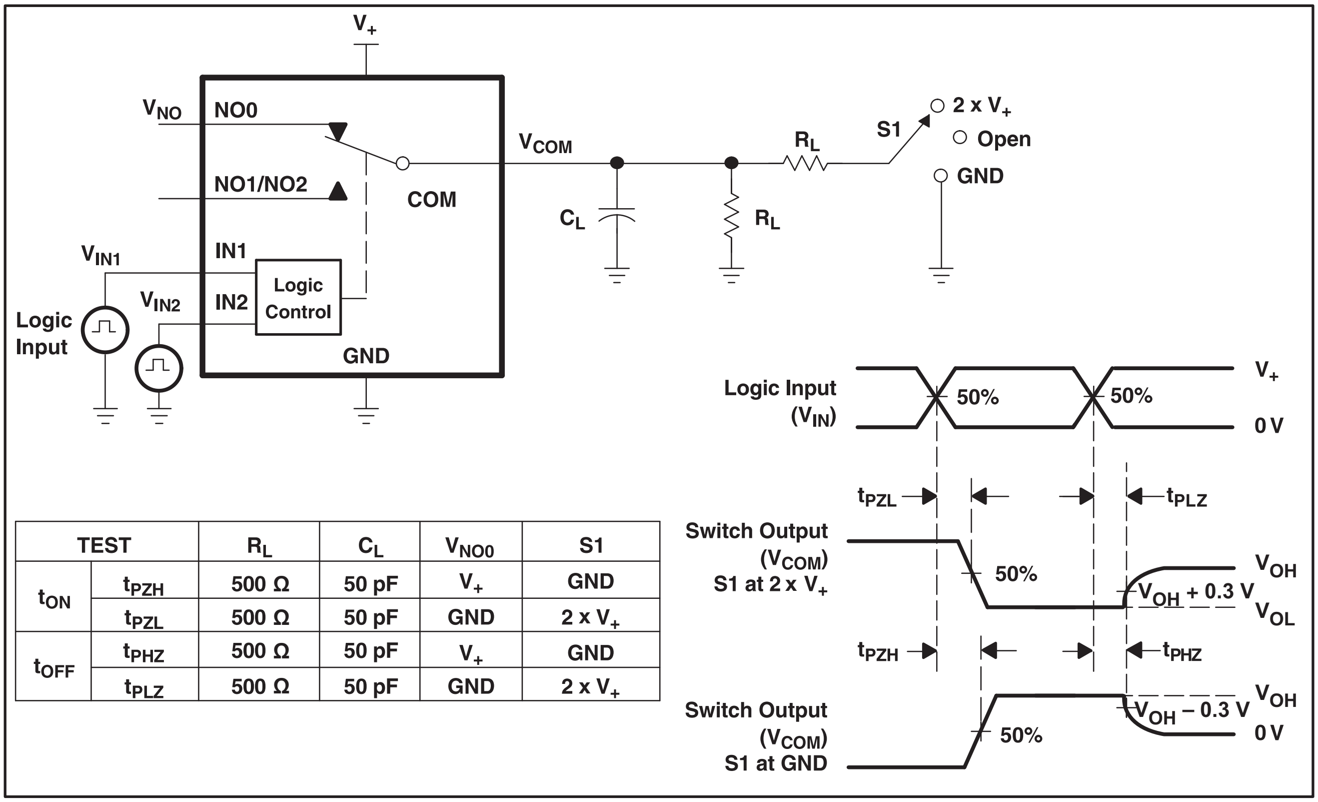


Figure 15. Capacitance (C_I, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)



TEST		R_L	C_L	V_{NO0}	S1
t_{ON}	t_{PZH}	500 Ω	50 pF	V_+	GND
	t_{PZL}	500 Ω	50 pF	GND	2 x V_+
t_{OFF}	t_{PHZ}	500 Ω	50 pF	V_+	GND
	t_{PLZ}	500 Ω	50 pF	GND	2 x V_+

Figure 16. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

D. C_L includes probe and jig capacitance.

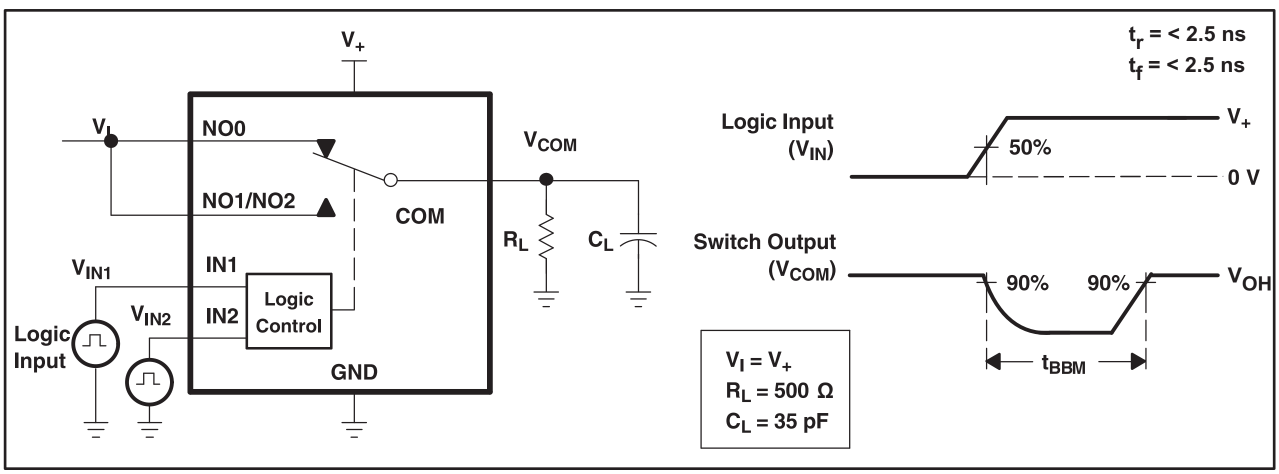


Figure 17. Break-Before-Make Time (t_{BBM})

PARAMETER MEASUREMENT INFORMATION (continued)

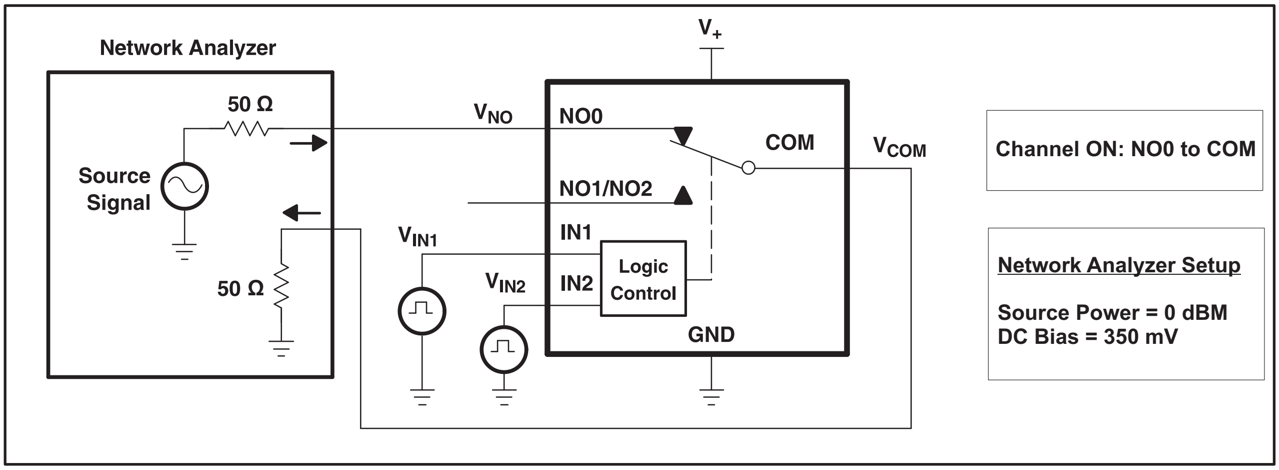


Figure 18. Bandwidth (BW)

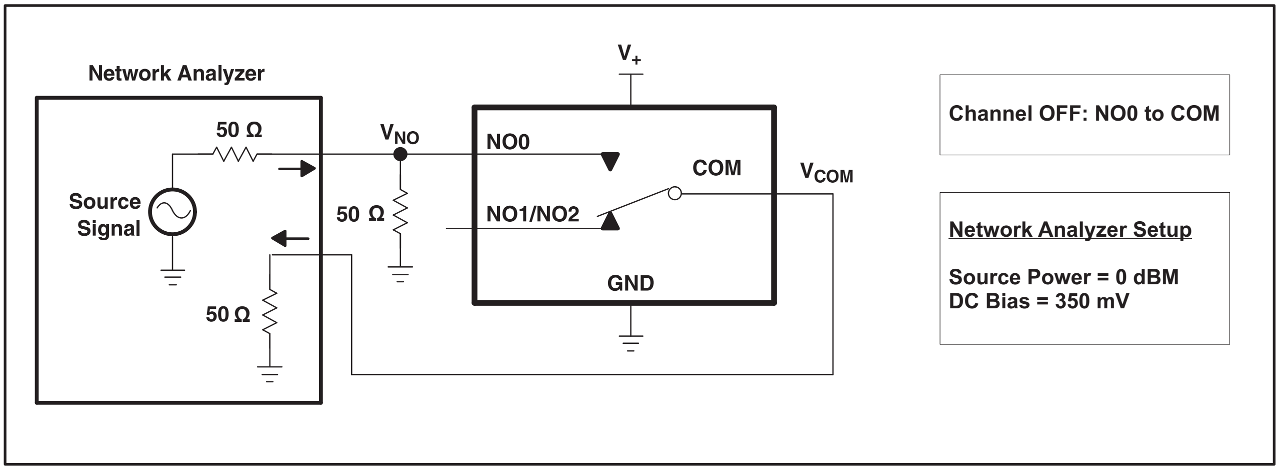


Figure 19. OFF Isolation (O_{ISO})

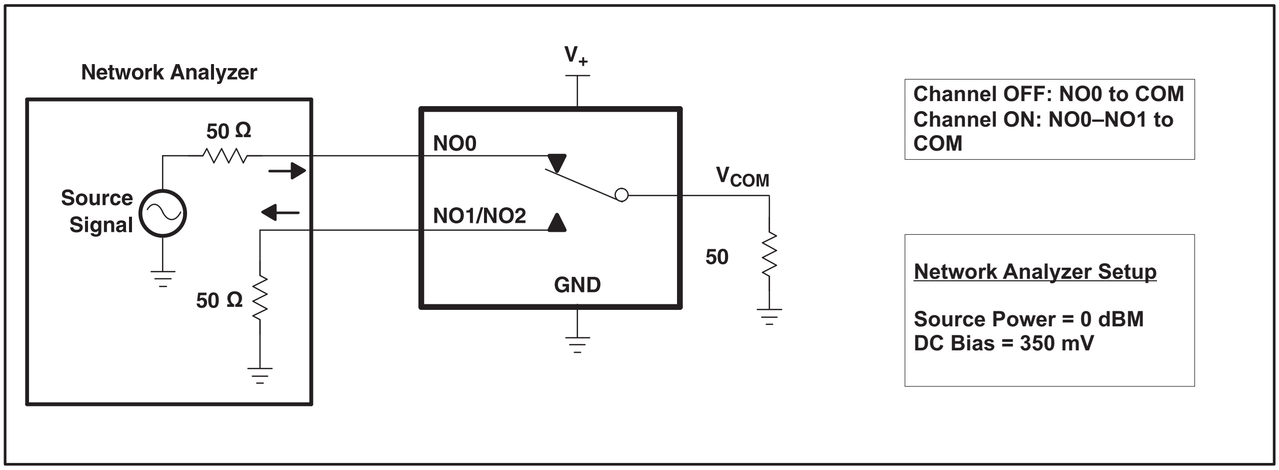


Figure 20. Crosstalk (X_{TALK})

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

F. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

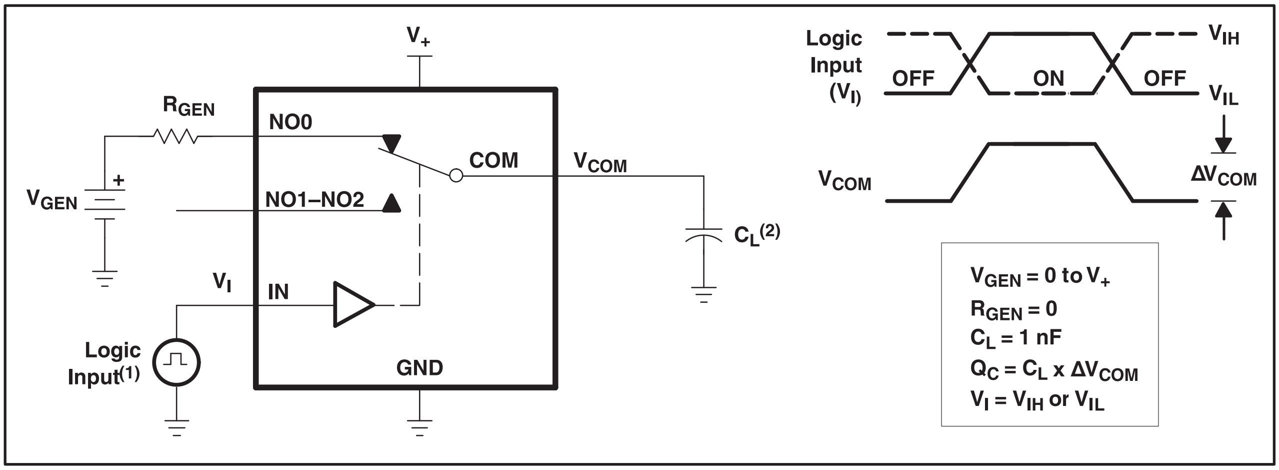


Figure 21. Charge Injection (Q_C)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3357QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JAVR	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS5A3357-Q1 :

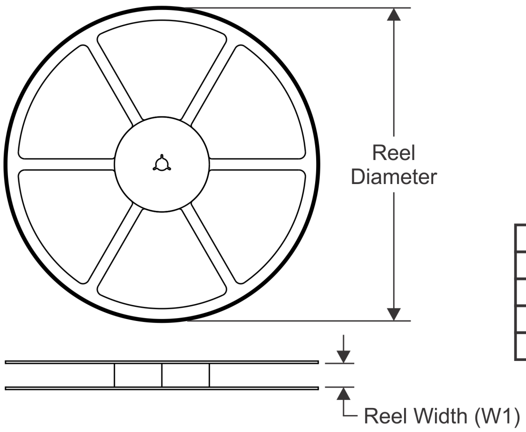
- Catalog: TS5A3357

NOTE: Qualified Version Definitions:

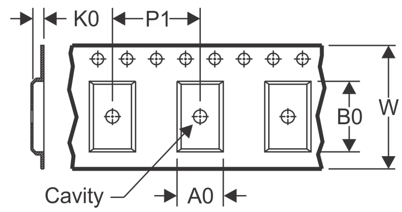
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

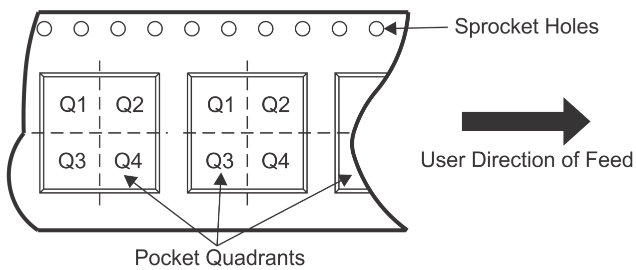


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

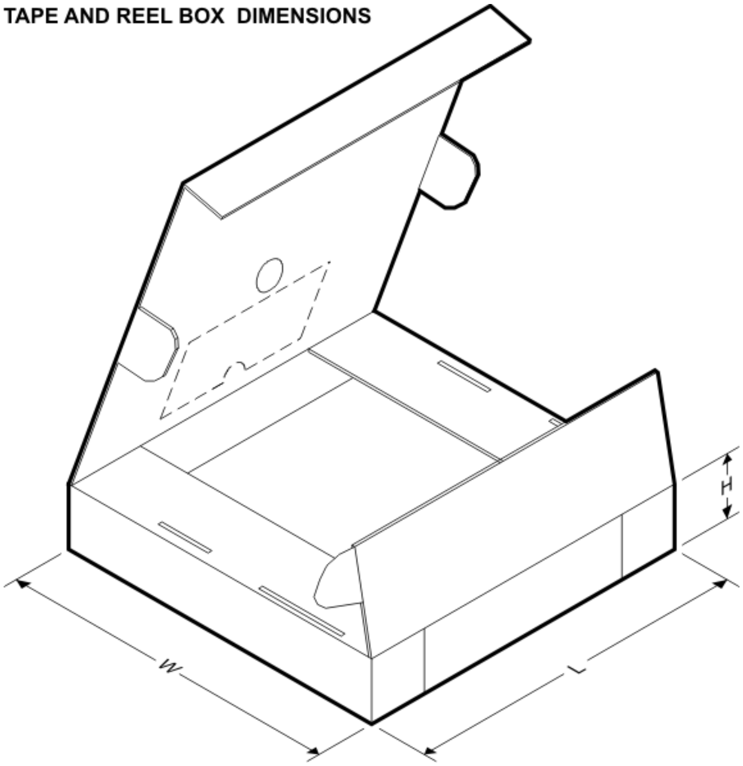
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

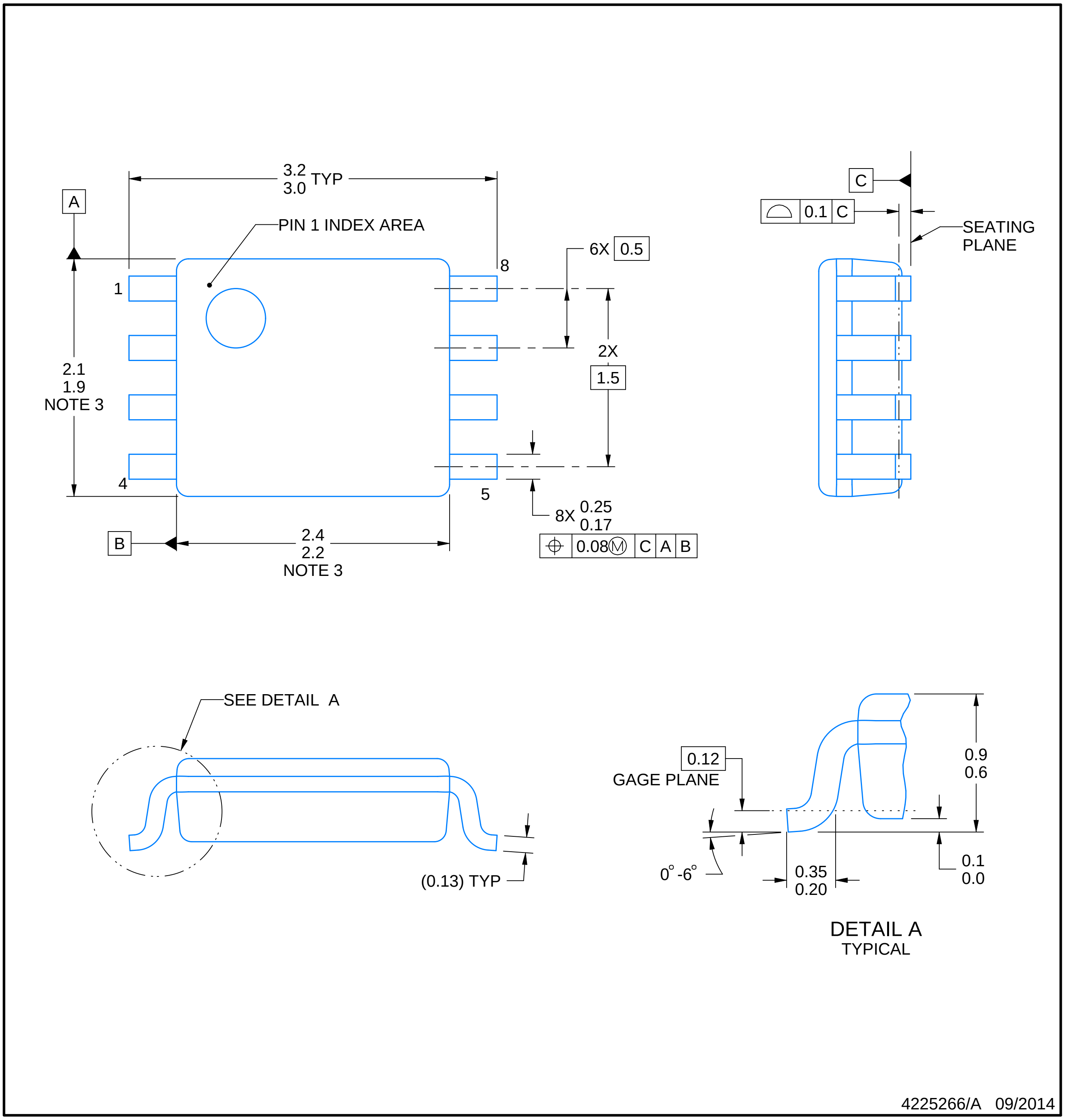
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3357QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



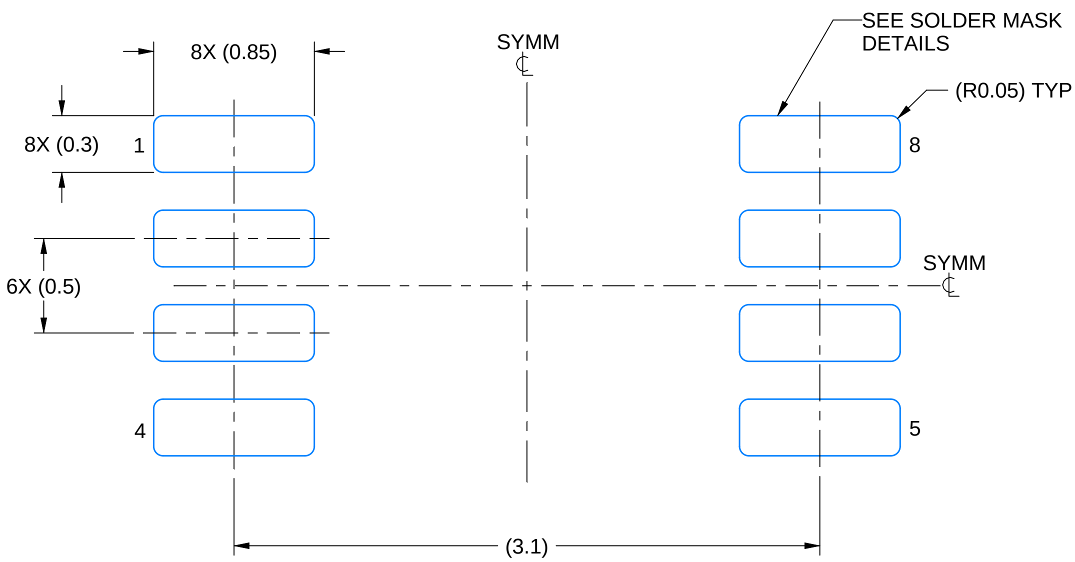
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3357QDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

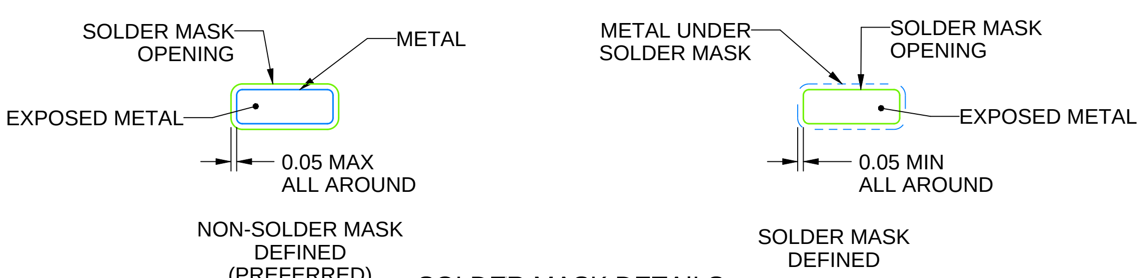


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

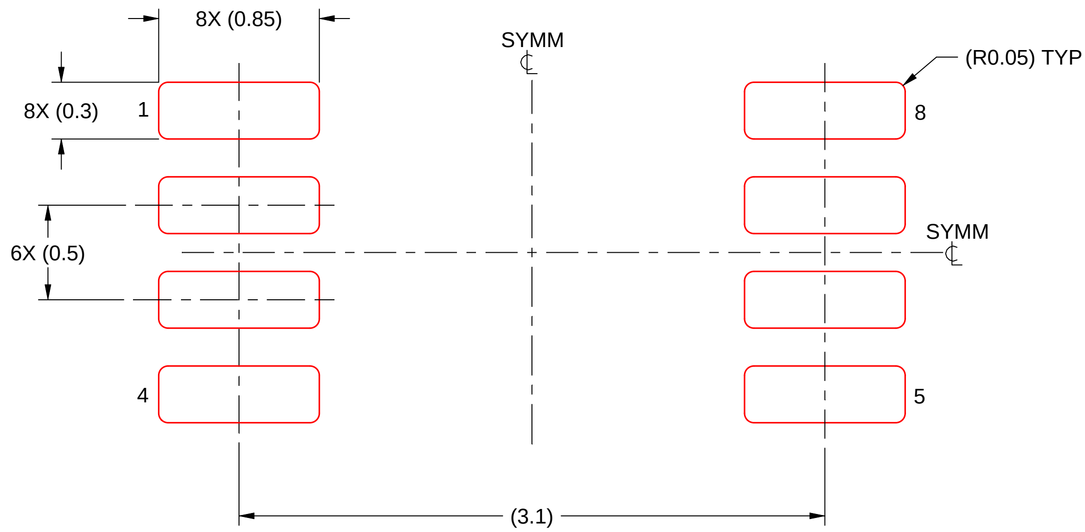


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265