
TRF7960, TRF7961 Multiple-Standard Fully Integrated 13.56-MHz RFID Analog Front End and Data-Framing Reader System

1 Device Overview

1.1 Features

- Completely Integrated Protocol Handling
- Separate Internal High-PSRR Power Supplies for Analog, Digital, and PA Sections Provide Noise Isolation for Superior Read Range and Reliability
- Dual Receiver Inputs With AM and PM Demodulation to Minimize Communication Holes
- Receiver AM and PM RSSI
- Reader-to-Reader Anticollision
- High Integration Reduces Total BOM and Board Area
 - Single External 13.56-MHz Crystal Oscillator
 - MCU-Selectable Clock-Frequency Output of RF, RF/2, or RF/4
 - Adjustable 20-mA High-PSRR LDO for Powering External MCU
- Easy to Use With High Flexibility
 - Automatically Configured Default Modes for Each Supported ISO Protocol
 - 12 User-Programmable Registers
- Selectable Receiver Gain
- Programmable Output Power (100 mW or 200 mW)
- Adjustable ASK Modulation Range (8% to 30%)
- Built-In Receiver Band-Pass Filter With User-Selectable Corner Frequencies
- Wide Operating Voltage Range of 2.7 V to 5.5 V
- Ultra-Low-Power Modes
 - Power Down: <1 μ A
 - Standby: 120 μ A
 - Active (RX Only): 10 mA
- Parallel 8-Bit or Serial 4-Pin Serial Peripheral Interface (SPI) With MCU Using 12-Byte FIFO
- Ultra-Small 32-Pin QFN Package (5 mm \times 5 mm)
- Available Tools (Also See [Tools and Software](#))
 - Reference Design and EVM With Development Software
 - Source Code Available for MSP430™ MCU

1.2 Applications

- Secure Access Control
- Product Authentication
- Medical Systems
- Public Transport or Event Ticketing

1.3 Description

The TRF7960 and TRF7961 devices are integrated analog front end and data-framing systems for a 13.56-MHz [RFID](#) reader system that supports multiple protocols including ISO/IEC 14443 A and B, FeliCa™, and ISO/IEC 15693. Built-in programming options make it suitable for a wide range of applications for proximity and vicinity identification systems.

The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine-tuning of various reader parameters as needed.

The device supports data rates up to 848 kbps with all framing and synchronization tasks for the ISO protocols onboard. Other standards and even custom protocols can be implemented by using one of the direct modes that the device offers. These direct modes let the application fully control the AFE and also gain access to the raw subcarrier data or the unframed, but already ISO-formatted, data and the associated (extracted) clock signal.

The receiver system has a dual-input receiver architecture to maximize communication robustness. The receivers also include various automatic and manual gain control options. The received signal strength from transponders, ambient sources, or internal levels is available in the RSSI register.

A SPI or parallel interface can be used for the communication between the MCU and the TRF796x reader. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 12-byte FIFO register. For direct transmit or receive functions, the encoders or decoders can be bypassed so the MCU can process the data in real time.



The TRF7960 and TRF7961 devices support a wide supply voltage range of 2.7 V to 5.5 V and data communication levels from 1.8 V to 5.5 V for the MCU I/O interface.

The transmitter has selectable output power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply and supports OOK and ASK modulation with selectable modulation depth.

Built-in programmable auxiliary voltage regulator delivers up to 20 mA to supply an MCU and additional external circuits within the reader system.

Start evaluating the TRF7960 multiprotocol transceiver IC with the [TRF7960AEVM](#) or the [TRF7960ATB](#).

[Documentation, Tools, Reference Designs, and Software, Samples](#)

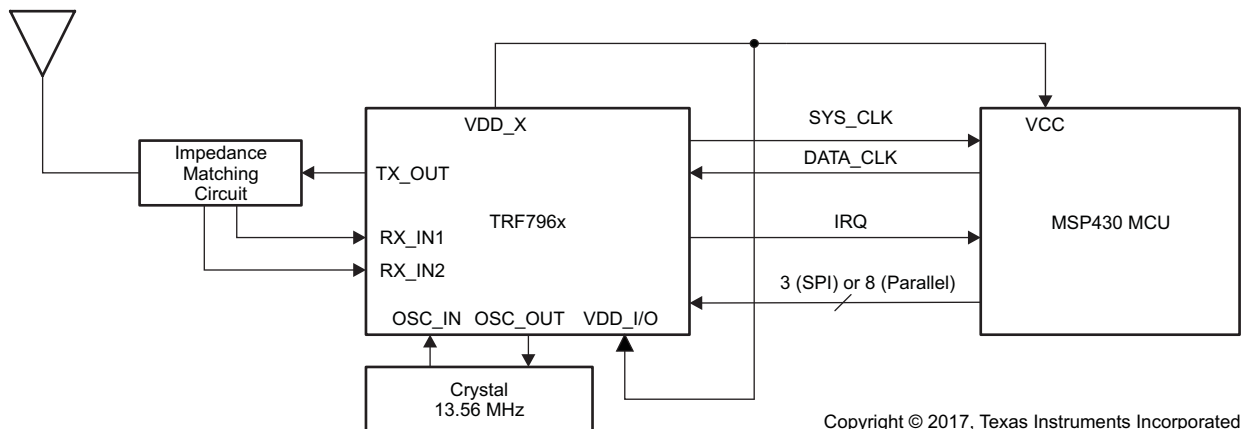
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
TRF7960RHB	VQFN (32)	5 mm x 5 mm
TRF7961RHB	VQFN (32)	5 mm x 5 mm

(1) For more information, see [Section 9, Mechanical, Packaging, and Orderable Information](#).

1.4 Typical Application

Figure 1-1 shows a typical application block diagram.



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Figure 1-1. Application Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 12, 2010 to May 18, 2017	Page
• Removed "and AGC" from "Selectable Receiver Gain" in Section 1.1, Features	1
• Updated list of applications	1
• Changed contents of Section 1.3, Description	1
• Added <i>Device Information</i> table	2
• Added Section 1.4, Typical Application	2
• Added Section 3, Device Comparison , and moved Table 3-1 to it	5
• Added Section 3.1, Related Products	5
• Changed the title of Section 4 from <i>Physical Characteristics</i> to <i>Terminal Configuration and Functions</i>	6
• Removed former Section 3.2, Packaging and Ordering Information (see Section 9, Mechanical, Packaging, and Orderable Information)	7
• Updated note (1) on Section 5.1, Absolute Maximum Ratings , to standard wording	8
• Moved ESD ratings from <i>Absolute Maximum Ratings</i> to Section 5.2, ESD Ratings ; changed ratings from positive voltages only to positive and negative; added notes for HBM and CDM	8
• Changed format of MIN, TYP, and MAX columns in Section 5.4, Electrical Characteristics	8
• Added the f_{D_CLKmax} parameter in Section 5.4, Electrical Characteristics	9
• Changed title of and moved Section 5.5, Thermal Resistance Characteristics	9
• Moved contents of Section 6.1, Overview from former Section 2	10
• Removed a paragraph that began "The second receiver gain stage and digitizer stage..." in Section 6.3, Receiver – Analog Section	17
• Added the last sentence to the paragraph that begins "The start of the receive operation (successfully received SOF)..." in Section 6.3.2, Receiver – Digital Section	18
• Added "and ISO/IEC 15693" to the first sentence of the paragraph that begins "The framing section also supports bit-collision detection..." in Section 6.3.2, Receiver – Digital Section	18
• Changed B2 to Reserved in Table 6-11, Chip Status Control Register (Address = 00h)	23
• Changed B1 and B0 to Reserved in Table 6-22, RX Special Setting Register (Address = 0Ah)	28
• Corrected the name of the Reset FIFO command in Table 6-31, Command Codes , and Section 6.5.2, Reset FIFO	31
• Added the last sentence to the paragraph that begins "The serial communications work in the same manner..." in Section 6.8, Serial Interface Communication	36
• Removed former section <i>External Power Amplifier Application</i>	40
• Added Section 7, Applications, Implementation, and Layout , and moved the application schematics to it	41
• Added Section 8, Device and Documentation Support	43
• Added Section 9, Mechanical, Packaging, and Orderable Information	46

3 Device Comparison

[Table 3-1](#) summarizes the device characteristics.

Table 3-1. Device Comparison

DEVICE	PROTOCOLS					Tag-it™
	ISO/IEC 14443 A AND B				ISO/IEC 15693, ISO/IEC 18000-3	
	106 kbps	212 kbps	424 kbps	848 kbps		
TRF7960	✓	✓	✓	✓	✓	✓
TRF7961					✓	✓

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Wireless Connectivity Connect more with the broadest wireless connectivity portfolio in the industry.

Products for NFC / RFID TI provides one of the most differentiated NFC and RFID product portfolios in the industry and is your solution to meet a broad range of NFC connectivity and RFID identification needs.

Companion Products for TRF7960 Review products that are frequently purchased or used with this product.

Reference Designs for TRF7960 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout of the 32-pin RHB package.

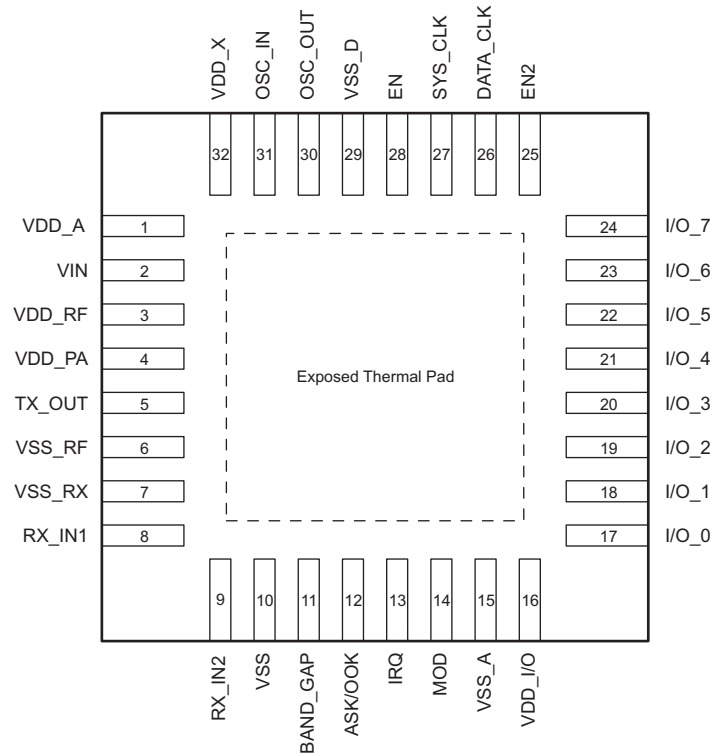


Figure 4-1. 32-Pin RHB Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the device signals.

Table 4-1. Signal Descriptions

TERMINAL		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VDD_A	1	OUT	Internal regulated supply (2.7 V to 3.4 V) for analog circuitry
VIN	2	SUP	External supply input to chip (2.7 V to 5.5 V)
VDD_RF	3	OUT	Internal regulated supply (2.7 V to 5 V), normally connected to VDD_PA (pin 4)
VDD_PA	4	INP	Supply for PA; normally connected externally to VDD_RF (pin 3)
TX_OUT	5	OUT	RF output (selectable output power, 100 mW at 8 Ω or 200 mW at 4 Ω , with $V_{DD} = 5$ V)
VSS_RF	6	SUP	Negative supply for PA; normally connected to circuit ground
VSS_RX	7	SUP	Negative supply for RX inputs; normally connected to circuit ground
RX_IN1	8	INP	RX input, used for AM reception
RX_IN2	9	INP	RX input, used for PM reception
VSS	10	SUP	Chip substrate ground
BAND_GAP	11	OUT	Band-gap voltage (1.6 V); internal analog voltage reference; must be AC-bypassed to ground
ASK/OOK	12	BID	Also can be configured to provide the received analog signal output (ANA_OUT) Direct mode, selects either ASK or OOK modulation (0 = ASK, 1 = OOK)
IRQ	13	OUT	Interrupt request

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

Table 4-1. Signal Descriptions (continued)

TERMINAL		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
MOD	14	INP	Direct mode, external modulation input
VSS_A	15	SUP	Negative supply for internal analog circuits; normally connected to circuit ground
VDD_I/O	16	SUP	Supply for I/O communications (1.8 V to 5.5 V). Should be connected to VIN for 5-V communication, VDD_X for 3.3-V communication, or any other voltage from 1.8 V to 5.5 V.
I/O_0	17	BID	I/O pin for parallel communication
I/O_1	18	BID	I/O pin for parallel communication
I/O_2	19	BID	I/O pin for parallel communication
I/O_3	20	BID	I/O pin for parallel communication
I/O_4	21	BID	I/O pin for parallel communication
I/O_5	22	BID	I/O pin for parallel communication
			Strobe out clock for serial communication
			Data clock output in direct mode
I/O_6	23	BID	I/O pin for parallel communication
			MISO for serial communication (SPI)
			Serial bit data output in direct mode 1 or subcarrier signal in direct mode 0
I/O_7	24	BID	I/O pin for parallel communication.
			MOSI for serial communication (SPI)
EN2	25	INP	Pulse enable and selection of power-down mode. If EN2 is connected to VIN, then VDD_X is active during power down to support the MCU. Pin can also be used for pulse wake up from power-down mode.
DATA_CLK	26	INP	Clock input for MCU communication (parallel and serial)
SYS_CLK	27	OUT	Clock for MCU (3.39 / 6.78 / 13.56 MHz) at EN = 1 and EN2 = don't care
			If EN = 0 and EN2 = 1, then system clock is set to 60 kHz
EN	28	INP	Chip enable input (If EN = 0, then chip is in power-down mode.)
VSS_D	29	SUP	Negative supply for internal digital circuits; normally connected to circuit ground
OSC_OUT	30	OUT	Crystal oscillator output
OSC_IN	31	INP	Crystal oscillator input
VDD_X	32	OUT	Internally regulated supply (2.7 V to 3.4 V) for external circuitry (MCU)
Thermal Pad			Connected to circuit ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{IN}	Supply voltage		6	V	
I _O	Output current		150	mA	
T _J	Maximum junction temperature	Any condition		140	°C
		Continuous operation, long-term reliability ⁽²⁾		125	
T _{stg}	Storage temperature range	-55	150	°C	
	Lead temperature	1,6 mm (1/16 inch) from case for 10 seconds		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

5.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	
		Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Supply voltage	2.7	5	5.5	V
T _J	Operating virtual junction temperature	-40		125	°C
T _A	Operating ambient temperature	-40	25	110	°C

5.4 Electrical Characteristics

TYP values at 25°C, MIN and MAX values over operating ambient temperature range, V_S = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{PD}	Supply current in power-down mode	All systems disabled, including supply voltage regulators		1	10	µA
I _{PD2}	Supply current in power-down mode 2	The reference voltage generator and VDD_X remain active to support external circuitry.		120	300	µA
I _{STBY}	Supply current in standby mode	Oscillator running, supply voltage regulators in low-consumption mode		1.5	4	mA
I _{ON1}	Supply current without antenna driver current	Oscillator, regulators, RX, and AGC are active, TX is off		10	16	mA
I _{ON2}	Supply current with antenna driver current	Oscillator, regulators, RX, AGC, and TX are active, P _{out} = 100 mW		70		mA
I _{ON3}	Supply current with antenna driver current	Oscillator, regulators, RX, AGC, and TX are all active, P _{out} = 200 mW		120		mA
BG	Band-gap voltage	Internal analog reference voltage	1.4	1.6	1.7	V
V _{POR}	Power-on-reset (POR) voltage		1.4	2	2.5	V
V _{DD_A}	Regulated supply for analog circuitry		3.1	3.5	3.8	V

Electrical Characteristics (continued)

TYP values at 25°C, MIN and MAX values over operating ambient temperature range, $V_S = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD_RF}	Regulated supply for RF circuitry	Regulator set for 5-V system with 250-mV difference	4	4.6	5.2	V
V_{DD_X}	Regulated supply for external circuitry		3.1	3.4	3.8	V
P_{PSRR}	Rejection of external supply noise on the supply V_{DD_RF} regulator	The difference between the external supply and the regulated voltage is higher than 250 mV, measured at 212 kHz	20	26		dB
R_{RFOUT}	PA driver output resistance	Half-power mode		8	12	Ω
		Full-power mode		4	6	
R_{RFIN}	RX_IN1 and RX_IN2 input resistance		5	10	20	k Ω
V_{RFIN}	Maximum input voltage	At RX_IN1 and RX_IN2 inputs		3.5		V_{PP}
V_{SENS}	Input sensitivity	$f_{SUBCARRIER} = 424\text{ kHz}$		1.2	2.5	mV $_{PP}$
		$f_{SUBCARRIER} = 848\text{ kHz}$		1.2	3	
t_{SET_PD}	Setup time after power down			10	20	ms
t_{SET_STBY}	Setup time after standby mode			30	100	μs
t_{REC}	Recovery time after modulation (ISO/IEC 14443)	Modulation signal: sine, 424 kHz, 10 mVpp			60	μs
f_{SYS_CLK}	SYS_CLK frequency	In PD2 mode EN = 0 and EN2 = 1	30	60	120	kHz
f_{D_CLKmax}	Maximum DATA_CLK frequency	Depends on capacitive load on the I/O lines, T1 recommends 2 MHz ⁽¹⁾	2	4	8	MHz
CLK_{MAX}	Maximum CLK frequency			2		MHz
V_{IL}	Input logic low			$0.2 \times V_{DD_I/O}$	$0.2 \times V_{DD_I/O}$	V
V_{IH}	Input logic high			$0.8 \times V_{DD_I/O}$		V
R_{OUT}	Output resistance of I/O_0 to I/O_7	low_io = H for $V_{DD_I/O} < 2.7\text{ V}$		400	800	Ω
R_{SYS_CLK}	Output resistance of SYS_CLK	low_io = H for $V_{DD_I/O} < 2.7\text{ V}$		200	400	Ω

- (1) Recommended DATA_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. The MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load is used).

5.5 Thermal Resistance Characteristics

PACKAGE	$R_{\theta_{JC}}$ (°C/W)	$R_{\theta_{JA}}$ ⁽¹⁾ (°C/W)	POWER RATING ⁽²⁾	
			$T_A \leq 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$
RHB (32)	31	36.4	2.7 W	1.1 W

- (1) This data was taken using the JEDEC standard high-K test PCB.
 (2) Power rating is determined with a junction temperature of 125°C. This is the temperature at which distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

6 Detailed Description

6.1 Overview

Figure 6-1 shows a typical application diagram for the TRF796x devices. A parallel or serial interface can be implemented for communication between the MCU and reader. Transmit and receive functions use internal encoders and decoders with a 12-byte FIFO register. For direct transmit or receive functions, the encoders and decoders can be bypassed so the MCU can process the data in real time. The transmitter has selectable output power levels of 100 mW (20 dBm) or 200 mW (23 dBm) into a 50-Ω load (5-V supply) and supports ASK or OOK modulation. Integrated voltage regulators ensure power-supply noise rejection for the complete reader system.

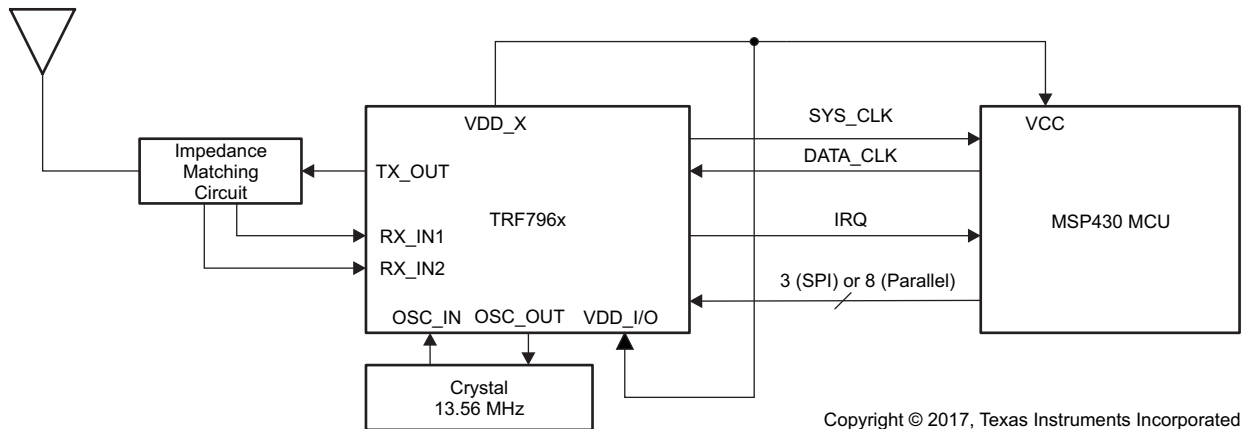


Figure 6-1. Typical Application Diagram

Data transmission supports low-level encoding for ISO/IEC 15693, modified Miller for ISO/IEC 14443 A, high-bit-rate systems for ISO/IEC 14443, and Tag-it coding systems. Included with the data encoding is automatic generation of SOF, EOF, CRC, and parity bits.

The receiver system enables AM and PM demodulation using a dual-input architecture. The receiver also includes an automatic gain control option and selectable gain. Also included is a selectable bandwidth to cover a broad range of input subcarrier signal options. The received signal strength for AM and PM modulation is accessible through the RSSI register. The receiver output is a digitized subcarrier signal among a selectable protocol and bit rate as outlined in Table 6-13. A selected decoder delivers bit stream and a data clock as outputs.

The receiver system also includes a framing system. This system performs a CRC or parity check, removes the EOF and SOF settings, and organizes the data in bytes. Framed data is then accessible to the MCU through a 12-byte FIFO register and MCU interface. The framing supports ISO/IEC 14443 and ISO/IEC 15693 protocols.

The TRF796x supports data communication levels from 1.8 V to 5.5 V for the MCU I/O interface, while also providing a data synchronization clock. An auxiliary 20-mA regulator (pin 32) is available for additional system circuits.

6.2 Power Supplies

The positive supply pin, VIN (pin 2), has an input voltage range of 2.7 V to 5.5 V. The positive supply input sources three internal regulators with output voltages V_{DD_RF} , V_{DD_A} , and V_{DD_X} that use external bypass capacitors for supply noise filtering. These regulators provide enhanced PSRR for the RFID reader system. Table 6-1 describes the power supplies.

The regulators are not independent and have common control bits for output voltage setting. The regulators can be configured to operate in either automatic or manual mode. The automatic regulator mode setting ensures an optimal compromise between regulator PSRR and highest possible supply voltage for RF output power. The manual mode allows the application to manually configure the regulator settings.

Table 6-1. Power Supplies

SUPPLY	DESCRIPTION
V_{DD_RF}	<p>The regulator V_{DD_RF} (pin 3) is used to source the RF output stage. The voltage regulator can be set for either 5-V or 3-V operation.</p> <p>When configured for 5-V operation, the output voltage can be set from 4.3 V to 5 V in 100-mV steps. The current sourcing capability for 5-V operation is 150 mA maximum over the adjusted output voltage range.</p> <p>When configured for 3-V operation, the output voltage can be set from 2.7 V to 3.4 V, also in 100-mV steps. The current sourcing capability for 3-V operation is 100 mA maximum over the adjusted output voltage range.</p>
V_{DD_A}	<p>Regulator V_{DD_A} (pin 1) supplies voltage to analog circuits within the reader chip. The voltage setting is divided in two ranges. When configured for 5-V operation, the output voltage is fixed at 3.5 V. When configured for 3-V operation, the output voltage can be set from 2.7 V to 3.4 V in 100-mV steps.</p> <p>NOTE: The V_{DD_A} and V_{DD_X} regulators are configured together (their settings are not independent).</p>
V_{DD_X}	<p>Regulator V_{DD_X} (pin 32) can be used to source the digital I/O of the reader chip together with other external system components. When configured for 5-V operation, the output voltage is fixed at 3.4 V. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps.</p> <p>The total current sourcing capability of the V_{DD_X} regulator is 20 mA (maximum) over the adjusted output range.</p> <p>NOTE: The V_{DD_A} and V_{DD_X} regulators are configured together (their settings are not independent).</p>
V_{DD_PA}	<p>The V_{DD_PA} pin (pin 4) is the positive supply pin for the RF output stage and is externally connected to the regulator output V_{DD_RF} (pin 3).</p>

6.2.1 Negative Supply Connections

The negative supply connections are all externally connected together (to GND). The substrate connection is V_{SS} (pin 10), the analog negative supply is V_{SS_A} (pin 15), the logic negative supply is V_{SS_D} (pin 29), the RF output stage negative supply is V_{SS_TX} (pin 6), and the negative supply for the RF receiver input is V_{SS_RX} (pin 7).

6.2.2 Digital I/O Interface

To allow compatible I/O signal levels, the TRF796x has a separate supply input $V_{DD_I/O}$ (pin 16), with an input voltage range of 1.8 V to 5.5 V. This pin supplies the I/O interface (I/O_0 to I/O_7), IRQ, SYS_CLK, and DATA_CLK pins of the reader. In typical applications, $V_{DD_I/O}$ is connected directly to V_{DD_X} to ensure that the I/O signal levels of the MCU are the same as the internal logic levels of the reader.

6.2.3 Supply Regulator Configuration

The supply regulators can be automatically or manually configured by the control bits. [Table 6-2](#) lists the manual regulator settings for a 5-V system. [Table 6-3](#) lists the manual regulator settings for a 3-V system. [Table 6-4](#) and [Table 6-5](#) list the automatic mode gain settings for 5-V and 3-V systems, respectively.

The automatic mode is the default configuration. In automatic mode, the regulators are automatically set every time the system is activated by asserting the EN input high. The internal regulators are also automatically reconfigured every time the automatic regulator selection bit is set high (on the rising edge).

The application can reset the automatic mode setting from a state in which the automatic setting bit is already high by changing the automatic setting bit from high to low to high. The regulator-configuration algorithm adjusts the regulator outputs 250 mV below the V_{IN} level, but not higher than 5 V for V_{DD_RF} , 3.5 V for V_{DD_A} , and 3.4 V for V_{DD_X} . This algorithm ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio). As an example, the application can improve the PSRR if there is a noisy supply voltage from V_{DD_X} by increasing the target voltage difference across the V_{DD_X} regulator as listed for automatic regulator settings in [Table 6-4](#) and [Table 6-5](#).

Table 6-2. Supply-Regulator Setting – Manual – 5-V System

BYTE ADDRESS	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
0x00								1	5-V system
0x0B	0								Manual regulator setting
0x0B	0					1	1	1	$V_{DD_RF} = 5\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					1	1	0	$V_{DD_RF} = 4.9\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					1	0	1	$V_{DD_RF} = 4.8\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					1	0	0	$V_{DD_RF} = 4.7\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					0	1	1	$V_{DD_RF} = 4.6\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					0	1	0	$V_{DD_RF} = 4.5\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					0	0	1	$V_{DD_RF} = 4.4\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$
0x0B	0					0	0	0	$V_{DD_RF} = 4.3\text{ V}$, $V_{DD_A} = 3.5\text{ V}$, $V_{DD_X} = 3.4\text{ V}$

Table 6-3. Supply-Regulator Setting – Manual – 3-V System

BYTE ADDRESS	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
0x00								0	3-V system
0x0B	0								Manual regulator setting
0x0B	0					1	1	1	$V_{DD_RF} = 3.4\text{ V}$, V_{DD_A} , $V_{DD_X} = 3.4\text{ V}$
0x0B	0					1	1	0	$V_{DD_RF} = 3.3\text{ V}$, V_{DD_A} , $V_{DD_X} = 3.3\text{ V}$
0x0B	0					1	0	1	$V_{DD_RF} = 3.2\text{ V}$, V_{DD_A} , $V_{DD_X} = 3.2\text{ V}$
0x0B	0					1	0	0	$V_{DD_RF} = 3.1\text{ V}$, V_{DD_A} , $V_{DD_X} = 3.1\text{ V}$
0x0B	0					0	1	1	$V_{DD_RF} = 3.0\text{ V}$, V_{DD_A} , $V_{DD_X} = 3.0\text{ V}$
0x0B	0					0	1	0	$V_{DD_RF} = 2.9\text{ V}$, V_{DD_A} , $V_{DD_X} = 2.9\text{ V}$
0x0B	0					0	0	1	$V_{DD_RF} = 2.8\text{ V}$, V_{DD_A} , $V_{DD_X} = 2.8\text{ V}$
0x0B	0					0	0	0	$V_{DD_RF} = 2.7\text{ V}$, V_{DD_A} , $V_{DD_X} = 2.7\text{ V}$

Table 6-4. Supply-Regulator Setting – Automatic – 5-V System

BYTE ADDRESS	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2 ⁽¹⁾	B1	B0	
0x00								1	5-V system
0x0B	1					x	1	1	Automatic regulator setting; approximately 250-mV difference
0x0B	1					x	1	0	Automatic regulator setting; approximately 350-mV difference
0x0B	1					x	0	0	Automatic regulator setting; approximately 400-mV difference

(1) x = Don't care

Table 6-5. Supply-Regulator Setting – Automatic – 3-V System

BYTE ADDRESS	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2 ⁽¹⁾	B1	B0	
0x00								0	3-V system
0x0B	1					x	1	1	Automatic regulator setting; approximately 250-mV difference
0x0B	1					x	1	0	Automatic regulator setting; approximately 350-mV difference
0x0B	1					x	0	0	Automatic regulator setting; approximately 400-mV difference

(1) x = Don't care

6.2.4 Power Modes

The chip has seven power states, which are controlled by two input pins (EN and EN2) and three bits in the Chip Status Control register (00h).

The main reader enable input is EN (which has a threshold level of 1 V [minimum]). Any input signal level from 1.8 V to V_{IN} can be used. When EN is set high, all of the reader regulators are enabled, together with the 13.56-MHz oscillator, and the SYS_CLK output clock for an external MCU.

The auxiliary enable input EN2 has two functions:

- A direct connection from EN2 to V_{IN} ensures availability of the regulated supply (V_{DD_X}) and an auxiliary clock signal (60 kHz) on the SYS_CLK output (same for the case EN = 0). This mode is intended for systems in which the MCU controlling the reader is also being supplied by the reader supply regulator (V_{DD_X}) and the MCU clock is supplied by the SYS_CLK output of the reader. This lets the MCU supply and clock be available during power down.
- EN2 enables start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case, the EN input is controlled by the MCU or other system device that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has a 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1). This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high by the MCU (or other system device), the reader stays active. If the EN input is not set high within 100 μ s after the SYS_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to a complete power-down mode. This option can be used to wake the reader system from complete power down by using a push-button switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits. [Table 6-6](#) lists the power mode options and functions.

Table 6-6. Power Modes

BYTE ADDRESS	OPTION BITS SETTING IN CHIP STATUS CONTROL REGISTER								EN	EN2	FUNCTIONALITY	CURRENT
	B7 stby	B6	B5 rfon	B4	B3 rf_pwr	B2	B1 rec_on	B0				
0x00									0	0	Complete power down	<1 μ A
0x00									0	1	VDD_X available, SYS_CLK auxiliary frequency 60 kHz is ON	120 μ A
0x00	1		x	x				x	1	x	All supply regulators active and in low power mode, 13.56-MHz oscillator on, SYS_CLK clock available	1.5 mA
0x00	0		0	x				0	1	x	All supply regulators active, 13.56-MHz oscillator on, SYS_CLK clock available	3.5 mA
0x00	0		0	x				1	1	x	All supply regulators active, 13.56-MHz oscillator on, SYS_CLK clock available, Receiver active	10 mA
0x00	0		1	1				x	1	x	All supply regulators active, 13.56-MHz oscillator on, SYS_CLK clock available, Receiver active, Transmitter active in half-power mode	70 mA (at 5 V)
0x00	0		1	0				x	1	x	All supply regulators active, 13.56-MHz oscillator running, SYS_CLK clock available, Receiver active, Transmitter active in full-power mode	120 mA (at 5 V)

During reader inactivity, the TRF796x can be placed in power-down mode (EN = 0). The power down can be complete (EN = 0, EN2 = 0) with no function running, or partial (EN = 0, EN2 = 1) with the regulated supply (V_{DD_X}) and 60-kHz auxiliary clock (SYS_CLK) available to the MCU or other system device.

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1), the supply regulators are activated and the 13.56-MHz oscillator is started. When the supplies are settled and the oscillator frequency is stable, the SYS_CLK output is switched from the auxiliary frequency of 60 kHz to the selected frequency derived from the crystal oscillator. At this time, the reader is ready to communicate and perform the required tasks. The control system (MCU) can then write appropriate bits to the Chip Status Control register (address 0x00) and select the operation mode.

The standby mode (bit 7 = 1 in register 0x00) is the active mode with the lowest current consumption. The reader can recover from this mode to full operation in 100 μ s.

The active mode with RF section disabled (bit 5 = 0 and bit 1 = 0 in register 0x00) is the next active mode with low power consumption. The reader is capable of recovering from this mode to full operation in 25 μ s.

The active mode with only the RF receiver section active (bit 1 = 1 in register 0x00) can be used to measure the external RF field (see [Section 6.3.1](#)) if reader-to-reader anticollision is implemented.

The active mode with the entire RF section active (bit 5 = 1 in register 0x00) is the normal mode used for transmit and receive operations.

6.2.5 Timing Diagrams

[Figure 6-2](#) shows an oscilloscope trace of chip power up.

[Figure 6-3](#) shows an oscilloscope trace of chip enable to clock start with EN2 low and EN high.

[Figure 6-4](#) shows an oscilloscope trace of chip enable to clock start with EN2 high and EN low.

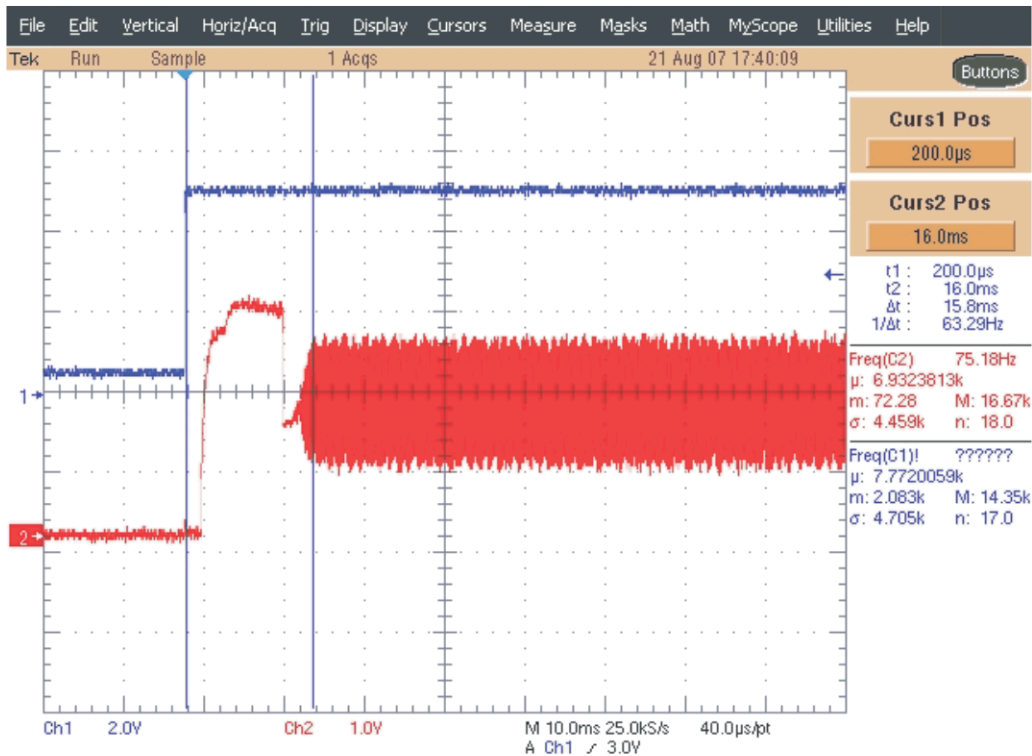


Figure 6-2. Chip Power Up [V_{IN} (Blue) to Crystal Start (Red)]

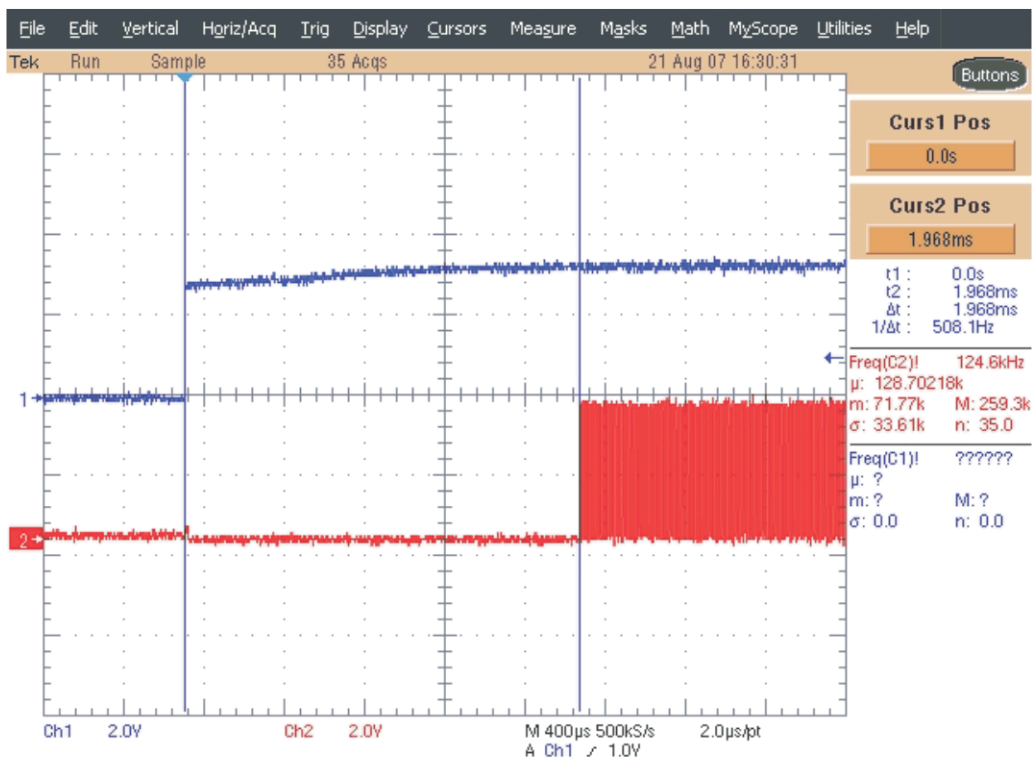


Figure 6-3. Chip Enable to Clock Start, EN2 Low and EN High (Blue) to Start of System Clock (Red)

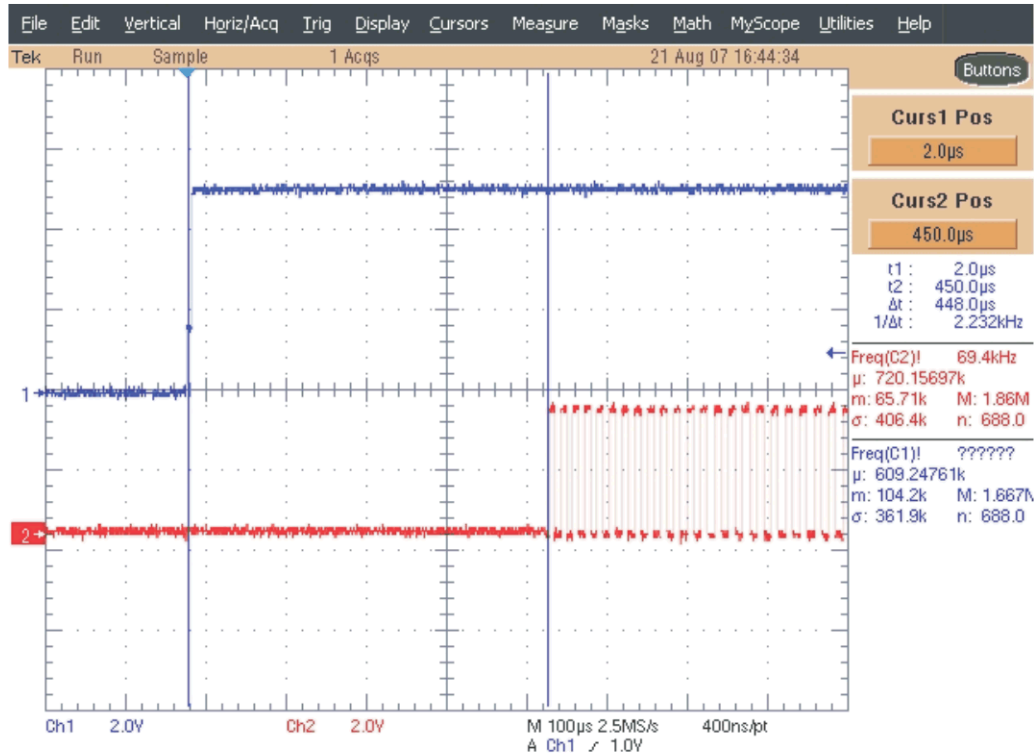


Figure 6-4. Chip Enable to Clock Start, EN2 High and EN Low (Blue) to Start of System Clock (Red)

6.3 Receiver – Analog Section

The TRF796x has two receiver inputs, RX_IN1 (pin 8) and RX_IN2 (pin 9). The two inputs are connected to an external filter to ensure that AM modulation from the tag is available on at least one of the two inputs. The external filter provides a 45° phase shift for the RX_IN2 input to allow further processing of a received PM-modulated signal (if it appears) from the tag. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs are multiplexed to two receiver channels: the main receiver and the auxiliary receiver. Receiver input multiplexing is controlled by control bit B3 (pm_on) in the Chip Status Control register (address 0x00). The main receiver is composed of an RF-detection stage, gain, filtering with AGC, and a digitizing stage whose output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal.

The primary function of the auxiliary receiver is to measure the RSSI of the modulation signal. It also has similar RF-detection, gain, filtering with AGC, and RSSI blocks.

The default setting is RX_IN1 connected to the main receiver and RX_IN2 connected to the auxiliary receiver (bit pm_on = 0). When a response from the tag is detected by the RSSI, values on both inputs are measured and stored in the RSSI Level register (address 0x0F). The control system reads the RSSI values and switches to the stronger receiver input (RX_IN1 or RX_IN2 by setting pm_on = 1).

The receiver input stage is an RF level detector. The RF amplitude level on RX_IN1 and RX_IN2 inputs should be approximately 3 V_{PP} for a V_{IN} supply level greater than 3.3 V. If the V_{IN} level is lower, the RF input peak-to-peak voltage level should not exceed the V_{IN} level. V_{IN} is the main supply voltage to the device at pin 2.

The first gain and filtering stage following the RF-envelope detector has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has adjustable 3-dB frequency steps (100 kHz to 400 kHz for high pass and 600 kHz to 1500 kHz for low pass). Following the band-pass filter is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first stage.

The internal filters are configured automatically, with internal presets for each new selection of a communication standard in the ISO Control register (address 0x01). If required, additional fine-tuning can be accomplished by writing directly to the RX Special Setting register (address 0x0A). [Table 6-22](#) lists the bits of the RX Special Settings register (address 0x0A) that control the receiver analog section.

6.3.1 Received Signal Strength Indicator (RSSI)

The RSSI measurement block measures the demodulated signal (except in the case of a direct command for RF-amplitude measurement; see [Section 6.5](#)). The measuring system latches the peak value, so the RSSI level can be read after the end of the receive packet. The RSSI register values reset with every transmission by the reader. This allows an updated RSSI measurement for each new tag response.

[Table 6-7](#) and [Table 6-8](#) list the correlation between the RF input level and RSSI designation levels on RX_IN1 and RX_IN2.

[Table 6-7](#) compares the RSSI level and the RSSI bit value. The RSSI has seven levels (3 bits each) with 4-dB increments. The input level is the peak-to-peak modulation level of the RF signal as measured on one side envelope (positive or negative).

Table 6-7. RSSI Level Versus Register Bit Value

RSSI	1	2	3	4	5	6	7
Input level	2 mVpp	3.2 mVpp	5 mVpp	8 mVpp	13 mVpp	20 mVpp	32 mVpp

As an example, from [Table 6-8](#), let B2 = 1, B1 = 1, B0 = 0. This yields an RSSI value of 6. From [Table 6-7](#) a bit value of 6 indicates an RSSI level of 20 mVpp.

Table 6-8. RSSI Bit Value and Oscillator Status Register (0x0F)

BIT	SIGNAL	FUNCTION	COMMENTS
B7	Unused		
B6	osc_ok	Crystal oscillator stable	
B5	rss_i_x2	Most significant bit (MSB) of auxiliary receiver RSSI	4 dB per step
B4	rss_i_x1	Auxiliary receiver RSSI	
B3	rss_i_x1	Least significant bit (LSB) of auxiliary receiver RSSI	
B2	rss_i_2	MSB of main receiver RSSI	4 dB per step
B1	rss_i_1	Main receiver RSSI	
B0	rss_i_0	LSB of main receiver RSSI	

6.3.2 Receiver – Digital Section

The received subcarrier is digitized to form a digital representation of the modulated RF envelope. This digitized signal is applied to digital decoders and framing circuits for further processing.

The digital part of the receiver consists of two sections, which partly overlap. The first section consists of the bit decoders for the various protocols, and the second section consists of the framing logic. The bit decoders convert the subcarrier coded signal to a bit stream and also to the data clock. Thus, the subcarrier-coded signal is transformed to serial data, and the data clock is extracted. The decoder logic is designed for maximum error tolerance. This enables the decoders to successfully decode even partly corrupted (due to noise or interference) subcarrier signals.

In the framing section, the serial bit stream data is formatted in bytes. In this process, special signals like the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are checked and also removed. The end result is clean or raw data, which is sent to the 12-byte FIFO register where it can be read by the external microcontroller system.

The start of the receive operation (successfully received SOF) sets the flags in the IRQ Status register. The end of the receive operation is indicated to the external system (MCU) by sending an interrupt request (pin 13, IRQ). If the receive data packet is longer than 8 bytes, an interrupt is sent to the MCU when the received data occupies 75% of the FIFO capacity to signal that the data should be removed from the FIFO. Use the FIFO Status register (0x1C) to provide the number of bytes that should be clocked out during the actual FIFO read.

If any error in data format, parity, or CRC is detected, the external system is notified of the error by an interrupt-request pulse. The source condition of the interrupt-request pulse is available in the IRQ Status register (address 0x0C) (see [Table 6-24](#)).

The ISO Control register (address 0x01) is the primary control for the digital part of the receiver. By writing to this register, the application selects the protocol to be used. With each new write in this register, the default presets are loaded in all related registers, so no further adjustments in other registers are typically needed for proper operation.

[Table 6-12](#) describes the coding of the ISO Control register. The TRF7961 does not include the ISO/IEC 14443 functionality; therefore, the features and commands for this protocol are not functional for the TRF7961.

The framing section also supports bit-collision detection as specified in ISO/IEC 14443 A and ISO/IEC 15693. When a bit collision is detected, an interrupt request is sent and a flag is set in the IRQ Status register. For ISO/IEC 14443 A specifically, the position of the bit collision is written in two registers: partly in the Collision Position register (0x0E) and partly in the Collision Position and Interrupt Mask register (0x0D) (bits B6 and B7). The collision position is presented as a sequential bit number, where the count starts immediately after the start bit. For example, the collision in the first bit of the UID would give the value 00 0001 0000 in the collision position registers. The count starts with 0, and the first 16 bits are the command code and the NVB byte (the NVB byte is the number of valid bits).

The receive section also has two timers. The RX wait time timer is controlled by the value in the RX Wait Time register (address 0x08). This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX Wait Time register defines this time in increments of 9.44 μ s. This register is preset at every write to ISO Control register (address 0x01) according to the minimum tag-response time defined by each standard.

The RX no response timer is controlled by the RX No Response Wait Time register (address 0x07). This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ Status Control register. This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 μ s. This register is also preset, automatically, for every new protocol selection.

6.3.3 Transmitter

The transmitter section consists of the 13.56-MHz oscillator, digital protocol processing, and RF output stage.

6.3.3.1 Transmitter – Analog Section

The 13.56-MHz crystal oscillator (connected to pins 31 and 32) directly generates the RF for the RF output stage. It also generates the clock signal for the digital section and the clock signal output on SYS_CLK (pin 27), which can be used by an external MCU system.

During partial power-down mode (EN = 0, EN2 = 1), the frequency of SYS_CLK is 60 kHz. During normal reader operation, SYS_CLK can be programmed by bits B4 and B5 in the Modulator and SYS_CLK Control register (address 0x09); available clock frequencies are 13.56 MHz, 6.78 MHz, or 3.39 MHz.

[Table 6-9](#) lists the recommendations for the reference crystal (HC49U).

Table 6-9. Crystal Recommendations

PARAMETER	SPECIFICATION
Frequency	13.560000 MHz
Mode of operation	Fundamental
Type of resonance	Parallel
Frequency tolerance	±20 ppm
Aging	<5 ppm/year
Operation temperature range	–40°C to 85°C
Equivalent series resistance	50 Ω, minimum

NOTE

The value of the two external shunt capacitors on the crystal oscillator is calculated based on the specified load capacitance of the crystal. The external capacitors (connected to the OSC pins 30 and 31), are calculated as two capacitors in series plus C_S (the internal I/O capacitance of the oscillator gate plus PCB stray capacitance). The stray capacitance (C_S) can be estimated at 5 ± 2 pF (typical).

As an example, given a crystal with a required load capacitance (C_L) of 18 pF,

$$C_L = ((C_1 \times C_2) / (C_1 + C_2)) + C_S$$

$$18 \text{ pF} = ((27 \text{ pF} \times 27 \text{ pF}) / (27 \text{ pF} + 27 \text{ pF})) + 4.5 \text{ pF}$$

From this example, 18-pF capacitors would be placed on pins 30 and 31 to ensure proper crystal oscillator operation.

The transmit power level is selectable as either half power of 100 mW (20 dBm) or full power of 200 mW (23 dBm) when configured for 5-V automatic operation. The transmit output impedance is 8 Ω when configured for half power and 4 Ω when configured for full power. Selection of the transmit power level is set by bit B4 (rf_pwr) in the Chip Status Control register (see [Table 6-11](#)). When configured for 3-V automatic operation, the transmit power level is typically selectable as either 33 mW (15 dBm) in half-power mode or 70 mW (18 dBm) in full-power mode (VDD_RF at 3.3 V). Lower operating voltages result in reduced transmit power levels.

In typical operation, the transmit modulation is configured by the selected ISO Control register (address 0x01). External control of the transmit modulation is possible by setting the ISO Control register (address 0x01) to direct mode. While in direct mode, the transmit modulation is set by the ASK/OOK pin (pin 12). External control of the modulation type is enabled by setting B6 = 1 (en_ook_p) in the Modulator and SYS_CLK Control register (address 0x09). ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS_CLK Control register (address 0x09). The range of the ASK modulation is 7% to 30%, or 100% (OOK).

[Table 6-21](#) describes the coding of the Modulator and SYS_CLK Control register.

The length of the modulation pulse is defined by the protocol selected in the ISO Control register. With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX Pulse Length register. If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 00h, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment is 73.7 ns to 18.8 μs.

6.3.3.2 Transmitter – Digital Section

The digital portion of the transmitter is very similar to that of the receiver. Before beginning data transmission, the FIFO should be cleared with a Reset command (0x0F). Data transmission is initiated with a selected command (see [Table 6-31](#)). The MCU then commands the reader to do a continuous Write command (3Dh, see [Table 6-33](#)) starting from register 1Dh. Data written into register 1Dh is the TX Length Byte1 (upper and middle nibbles), while the following byte in register 1Eh is the TX Length Byte2 (lower nibble and broken byte length). The TX byte length determines when the reader sends the EOF byte. After the TX length bytes, FIFO data is loaded in register 1Fh with byte storage locations 0 to 11. Data transmission begins automatically after the first byte is written into the FIFO. The TX Length bytes and FIFO can be loaded with a continuous-write command because the addresses are sequential.

If the data length is longer than the allowable size of the FIFO, the external system (MCU) is warned when the majority of data from the FIFO has already been transmitted by sending an interrupt request with a flag in the IRQ register signaling FIFO low or high status. The external system should respond by loading the next data packet into the FIFO.

At the end of the transmit operation, the external system is notified by another interrupt request with a flag in the IRQ register that signals the end of TX.

The TX Length register also supports incomplete bytes transmitted. The high 2 nibbles in register 0x1D and the nibble composed of bits B4 to B7 in register 0x1E store the number of complete bytes to be transmitted. Bit 0 (in register 0x1E) is a flag that signals the presence of additional bits to be transmitted that do not form a complete byte. The number of bits are stored in bits B1 to B3 of the same register (0x1E).

The protocol is selected by the ISO Control register (address 0x01), which also selects the receiver protocol. As defined by the selected protocol, the reader automatically adds all the special signals, like start of communication, end of communication, SOF, EOF, parity bits, and CRC bytes. The data is then coded to the modulation pulse level and sent to the modulation control of the RF output stage. This means that the external system is only required to load the FIFO with data, and all the low-level coding is done automatically. Also, all registers used in transmission are automatically preset to the optimum value when a new selection is entered into the ISO Control register.

Some protocols have options, and two registers are provided to select the TX protocol options. The first register is ISO14443B TX Options (address 0x02). This register controls the SOF and EOF selection and EGT (extra guard time) selection for the ISO/IEC 14443 B protocol (see [Table 6-14](#)).

The second register controls the ISO/IEC 14443 high-bit-rate options. This register enables the use of different bit rates for RX and TX operations in the ISO/IEC 14443 high bit-rate protocol. Additionally, it also selects the parity system for the ISO/IEC 14443 A high-bit-rate selection (see [Table 6-15](#)).

The transmit section also has a timer that can be used to start the transmit operation at a precise time interval from a selected event. This is necessary if the tag requires a reply in an exact window of time following the tag response. The TX timer uses two registers (addresses 0x04 and 0x05). In first register (address 0x04), two bits (B7 and B6) define the trigger conditions. The remaining 6 bits are the upper bits and the 8 bits in register address 0x05 are lower bits, which are preset to the counter. The increment is 590 ns and the range of this counter is from 590 ns to 9.7 ms. See [Table 6-16](#) for the bit definitions (trigger conditions).

6.3.4 Direct Mode

Direct mode supports two configurations:

Direct mode 0 (bit 6 = 0 in the ISO Control register) enables use of only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the application has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the application has direct access to the subcarrier signal (digitized RF envelope signal) on I/O_6 (pin 23).

Direct mode 1 (bit 6 = 1 in the ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in the ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O_6 (pin 23) and the bit clock is available on I/O_5 (pin 22). The transmit side is identical; the application has direct control over the RF modulation through the MOD input. This mode is provided so that the application can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To use direct mode, first select the direct mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the direct mode when B6 (direct) is set to 1 in the Chip Status Control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the direct mode and clears B6. This is necessary as the direct mode uses one or two I/O pins (I/O_6, I/O_5). Standard parallel communication is not possible in direct mode. Sending a stop condition terminates direct mode.

Figure 6-5 shows mode 0 and mode 1 in direct mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.

In mode 2 (standard mode), data is ISO-standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data through a 12-byte FIFO.

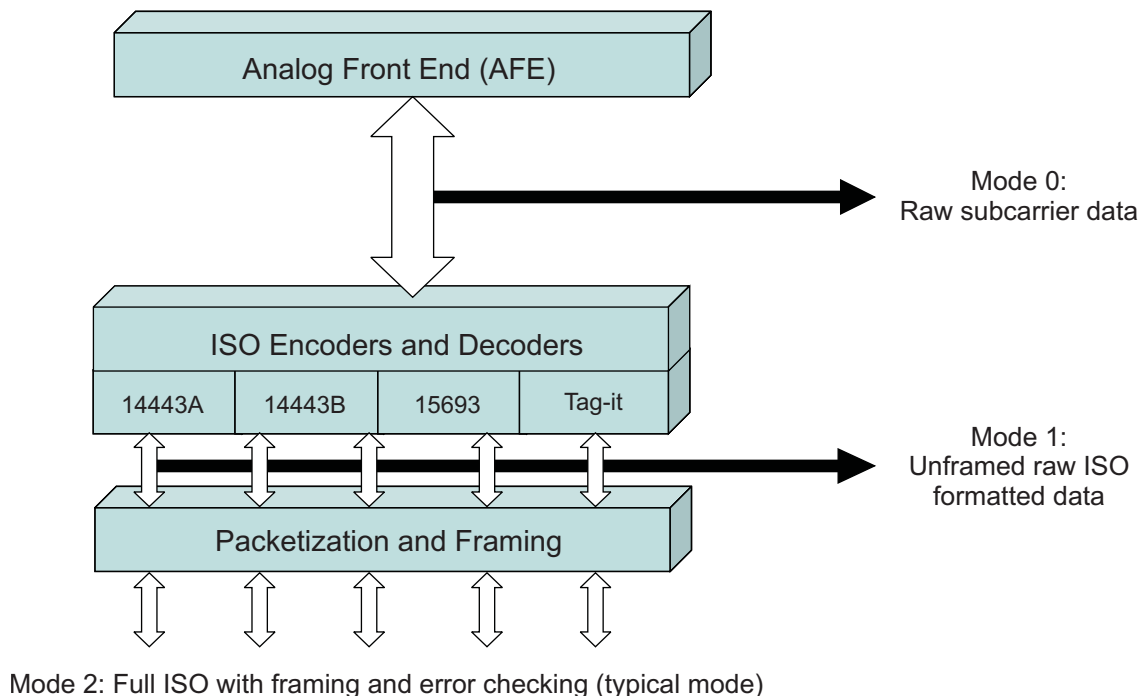


Figure 6-5. User-Configurable Modes

6.3.5 Register Preset

After power up and the EN pin low-to-high transition, the reader is in the default mode. The default configuration is ISO/IEC 15693, single subcarrier, high data rate, 1-out-of-4 operation. The low-level option registers (0x02 to 0x0B) are automatically set to adapt the circuitry optimally to the appropriate protocol parameters.

When entering another protocol (writing to the ISO Control register [0x01]), the low-level option registers (0x02 to 0x0B) are automatically configured to the new protocol parameters.

After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back, reloads the default settings, and the application must reload the custom settings.

The Clo1 and Clo0 bits in register 0x09, which define the microcontroller frequency available on the SYS_CLK pin, are the only two bits in the configuration registers that are not cleared during protocol selection.

6.4 Register Descriptions

Table 6-10 lists the registers by address.

Table 6-10. Register Address Space

ADDRESS	REGISTER	READ/WRITE	DETAILS
Main Control Registers			
0x00	Chip status control	R/W	Table 6-11
0x01	ISO control	R/W	Table 6-12
Protocol Subsetting Registers			
0x02	ISO14443B TX options	R/W	Table 6-14
0x03	ISO14443A high bit rate options	R/W	Table 6-15
0x04	TX timer setting, H-byte	R/W	Table 6-16
0x05	TX timer setting, L-byte	R/W	Table 6-17
0x06	TX pulse-length control	R/W	Table 6-18
0x07	RX no response wait	R/W	Table 6-19
0x08	RX wait time	R/W	Table 6-20
0x09	Modulator and SYS_CLK control	R/W	Table 6-21
0x0A	RX special setting	R/W	Table 6-22
0x0B	Regulator and I/O control	R/W	Table 6-23
0x16	Unused	NA	
0x17	Unused	NA	
0x18	Unused	NA	
0x19	Unused	NA	
Status Registers			
0x0C	IRQ status	R	Table 6-24
0x0D	Collision position and interrupt mask register	R/W	Table 6-25
0x0E	Collision position	R	Table 6-26
0x0F	RSSI levels and oscillator status	R	Table 6-27
FIFO Registers			
0x1C	FIFO status	R	Table 6-28
0x1D	TX length byte1	R/W	Table 6-29
0x1E	TX length byte2	R/W	Table 6-30
0x1F	FIFO I/O register	R/W	

6.4.1 Control Registers – Main Configuration Registers

Table 6-11 describes the Chip Status Control register. This register controls the power mode, RF on or off, and AM or PM. The register default is 0x01 and is reset at EN = L or POR = H.

Table 6-11. Chip Status Control Register (Address = 00h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	stby	1 = Standby mode 0 = Active mode	Standby mode keeps regulators and oscillator running when en_rec = L and en_tx = L.
B6	direct	1 = Received subcarrier signal (decoders bypassed) 0 = Received decoded signal from selected decoder	The modulation control is direct through MOD input. The receiver subcarrier signal is on I/O_6.
B5	rf_on	1 = RF output active 0 = RF output not active	When B5 = 1, the RF field is active.
B4	rf_pwr	1 = Half output power 0 = Full output power	1 = RF driver at 8 Ω 0 = RF driver at 4 Ω
B3	pm_on	1 = RX_IN2 0 = RX_IN1	1 = Selects PM signal input 0 = Selects AM signal input
B2	Reserved		
B1	rec_on	1 = Receiver enable for external field measurement	Receiver and oscillator are enabled; intended for external field measurement.
B0	vrs5_3	1 = 5-V operation (V_{IN}) 0 = 3-V operation (V_{IN})	Selects the V_{DD_RF} range: 5 V (4.3 V to 5 V) or 3 V (2.7 V to 3.4 V)

Table 6-12 describes the ISO Control register. This register controls the ISO selection. The register default is 0x02, which is ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4. The default is reset at EN = L or POR = H.

Table 6-12. ISO Control Register (Address = 01h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	rx_crc_n	Receiving without CRC	1 = No RX CRC 0 = RX CRC
B6	dir_mode	Direct mode type	0 = Output is subcarrier data. 1 = Output is bit stream (I/O_6) and bit clock (I/O_5) from decoder selected by ISO bits
B5	rfd	RFID mode	Always set to 0.
B4	iso_4	RFID mode	See Table 6-13 .
B3	iso_3		
B2	iso_2		
B1	iso_1		
B0	iso_0		

Table 6-13. RFID Mode Selections

Iso_4	Iso_3	Iso_2	Iso_1	Iso_0	PROTOCOL	REMARKS
0	0	0	0	0	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 4	Default for reader
0	0	0	1	1	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO/IEC 14443 A bit rate, 106 kbps	RX bit rate when TX bit rate is different from RX (see Table 6-15)
0	1	0	0	1	ISO/IEC 14443 A high bit rate, 212 kbps	
0	1	0	1	0	ISO/IEC 14443 A high bit rate, 424 kbps	
0	1	0	1	1	ISO/IEC 14443 A high bit rate, 848 kbps	
0	1	1	0	0	ISO/IEC 14443 B bit rate, 106 kbps	RX bit rate when TX bit rate is different from RX (see Table 6-15)
0	1	1	0	1	ISO/IEC 14443 B high bit rate, 212 kbps	
0	1	1	1	0	ISO/IEC 14443 B high bit rate, 424 kbps	
0	1	1	1	1	ISO/IEC 14443 B high bit rate, 848 kbps	
1	0	0	1	1	Tag-it	

6.4.2 Control Registers – Sublevel Configuration Registers

Table 6-14 describes the ISO14443B TX Options register. This register selects the ISO subsets for ISO/IEC 14443 B transmit. The register default is 0x00 and is reset at POR = H or EN = L.

Table 6-14. ISO14443B TX Options Register (Address = 02h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	egt2	TX EGT time select MSB	This 3-bit code defines the number of etu (0 to 7) that separate two characters. ISO/IEC 14443 B TX only.
B6	egt1	TX EGT time select	
B5	egt0	TX EGT time select LSB	
B4	eof_l0	1 = EOF, 0 length 11 etu	ISO/IEC 14443 B TX only
		0 = EOF, 0 length 10 etu	
B3	sof_l1	1 = SOF, 1 length 03 etu	
		0 = SOF, 1 length 02 etu	
B2	sof_l0	1 = SOF, 0 length 11 etu	
		0 = SOF, 0 length 10 etu	
B1	l_egt	1 = EGT after each byte	
		0 = EGT after last byte is omitted	
B0	Unused		

Table 6-15 describes the ISO14443A High-Bit-Rate Options register. The register default is 0x00 and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-15. ISO14443A High-Bit-Rate Options Register (Address = 03h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	dif_tx_br	TX bit rate different from RX bit rate enable	Valid for ISO/IEC 14443 A or B high bit rate
B6	tx_br1	TX bit rate	tx_br1 = 0, tx_br = 0: 106 kbps tx_br1 = 0, tx_br = 1: 212 kbps tx_br1 = 1, tx_br = 0: 424 kbps tx_br1 = 1, tx_br = 1: 848 kbps
B5	tx_br0		
B4	parity-2tx	1 = Parity odd except last byte, which is even for TX	For ISO/IEC 14443 A high bit rate, coding and decoding
B3	parity-2rx	1 = Parity odd except last byte, which is even for RX	
B2	Unused		
B1	Unused		
B0	Unused		

Table 6-16 describes the TX Timer H-Byte register. The register default is 0xC2 and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-16. TX Timer H-Byte Register (Address = 04h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Tm_st1	Timer start condition	tm_st1 = 0, tm_st0 = 0: Beginning of TX SOF tm_st1 = 0, tm_st0 = 1: End of TX SOF tm_st1 = 1, tm_st0 = 0: Beginning of RX SOF tm_st1 = 1, tm_st0 = 1: End of RX SOF
B6	Tm_st0		
B5	Tm_lengthD	Timer length. MSB is B5.	
B4	Tm_lengthC		
B3	Tm_lengthB		
B2	Tm_lengthA		
B1	Tm_length9		
B0	Tm_length8		

Table 6-17 describes the TX Timer L-Byte register. The register default is 0x00 and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-17. TX Timer L-Byte Register (Address = 05h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Tm_length7	Timer length. MSB is B7.	Defines the time when delayed transmission is started. RX wait range is 590 ns to 9.76 ms (1 to 16383), and the step size is 590 ns. All bits low (00) = Timer is disabled (preset for all protocols)
B6	Tm_length6		
B5	Tm_length5		
B4	Tm_length4		
B3	Tm_length3		
B2	Tm_length2		
B1	Tm_length1		
B0	Tm_length0		

Table 6-18 describes the TX Pulse Length Control register. This register controls the length of TX pulse. The register default is 0x00 and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-18. TX Pulse Length Control Register (Address = 06h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Pul_p2	Pulse length. MSB is B7.	The pulse range is 73.7 ns to 18.8 μ s (1 to 255), and the step size is 73.7 ns.
B6	Pul_p1		All bits low (00) = Pulse length control is disabled
B5	Pul_p0		Presets are:
B4	Pul_c4		9.44 μ s for ISO/IEC 15693
B3	Pul_c3		11 μ s for Tag-it
B2	Pul_c2		2.36 μ s for ISO/IEC 14443 A at 106 kbps
B1	Pul_c1		1.4 μ s for ISO/IEC 14443 A at 212 kbps
B0	Pul_c0		737 ns for ISO/IEC 14443 A at 424 kbps 442 ns for ISO/IEC 14443 A at 848 kbps

Table 6-19 describes the RX No Response Wait Time register. This register defines the time when a no response interrupt is sent. The default is 0x0E and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-19. RX No Response Wait Time Register (Address = 07h)

BIT	BIT NAME	FUNCTION	COMMENTS	
B7	NoResp7	No response. MSB is B7.	Defines the time when the no response interrupt is sent. Time starts from the end of TX EOF. RX no response wait range is 37.76 μ s to 9628 μ s (1 to 255), and step size is 37.76 μ s. Presets are:	
B6	NoResp6			
B5	NoResp5			
B4	NoResp4			
B3	NoResp3			755 μ s for ISO/IEC 15693
B2	NoResp2			1812 μ s for ISO/IEC 15693 low data rate
B1	NoResp1			604 μ s for Tag-it
B0	NoResp0			529 μ s for all other protocols

Table 6-20 describes the RX Wait Time register. This register defines the time after TX EOF when the RX input is disregarded. The default is 0x1F and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-20. RX Wait Time Register (Address = 08h)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Rxw7	RX wait	Defines the time during which the RX input is ignored. Starts from the end of TX EOF. RX wait range is 9.44 μ s to 2407 μ s (1 to 255), and step size is 9.44 μ s. Presets are: 293 μ s for ISO/IEC 15693 66 μ s for ISO/IEC 14443 A and B 180 μ s for Tag-it
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		

Table 6-21 describes the Modulator and SYS_CLK Control register. This register controls the modulation depth, modulation input, and ASK/OOK pin control. The default is 0x11 and is reset at POR = H or EN = L and at each write to the ISO Control register, except for the Clo1 and Clo0 bits.

Table 6-21. Modulator and SYS_CLK Control Register (Address = 09h)

BIT	BIT NAME	FUNCTION	COMMENTS																																				
B7	Unused																																						
B6	en_ook_p	1 = Enables external selection of ASK or OOK modulation	Valid only when ISO control register (0x01) is configured to direct mode																																				
B5	Clo1	SYS_CLK output frequency. MSB is B5.	<table border="1"> <thead> <tr> <th>Clo1</th> <th>Clo0</th> <th>SYS_CLK Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>3.3 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>6.78 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>13.56 MHz</td> </tr> </tbody> </table>	Clo1	Clo0	SYS_CLK Output	0	0	Disabled	0	1	3.3 MHz	1	0	6.78 MHz	1	1	13.56 MHz																					
			Clo1	Clo0	SYS_CLK Output																																		
0	0	Disabled																																					
0	1	3.3 MHz																																					
1	0	6.78 MHz																																					
1	1	13.56 MHz																																					
B4	Clo0																																						
B3	en_ana	1 = Enables analog output on the ASK/OOK pin (pin 12)	For test and measurement																																				
B2	Pm2	Modulation depth. MSB is B2.	<table border="1"> <thead> <tr> <th>Pm2</th> <th>Pm1</th> <th>Pm0</th> <th>Modulation Type and Percentage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>ASK 10%</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>OOK (100%)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ASK 7%</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ASK 8.5%</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>ASK 13%</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>ASK 16%</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>ASK 22%</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>ASK 30%</td> </tr> </tbody> </table>	Pm2	Pm1	Pm0	Modulation Type and Percentage	0	0	0	ASK 10%	0	0	1	OOK (100%)	0	1	0	ASK 7%	0	1	1	ASK 8.5%	1	0	0	ASK 13%	1	0	1	ASK 16%	1	1	0	ASK 22%	1	1	1	ASK 30%
			Pm2	Pm1	Pm0	Modulation Type and Percentage																																	
0	0	0	ASK 10%																																				
0	0	1	OOK (100%)																																				
0	1	0	ASK 7%																																				
0	1	1	ASK 8.5%																																				
1	0	0	ASK 13%																																				
1	0	1	ASK 16%																																				
1	1	0	ASK 22%																																				
1	1	1	ASK 30%																																				
B1	Pm1																																						
B0	Pm0																																						

Table 6-22 describes the RX Special Setting register. This register sets the gains and filters directly. The default is 0x40 and is reset at POR = H or EN = L and at each write to the ISO Control register.

Table 6-22. RX Special Setting Register (Address = 0Ah)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	C212	Band-pass filter of 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system
B6	C424	Band-pass filter of 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO/IEC 15693 and Tag-it
B5	M848	Band-pass filter of 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO/IEC 14443 A
B4	hbt	Band-pass filter of 100 kHz to 1.5 MHz Gain reduced for 7 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO/IEC 14443
B3	gd1	01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction
B2	gd2		
B1	Reserved		
B0	Reserved		

Table 6-23 describes the Regulator and I/O Control register. This register controls the three voltage regulators. The default is 0x87 and is reset at POR = H or EN = L.

Table 6-23. Regulator and I/O Control Register (Address = 0Bh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	auto_reg	0 = Setting regulator by option bits (vrs3_5 and vrs2, vrs1, and vrs0) 1 = Automatic setting	Automatic system sets VDD_RF = (V _{IN} – 250 mV) and sets VDD_A = VDD_X = (V _{IN} – 250 mV) but not higher than 3.4 V.
B6	en_ext_pa	Support for external power amplifier	Receiver inputs accept externally demodulated subcarrier, OOK pin becomes modulation output for external amplifier.
B5	io_low	1 = Enable low peripheral communication voltage	When high, the output resistance of logic outputs is decreased. Should be set high when VDD_I/O voltage is below 2.7 V.
B4	Unused		Default is low.
B3	Unused		Default is low.
B2	vrs2	Voltage set. MSB is B2.	vrs3_5 = L: VDD_RF, VDD_A, VDD_X range 2.7 V to 3.4 V
B1	vrs1		
B0	vrs0		

6.4.3 Status Registers

Table 6-24 describes the IRQ Status register. This register displays the cause of IRQ and TX and RX status. The default is 0x00 and is reset at POR = H or EN = L and at each write to the ISO Control register. The register is also automatically set to default at the end of a read phase. This reset also removes the IRQ flag.

Table 6-24. IRQ Status Register (Address = 0Ch)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request is sent when TX is finished.
B6	Irq_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low (less than 4 or more than 8)
B4	Irq_err1	CRC error	Indicates receive CRC error
B3	Irq_err2	Parity error	Indicates parity error
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	For ISO/IEC 14443 A and ISO/IEC 15693 single subcarrier
B0	Irq_noresp	No response interrupt	Signal to MCU that next slot command can be sent

Table 6-25 describes the Collision Position and Interrupt Mask register. The default is 0x3E and is reset at POR = H and EN = L. Collision bits are reset automatically after a read operation.

Table 6-25. Collision Position and Interrupt Mask Register (Address = 0Dh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Col9	Bit position of collision MSB	Supported: ISO/IEC 15693, single subcarrier, and ISO/IEC 14443 A
B6	Col8	Bit position of collision	
B5	En_irq_fifo	Interrupt enable for FIFO	
B4	En_irq_err1	Interrupt enable for CRC	
B3	En_irq_err2	Interrupt enable for Parity	
B2	En_irq_err3	Interrupt enable for Framing error or EOF	
B1	En_irq_col	Interrupt enable for collision error	
B0	En_irq_noresp	Enables no-response interrupt	

Table 6-26 describes the Collision Position register. This register displays the bit position of collision or error. The default is 0x00 and is reset at POR = H and EN = L. Collision bits are reset automatically after a read operation.

Table 6-26. Collision Position Register (Address = 0Eh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Col7	Bit position of collision. MSB is B7.	Supports ISO/IEC 15693 single subcarrier and ISO/IEC 14443 A. In other protocols, it shows the bit position of error, either frame, SOF-EOF, parity, or CRC error.
B6	Col6		
B5	Col5		
B4	Col4		
B3	Col3		
B2	Col2		
B1	Col1		
B0	Col0		

Table 6-27 describes the RSSI Levels and Oscillator Status register. This register reports the signal strength on both reception channels and RF amplitude during RF-off state. The RSSI values are valid from reception start until the start of the next transmission.

Table 6-27. RSSI Levels and Oscillator Status Register (Address = 0Fh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Unused		
B6	Oscok	Crystal oscillator stable indicator	
B5	rss_i_x2	RSSI value of auxiliary channel (4 dB per step). MSB is B5.	Auxiliary channel is PM by default. It can be set to AM with option bit B3 of the Chip State Control register (00h).
B4	rss_i_x1		
B3	rss_i_x0		
B2	rss_i_2	RSSI value of active channel (4 dB per step). MSB is B2.	Active channel is AM by default. It can be set to PM with option bit B3 of the Chip State Control register (00h).
B1	rss_i_1		
B0	rss_i_0		

6.4.4 FIFO Control Registers

Table 6-28 describes the FIFO Status register. This register reports the low nibbles of complete bytes to be transferred through FIFO, information about a broken byte, and the number of bits to be transferred from it.

Table 6-28. FIFO Status Register (Address = 1Ch)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	RFU	Set to low	Reserved for future use
B6	Fhil	FIFO level high	Indicates that 9 bytes are in the FIFO (for RX)
B5	FloI	FIFO level low	Indicates that 3 bytes are in the FIFO (for TX)
B4	Fove	FIFO overflow error	Too much data was written to the FIFO
B3	Fb3	FIFO bytes fb[3]	Bits B0:B3 indicate how many bytes that are loaded in FIFO were not read out yet. Reports (N – 1) number of bytes; for example, if 8 bytes are in the FIFO, this number is 7.
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

Table 6-29 describes the TX Length Byte1 register. This register reports the high 2 nibbles of complete bytes to be transferred through the FIFO. The default is 0x00 and is reset at POR and EN = 0. It is also automatically reset at TX EOF.

Table 6-29. TX Length Byte1 Register (Address = 1Dh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Txl11	Number of complete byte bn[11]	High nibble of complete bytes to be transmitted
B6	Txl10	Number of complete byte bn[10]	
B5	Txl9	Number of complete byte bn[9]	
B4	Txl8	Number of complete byte bn[8]	
B3	Txl7	Number of complete byte bn[7]	Middle nibble of complete bytes to be transmitted
B2	Txl6	Number of complete byte bn[6]	
B1	Txl5	Number of complete byte bn[5]	
B0	Txl4	Number of complete byte bn[4]	

Table 6-30 describes the TX Length Byte2 register. This register reports the low nibble of complete bytes to be transferred through the FIFO, information about a broken byte, and the number of bits to be transferred from it. The default is 0x00 and is reset at POR and EN = 0. It is also automatically reset at TX EOF.

Table 6-30. TX Length Byte2 Register (Address = 1Eh)

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Txl3	Number of complete byte bn[3]	Low nibble of complete bytes to be transmitted
B6	Txl2	Number of complete byte bn[2]	
B5	Txl1	Number of complete byte bn[1]	
B4	Txl0	Number of complete byte bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last broken byte to be transmitted. This bit is taken into account only when the broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	If 1, the last byte is not complete and is less than 8 bits wide.

6.5 Direct Commands From MCU to Reader

6.5.1 Command Codes

Table 6-31 describes the command codes.

Table 6-31. Command Codes

COMMAND CODE	COMMAND	COMMENTS
0x00	Idle	
0x03	Software Initialization	Software initialization, same as power-on reset
0x0F	Reset FIFO	
0x10	Transmission Without CRC	
0x11	Transmission With CRC	
0x12	Delayed Transmission Without CRC	
0x13	Delayed Transmission With CRC	
0x14	Transmit Next Time Slot	Used for ISO/IEC 15693 only
0x16	Block Receiver	
0x17	Enable Receiver	
0x18	Test Internal RF	RSSI at RX input with TX on
0x19	Test External RF	RSSI at RX input with TX off
0x1A	Receiver Gain Adjust	

NOTE

The command code values in Table 6-31 are substituted in Table 6-33, bit 0 to bit 4. The MSB in Table 6-33 must be set to 1.

6.5.2 Reset FIFO

The Reset FIFO command clears the FIFO contents and FIFO Status register (1Ch) and the Collision Position register (0Eh).

6.5.3 Transmission With CRC

The transmission command must be sent first, followed by transmission length bytes, and then the FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

6.5.4 Transmission Without CRC

Same as [Section 6.5.3](#) with CRC excluded.

6.5.5 Delayed Transmission With CRC

The transmission command must be sent first, followed by the transmission length bytes, and then the FIFO data. The reader transmission is triggered by the TX timer.

6.5.6 Delayed Transmission Without CRC

Same as [Section 6.5.5](#) with CRC excluded.

6.5.7 Transmit Next Time Slot

When this command is received, the reader transmits the next slot command. The next slot sign is defined by the protocol selection. This command is used for ISO/IEC 15693 only.

6.5.8 Receiver Gain Adjust

This command should be executed when the MCU determines that no tag response is coming and when the RF and receivers are on. When this command is received, the reader reads the digitized receiver output. If more than two edges are observed in 100 μ s, the window comparator voltage is increased. The procedure is repeated until the number of edges (changes of logical state) of the digitized reception signal is less than 2 (in 100 μ s). The command can reduce the input sensitivity in 5-dB increments up to 15 dB. This command ensures better operation in a noisy environment.

The gain setting is reset to maximum gain at EN = 0, POR = 1.

6.5.9 Test External RF (RSSI at RX Input With TX Off)

This command can be used in active mode when the RF receiver is on, and the RF output is off (rec-on, bit B1 = 1 in the Chip Status Control register [see [Table 6-11](#)]). The level of the RF signal received on the antenna is measured and reported in the RSSI Levels register. The relation between the 3-bit code and the external RF field strength (in A/m) must be determined by calculation or by experiments for each antenna design. The antenna Q and connection to the RF input influence the result. The nominal relationship between the RF peak-to-peak voltage at the receiver inputs and the corresponding RSSI level is as follows.

Receiver Input (mV _{PP}):	40	60	80	100	140	180	300
RSSI Level:	1	2	3	4	5	6	7

If the direct command Test RF Internal or Test RF External is used immediately after activation, the command should be preceded by the Enable RX command to activate the RX section. For proper execution of the test RF commands, the RX section must be enabled. This section is enabled automatically when a data exchange between the reader and the tag is done, or by sending the Enable RX direct command.

6.5.10 Test Internal RF (RSSI at RX Input With TX On)

This command measures the level of the RF carrier at the receive inputs. Its operating range is 300 mVp to 2.1 Vp with a step size of 300 mV. The two values are displayed in the RSSI Levels register. The command is intended for diagnostic purposes to set the correct RX_IN levels. The optimum RX_IN input level is approximately 1.6 Vp, or an RSSI level of 5 or 6. The nominal relationship between the input RF peak level and the corresponding RSSI code is as follows.

Receiver Input (mV _{PP}):	300	600	900	1200	1500	1800	2100
RSSI Level:	1	2	3	4	5	6	7

6.5.11 Block Receiver

The Block Receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch an SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of an RX operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode. The reset mode can be terminated in two ways. The external system can send the Enable Receiver command. The reset mode is also automatically terminated at the end of a TX operation. The receiver can stay in reset after end of TX if the RX Wait Time register (address 0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

6.5.12 Enable Receiver

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the Block Receiver command.

6.6 Reader Communication Interface

6.6.1 Introduction

The communication interface to the reader can be configured as a parallel 8-pin interface with a data clock or as a serial peripheral interface (SPI). These modes are mutually exclusive; only one mode can be used at a time in the application.

When the SPI is selected, the unused I/O_2, I/O_1, and I/O_0 pins must be hardwired according to [Table 6-32](#). At power up, the TRF7960 IC samples the status of these three pins and then enters one of the possible SPI modes (see [Table 6-32](#)).

The reader always acts as the slave while the microcontroller (MCU) acts as the master device. The MCU initiates all communications with the reader and is also used to communicate with the higher levels (application layer). The reader has an IRQ pin to prompt the MCU for attention if the reader detects a response from a proximity integrated circuit card (PICC) or a vicinity integrated circuit card (VICC).

Communication is initialized by a start condition, which is expected to be followed by an Address/Command (Adr/Cmd) word. The Adr/Cmd word is 8 bits long (see [Table 6-33](#)).

Table 6-32. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode

PIN	PARALLEL	PARALLEL DIRECT	SPI WITH SS	SPI WITHOUT SS
DATA_CLK	DATA_CLK	DATA_CLK	DATA_CLK from master	DATA_CLK from master
I/O_7	A/D[7]		MOSI ⁽¹⁾ = data in (reader in)	MOSI ⁽¹⁾ = data in (reader in)
I/O_6	A/D[6]	Direct mode, data out (subcarrier or bit stream)	MISO ⁽²⁾ = data out (MCU out)	MISO ⁽²⁾ = data out (MCU out)
I/O_5	A/D[5]	Direct mode, strobe – bit clock out	See ⁽³⁾	See ⁽³⁾
I/O_4	A/D[4]		SS – slave select ⁽⁴⁾	–
I/O_3	A/D[3]	–	–	–
I/O_2	A/D[2]	–	At V _{DD}	At V _{DD}
I/O_1	A/D[1]	–	At V _{DD}	At V _{SS}
I/O_0	A/D[0]	–	At V _{SS}	At V _{SS}
IRQ	IRQ interrupt	IRQ interrupt	IRQ interrupt	IRQ interrupt

(1) MOSI = master out, slave in

(2) MISO = master in, slave out

(3) IO_5 pin is used only when data is output from the chip (for example, reading 1 byte from the chip). The master must first write the address of the register (8 clocks) and then generate another 8 clocks to read the data. The IO_5 pin goes high during this second 8 clocks. For normal SPI operation, this pin is not used.

(4) The slave-select pin is active low.

Table 6-33. Address/Command Word Bit Distribution

BIT	DESCRIPTION	BIT FUNCTION	ADDRESS	COMMAND
Bit 7	Command control bit	1 = Command, 0 = Address	0	1
Bit 6	Read/write	1 = Read, 0 = Write	R/W	0
Bit 5	Continuous address mode	1 = Continuous mode	R/W	0
Bit 4	Address/command bit 4		Adr 4	Cmd 4
Bit 3	Address/command bit 3		Adr 3	Cmd 3
Bit 2	Address/command bit 2		Adr 2	Cmd 2
Bit 1	Address/command bit 1		Adr 1	Cmd 1
Bit 0	Address/command bit 0		Adr 0	Cmd 0

The MSB (bit 7) determines if the word is to be used as a command or as an address. The ADDRESS and COMMAND columns of Table 6-33 list the function of the separate bits if either address or command is written. Data is expected when the address word is sent. In continuous-address mode (B5 = 1), the first data that follows the address is written to or read from the given address. For each additional data, the address is incremented by 1. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the nonvolatile memory of the MCU to the reader. In noncontinuous address mode (simple addressed mode), only one data word is expected after the address.

Address mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the continuous address mode should be set to 1.

The command mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, or turn reader on or off).

The following examples show the expected communication between the MCU and reader.

Continuous address mode

Start	Adr x	Data(x)	Data(x+1)	Data(x+2)	Data(x+3)	Data(x+4)	...	Data(x+n)	StopCont
-------	-------	---------	-----------	-----------	-----------	-----------	-----	-----------	----------

Noncontinuous address mode (single address mode)

Start	Adr x	Data(x)	Adr y	Data(y)	...	Adr z	Data(z)	StopSgl
-------	-------	---------	-------	---------	-----	-------	---------	---------

Command mode

Start	Cmd x	(Optional data or command)	Stop
-------	-------	----------------------------	------

6.7 Parallel Interface Communication

In parallel mode, the start condition is generated on the rising edge of the I/O_7 pin while the CLK is high. This condition resets the interface logic. Figure 6-6 shows the sequence of the data, with an 8-bit address word followed by data and ending with the StopSmpl condition. Figure 6-7 shows a similar sequence, except that it ends with the StopCont condition.

Communication is ended by:

- The StopSmpl condition, which is indicated when the falling edge on the I/O_7 pin is detected while CLK is high
- The StopCont condition, which is indicated when the I/O_7 pin has successive rising and falling edges while CLK is low. This condition resets the parallel interface, and the device is ready for a new communication sequence.

The StopSmpl condition also terminates the direct mode.

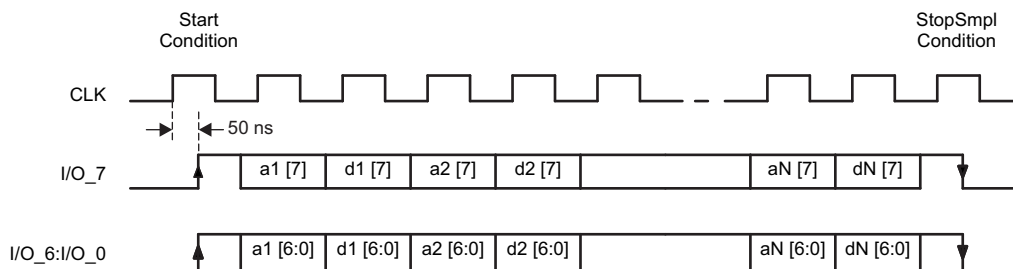


Figure 6-6. Parallel Interface Communication With Simple Stop Condition StopSmpl

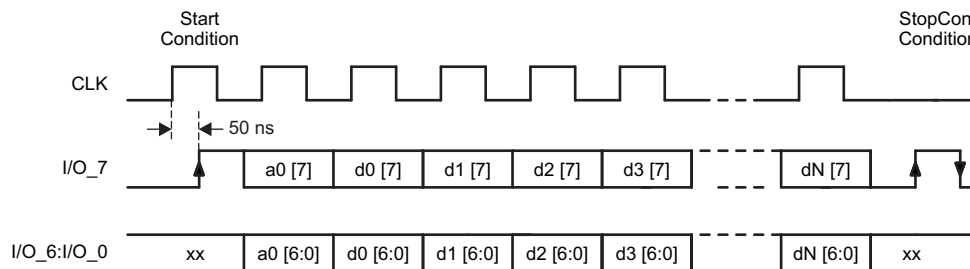


Figure 6-7. Parallel Interface Communication With Continuous Stop Condition StopCont

6.7.1 Receive

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An interrupt request is sent to the MCU at the end of the receive operation if the receive data string was shorter than or equal to 8 bytes. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (address 0Ch), after which the MCU reads the data from the FIFO.

If the received packet is longer than 8 bytes, the interrupt is sent before the end of the receive operation when the ninth byte is loaded into the FIFO (75% full). The MCU should again read the content of the IRQ Status register to determine the cause of the interrupt request. If the FIFO is 75% full (as marked with flag B5 in the IRQ Status register and by reading the FIFO Status register), the MCU should respond by reading the data from the FIFO to make room for new incoming receive data. When the receive operation is finished, the interrupt is sent and the MCU must check how many words are still present in the FIFO before it finishes reading.

If the reader detects a receive error, the corresponding error flag is set (for example, framing error or CRC error) in the IRQ Status register, which indicates that the MCU reception was completed incorrectly.

6.7.2 Transmit

Before beginning data transmission (see Figure 6-8), the FIFO should be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see Table 6-31). The MCU then commands the reader to do a continuous write command (3Dh, see Table 6-33) starting from register 1Dh. Data written into register 1Dh is the TX Length Byte1 (upper and middle nibbles), while the next byte in register 1Eh is the TX Length Byte2 (lower nibble and broken byte length). The TX byte length determines when the reader sends the EOF byte. After the TX Length Bytes are written, FIFO data is loaded in register 1Fh with byte storage locations 0 to 11. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX Length Bytes and the FIFO can be done with a continuous-write command, because the addresses are sequential.

At the start of transmission, the Irq_tx flag (B7) is set in the IRQ Status register. If the transmit data is shorter than or equal to 4 bytes, the interrupt is sent only at the end of the transmit operation. If the number of bytes to be transmitted is greater than or equal to 5, the interrupt is generated. The interrupt is also generated when the number of bytes in the FIFO reaches 3. The MCU should check the IRQ Status register and the FIFO Status register and then load additional data to the FIFO, if needed. At the end of the transmit operation, an interrupt is sent to notify the MCU that the task is complete.

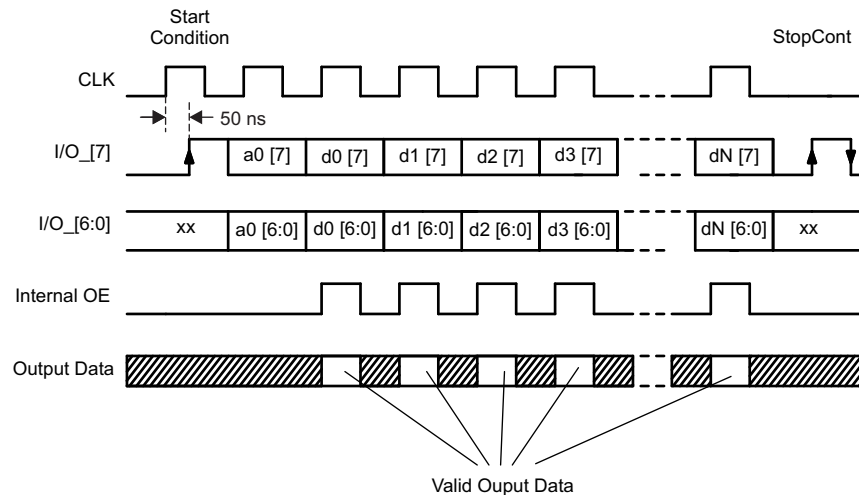


Figure 6-8. Data Output Only When CLK Is High

6.8 Serial Interface Communication

When a SPI is required, parallel I/O pins I/O_2, I/O_1, and I/O_0, must be hardwired according to [Table 6-32](#). On power up, the reader detects the status of these pins; if they are not the same (not all high, or not all low), the reader enters into one of two possible SPI modes.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the IRQ Status register of the reader to determine how to service the reader. After this, the MCU must do a dummy read to clear the IRQ Status register of the reader. The dummy read is required in SPI mode, because the IRQ Status register of the reader needs an additional clock cycle to clear the register. This is not required in parallel mode, because the additional clock cycle is included in the stop condition. The recommended clock frequency on the DATA_CLK line is 2 MHz.

A procedure for a dummy read follows:

1. Start the dummy read:
 - (a) When using slave select (SS), set the SS bit low.
 - (b) When not using SS, the start condition occurs when SCLK is high (see [Figure 6-9](#)).
2. Send the address word to the IRQ Status register (0Ch) with read and continuous address mode bits set to 1 (see [Table 6-33](#)).
3. Read 1 byte (8 bits) from the IRQ Status register (0Ch).
4. Dummy read 1 byte from register 0Dh (collision position and interrupt mask).
5. Stop the dummy read:
 - (a) When using slave select (SS), set the SS bit high.
 - (b) When not using SS, the stop condition occurs when SCLK is high (see [Figure 6-9](#)).

6.8.1 SPI Without SS* (Slave Select) Pin

The serial interface without the slave select pin must use delimiters for the start and stop conditions. Between these delimiters, the address, data, and command words can be transferred. All words must be 8 bits long with MSB transmitted first.

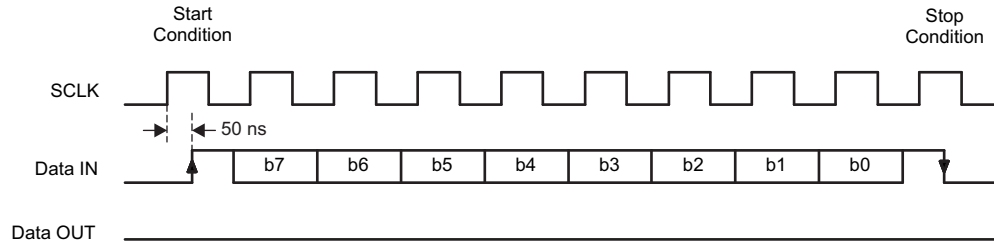


Figure 6-9. Serial – SPI Communication (No SS* Pin)

In this mode, a rising edge on Data IN (I/O_7, pin 24) while SCLK is high resets the serial interface and prepares it to receive data. Data IN can change only when SCLK is low and is taken by the reader on the rising edge of SCLK. Communication is terminated by the stop condition when the falling edge of Data IN occurs during a high SCLK period.

6.8.2 SPI With SS* (Slave Select) Pin

The serial interface is in reset while the SS* signal is high. Serial data-in (MOSI) changes on the falling edge, and is validated in the reader on the rising edge, as shown in Figure 6-10. Communication is terminated when the SS* signal goes high.

All words must be 8 bits long with the MSB transmitted first.

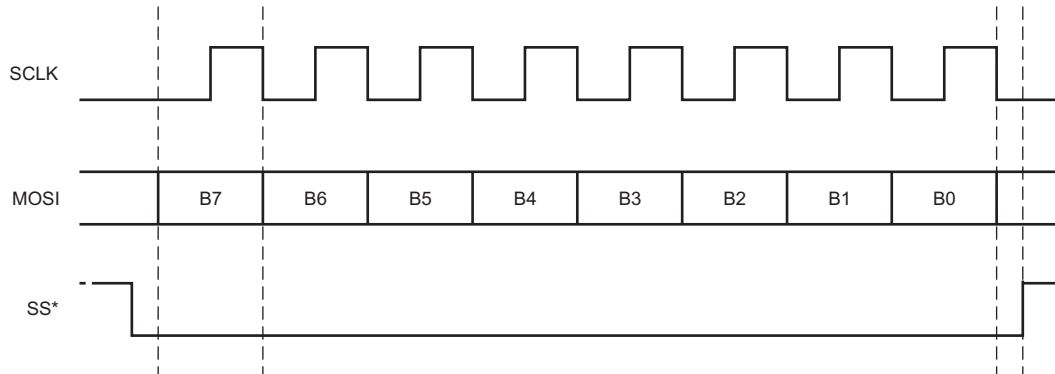


Figure 6-10. Serial – SPI Communication (Write Mode)

Figure 6-11 shows the SPI read operation.

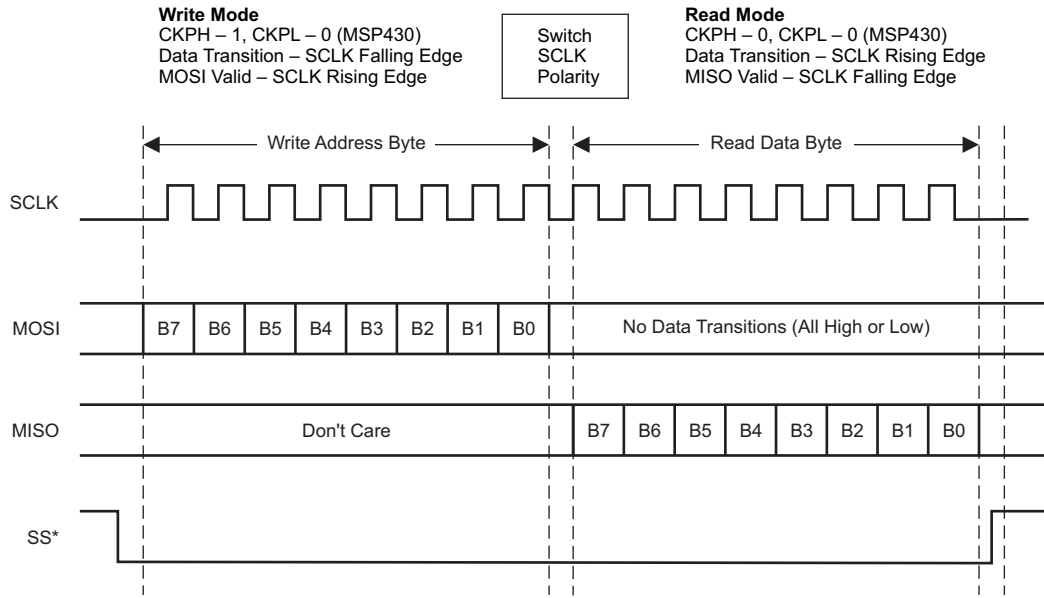


Figure 6-11. Serial – SPI Communication (Read Mode)

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the falling edge, and is validated in the reader on the rising edge (see [Figure 6-11](#)). During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth rising edge of SCLK, after half a clock cycle, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first).

NOTE

When using the hardware SPI (for example, an MSP430 hardware SPI) to implement this feature, take care to switch the SCLK polarity after the write phase for proper read operation. [Figure 6-11](#) shows the example clock polarity for the MSP430-specific environment in the Write Mode and Read Mode sections. See the SPI chapter of the family user's guide for any specific microcontroller family for further information on the setting the appropriate clock polarity.

This clock polarity switch must be done for all read operations (single or continuous).

The MOSI (serial data out) should not have any transitions (all high or all low) during the read cycle. Also, the SS* signal should be low during the whole write and read operation.

[Figure 6-12](#) shows the continuous read operation.

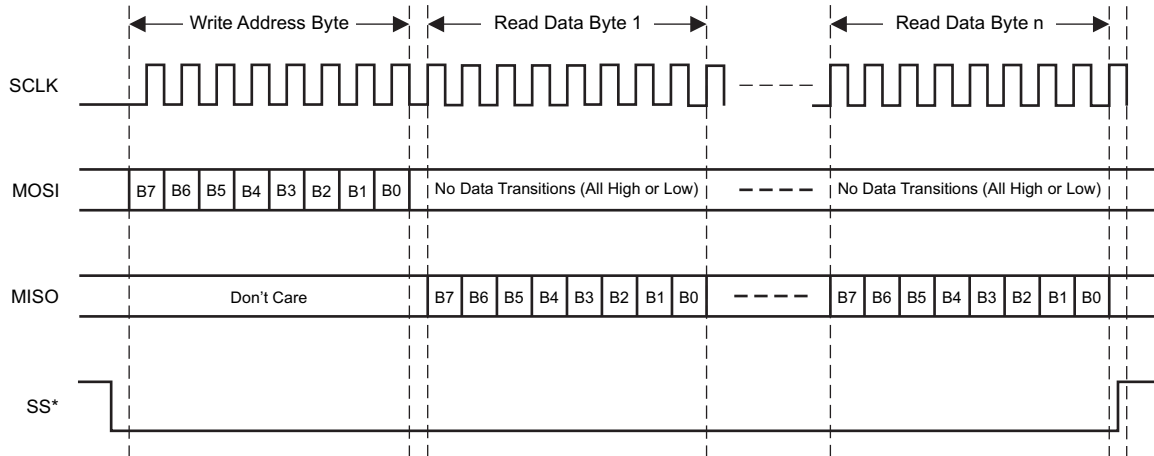


Figure 6-12. SPI Communication (Continuous Read Mode)

NOTE

Special steps are needed to read the TRF796x IRQ Status register (register address 0x0C) in SPI mode. The status of the bits in this register are cleared after a dummy read. The following steps must be followed when reading the IRQ Status register.

1. Write command 0x6C: read the IRQ Status register in continuous mode (eight clocks).
2. Read the data in register 0x0C (eight clocks).
3. Generate another eight clocks (as if reading the data in register 0x0D) but ignore the MISO data line.

See [Figure 6-13](#) for an example of this process.

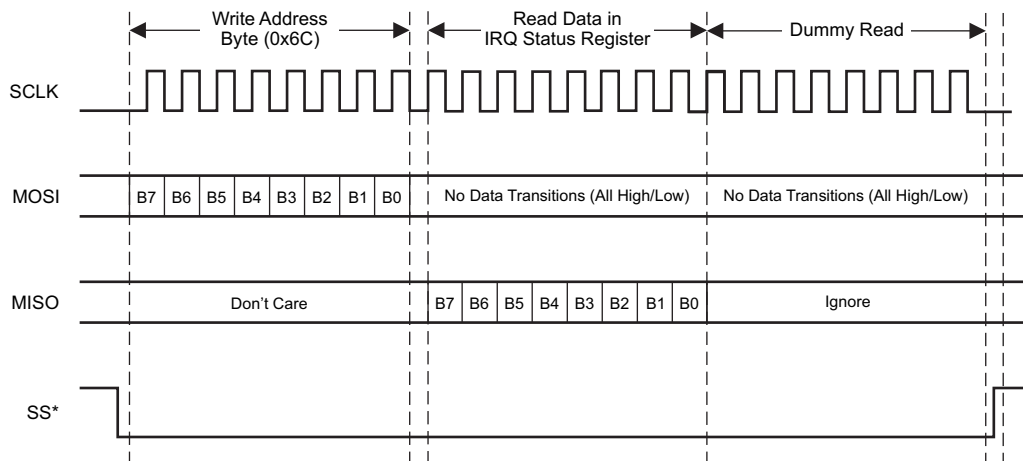


Figure 6-13. SPI Communication (IRQ Status Register Read)

6.8.2.1 FIFO Operation

The FIFO is a 12-byte register at address 0x1F with byte storage locations 0 to 11. FIFO data is loaded in a cyclical manner and can be cleared by a Reset command (0x0F).

Two counters and three FIFO status flags are associated with the FIFO. The first counter is a 4-bit FIFO byte counter (bits B0 to B3 in register 0x1C) that keeps track of the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is n , the register value is $(n - 1)$ number of bytes in FIFO register. For example, if 8 bytes are in the FIFO, the FIFO counter (bits B0 to B3 in register 0x1C) has the value 7.

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 1Dh and 1Eh) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 1Eh (bits B0:B3). Together, these counters make up the TX length value that determines when the reader generates the EOF byte.

FIFO status flags are as follows:

1. **FIFO overflow** (bit B4 of register 0x1C) – indicates that the FIFO was loaded too soon
2. **FIFO level too low** (bit B5 of register 0x1C) – indicates that only 3 bytes are left to be transmitted (Can be used during transmission.)
3. **FIFO level high** (bit B6 of register 0x1C) – indicates that 9 bytes are already loaded into the FIFO (Can be used during reception to generate a FIFO reception IRQ. This is to notify the MCU to service the reader in time to ensure a continuous data stream.)

During transmission, the FIFO is checked for an almost-empty condition, and during reception, the FIFO is checked for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in one sequence is 12 bytes. The number of bytes in a frame, transmitted or received, can be greater than 12 bytes.

During transmission, the MCU loads the reader FIFO (or during reception, the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO is less than 3 or greater than 9, so that the MCU can send new data or remove the data as necessary. The MCU also checks the number of data bytes to be sent, so as to not surpass the value defined in TX Length Bytes. The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception. Transmission starts automatically after the first byte is written into the FIFO.

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Schematics

Figure 7-1 shows a schematic for parallel communication.

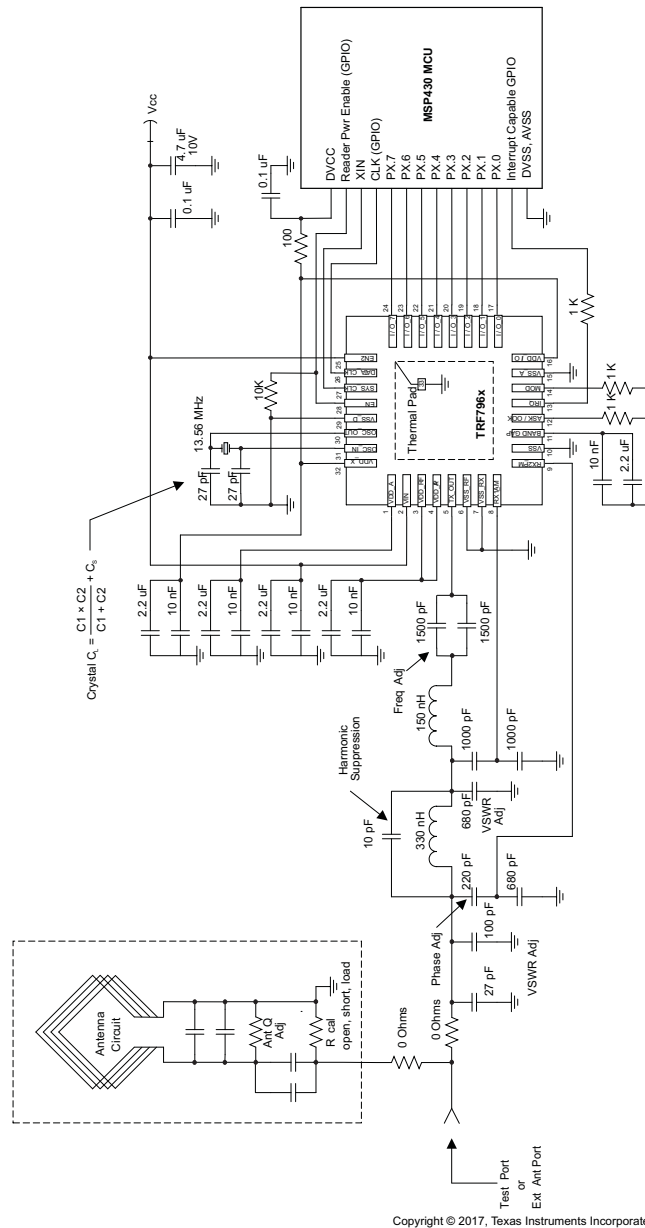


Figure 7-1. Application Schematic for the TRF796x EVM (Parallel Mode)

Figure 7-2 shows a schematic for SPI communication.

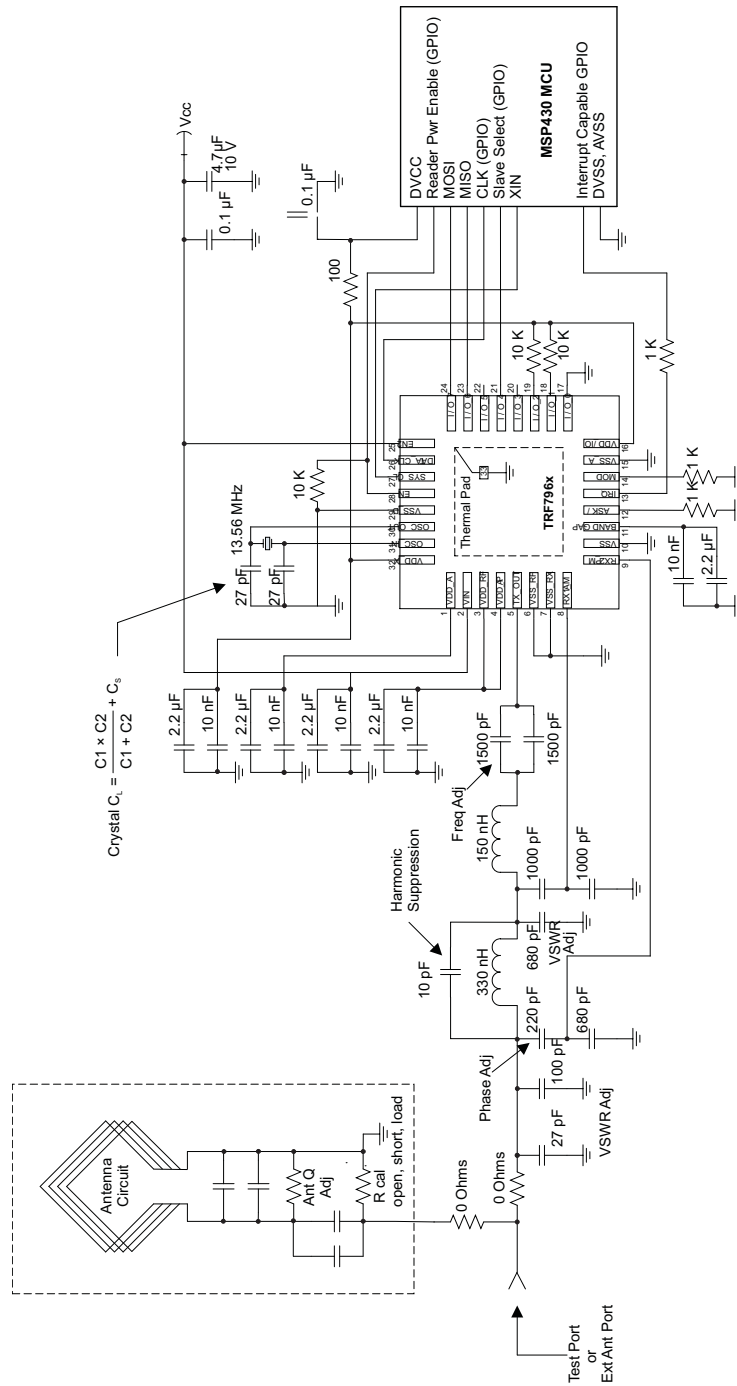


Figure 7-2. Application Schematic for the TRF796x EVM (SPI Mode)

8 Device and Documentation Support

8.1 Getting Started and Next Steps

For more information on the TI NFC/RFID devices and the tools and software that are available to help with your development, visit [Overview for NFC / RFID](#).

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of devices. Each commercial family member has one of three prefixes: x, p, or no prefix. These prefixes represent evolutionary stages of product development from engineering prototypes (with prefix x) through fully qualified production devices (with no prefix).

Device development evolutionary flow:

xTRF... – Experimental device that is not necessarily representative of the electrical specifications of the final device

pTRF... – Final device that conforms to the electrical specifications of the final product but has not completed quality and reliability verification

TRF... – Fully qualified production device

Devices with a prefix of **x** or **p** are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type and, optionally, the temperature range. [Figure 8-1](#) provides a legend for reading the complete device name.

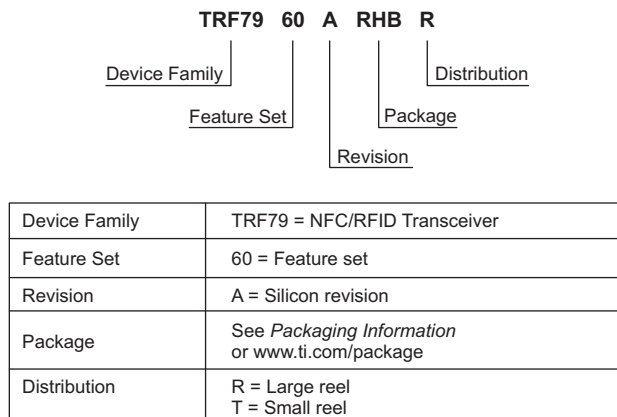


Figure 8-1. Device Nomenclature

8.3 Tools and Software

Design Kits and Evaluation Modules

TRF7960A Evaluation Module The TRF7960EVM let the software application developer experiment with the functions of the TRF796x multiple-standard fully integrated 13.56-MHz RFID analog front end and data framing reader system.

TRF7960A Target Board The TRF7960ATB EVM lets the software application developer experiment with the functions of the TRF796x multiple-standard fully integrated 13.56-MHz RFID writer/reader IC on the Texas Instruments embedded microcontroller platform of choice without having to worry about the RF section.

Software

TRF7960 Firmware Source Code for CCS Sample source code for direct register control of the device functions.

TRF7960EVM GUI Source Code Source code for the GUI that is included in the [TRF7960A evaluation module](#).

TRF7960EVM GUI Software The GUI that runs on the host PC for use with the TRF7960A evaluation module.

8.4 Documentation Support

The following documents describe the TRF7960 and TRF7961 devices. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folders, see [Section 8.5](#)). In the upper-right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Application Notes

TRF79xxA HF-RFID Reader Layout Design Guide Describes suggested guidelines for laying out the TRF79xxA family of HF RFID readers.

Antenna Matching for the TRF7960 RFID Reader Describes the design method for determining an antenna matching circuit.

TRF796x Software Design Hints This application report provides guidance on designing software that works around certain device and protocol limitations.

Management of the TRF7960 and TRF7960A Start-up Sequence System developers concerned about minimizing the current draw of TRF7960, TRF7960A, and their variants systems at start-up time need guidance about handling the Regulator Control register (0x0B) value. Valid application use case for this guidance is battery-powered RFID applications in which controlling the entire system current draw over time is of the utmost concern.

TRF7960A RFID Multiplexer Example System This application report describes the 16-channel high-frequency (HF) (13.56 MHz) RFID reader system (based on the TRF7960A IC) designed by TI for customer use. The system firmware resides on an MSP430F2370 MCU and supports the ISO/IEC 15693 protocol in addition to communication with a host.

Firmware Description of the TI TRF796x Evaluation Module (EVM) This application note discusses the firmware implemented in the MSP430F2370 (a 16-bit ultra-low power microcontroller from the TI MSP430 family) used with the TRF796x devices.

Comparison of TRF7960 and TRF7960A This application report helps current and new users of the TRF7960 high-frequency RFID/NFC reader understand the differences between the TRF7960 and the TRF7960A devices. Understanding these differences in detail and applying this knowledge to application-specific requirements helps designers make informed decisions about whether or not a bill of materials change is needed.

8.5 Related Links

[Table 8-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TRF7960	Click here	Click here	Click here	Click here	Click here
TRF7961	Click here	Click here	Click here	Click here	Click here

8.6 Community Resources

The following link connects to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

8.7 Trademarks

MSP430, Tag-it, E2E are trademarks of Texas Instruments.
FeliCa is a trademark of Sony Corporation.

8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF7960RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7960	Samples
TRF7960RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7960	Samples
TRF7961RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7961	Samples
TRF7961RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7961	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF7960RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF7960RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF7961RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF7961RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF7960RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
TRF7960RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TRF7961RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
TRF7961RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

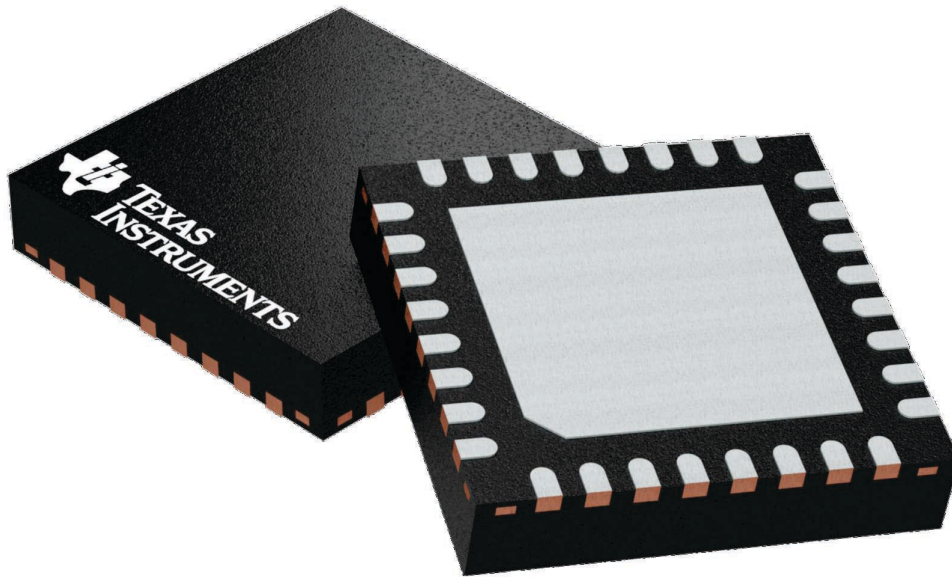
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

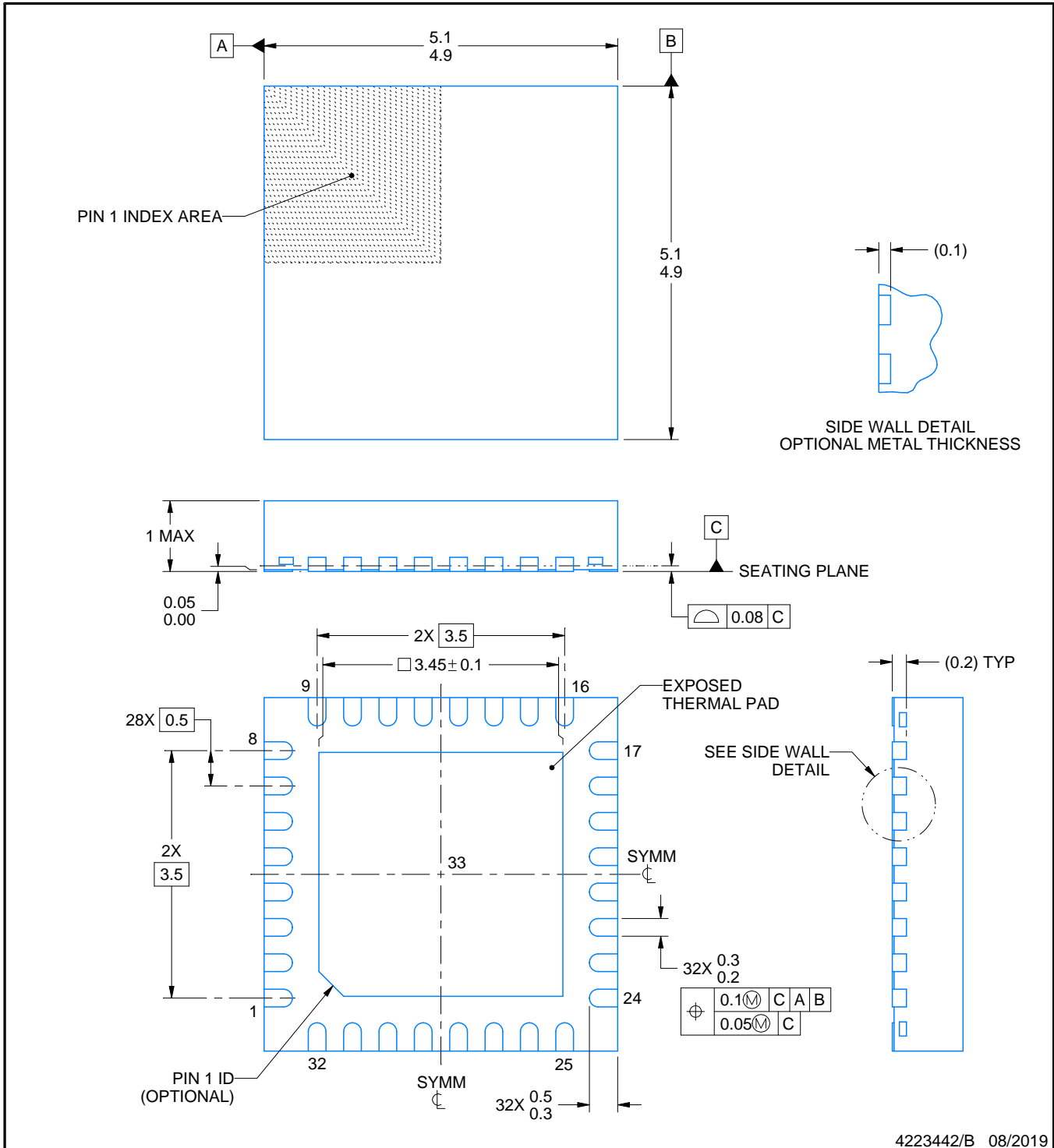
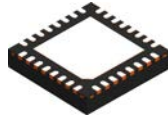
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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NOTES:

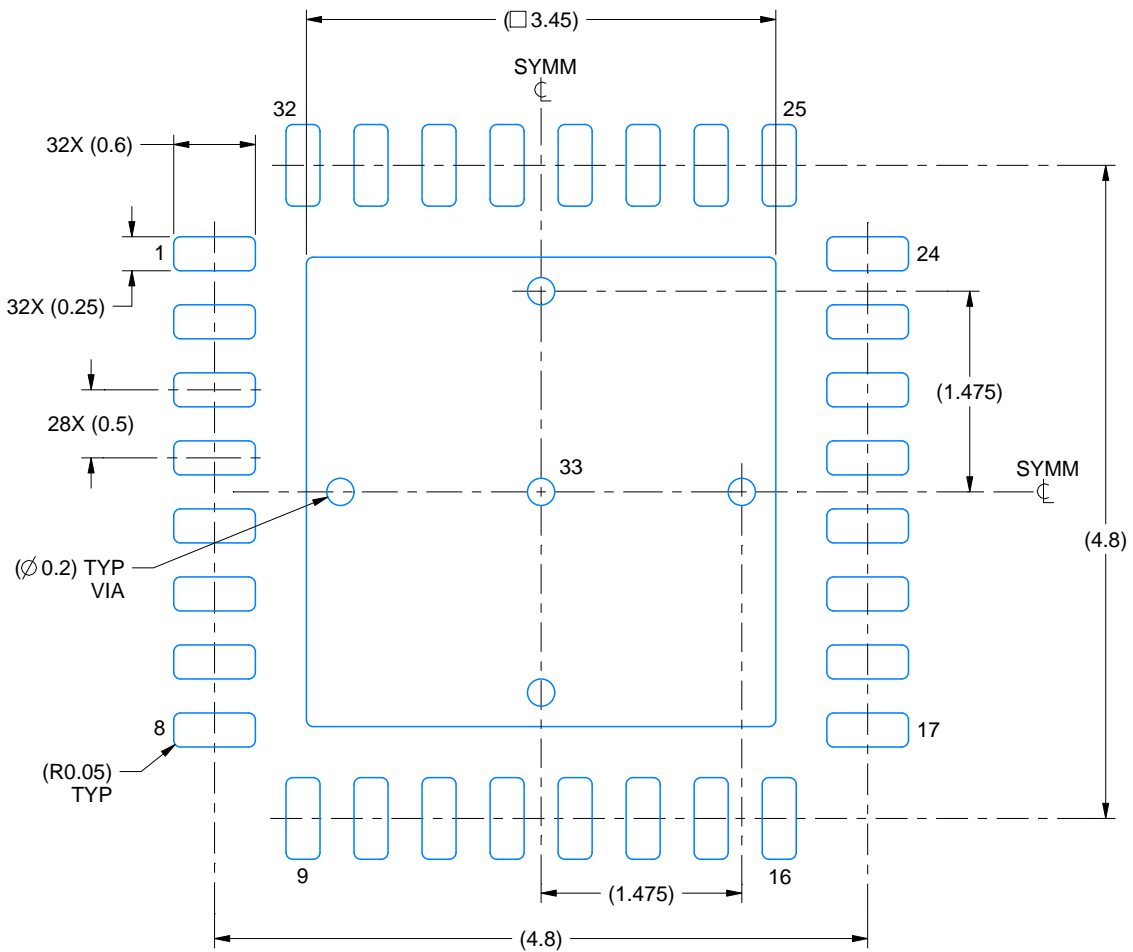
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

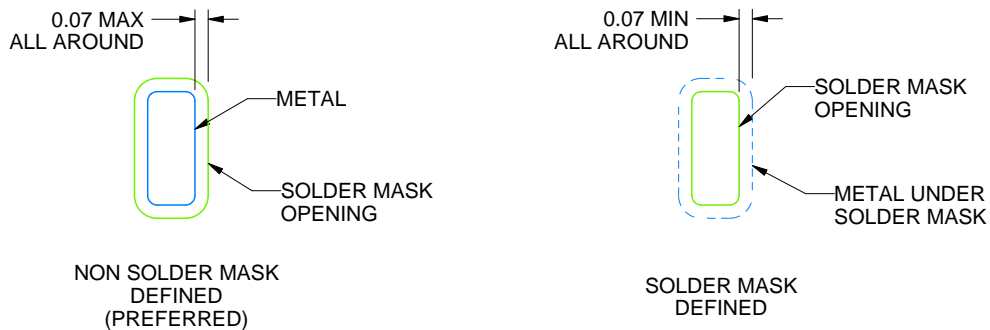
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

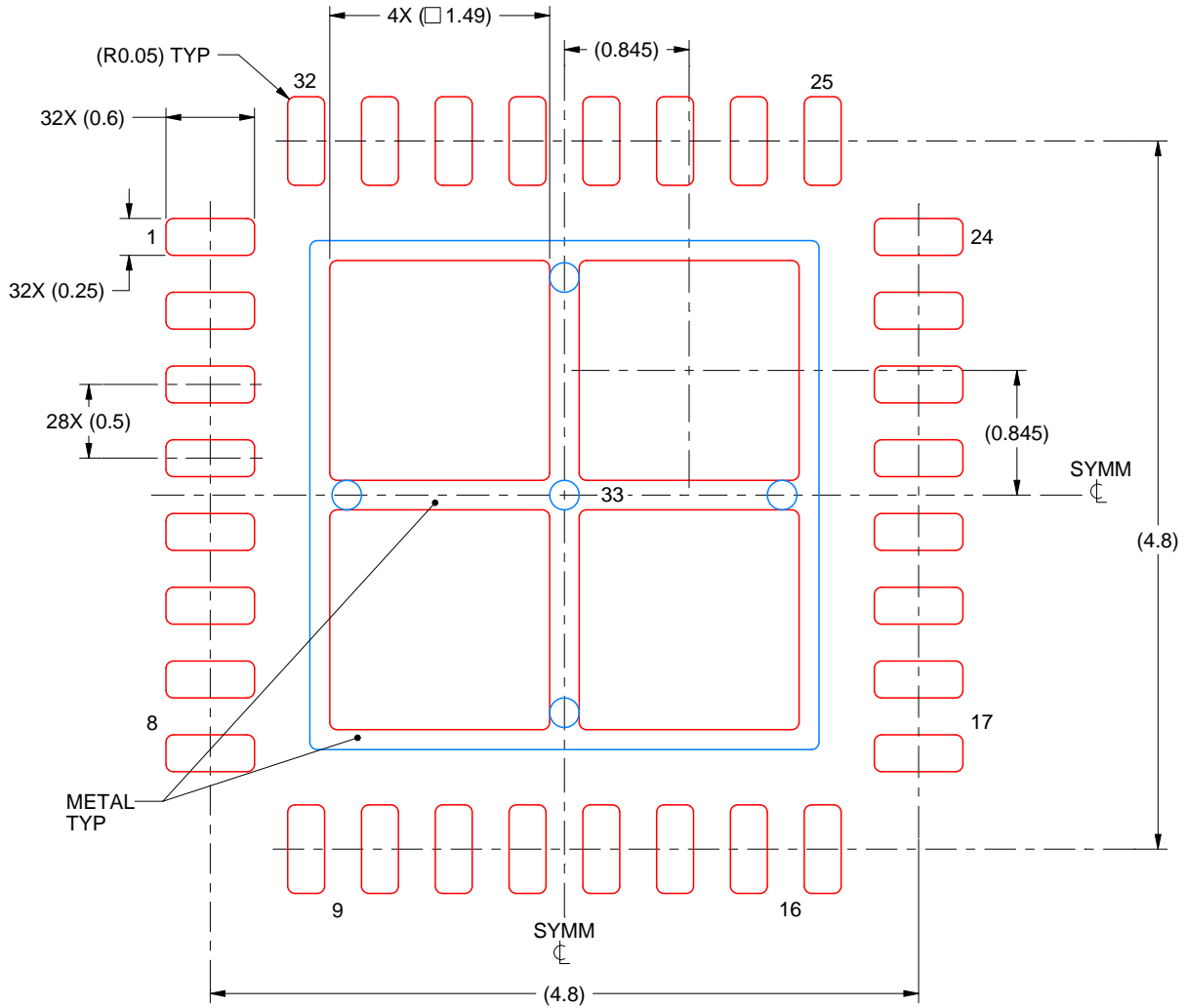
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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