

# TPS65216 Power Management IC (PMIC) With 4 DC/DC Converters, 1 LDO, and Integrated Power Sequencing

## 1 Device Overview

### 1.1 Features

- Three Adjustable Step-Down Converters With Integrated Switching FETs (DCDC1, DCDC2, and DCDC3):
  - DCDC1: 1.1-V Default, up to 1.8 A
  - DCDC2: 1.1-V Default, up to 1.8 A
  - DCDC3: 1.2-V Default, up to 1.8 A
  - VIN Range From 3.6 V to 5.5 V
  - Adjustable Output Voltage Range 0.85 V to 1.675 V (DCDC1 and DCDC2)
  - Adjustable Output Voltage Range 0.9 V to 3.4 V (DCDC3)
  - Power Save Mode at Light Load Current
  - 100% Duty Cycle for Lowest Dropout
  - Active Output-Discharge When Disabled
- One Adjustable Buck-Boost Converter With Integrated Switching FETs (DCDC4):
  - DCDC4: 3.3-V Default, up to 1.6 A
  - VIN Range from 3.6 V to 5.5 V
  - Adjustable Output Voltage Range from 1.175 V to 3.4 V
  - Active Output-Discharge When Disabled
- Adjustable General-Purpose LDO (LDO1)
  - LDO1: 1.8-V Default up to 400 mA
  - VIN Range from 1.8 V to 5.5 V
  - Adjustable Output Voltage Range from 0.9 V to 3.4 V
  - Active Output-Discharge When Disabled
- High-Voltage Load Switch (LS) With 100-mA or 500-mA Selectable Current Limit
  - VIN Range From 1.8 V to 10 V
  - 500-m $\Omega$  (Max) Switch Impedance
- Supervisor With Built-in Supervisor Function Monitors
  - DCDC1, DCDC2  $\pm$ 4% Tolerance
  - DCDC3, DCDC4  $\pm$ 5% Tolerance
  - LDO1  $\pm$ 5% Tolerance
- Protection, Diagnostics, and Control:
  - Undervoltage Lockout (UVLO)
  - Always-on Push-Button Monitor
  - Overtemperature Warning and Shutdown
  - I<sup>2</sup>C Interface (Address 0x24) (See [Timing Requirements](#) for I<sup>2</sup>C Operation at 400 kHz)

### 1.2 Applications

- [Grid Infrastructure](#)
- [Human-Machine Interface \(HMI\)](#)
- [Industrial Automation](#)
- [Electronic Point of Sale \(ePOS\)](#)
- [Test and Measurement](#)
- [Industrial Communications](#)
- [Backplane I/O](#)
- [Connected Industrial Drives](#)

### 1.3 Description

The TPS65216 is a single chip, power-management IC (PMIC) specifically designed to support the AMIC110, AMIC120, AM335x, and AM437x line of processors in line-powered (5 V) applications. The device is characterized across a  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  temperature range, making it suitable for various industrial applications.

The TPS65216 is specifically designed to provide power management for all the functionalities of the AMIC110, AMIC120, AM335x, and AM437x. The DC/DC converters DCDC1 through DCDC4 are intended to power the core, MPU, DDR memory, and 3.3-V analog and I/O, respectively. LDO1 provides the 1.8-V analog and I/O for the processor. GPIO2 allows for warm reset of the DCDC1 and DCDC2 converters. The I<sup>2</sup>C interface allows the user to enable and disable all voltage regulators, the load switch, and GPIOs. Additionally, UVLO and supervisor voltage thresholds, power-up sequence, and power-down sequence can be programmed through I<sup>2</sup>C. Interrupts for overtemperature, overcurrent, and undervoltage can be monitored as well. The supervisor monitors DCDC1 through DCDC4 and LDO1. The supervisor has two settings, one for typical undervoltage tolerance (STRICT = 0b), and one for tight undervoltage and overvoltage tolerances (STRICT = 1b). A power-good signal indicates proper regulation of the five voltage regulators.



Three hysteretic step-down converters are targeted at providing power for the processor core, MPU, and DDRx memory. The default output voltages for each converter can be adjusted through the I<sup>2</sup>C interface. DCDC1 and DCDC2 feature dynamic voltage scaling to provide power at all operating points of the processor. DCDC1 and DCDC2 also have programmable slew rates to help protect processor components. DCDC3 remains powered while the processor is in sleep mode to maintain power to DDRx memory.

The TPS65216 device is available in a 48-pin VQFN package (6 mm × 6 mm, 0.4-mm pitch).

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65216	VQFN (48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Device Overview</b> .....	<b><a href="#">1</a></b>	5.4 Device Functional Modes .....	<b><a href="#">38</a></b>
1.1 Features .....	<a href="#">1</a>	5.5 Register Maps .....	<a href="#">40</a>
1.2 Applications .....	<a href="#">1</a>	<b>6 Application and Implementation</b> .....	<b><a href="#">81</a></b>
1.3 Description .....	<a href="#">1</a>	6.1 Application Information .....	<a href="#">81</a>
1.4 Simplified Schematic .....	<a href="#">3</a>	6.2 Typical Application .....	<a href="#">82</a>
<b>2 Revision History</b> .....	<b><a href="#">4</a></b>	<b>7 Power Supply Recommendations</b> .....	<b><a href="#">85</a></b>
<b>3 Pin Configuration and Functions</b> .....	<b><a href="#">5</a></b>	<b>8 Layout</b> .....	<b><a href="#">85</a></b>
3.1 Pin Functions .....	<a href="#">5</a>	8.1 Layout Guidelines .....	<a href="#">85</a>
<b>4 Specifications</b> .....	<b><a href="#">7</a></b>	8.2 Layout Example .....	<a href="#">86</a>
4.1 Absolute Maximum Ratings .....	<a href="#">7</a>	<b>9 Device and Documentation Support</b> .....	<b><a href="#">87</a></b>
4.2 ESD Ratings .....	<a href="#">7</a>	9.1 Device Support .....	<a href="#">87</a>
4.3 Recommended Operating Conditions .....	<a href="#">8</a>	9.2 Documentation Support .....	<a href="#">87</a>
4.4 Thermal Information .....	<a href="#">8</a>	9.3 Receiving Notification of Documentation Updates ..	<a href="#">87</a>
4.5 Electrical Characteristics .....	<a href="#">9</a>	9.4 Support Resources .....	<a href="#">87</a>
4.6 Timing Requirements .....	<a href="#">15</a>	9.5 Trademarks .....	<a href="#">87</a>
4.7 Typical Characteristics .....	<a href="#">17</a>	9.6 Electrostatic Discharge Caution .....	<a href="#">88</a>
<b>5 Detailed Description</b> .....	<b><a href="#">18</a></b>	9.7 Glossary .....	<a href="#">88</a>
5.1 Overview .....	<a href="#">18</a>	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	<b><a href="#">88</a></b>
5.2 Functional Block Diagram .....	<a href="#">19</a>	10.1 Package Option Addendum .....	<a href="#">89</a>
5.3 Feature Description .....	<a href="#">20</a>		

## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2018) to Revision A	Page
• Updated <i>Title</i> and <i>Description</i> section .....	<a href="#">1</a>

### 3 Pin Configuration and Functions

Figure 3-1 shows the 48-pin RSL Plastic Quad Flatpack No-Lead.

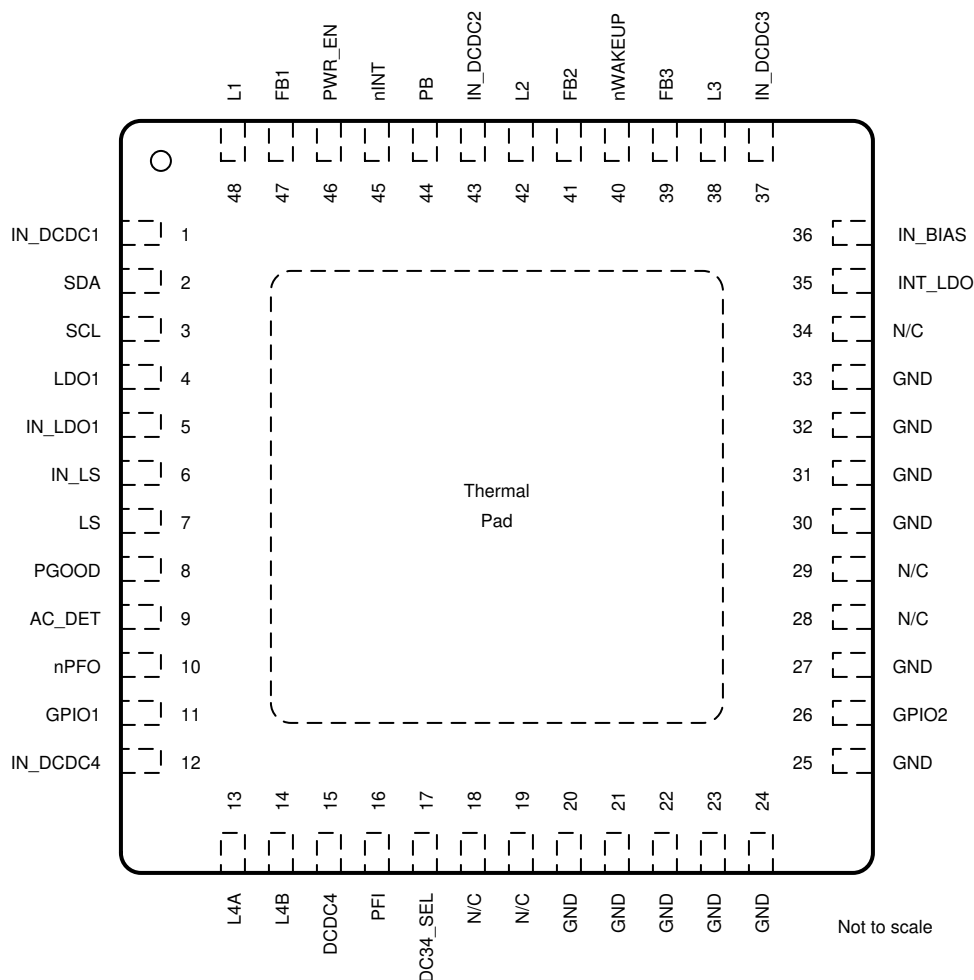


Figure 3-1. 48-Pin RSL VQFN With Exposed Thermal Pad (Top View, 6 mm × 6 mm × 1 mm With 0.4-mm Pitch)

#### 3.1 Pin Functions

##### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN_DCDC1	P	Input supply pin for DCDC1.
2	SDA	I/O	Data line for the I <sup>2</sup> C interface. Connect to pullup resistor.
3	SCL	I	Clock input for the I <sup>2</sup> C interface. Connect to pullup resistor.
4	LDO1	O	Output voltage pin for LDO1. Connect to capacitor.
5	IN_LDO1	P	Input supply pin for LDO1.
6	IN_LS	P	Input supply pin for the load switch.
7	LS	O	Output voltage pin for the load switch. Connect to capacitor.
8	PGOOD	O	Power-good output (configured as open drain). Pulled low when either DCDC1-4 or LDO1 are out of regulation. Load switch does not affect PGOOD pin.
9	AC_DET	I	AC monitor input and enable for DCDC1-4, LDO1 and load switch. See Section 5.4.1 for details. Tie pin to IN_BIAS if not used.

## Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
10	nPFO	O	Power-fail comparator output, deglitched (open drain). Pin is pulled low when PFI input is below power-fail threshold.
11	GPIO1	I/O	General-purpose, open-drain output. See <a href="#">Section 5.3.1.11</a> for more information.
12	IN_DCDC4	P	Input supply pin for DCDC4.
13	L4A	P	Switch pin for DCDC4. Connect to inductor.
14	L4B	P	Switch pin for DCDC4. Connect to inductor.
15	DCDC4	P	Output voltage pin for DCDC4. Connect to capacitor.
16	PFI	I	Power-fail comparator input. Connect to resistor divider.
17	DC34_SEL	I	Power-up default selection pin for DCDC3 or DCDC4. Power-up default is programmed by a resistor connected to ground. See <a href="#">Section 5.3.1.10</a> for resistor options.
18	N/C	–	No connect. Leave pin floating.
19	N/C	–	No connect. Leave pin floating.
20	GND	—	Connect pin to ground.
21	GND		
22	GND		
23	GND		
24	GND		
25	GND		
26	GPIO2	I/O	Pin can be configured as warm reset (negative edge) for DCDC1 and DCDC2 or as a general-purpose, open-drain output. See <a href="#">Section 5.3.1.11</a> for more details.
27	GND	–	Connect pin to ground.
28	N/C	—	No connect. Leave pin floating.
29	N/C		
30	GND	—	Connect pin to ground.
31	GND		
32	GND		
33	GND		
34	N/C	–	No connect. Leave pin floating.
35	INT_LDO	P	Internal bias voltage. Connect to a 1- $\mu$ F capacitor. TI does not recommended connecting any external load to this pin.
36	IN_BIAS	P	Input supply pin for reference system.
37	IN_DCDC3	P	Input supply pin for DCDC3.
38	L3	P	Switch pin for DCDC3. Connect to inductor.
39	FB3	I	Feedback voltage pin for DCDC3. Connect to output capacitor.
40	nWAKEUP	O	Signal to SOC to indicate a power on event (active low, open-drain output).
41	FB2	I	Feedback voltage pin for DCDC2. Connect to output capacitor.
42	L2	P	Switch pin for DCDC2. Connect to inductor.
43	IN_DCDC2	P	Input supply pin for DCDC2.
44	PB	I	Push-button monitor input. Typically connected to a momentary switch to ground (active low). See <a href="#">Section 5.4.1</a> for details.
45	nINT	O	Interrupt output (active low, open drain). Pin is pulled low if an interrupt bit is set. The pin returns to Hi-Z state after the bit causing the interrupt has been read. Interrupts can be masked.
46	PWR_EN	I	Power enable input for DCDC1-4, LDO1 and load switch. See <a href="#">Section 5.4.1</a> for details.
47	FB1	I	Feedback voltage pin for DCDC1. Connect to output capacitor.
48	L1	P	Switch pin for DCDC1. Connect to inductor.
—	Thermal Pad	P	Power ground and thermal relief. Connect to ground plane.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

Operating under free-air temperature range (unless otherwise noted).<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	IN_BIAS, IN_LDO1, IN_DCDC1, IN_DCDC2, IN_DCDC3, IN_DCDC4	-0.3	7	V
	IN_LS	-0.3	11.2	
Input voltage	All pins unless specified separately	-0.3	7	V
Output voltage	All pins unless specified separately	-0.3	7	V
Sink current	PGOOD, nWAKEUP, nINT, nPFO, SDA, GPIO1, GPIO2		6	mA
T <sub>A</sub>	Operating ambient temperature	-40	105	°C
T <sub>J</sub>	Junction temperature	-40	125	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		V
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, IN_BIAS		3.6		5.5	V
Input voltage for DCDC1, DCDC2, DCDC3, and DCDC4		3.6		5.5	V
Input voltage for LDO1		1.8		5.5	V
Input voltage for LS		1.8		10	V
Output voltage for DCDC1		0.85		1.675	V
Output voltage for DCDC2		0.85		1.675	V
Output voltage for DCDC3		0.9		3.4	V
Output voltage for DCDC4		1.175		3.4	V
Output voltage for LDO1		0.9		3.4	V
Output current for DCDC1, DCDC2, and DCDC3		0		1.8	A
Output current for DCDC4	VIN_DCDC4 = 2.8 V			1	A
	VIN_DCDC4 = 3.6 V			1.3	
	VIN_DCDC4 = 5 V			1.6	
Output current for LDO1		0		400	mA
Output current for LS	VIN_LS > 2.3 V	0		900	mA
	VIN_LS ≤ 2.3 V	0		475	

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65216	UNIT
		RSL (VQFN)	
		48 PINS	
R <sub>θJC(top)</sub>	Junction-to-case (top)	17.2	°C/W
R <sub>θJB</sub>	Junction-to-board	5.8	°C/W
R <sub>θJA</sub>	Thermal resistance, junction-to-ambient. JEDEC 4-layer, high-K board.	30.6	°C/W
Ψ <sub>JT</sub>	Junction-to-package top	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board	5.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom)	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.



## 4.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT VOLTAGE AND CURRENTS</b>							
V <sub>IN_BIAS</sub>	Input supply voltage range	Normal operation		3.6		5.5	V
		EEPROM programming		4.5		5.5	
	Deglitch time				5		ms
I <sub>OFF</sub>	OFF state current, total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LS	V <sub>IN</sub> = 3.6 V; All rails disabled. T <sub>J</sub> = 0°C to 85°C			5		μA
I <sub>SUSPEND</sub>	SUSPEND current, total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LS	V <sub>IN</sub> = 3.6 V; DCDC3 enabled, low-power mode, no load. All other rails disabled. T <sub>J</sub> = 0°C to 105°C			220		μA
<b>INT_LDO</b>							
V <sub>INT_LDO</sub>	Output voltage				2.5		V
	DC accuracy	I <sub>OUT</sub> < 10 mA		-2%		2%	
I <sub>OUT</sub>	Output current range	Maximum allowable external load		0		10	mA
I <sub>LIMIT</sub>	Short circuit current limit	Output shorted to GND			23		mA
t <sub>HOLD</sub>	Hold-up time	Measured from V <sub>INT_LDO</sub> = to V <sub>INT_LDO</sub> = 1.8 V All rails enabled before power off, V <sub>IN_BIAS</sub> = 2.8 V to 0 V in < 5 μs No external load on INT_LDO C <sub>INT_LDO</sub> = 1 μF, see <a href="#">Table 6-3</a> .		150			ms
C <sub>OUT</sub>	Nominal output capacitor value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .		0.1	1	22	μF
	Tolerance	Ceramic, X5R or X7R, rated voltage ≥ 6.3 V		-20%		20%	
<b>DCDC1 (1.1-V BUCK)</b>							
V <sub>IN_DCDC1</sub>	Input voltage range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub>		3.6		5.5	V
V <sub>DCDC1</sub>	Output voltage range	Adjustable through I <sup>2</sup> C		0.85		1.675	V
	DC accuracy	3.6 V ≤ V <sub>IN</sub> ≤ 5.5 V; 0 A ≤ I <sub>OUT</sub> ≤ 1.8 A		-2%		2%	
	Dynamic accuracy	In respect to nominal output voltage I <sub>OUT</sub> = 50 mA to 450 mA in < 1 μs C <sub>OUT</sub> ≥ 10 μF, over full input voltage range.		-2.5%		2.5%	
I <sub>OUT</sub>	Continuous output current	V <sub>IN_DCDC1</sub> > 3.6 V				1.8	A
I <sub>Q</sub>	Quiescent current	Total current from I <sub>N_DCDC1</sub> pin; Device not switching, no load			25	50	μA
R <sub>DS(ON)</sub>	High-side FET on resistance	V <sub>IN_DCDC1</sub> = 3.6 V			230	355	mΩ
	Low-side FET on resistance	V <sub>IN_DCDC1</sub> = 3.6 V			90	145	
I <sub>LIMIT</sub>	High-side current limit	V <sub>IN_DCDC1</sub> = 3.6 V			2.8		A
	Low-side current limit	V <sub>IN_DCDC1</sub> = 3.6 V			3.1		
V <sub>PG</sub>	Power-good threshold	V <sub>OUT</sub> falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	96%	96.5%	97%	
	Hysteresis	V <sub>OUT</sub> rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V <sub>OUT</sub> falling	STRICT = 0b		1		ms
			STRICT = 1b		50		μs
			V <sub>OUT</sub> rising	STRICT = 0b		10	
STRICT = 1b		10			μs		
Time-out				5		ms	
V <sub>OV</sub>	Overvoltage detection threshold	V <sub>OUT</sub> rising, STRICT = 1b		103%	103.5%	104%	
	Hysteresis	V <sub>OUT</sub> falling, STRICT = 1b			0.25%		
	Deglitch	V <sub>OUT</sub> rising, STRICT = 1b			50		μs
I <sub>INRUSH</sub>	Inrush current	V <sub>IN_DCDC1</sub> = 3.6 V; C <sub>OUT</sub> = 10 μF to 100 μF				500	mA

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
R <sub>DIS</sub>	Discharge resistor		150	250	350	Ω	
L	Nominal inductor value	See <a href="#">Table 6-2</a> .	1	1.5	2.2	μH	
	Tolerance		-30%		30%		
C <sub>OUT</sub>	Output capacitance value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .	10	22	100 <sup>(1)</sup>	μF	
<b>DCDC2 (1.1-V BUCK)</b>							
V <sub>IN_DCDC2</sub>	Input voltage range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub>	3.6		5.5	V	
V <sub>DCDC2</sub>	Output voltage range	Adjustable through I <sup>2</sup> C	0.85		1.675	V	
	DC accuracy	3.6 V ≤ V <sub>IN</sub> ≤ 5.5 V; 0 A ≤ I <sub>OUT</sub> ≤ 1.8 A	-2%		2%		
	Dynamic accuracy	In respect to nominal output voltage I <sub>OUT</sub> = 50 mA to 450 mA in < 1 μs C <sub>OUT</sub> ≥ 10 μF, over full input voltage range	-2.5%		2.5%		
I <sub>OUT</sub>	Continuous output current	V <sub>IN_DCDC2</sub> > 3.6 V			1.8	A	
I <sub>Q</sub>	Quiescent current	Total current from I <sub>N_DCDC2</sub> pin; device not switching, no load		25	50	μA	
R <sub>DS(ON)</sub>	High-side FET on resistance	V <sub>IN_DCDC2</sub> = 3.6 V		230	355	mΩ	
	Low-side FET on resistance	V <sub>IN_DCDC2</sub> = 3.6 V		90	145		
I <sub>LIMIT</sub>	High-side current limit	V <sub>IN_DCDC2</sub> = 3.6 V		2.8		A	
	Low-side current limit	V <sub>IN_DCDC2</sub> = 3.6 V		3.1			
V <sub>PG</sub>	Power-good threshold	V <sub>OUT</sub> falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	96%	96.5%	97%	
	Hysteresis	V <sub>OUT</sub> rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V <sub>OUT</sub> falling	STRICT = 0b		1		ms
			STRICT = 1b		50		μs
		V <sub>OUT</sub> rising	STRICT = 0b		10		μs
			STRICT = 1b		10		μs
Time-out	Occurs at enable of DCDC2 and after DCDC2 register write (register 0x17).			5		ms	
V <sub>OV</sub>	Overvoltage detection threshold	V <sub>OUT</sub> rising, STRICT = 1b	103%	103.5%	104%		
	Hysteresis	V <sub>OUT</sub> falling, STRICT = 1b		0.25%			
	Deglitch	V <sub>OUT</sub> rising, STRICT = 1b		50		μs	
I <sub>INRUSH</sub>	Inrush current	V <sub>IN_DCDC2</sub> = 3.6 V; C <sub>OUT</sub> = 10 μF to 100 μF			500	mA	
R <sub>DIS</sub>	Discharge resistor		150	250	350	Ω	
L	Nominal inductor value	See <a href="#">Table 6-2</a> .	1	1.5	2.2	μH	
	Tolerance		-30%		30%		
C <sub>OUT</sub>	Output capacitance value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .	10	22	100 <sup>(1)</sup>	μF	
<b>DCDC3 (1.2-V BUCK)</b>							
V <sub>IN_DCDC3</sub>	Input voltage range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub>	3.6		5.5	V	
V <sub>DCDC3</sub>	Output voltage range	Adjustable through I <sup>2</sup> C	0.9		3.4	V	
	DC accuracy	3.6 V ≤ V <sub>IN</sub> ≤ 5.5 V; 0 A ≤ I <sub>OUT</sub> ≤ 1.8 A, V <sub>IN_DCDC3</sub> ≥ (V <sub>DCDC3</sub> + 700 mV)	-2%		2%		
	Dynamic accuracy	In respect to nominal output voltage I <sub>OUT</sub> = 50 mA to 450 mA in < 1 μs C <sub>OUT</sub> ≥ 10 μF, over full input voltage range	-2.5%		-2.5%		
I <sub>OUT</sub>	Continuous output current	V <sub>IN_DCDC3</sub> > 3.6 V			1.8	A	
I <sub>Q</sub>	Quiescent current	Total current from I <sub>N_DCDC3</sub> pin; Device not switching, no load		25	50	μA	

(1) 500-μF of remote capacitance can be supported for DCDC1 and DCDC2.

**Electrical Characteristics (continued)**

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
R <sub>DS(ON)</sub>	High-side FET on resistance	V <sub>IN_DCDC3</sub> = 3.6 V			230	345	mΩ	
	Low-side FET on resistance	V <sub>IN_DCDC3</sub> = 3.6 V			100	150		
I <sub>LIMIT</sub>	High-side current limit	V <sub>IN_DCDC3</sub> = 3.6 V			2.8		A	
	Low-side current limit	V <sub>IN_DCDC3</sub> = 3.6 V			3			
V <sub>PG</sub>	Power-good threshold	V <sub>OUT</sub> falling	STRICT = 0b	88.5%	90%	91.5%		
		V <sub>OUT</sub> falling	STRICT = 1b	95%	95.5%	96%		
	Hysteresis	V <sub>OUT</sub> rising	STRICT = 0b	3.8%	4.1%	4.4%		
		V <sub>OUT</sub> rising	STRICT = 1b		0.25%			
	Deglitch	V <sub>OUT</sub> falling	STRICT = 0b		1		ms	
			STRICT = 1b		50		μs	
		V <sub>OUT</sub> rising	STRICT = 0b			10		μs
			STRICT = 1b			10		μs
Time-out	Occurs at enable of DCDC3 and after DCDC3 register write (register 0x18).			5		ms		
V <sub>OV</sub>	Overvoltage detection threshold	V <sub>OUT</sub> rising, STRICT = 1b		104%	104.5%	105%		
	Hysteresis	V <sub>OUT</sub> falling, STRICT = 1b			0.25%			
	Deglitch	V <sub>OUT</sub> rising, STRICT = 1b			50		μs	
I <sub>INRUSH</sub>	Inrush current	V <sub>IN_DCDC3</sub> = 3.6 V; C <sub>OUT</sub> = 10 μF to 100 μF				500	mA	
R <sub>DIS</sub>	Discharge resistor			150	250	350	Ω	
L	Nominal inductor value	See <a href="#">Table 6-2</a> .		1.0	1.5	2.2	μH	
	Tolerance			-30%		30%		
C <sub>OUT</sub>	Output capacitance value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .		10	22	100	μF	
<b>DCDC4 (3.3-V BUCK-BOOST) / ANALOG AND I/O</b>								
V <sub>IN_DCDC4</sub>	Input voltage operating range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub> , -40°C to +105°C		3.6		5.5	V	
V <sub>DCDC4</sub>	Output voltage range	Adjustable through I <sup>2</sup> C		1.175		3.3	V	
V <sub>DCDC4</sub>	DC accuracy	4.2 V ≤ V <sub>IN</sub> ≤ 5.5 V; 3 V < V <sub>OUT</sub> ≤ 3.4 V 0 A ≤ I <sub>OUT</sub> ≤ 1.6 A		-2%		2%		
		3.3 V ≤ V <sub>IN</sub> ≤ 4.2 V; 3 V < V <sub>OUT</sub> ≤ 3.4 V 0 A ≤ I <sub>OUT</sub> ≤ 1.3 A		-2%		2%		
		2.8 V ≤ V <sub>IN</sub> ≤ 5.5 V; 1.65 V < V <sub>OUT</sub> ≤ 3 V 0 A ≤ I <sub>OUT</sub> ≤ 1 A		-2%		2%		
		2.8 V ≤ V <sub>IN</sub> ≤ 5.5 V; 1.175 V < V <sub>OUT</sub> ≤ 1.65 V 0 A ≤ I <sub>OUT</sub> ≤ 1 A		-2.5%		2.5%		
	Output voltage ripple	PFM mode enabled; 4.2 V ≤ V <sub>IN</sub> ≤ 5.5 V; 0 A ≤ I <sub>OUT</sub> ≤ V <sub>OUT</sub> = 3.3 V					mV <sub>pp</sub>	
	Minimum duty cycle in step-down mode					18%		
I <sub>OUT</sub>	Continuous output current	V <sub>IN_DCDC4</sub> = 2.8 V, V <sub>OUT</sub> = 3.3 V				1	A	
		V <sub>IN_DCDC4</sub> = 3.6 V, V <sub>OUT</sub> = 3.3 V				1.3		
		V <sub>IN_DCDC4</sub> = 5 V, V <sub>OUT</sub> = 3.3 V				1.6		
I <sub>Q</sub>	Quiescent current	Total current from IN_DCDC4 pin; Device not switching, no load.			25	50	μA	
f <sub>SW</sub>	Switching frequency				2400		kHz	

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R <sub>DS(ON)</sub>	High-side FET on resistance	V <sub>IN_DCDC3</sub> = 3.6 V	IN_DCDC4 to L4A	166			mΩ
			L4B to DCDC4	149			
	Low-side FET on resistance	V <sub>IN_DCDC3</sub> = 3.6 V	L4A to GND	142	190		
			L4B to GND	144	190		
I <sub>LIMIT</sub>	Average switch current limit	V <sub>IN_DCDC4</sub> = 3.6 V	3000			mA	
V <sub>PG</sub>	Power-good threshold	V <sub>OUT</sub> falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	95%	95.5%	96%	
	Hysteresis	V <sub>OUT</sub> rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b	0.25%			
	Deglitch	V <sub>OUT</sub> falling	STRICT = 0b	1			ms
			STRICT = 1b	50			μs
		V <sub>OUT</sub> rising	STRICT = 0b	10			μs
			STRICT = 1b	10			μs
Time-out	Occurs at enable of DCDC4 and after DCDC4 register write (register 0x19)		5			ms	
V <sub>OV</sub>	Overvoltage detection threshold	V <sub>OUT</sub> rising, STRICT = 1b		104%	104.5%	105%	
	Hysteresis	V <sub>OUT</sub> falling, STRICT = 1b		0.25%			
	Deglitch	V <sub>OUT</sub> rising, STRICT = 1b		50			μs
I <sub>INRUSH</sub>	Inrush current	V <sub>IN_DCDC4</sub> = 3.6 V ≤ V <sub>INDCDC4</sub> ≤ 5.5 V; 40 μF ≤ C <sub>OUT</sub> ≤ 100 μF		500			mA
R <sub>DIS</sub>	Discharge resistor			150	250	350	Ω
L	Nominal inductor value	See <a href="#">Table 6-2</a> .		1.2	1.5	2.2	μH
	Tolerance			-30%		30%	
C <sub>OUT</sub>	Output capacitance value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .		40	80	100	μF

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>LDO1 (1.8-V LDO)</b>							
V <sub>IN_LDO1</sub>	Input voltage range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub>	1.8		5.5	V	
I <sub>Q</sub>	Quiescent current	No load		35		μA	
V <sub>OUT</sub>	Output voltage range	Adjustable through I <sup>2</sup> C	0.9		3.4	V	
	DC accuracy	V <sub>OUT</sub> + 0.2 V ≤ V <sub>IN</sub> ≤ 5.5 V; 0 A ≤ I <sub>OUT</sub> ≤ 200 mA	-2%		2%		
I <sub>OUT</sub>	Output current range	V <sub>IN_LDO1</sub> - V <sub>DO</sub> = V <sub>OUT</sub>	0		200	mA	
		V <sub>IN_LDO1</sub> > 2.7 V, V <sub>OUT</sub> = 1.8 V	0		400		
I <sub>LIMIT</sub>	Short circuit current limit	Output shorted to GND	445	550		mA	
V <sub>DO</sub>	Dropout voltage	I <sub>OUT</sub> = 100 mA, V <sub>IN</sub> = 3.6 V			200	mV	
V <sub>PG</sub>	Power-good threshold	V <sub>OUT</sub> falling	STRICT = 0b	86%	90%	94%	
			STRICT = 1b	95%	95.5%	96%	
		Hysteresis, V <sub>OUT</sub> rising	STRICT = 0b	3%	4%	5%	
			STRICT = 1b		0.25%		
	Deglitch	V <sub>OUT</sub> falling	STRICT = 0b		1		ms
			STRICT = 1b		50		μs
		V <sub>OUT</sub> rising	STRICT = 0b		10		μs
			STRICT = 1b		10		μs
Time-out			5		ms		
V <sub>OV</sub>	Overvoltage detection threshold	V <sub>OUT</sub> rising, STRICT = 1b	104%	104.5%	105%		
	Hysteresis	V <sub>OUT</sub> falling, STRICT = 1b		0.25%			
	Deglitch	V <sub>OUT</sub> rising, STRICT = 1b		50		μs	
		V <sub>OUT</sub> falling, STRICT = 1b		1		ms	
R <sub>DIS</sub>	Discharge resistor		150	250	380	Ω	
C <sub>OUT</sub>	Output capacitance value	Ceramic, X5R or X7R		22	100	μF	
<b>LOAD SWITCH</b>							
V <sub>IN_LS</sub>	Input voltage range	V <sub>IN_BIAS</sub> > V <sub>UVLO</sub>	1.8		10	V	
R <sub>DS(ON)</sub>	Static on resistance	V <sub>IN_LS</sub> = 9 V, I <sub>OUT</sub> = 500 mA, over full temperature range			440	mΩ	
		V <sub>IN_LS</sub> = 5 V, I <sub>OUT</sub> = 500 mA, over full temperature range			526		
		V <sub>IN_LS</sub> = 2.8 V, I <sub>OUT</sub> = 200 mA, over full temperature range			656		
		V <sub>IN_LS</sub> = 1.8 V, I <sub>OUT</sub> = 200 mA, over full temperature range			910		
I <sub>LIMIT</sub>	Short circuit current limit	V <sub>IN_LS</sub> > 2.3 V, Output shorted to GND	LSILIM[1:0] = 00b	98		126	mA
			LSILIM[1:0] = 01b	194		253	
			LSILIM[1:0] = 10b	475		738	
			LSILIM[1:0] = 11b	900		1234	
		V <sub>IN_LS</sub> ≤ 2.3 V, Output shorted to GND	LSILIM[1:0] = 00b	98		126	
			LSILIM[1:0] = 01b	194		253	
LSILIM[1:0] = 10b	475		738				
t <sub>BLANK</sub>	Interrupt blanking time	Output shorted to GND until interrupt is triggered.		15		ms	
R <sub>DIS</sub>	Internal discharge resistor at output <sup>(2)</sup>	LSDCHRG = 1	650	1000	1500	Ω	
T <sub>OTS</sub>	Overtemperature shutdown <sup>(3)</sup>		125	132	139	°C	
	Hysteresis			10		°C	

(2) Discharge function disabled by default.

(3) Switch is temporarily turned OFF if input voltage drops below UVLO threshold.

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>OUT</sub>	Nominal output capacitance value	Ceramic, X5R or X7R, see <a href="#">Table 6-3</a> .	1	100	220	μF
<b>I/O LEVELS AND TIMING CHARACTERISTICS</b>						
PG <sub>DLY</sub>	PGOOD delay time	PGDLY[1:0] = 00b		10		ms
		PGDLY[1:0] = 01b		20		
		PGDLY[1:0] = 10b		50		
		PGDLY[1:0] = 11b		150		
t <sub>DG</sub>	Deglitch time	PB input	Rising edge		100	ms
			Falling edge		50	ms
		AC_DET input	Rising edge		100	μs
			Falling edge		10	ms
		PWR_EN input	Rising edge		10	ms
			Falling edge		100	μs
		GPIO1	Rising edge		1	ms
			Falling edge		1	ms
		GPIO2	Rising edge		5	μs
			Falling edge		5	μs
t <sub>RESET</sub>	Reset time	PB input held low	TRST = 0b		8	s
			TRST = 1b		15	
V <sub>IH</sub>	High level input voltage	SCL, SDA, GPIO1, and GPIO2		1.3		V
		AC_DET, PB		0.66 × IN_BIAS		
		PWR_EN		1.3		
V <sub>IL</sub>	Low level input voltage	SCL, SDA, PWR_EN, AC_DET, PB, GPIO1, and GPIO2		0	0.4	V
V <sub>OL</sub>	Low level output voltage	nWAKEUP, nINT, SDA, PGOOD, GPIO1, and GPIO2; I <sub>SINK</sub> = 2 mA		0	0.3	V
		nPFO; I <sub>SINK</sub> = 2 mA		0	0.35	
V <sub>PFI</sub>	Power-fail comparator threshold	Input falling		800		mV
	Hysteresis	Input rising		40		mV
	Accuracy			-4%	4%	
	Deglitch	Input falling			25	
Input rising				10		ms
I <sub>DC34_SEL</sub>	DC34_SEL bias current	Enabled only at power-up.		10		μA
V <sub>DC34_SEL</sub>	DCDC3 and DCDC4 power-up default selection thresholds	Threshold 1		100		mV
		Threshold 2		163		
		Threshold 3		275		
		Threshold 4		400		
		Threshold 5		575		
		Threshold 6		825		
		Threshold 7		1200		

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DC34_SEL</sub>	DCDC3 and DCDC4 power-up default selection resistor values	Setting 0	0	0	7.7	kΩ
		Setting 1		12.1		
		Setting 2		20		
		Setting 3	30.9	31.6	32.3	
		Setting 4		45.3		
		Setting 5				
		Setting 6		95.3		
		Setting 7		150		
I <sub>BIAS</sub>	Input bias current	SCL, SDA, GPIO1 <sup>(4)</sup> , GPIO2 <sup>(4)</sup> ; V <sub>IN</sub> = 3.3 V		0.01	1	μA
		PB, AC_DET, PFI; V <sub>IN</sub> = 3.3 V			500	nA
I <sub>LEAK</sub>	Pin leakage current	nINT, nWAKEUP, nPFO, PGOOD, PWR_EN, GPIO1 <sup>(5)</sup> , GPIO2 <sup>(5)</sup> V <sub>OUT</sub> = 3.3 V			500	nA
<b>OSCILLATOR</b>						
f <sub>OSC</sub>	Oscillator frequency			2400		kHz
	Frequency accuracy	T <sub>J</sub> = -40°C to +105°C	-12%		12%	
<b>OVERTEMPERATURE SHUTDOWN</b>						
T <sub>OTS</sub>	Overtemperature shutdown	Increasing junction temperature	135	145	155	°C
	Hysteresis	Decreasing junction temperature		20		
T <sub>WARN</sub>	High-temperature warning	Increasing junction temperature	90	100	110	°C
	Hysteresis	Decreasing junction temperature		15		

(4) Configured as input.

(5) Configured as output.

## 4.6 Timing Requirements

		MIN	NOM	MAX	UNIT
f <sub>SCL</sub>	Serial clock frequency		100		kHz
			400		
t <sub>HD;STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 kHz	4		μs
		SCL = 400 kHz	600		ns
t <sub>LOW</sub>	LOW period of the SCL clock	SCL = 100 kHz	4.7		μs
		SCL = 400 kHz	1.3		
t <sub>HIGH</sub>	HIGH period of the SCL clock	SCL = 100 kHz	4		μs
		SCL = 400 kHz <sup>(1)</sup>	1		
t <sub>SU;STA</sub>	Set-up time for a repeated START condition	SCL = 100 kHz	4.7		μs
		SCL = 400 kHz	600		ns
t <sub>HD;DAT</sub>	Data hold time	SCL = 100 kHz	0	3.45	μs
		SCL = 400 kHz	0	900	ns
t <sub>SU;DAT</sub>	Data set-up time	SCL = 100 kHz	250		ns
		SCL = 400 kHz	100		
t <sub>r</sub>	Rise time of both SDA and SCL signals	SCL = 100 kHz		1000	ns
		SCL = 400 kHz		300	
t <sub>f</sub>	Fall time of both SDA and SCL signals	SCL = 100 kHz		300	ns
		SCL = 400 kHz		300	
t <sub>SU;STO</sub>	Set-up time for STOP condition	SCL = 100 kHz	4		μs
		SCL = 400 kHz	600		ns

(1) The SCL duty cycle at 400 kHz must be > 40%.

**Timing Requirements (continued)**

		MIN	NOM	MAX	UNIT
t <sub>BUF</sub>	Bus free time between STOP and START condition	SCL = 100 kHz		4.7	μs
		SCL = 400 kHz		1.3	
t <sub>SP</sub>	Pulse width of spikes which must be suppressed by the input filter	SCL = 100 kHz	— <sup>(2)</sup>	— <sup>(2)</sup>	ns
		SCL = 400 kHz	0	50	
C <sub>b</sub>	Capacitive load for each bus line	SCL = 100 kHz		400	pF
		SCL = 400 kHz		400	

(2) The inputs of I<sup>2</sup>C devices in Standard-mode do not require spike suppression.



### 4.7 Typical Characteristics

At  $T_J = 25^\circ\text{C}$  unless otherwise noted.

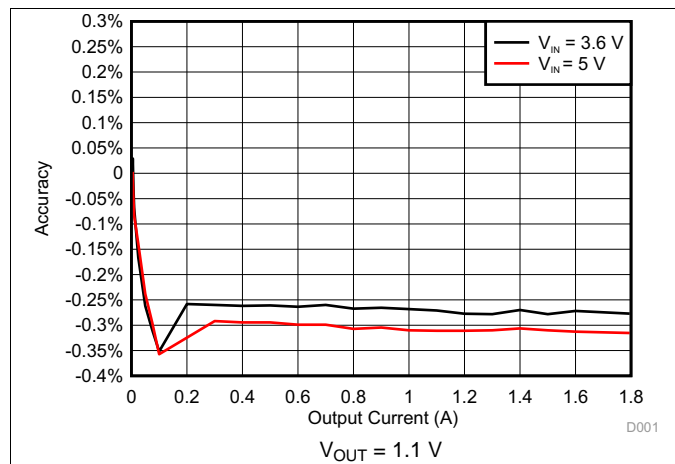


Figure 4-1. DCDC1 Accuracy

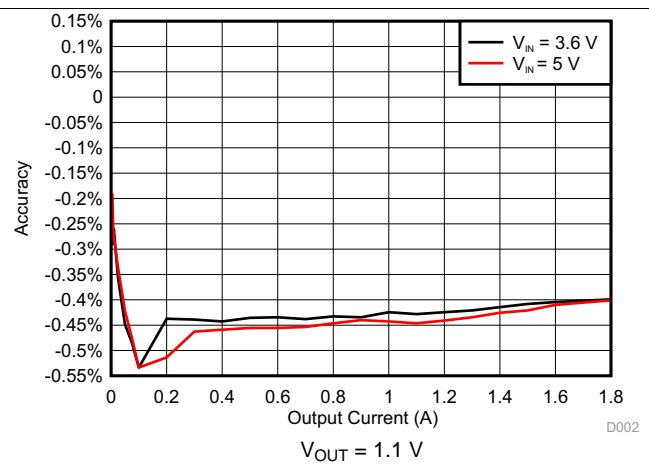


Figure 4-2. DCDC2 Accuracy

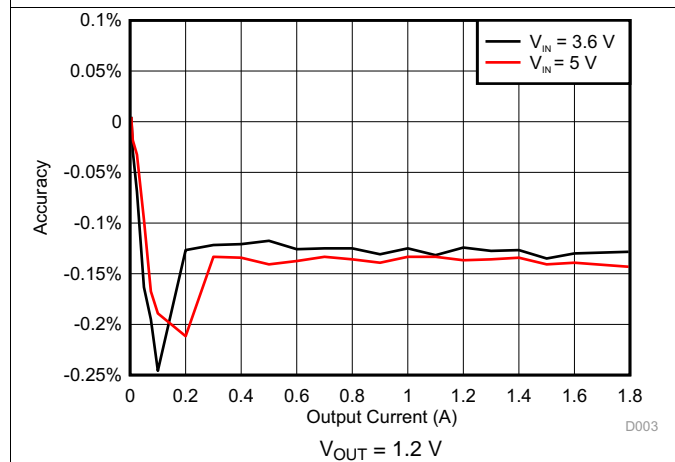


Figure 4-3. DCDC3 Accuracy

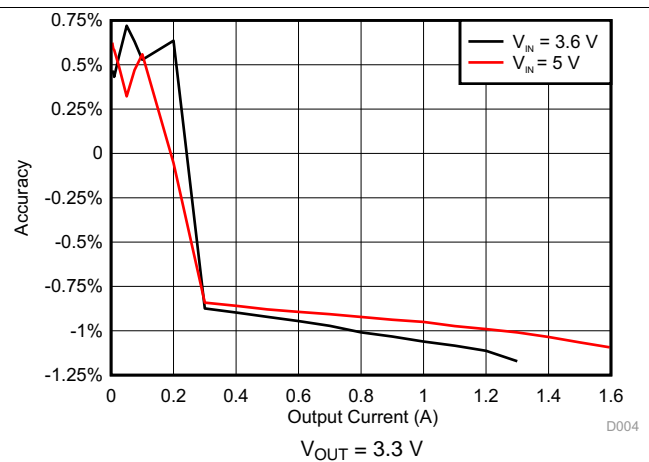


Figure 4-4. DCDC4 Accuracy

## 5 Detailed Description

### 5.1 Overview

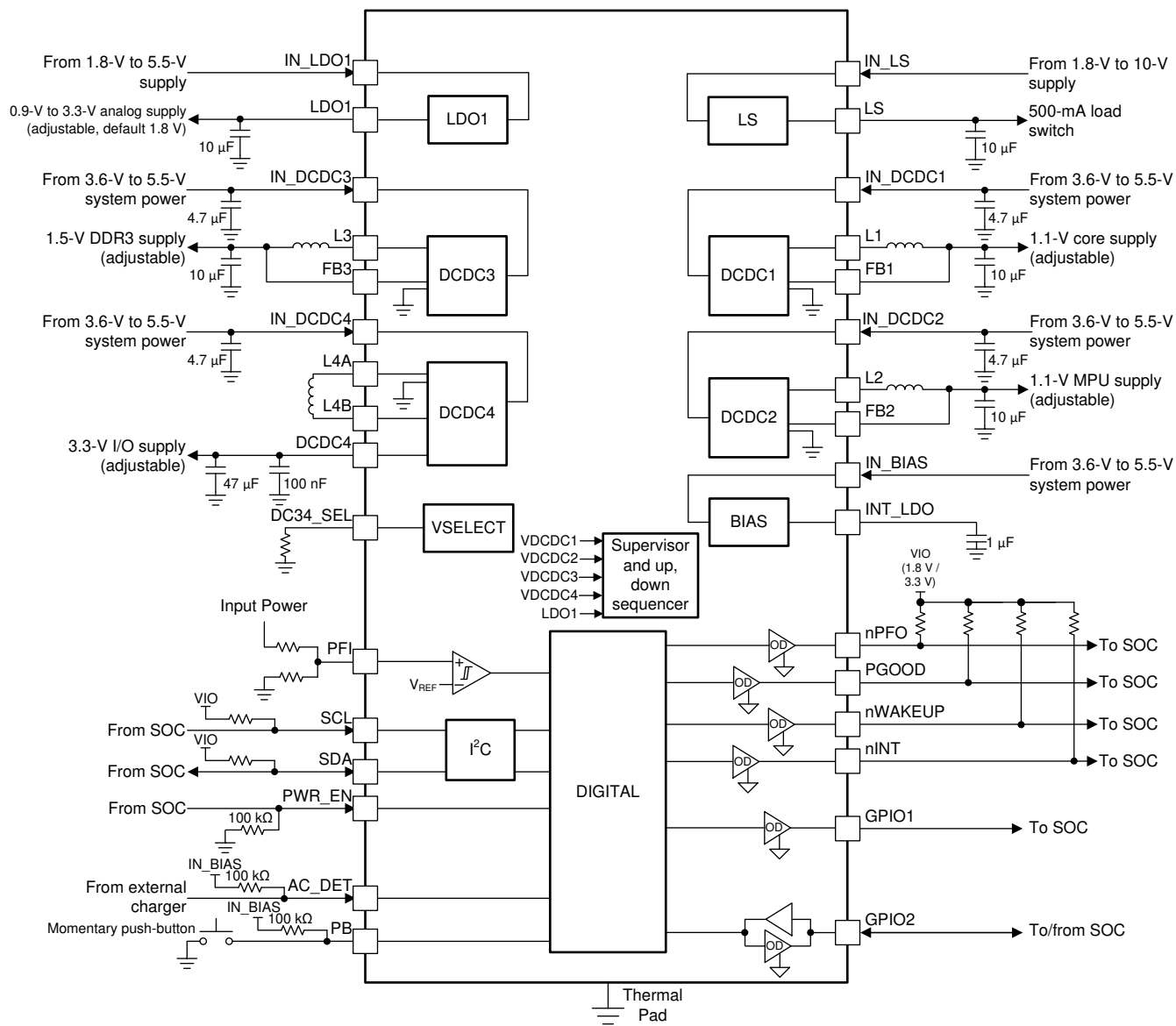
The TPS65216 provides three step-down converters three general-purpose I/Os, one buck-boost converter, one load switch, and one LDO. The system can be supplied by a regulated 5-V supply. The device is characterized across a  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  temperature range, which makes it suitable for various industrial applications.

The I<sup>2</sup>C interface provides comprehensive features for using TPS65216. All rails, the load switch, and GPIOs can be enabled and disabled. Voltage thresholds for the UVLO and supervisor can be customized. Power-up and power-down sequences can also be programmed through I<sup>2</sup>C. Interrupts for overtemperature, overcurrent, and undervoltage can be monitored for the load-switch.

The integrated voltage supervisor monitors DCDC 1-4 and LDO1. It has two settings; the standard settings only monitor for undervoltage, while the strict settings implement tight tolerances on both undervoltage and overvoltage. A power-good signal is provided to report the regulation state of the five rails.

The three hysteretic step-down converters can each supply up to 1.8 A of current. The default output voltages for each converter can be adjusted through the I<sup>2</sup>C interface. DCDC1 and DCDC2 features dynamic voltage scaling with an adjustable slew rate. The step-down converters operate in a low power mode at light load, and can be forced into power mode (PWM) operation for noise sensitive applications.

## 5.2 Functional Block Diagram



## 5.3 Feature Description

### 5.3.1 Wake-Up and Power-Up and Power-Down Sequencing

The TPS65216 has a predefined power-up and power-down sequence, which does not change in a typical application. The user can define custom sequences with I<sup>2</sup>C. The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order of enabling rails. A single rail is assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times between strobes are between 2 ms and 5 ms.

#### 5.3.1.1 Power-Up Sequencing

When the power-up sequence initiates, STROBE 1 occurs, and any rail assigned to this strobe is enabled. After a delay time of DLY1, STROBE 2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I<sup>2</sup>C control. The power-up sequence executes if one of the following events occurs:

- From the OFF state:
  - The push-button (PB) is pressed (falling edge on PB) *or*
  - The AC\_DET pin is pulled low (falling edge) *or*
  - The PWR\_EN is asserted (driven to high-level) *or*
  - The main power is connected (IN\_BIAS) and AC\_DET is grounded *and*
  - The device is not in undervoltage lockout (UVLO) or overtemperature shutdown (OTS).
- From the PRE\_OFF state:
  - The PB is pressed (falling edge on PB) *or*
  - The AC\_DET pin is pulled low (falling edge) *or*
  - The PWR\_EN is asserted (driven to high-level) *and*
  - The device is not in UVLO or OTS.
- From the SUSPEND state:
  - The PB is pressed (falling edge on PB) *or*
  - The AC\_DET pin is pulled low (falling edge) *or*
  - The PWR\_EN pin is pulled high (level sensitive) *and*
  - The device is not in UVLO or OTS.

When a power-up event is detected, the device enters a WAIT\_PWR\_EN state and triggers the power-up sequence. The device remains in WAIT\_PWR\_EN as long as the PWR\_EN and either the PB or AC\_DET pin are held low. If both, the PB and AC\_DET return to logic-high state and the PWR\_EN pin has not been asserted within 20 s of entering WAIT\_PWR\_EN state, the power-down sequence is triggered and the device returns to OFF state. Once PWR\_EN is asserted, the device advances to ACTIVE state, which is functionally equivalent to WAIT\_PWR\_EN. However, the AC\_DET pin is ignored and power-down is controlled by the PWR\_EN pin only.

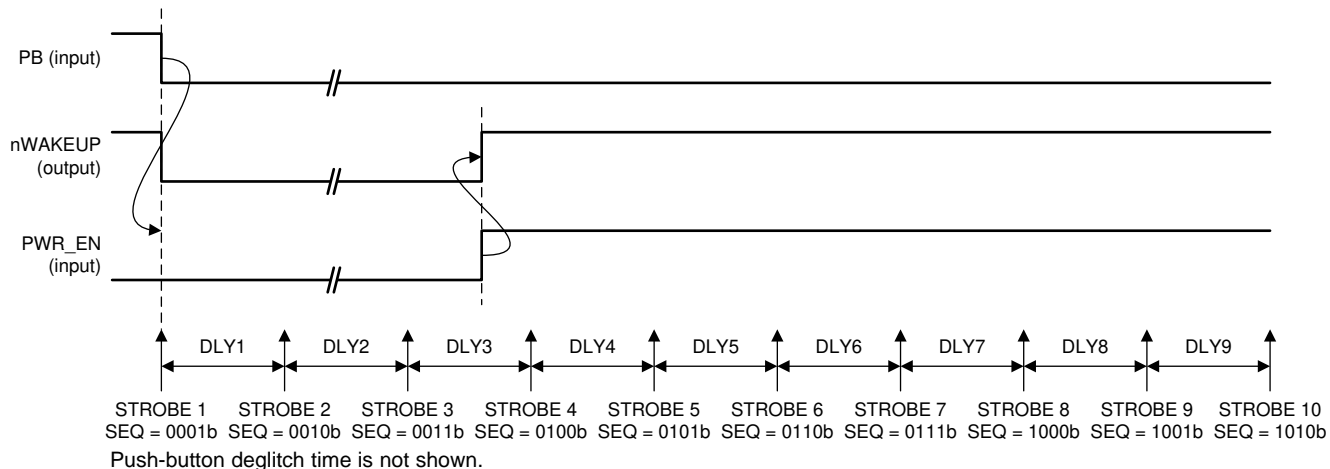
Rails not assigned to a strobe (SEQ = 0000b) are not affected by power-up and power-down sequencing and remain in their current ON or OFF state regardless of the sequencer. A rail can be enabled and disabled at any time by setting the corresponding enable bit in the ENABLEx register, with the exception that the ENABLEx register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail. For example, the sequencer sets and resets the enable bits for the rails under its control.

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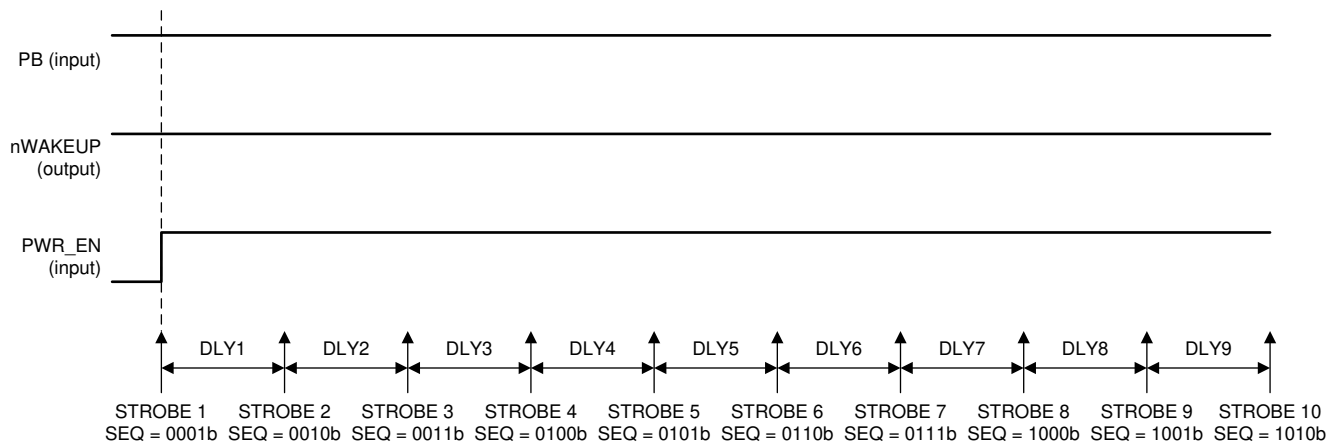
#### NOTE

The power-up sequence is defined by strobes and delay times, and can be triggered by the PB, AC\_DET (not shown, same as PB), or PWR\_EN pin.

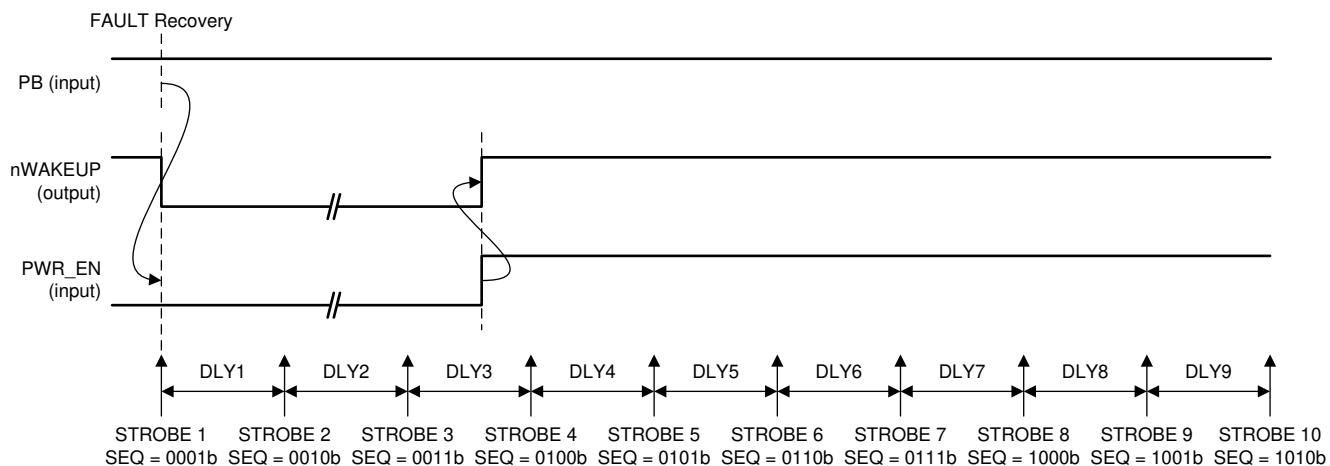
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**Figure 5-1. Power-Up Sequences from OFF or SUSPEND State; PB is Power-Up Event**



**Figure 5-2. Power-Up Sequences from SUSPEND State; PWR\_EN is Power-Up Event**



**Figure 5-3. Power-Up Sequences from RECOVERY State**

### 5.3.1.2 Power-Down Sequencing

By default, the power-down sequence follows the reverse of the power-up sequence. When the power-down sequence is triggered, STROBE 10 occurs and any rail assigned to STROBE 10 is shut down and its discharge circuit is enabled. After a delay time of DLY9, STROBE 9 occurs and any rail assigned to it is shut down and its discharge circuit is enabled. The sequence continues until all strobes occur and all DLYx times execute. The DLYx times are extended by a factor of 10x to provide ample time for discharge, and preventing output voltages from crossing during shut-down. The DLYFCTR bit is applied globally to all power-down delay times. Regardless of the DLYx and DLYFCTR settings, the PMIC enters OFF, SUSPEND, or RECOVERY state 500 ms after the power-down sequence initiates, to ensure that the discharge circuits remain enabled for a minimum of 150 ms before the next power-up sequence starts.

A power-down sequence executes if one of the following events occurs:

- The device is in the WAIT\_PWR\_EN state, the PB and AC\_DET pins are high, PWR\_EN is low, and the 20-s timer has expired.
- The device is in the ACTIVE state and the PWR\_EN pin is pulled low.
- The device is in the WAIT\_PWR\_EN, ACTIVE, or SUSPEND state and the push-button is held low for > 8 s (15 s if TRST = 1b).
- A fault occurs in the device (OTS, UVLO, PGOOD failure).

When transitioning from ACTIVE to SUSPEND state, the rails not controlled by the power-down sequencer maintains the same ON/OFF state in SUSPEND state that it had in ACTIVE state. This allows for the selected power rails to remain powered up when in the SUSPEND state.

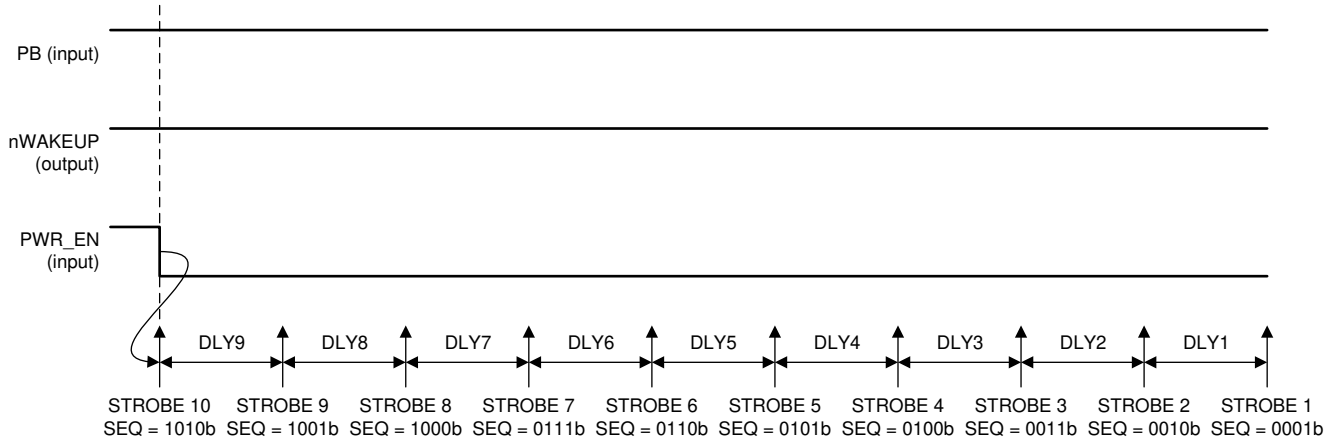
When transitioning to the OFF or RECOVERY state, rails not under sequencer control are shut-down as follows:

- DCDC1, DCDC2, DCDC3, DCDC4, , and LDO1 shut down at the beginning of the power-down sequence, if not under sequencer control (SEQ = 0b).
- LS shuts down as the state machine enters an OFF or RECOVERY state; 500 ms after the power-down sequence is triggered.

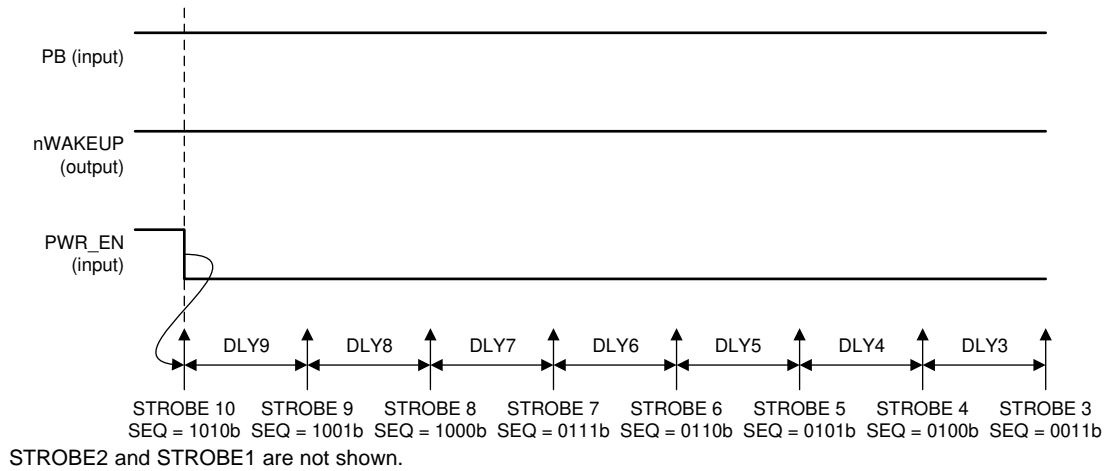
If the supply voltage on IN\_BIAS drops below 2.5 V, the digital core is reset and all power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4, and LDO1). The amount of time the discharge circuitry remains active is a function of the INT\_LDO hold up time (see [Section 5.3.1.5](#) for more details).

### 5.3.1.3 Strobe 1 and Strobe 2

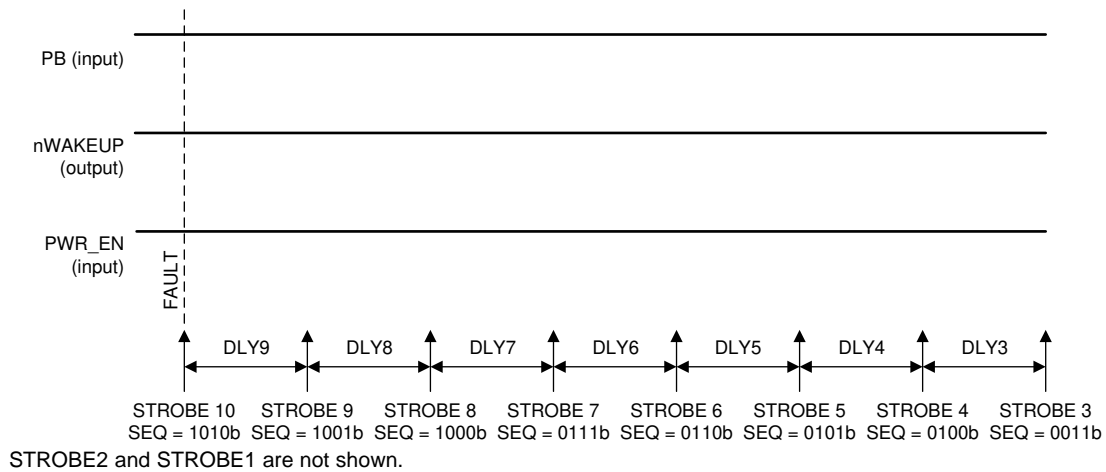
STROBE 1 and STROBE 2 are special strobes that are not used in the TPS65216 device, but STROBE 1 and STROBE 2 are still executed for power-up. The power-up sequence starts at STROBE 3 after DLY1 and DLY2 timers. The power-down sequence ends at STROBE 3.



**Figure 5-4. Power-Down Sequences to OFF State;  
PWR\_EN is Power-Down Event**



**Figure 5-5. Power-Down Sequences to SUSPEND State;  
PWR\_EN is Power-Down Event**



**Figure 5-6. Power-Down Sequences to RECOVERY State;  
TSD or UV is Power-Down Event**

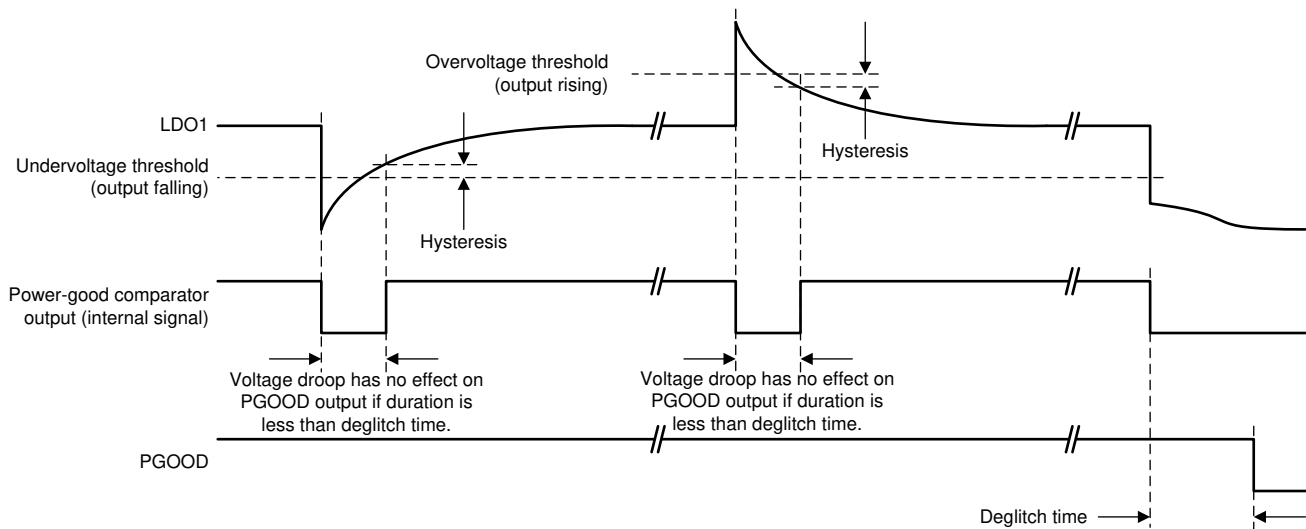
### 5.3.1.4 Supply Voltage Supervisor and Power-Good (PGOOD)

Power-good (PGOOD) is an open-drain output of the built-in voltage supervisor that monitors DCDC1, DCDC2, DCDC3, DCDC4, and LDO1. The output is Hi-Z when all enabled rails are in regulation and driven low when one or more rails encounter a fault which brings the output voltage outside the specified tolerance range. In a typical application PGOOD drives the reset signal of the SOC.

The supervisor has two modes of operation, controlled by the STRICT bit. With the STRICT bit set to 0, all enabled rails of the five regulators are monitored for undervoltage only with relaxed thresholds and deglitch times. With the STRICT bit set to 1, all enabled rails of the five regulators are monitored for undervoltage and overvoltage with tight limits and short deglitch times. Table 5-1 summarizes these details.

**Table 5-1. Supervisor Characteristics Controlled by the STRICT Bit**

PARAMETER		STRICT = 0b (TYP)	STRICT = 1b (TYP)
Undervoltage monitoring	Threshold (output falling)	90%	96.5% (DCDC1 and DCDC2) 95.5% (DCDC3, DCDC4, and LDO1)
	Deglitch (output falling)	1 ms	50 μs
	Deglitch (output rising)	10 μs	10 μs
Overvoltage monitoring	Threshold (output falling)	N/A	103.5% (DCDC1 and DCDC2) 104.5% (DCDC3, DCDC4, and LDO1)
	Deglitch (output falling)	N/A	1 ms
	Deglitch (output rising)	N/A	50 μs



**Figure 5-7. Definition of Undervoltage, Overvoltage Thresholds, Hysteresis, and Deglitch Times**

The following rules apply to the PGOOD output:

- The power-up default state for THE PGOOD is low. When all rails are disabled, the PGOOD output is driven low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5 ms after the rail is enabled and is continuously monitored thereafter. This allows the rail to power-up.
- The PGOOD is delayed by PGDLY time after the sequencer is finished and the last rail is enabled.
- If an enabled rail is continuously outside the monitoring threshold for longer than the deglitch time, then the PGOOD is pulled low, and all rails are shut-down following the power-down sequence. PGDLY does not apply.



- Disabling a rail manually by resetting the DCx\_EN or LDO1\_EN bit has no effect on the PGOOD pin. If all rails are disabled, the PGOOD is driven low as the last rail is disabled.
- If the power-down sequencer is triggered, PGOOD is driven low.
- The PGOOD is driven low in the SUSPEND state, regardless of the number of rails that are enabled.

Figure 5-8 shows a typical power-up sequence and PGOOD timing.

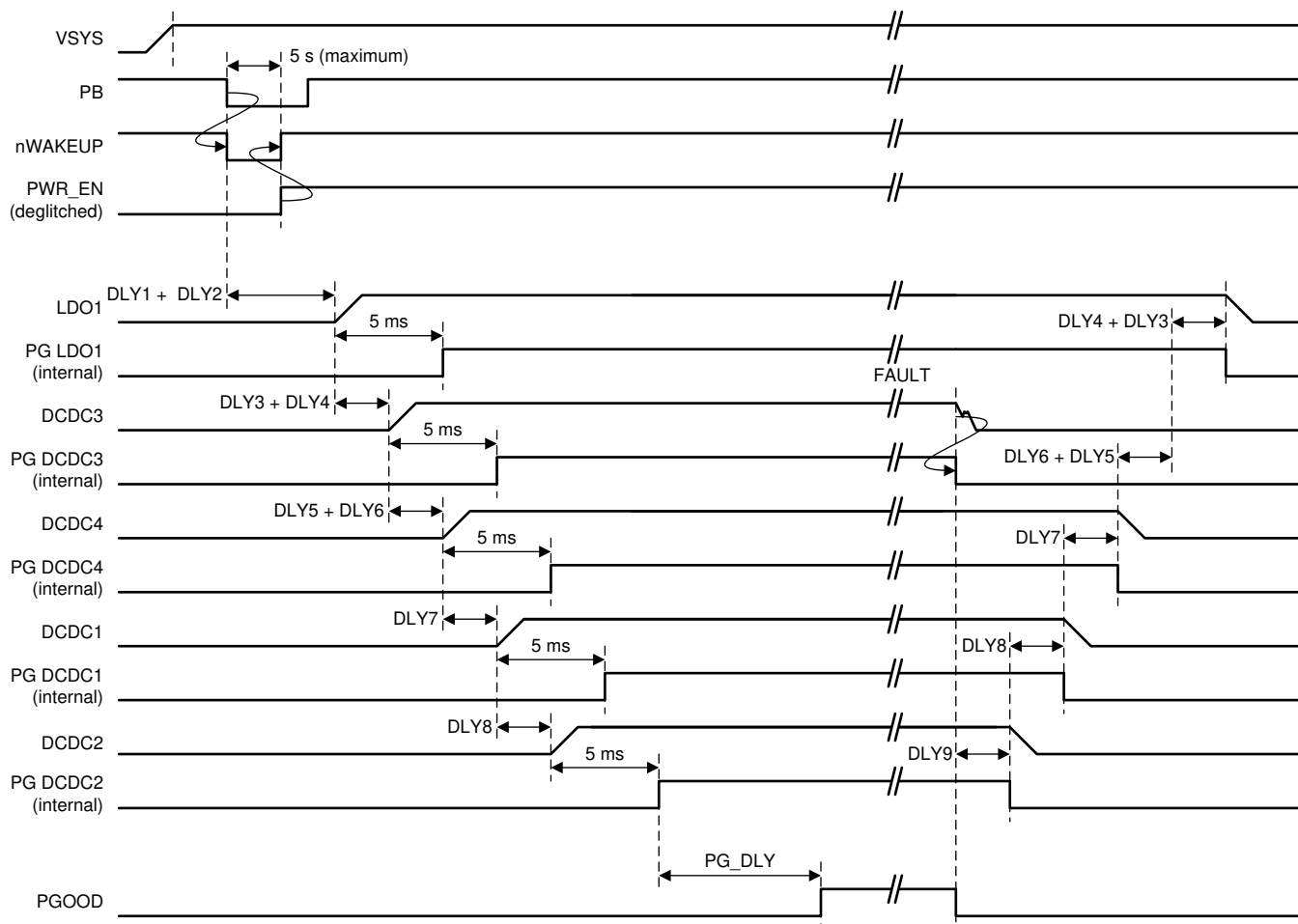


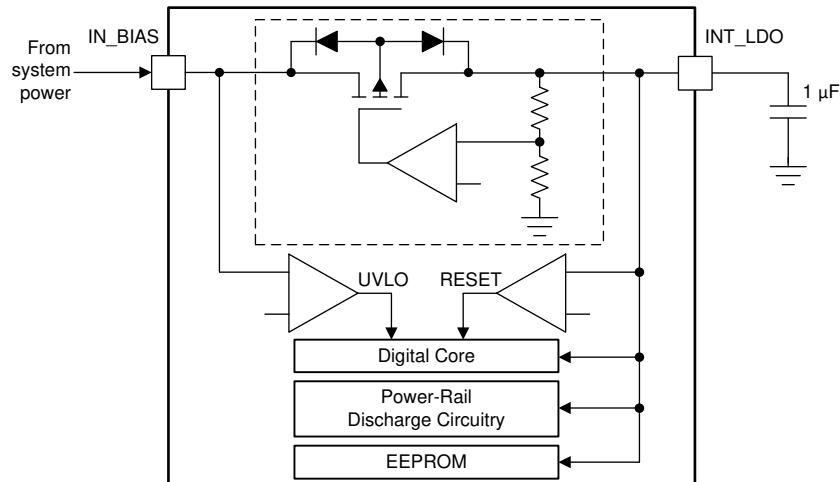
Figure 5-8. Typical Power-Up Sequence of the Main Output Rails

### 5.3.1.5 Internal LDO (INT\_LDO)

The internal LDO provides a regulated voltage to the internal digital core and analog circuitry. The internal LDO has a nominal output voltage of 2.5 V and can support up to 10 mA of external load.

When system power fails, the UVLO comparator triggers the power-down sequence. If system power drops below , the digital core is reset and all remaining power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4 and LDO1).

The internal LDO reverse blocks to prevent the discharging of the output capacitor ( $C_{INT\_LDO}$ ) on the INT\_LDO pin. The remaining charge on the INT\_LDO output capacitor provides a supply for the power rail discharge circuitry to ensure the outputs are discharged to ground even if the system supply has failed. The amount of hold-up time specified in Section 4.5 is a function of the output capacitor value ( $C_{INT\_LDO}$ ) and the amount of external load on the INT\_LDO pin, if any. The design allows for enough hold-up time to sufficiently discharge DCDC1-4, and LDO1 to ensure proper processor power-down sequencing.



**Figure 5-9. Internal LDO and UVLO Sensing**

### 5.3.1.6 Current Limited Load Switch

The TPS65216 provides a current limited load switch with individual enable control. The load switch provides the following control and diagnostic features:

- The ON or OFF state of the switch is controlled by the corresponding LS\_EN bit in the ENABLE register.
- The load switch can only be controlled through I<sup>2</sup>C communication. The sequencer has no control over the load switch.
- The load switch has an active discharge function, disabled by default, and enabled through the LSDCHRG bit. When enabled, the switch output is discharged to ground whenever the switch is disabled.
- When the PFI input drops below the power-fail threshold (the power-fail comparator trips), the load switch is automatically disabled to shed system load. This function must be individually through the corresponding LSnPFO bit. The switch does not turn back on automatically as the system voltage recovers, and must be manually re-enabled.
- An interrupt (LS\_I) issues whenever the load switch actively limits the output current, such as when the output load exceeds the current limit value. The switch remains ON and provides current to the load according to the current-limit setting.
- The load switch has a local overtemperature sensor which disables the switch if the power dissipation and junction temperature exceeds safe operating value. The switch automatically recovers once the temperature drops below the OTS threshold value minus hysteresis. The LS\_F (fault) interrupt bit is set while the switch is held OFF by the OTS function.

The load switch (LS) is a non-reverse blocking, medium-voltage (< 10 V), low-impedance switch that can be used to provide 1.8-V to 10-V power to an auxiliary port. LS has four selectable current limit values that are selectable through LSILIM[1:0].

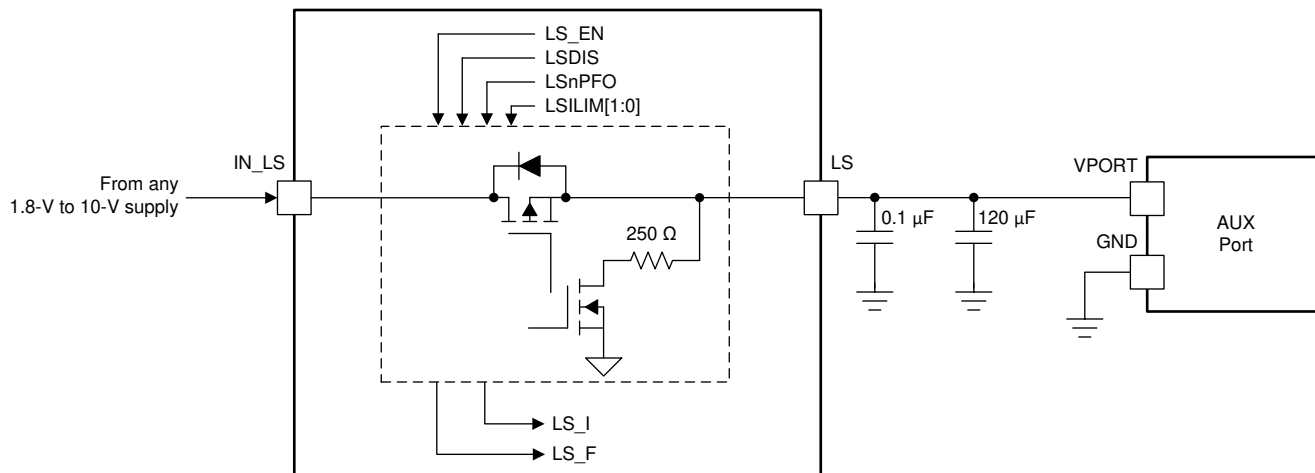


Figure 5-10. Typical Application of Load Switch

### 5.3.1.7 LDO1

LDO1 is a general-purpose LDO intended to provide power to analog circuitry on the SOC. LDO1 has an input voltage range from 1.8 V to 5.5 V, and can be connected either directly to the system power or the output of a DCDC converter. The output voltage is programmable in the range of 0.9 V to 3.4 V with a default of 1.8 V. LDO1 supports up to 200 mA at the minimum specified headroom voltage, and up to 400 mA at the typical operating condition of  $V_{OUT} = 1.8\text{ V}$ ,  $V_{IN\_LDO1} > 2.7\text{ V}$ .

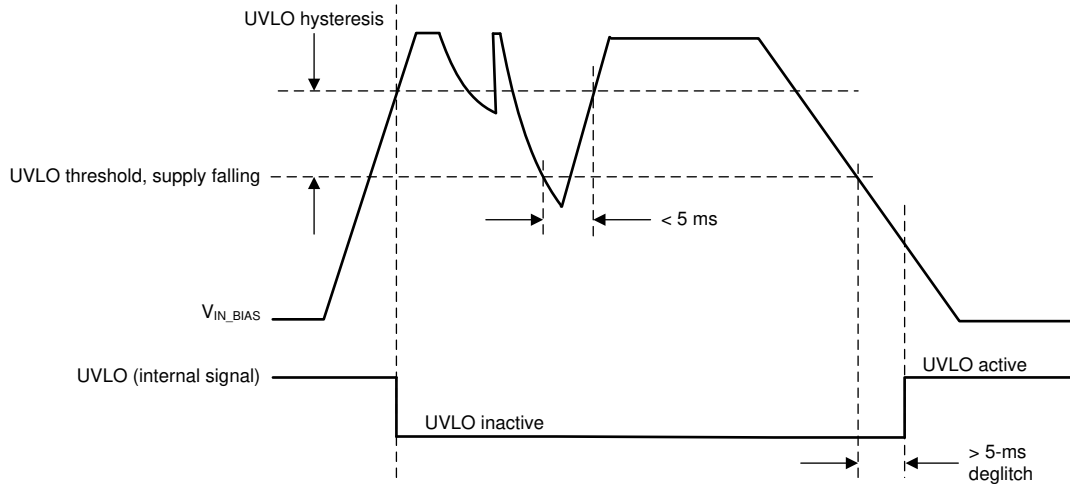
### 5.3.1.8 UVLO

Depending on the slew rate of the input voltage into the IN\_BIAS pin, the power rails of TPS65216 will be enabled at either  $V_{ULVO}$  or  $V_{ULVO} + V_{HYS}$ .

If the slew rate of the IN\_BIAS voltage is greater than 30 V/s, then TPS65216 will power up at  $V_{ULVO}$ . Once the input voltage rises above this level, the input voltage may drop to the  $V_{ULVO}$  level before the PMIC shuts down. In this scenario, if the input voltage were to fall below  $V_{ULVO}$  but above 2.55 V, the input voltage would have to recover above  $V_{ULVO}$  in less than 5 ms for the device to remain active.

If the slew rate of the IN\_BIAS voltage is less than 30 V/s, then TPS65216 will power up at  $V_{ULVO} + V_{HYS}$ . Once the input voltage rises above this level, the input voltage may drop to the  $V_{ULVO}$  level before the PMIC shuts down. In this scenario, if the input voltage were to fall below  $V_{ULVO}$  but above 2.5 V, the input voltage would have to recover above  $V_{ULVO} + V_{HYS}$  in less than 5 ms for the device to remain active.

In either slew rate scenario, if the input voltage were to fall below 2.5 V, the digital core is reset and all remaining power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4 and LDO1).



**Figure 5-11. Definition of UVLO and Hysteresis**

After the UVLO triggers, the internal LDO blocks current flow from its output capacitor back to the IN\_BIAS pin, allowing the digital core and the discharge circuits to remain powered for a limited amount of time to properly shut-down and discharge the output rails. The hold-up time is determined by the value of the capacitor connected to INT\_LDO. See [Section 5.3.1.5](#) for more details.

### 5.3.1.9 Power-Fail Comparator

The power-fail comparator notifies the system host if the system supply voltage drops and the system is at risk of shutting down. The comparator has an internal 800-mV threshold and the trip-point is adjusted by an external resistor divider.

By default, the power-fail comparator has no impact on any of the power rails or the load switch. The load switch can be configured to be disabled when the PFI comparator trips to shed system load and extend hold-up time. The power-fail comparator also triggers the power-down sequencer, such that all or selective rails power-down when the system voltage fails. To tie the power-fail comparator into the power-down sequence, the OFFnPFO bit in the CONTROL register must be set to 1.

The power-fail comparator cannot be monitored by software, such that no interrupt or status bit is associated to this function.

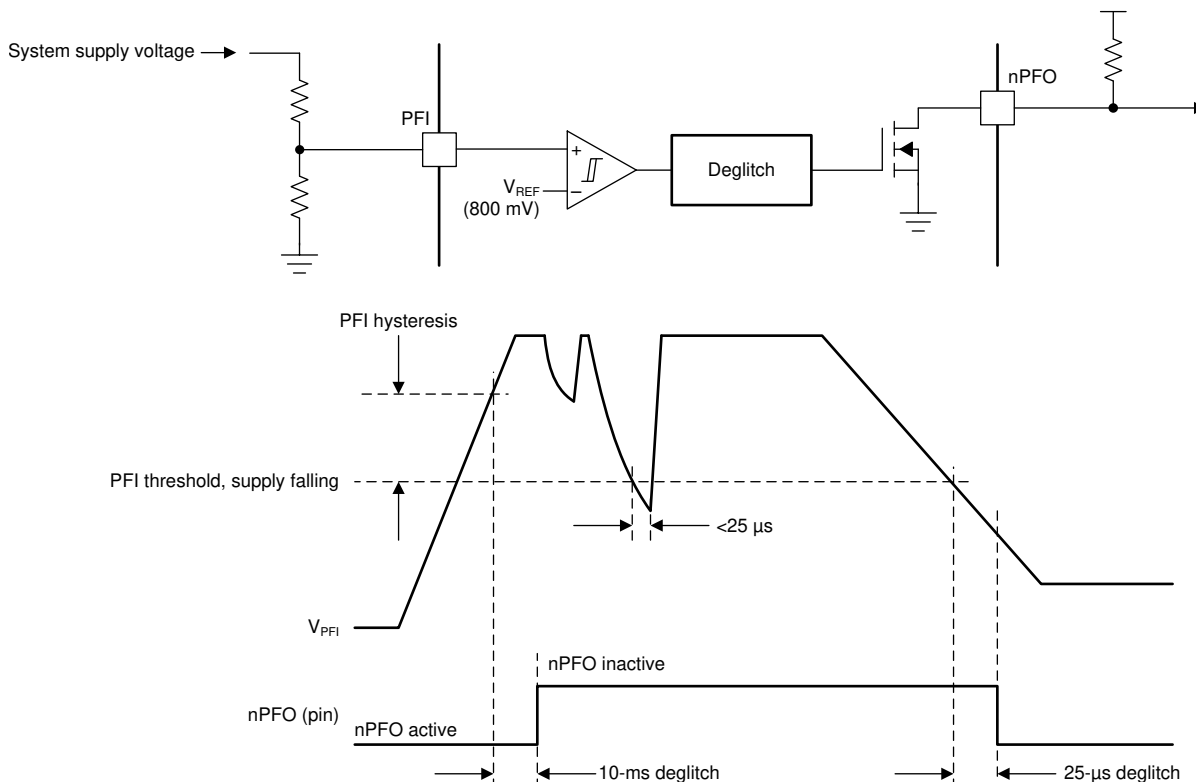


Figure 5-12. Power-Fail Comparator Simplified Circuit and Timing Diagram

### 5.3.1.10 DCDC3 and DCDC4 Power-Up Default Selection

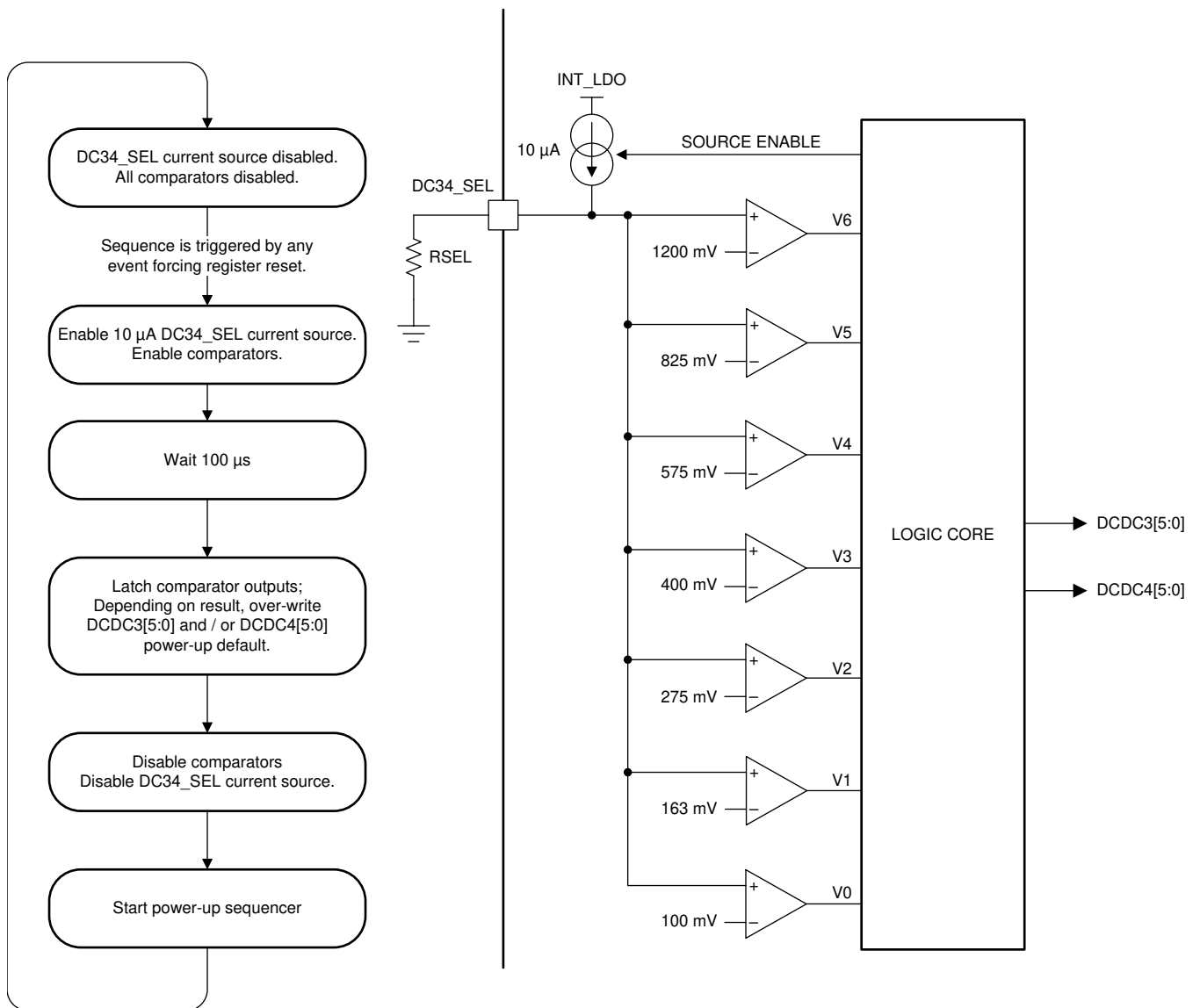


Figure 5-13. Left: Flow Chart for Selecting DCDC Power-Up Default Voltage  
Right: Comparator Circuit

Table 5-2. Power-Up Default Values of DCDC3 and DCDC4

RSEL [KΩ]			POWER-UP DEFAULT	
MIN	TYP	MAX	DCDC3[5:0]	DCDC4[5:0]
0	0	7.7	Programmed default (1.2 V)	Programmed default (3.3 V)
	12.1		0x12 (1.35 V)	Programmed default (3.3 V)
	20		0x18 (1.5 V)	Programmed default (3.3 V)
30.9	31.6	32.3	0x1F (1.8 V)	Programmed default (3.3 V)
	45.3		0x3D (3.3 V)	0x01 (1.2 V)
			Programmed default (1.2 V)	0x07 (1.35 V)
	95.3		Programmed default (1.2 V)	0x0D (1.5 V)
	150	Tied to INT_LDO	Programmed default (1.2 V)	0x14 (1.8 V)

### 5.3.1.11 I/O Configuration

The device has two GPIO pins, which are configured as follows:

- GPIO1:
  - General-purpose, open-drain output is controlled by the GPO1 user bit or sequencer.
- GPIO2:
  - General-purpose, open-drain output id controlled by the GPO2 user bit or sequencer.
  - Reset input-signal for DCDC1 and DCDC2.

**Table 5-3. GPIO1 Configuration**

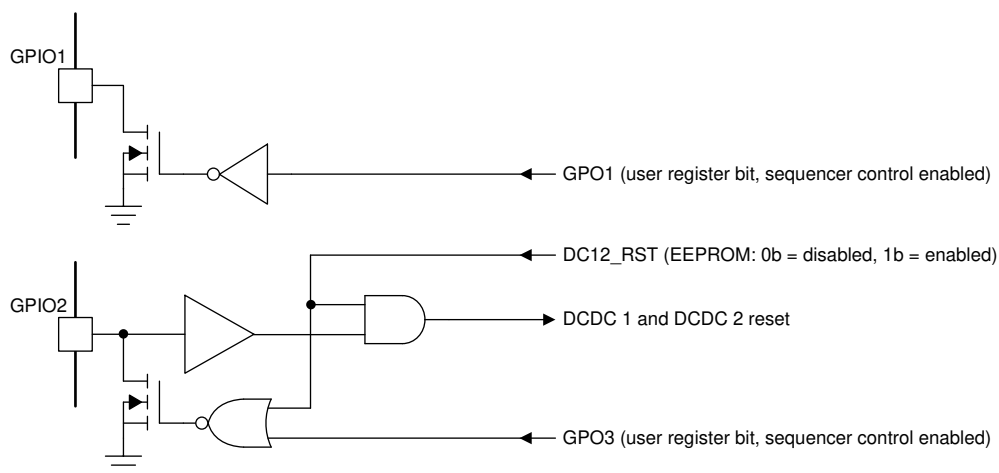
GPO1 (USER BIT)	GPIO1 (I/O PIN)	COMMENTS
0	0	Open-drain output, driving low
1	HiZ	Open-drain output, HiZ

**Table 5-4. GPIO2 Configuration**

DC12_RST (EEPROM)	GPO2 (USER BIT)	GPIO2 (I/O PIN)	COMMENTS
0	0	0	Open-drain output, driving low
0	1	HiZ	Open-drain output, HiZ
1	X	Active low	GPIO2 is DCDC1 and DCDC2 reset input signal to PMIC (active low). See <a href="#">Section 5.3.1.11.1</a> for details.

#### 5.3.1.11.1 Using GPIO2 as Reset Signal to DCDC1 and DCDC2

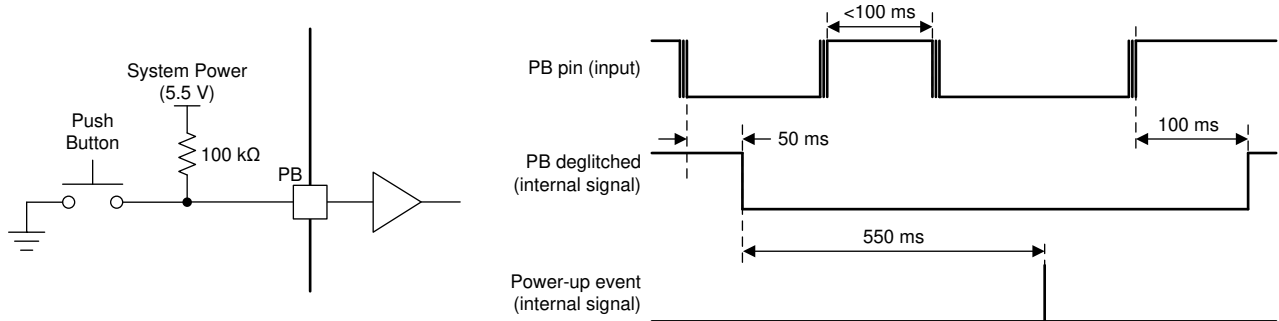
The GPIO2 is an edge-sensitive reset input to the PMIC, when the DC12\_RST bit set to 1. The reset signal affects DCDC1 and DCDC2 only, so that only those two registers are reset to the power-up default whenever GPIO2 input transitions from high to low, while all other registers maintain their current values. DCDC1 and DCDC2 transition back to the default value following the SLEW settings, and are not power cycled. This function recovers the processor from reset events while in low-power mode.



**Figure 5-14. I/O Pin Logic**

### 5.3.1.12 Push Button Input (PB)

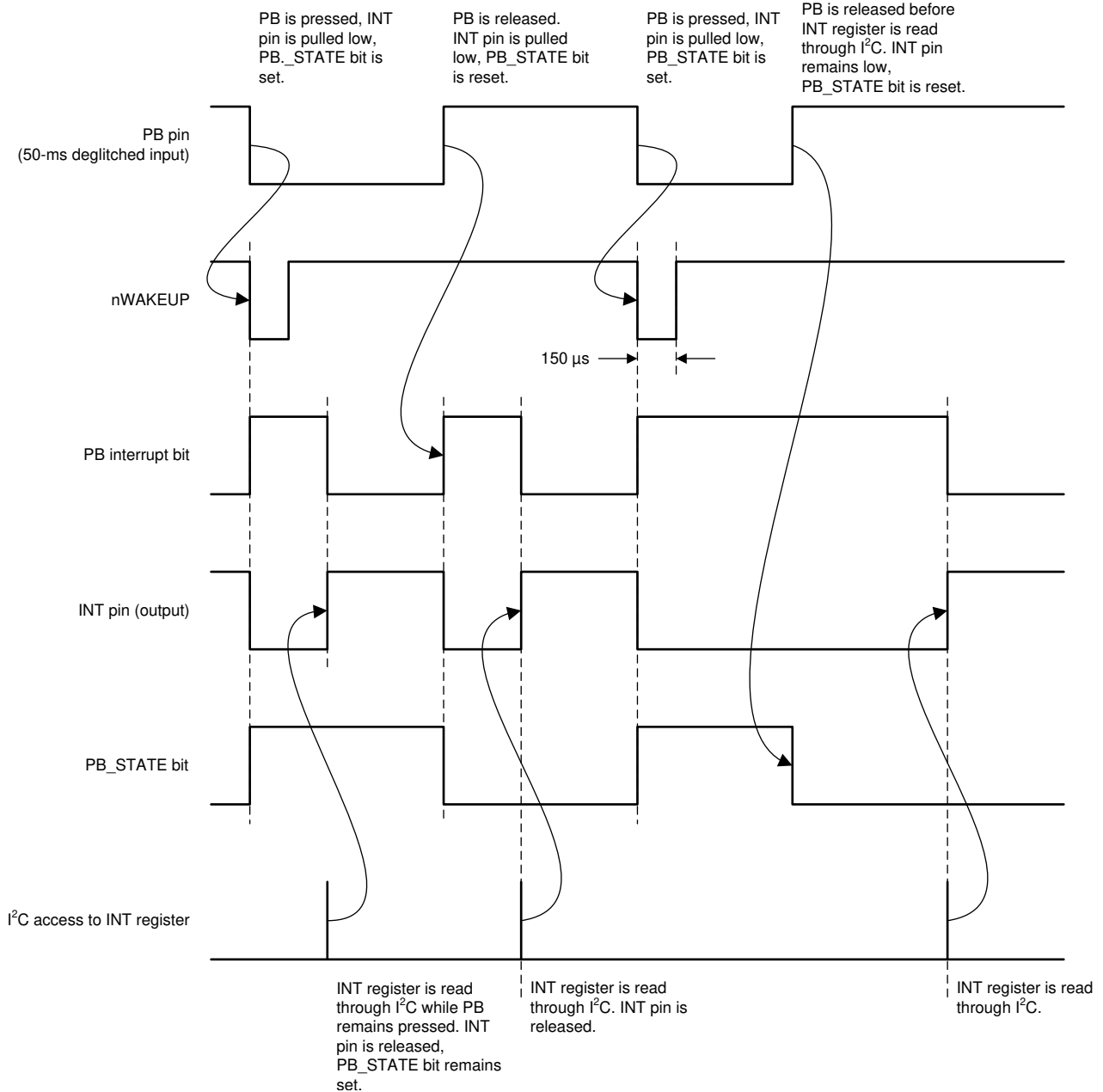
The PB pin is a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor. The power-up sequence is triggered if the PB input is held low for 600 ms.



**Figure 5-15. Left: Typical PB Input Circuit  
Right: Push-Button Input (PB) Deglitch and Power-Up Timing**

In ACTIVE mode, the TPS65216 monitors the PB input and issues an interrupt when the pin status changes, such as when it drops below or rises above the PB input-low or input-high thresholds. The interrupt is masked by the PBM bit in the INT\_MASK1 register.





**Figure 5-16. PB Input-Low or Input-High Thresholds**

**NOTE**

Interrupts are issued whenever the PB pin status changes. The PB\_STATE bit reflects the current status of the PB input. nWAKEUP is pulled low for 150 μs on every falling edge of PB.

### 5.3.1.12.1 Signaling PB-Low Event on the nWAKEUP Pin

In ACTIVE state, the nWAKEUP pin is pulled low for five 32-kHz clock cycles (approximately 150  $\mu$ s) whenever a falling edge on the PB input is detected. This allows the host processor to wakeup from DEEP SLEEP mode of operation. It is recommended to pull-up the nWAKEUP pin to a I/O power supply through a pull-up resistor. For nWAKEUP to function properly in the SUSPEND state, this pin must be pulled up to a power supply that is disconnected from the sequencer before entering SUSPEND. .

### 5.3.1.12.2 Push Button Reset

If the PB input is pulled low for 8 s (15 s if TRST = 1b) or longer, then all rails are disabled, and the device enters the RECOVERY state. The device powers up automatically after the 500 ms power-down sequence is complete, regardless of the state of the PB input. Holding the PB pin low for 8 s (15 s if TRST = 1b), only turns off the device temporarily and forces a system restart, and is not a power-down function. If the PB is held low continuously, the device power-cycles in 8-s and 15-s intervals.

### 5.3.1.13 AC\_DET Input (AC\_DET)

The AC\_DET pin is a CMOS-type input used in three different ways to control the power-up of the PMIC:

- In a battery operated system, AC\_DET is typically connected to an external battery charger with an open-drain power-good output pulled low when a valid charger supply is connected to the system. A falling edge on the AC\_DET pin causes the PMIC to power up.
- In a non-portable system, the AC\_DET pin may be shorted to ground and the device powers up whenever system power is applied to the chip.
- If none of the above behaviors are desired, AC\_DET may be tied to system power (IN\_BIAS). Power-up is then controlled through the push-button input or PWR\_EN input.

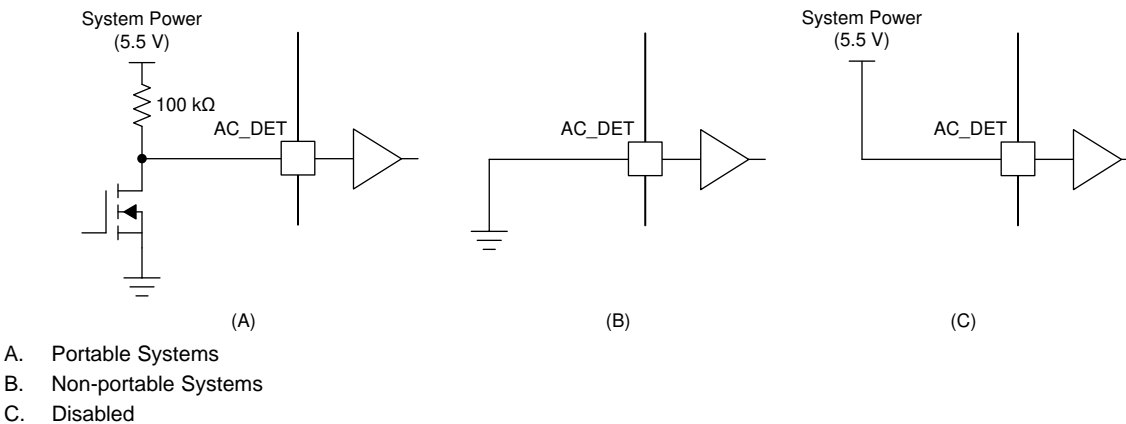


Figure 5-17. AC\_DET Pin Configurations

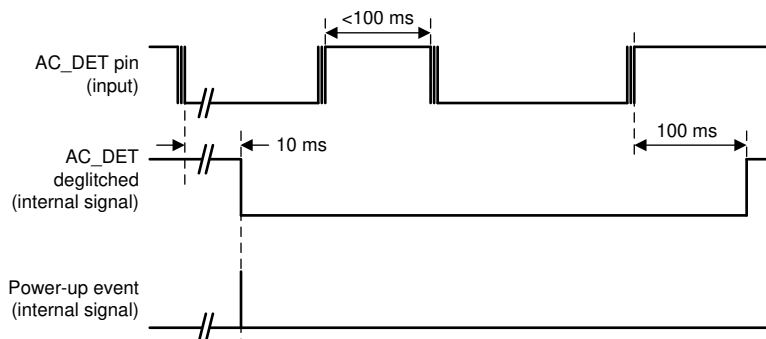


Figure 5-18. AC\_DET Input Deglitch and Power-Up Timing (Portable Systems)

In ACTIVE state, the TPS65216 monitors the AC\_DET input and issues an interrupt when the pin status changes, such as when it drops below or rises above the AC\_DET input-low or input-high thresholds. The interrupt is masked by the ACM bit in the INT\_MASK1 register.

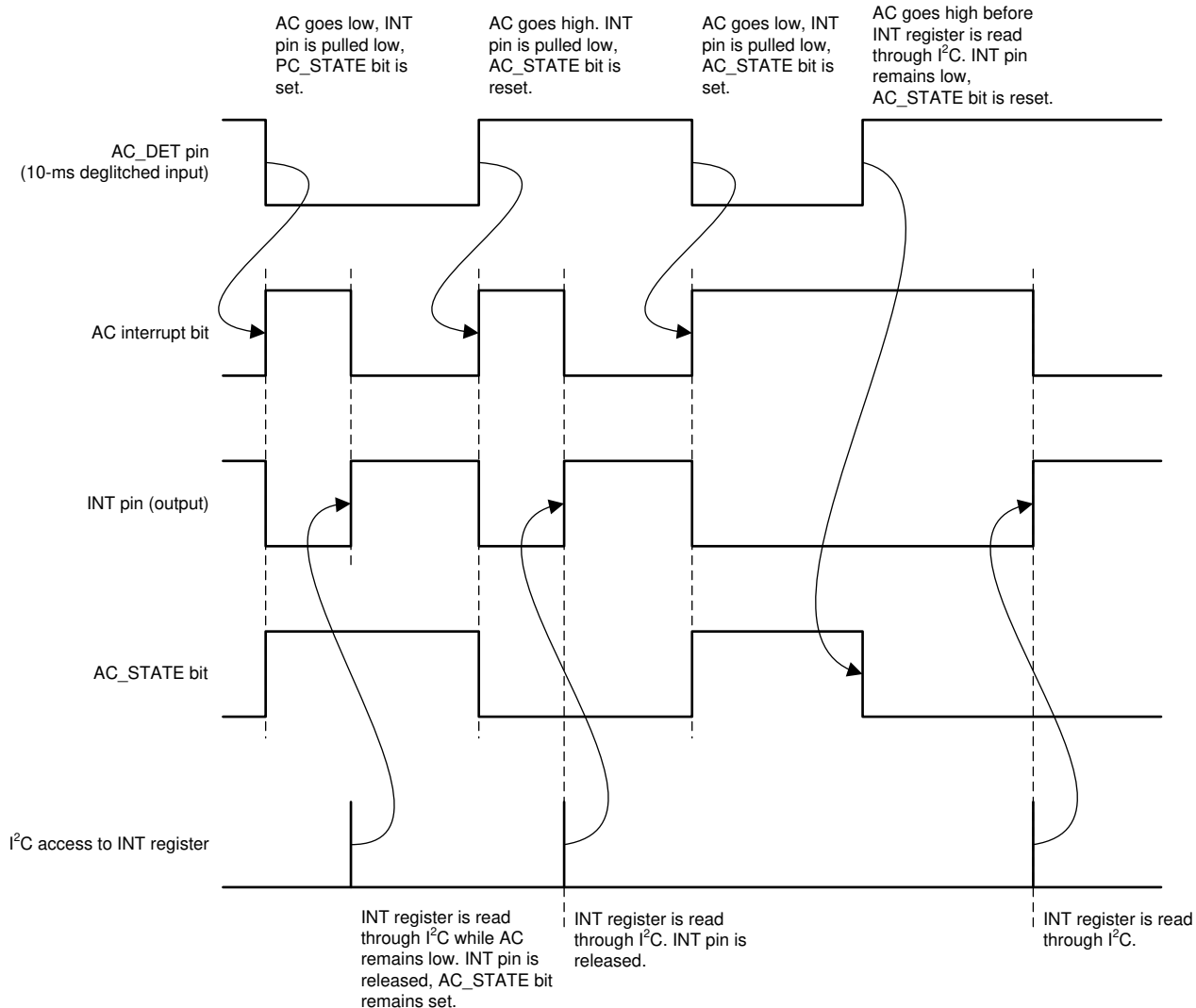


Figure 5-19. AC\_STATE Pin

**NOTE**

Interrupts are issued whenever the AC\_DET pin status changes. The AC\_STATE bit reflects the current status of the AC\_DET input.

**5.3.1.14 Interrupt Pin (INT)**

The interrupt pin signals any event or fault condition to the host processor. Whenever a fault or event occurs in the device, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INT pin is released (returns to Hi-Z state) and fault bits are cleared when the host reads the INT register. If a failure persists, the corresponding INT bit remains set and the INT pin is pulled low again after a maximum of 32  $\mu$ s.

The MASK register masks events from generating interrupts. The MASK settings affect the INT pin only, and have no impact on the protection and monitor circuits.

### 5.3.1.15 I<sup>2</sup>C Bus Operation

The TPS65216 hosts a slave I<sup>2</sup>C interface (address 0x24) that supports data rates up to 400 kbps, auto-increment addressing. <sup>(1)</sup>

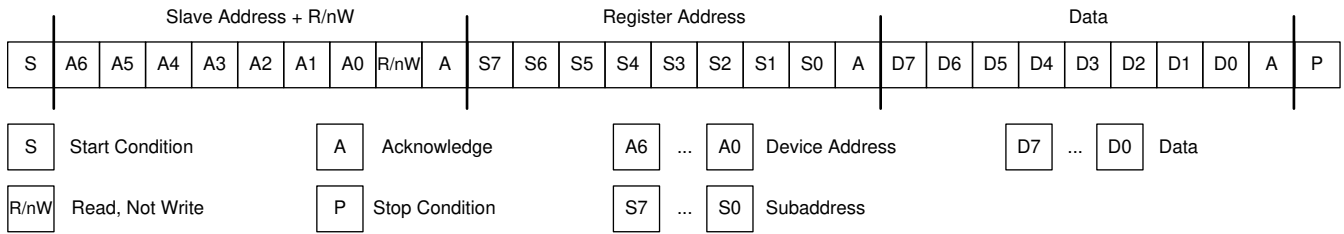


Figure 5-20. Subaddress in I<sup>2</sup>C Transmission

The I<sup>2</sup>C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission initiates with a start bit from the controller as shown in Figure 5-22. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and checks for valid address and control information. If the appropriate slave address is set for the device, the device issues an acknowledge pulse and prepares to receive register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge issues after the reception of valid slave address, register-address, and data words. The I<sup>2</sup>C interfaces an auto-sequence through the register addresses, so that multiple data words can be sent for a given I<sup>2</sup>C transmission. Reference Figure 5-21 and Figure 5-22 for details.

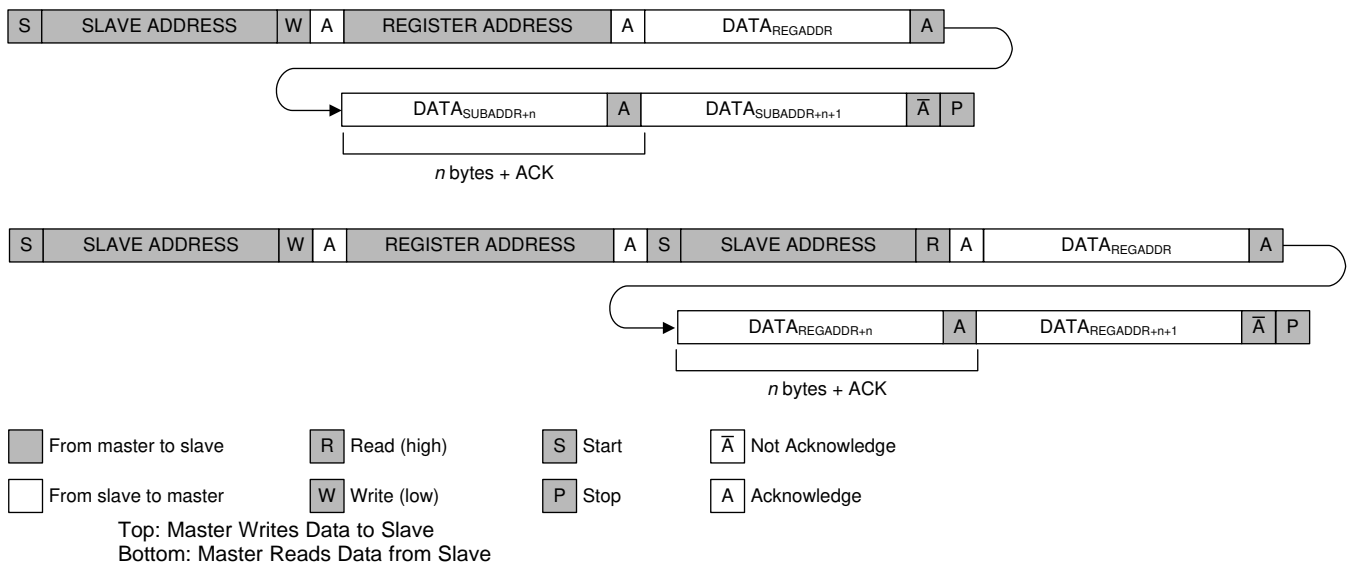
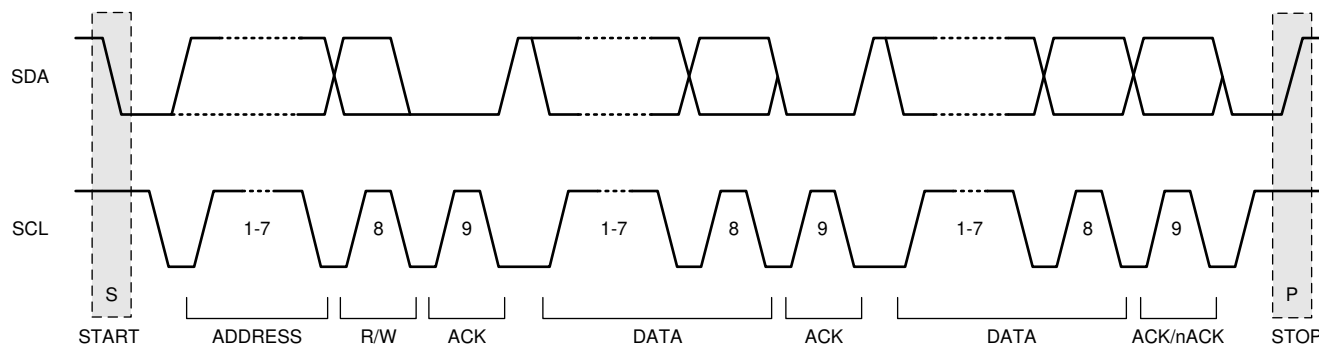
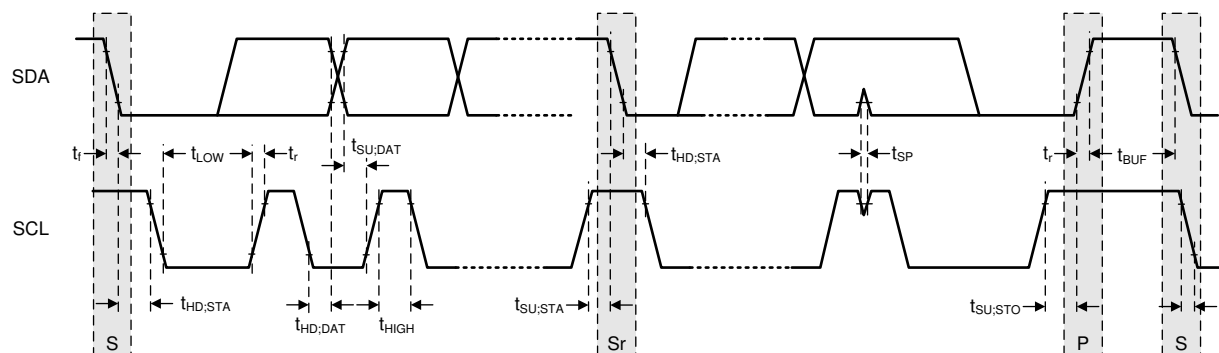


Figure 5-21. I<sup>2</sup>C Data Protocol

(1) Note: The SCL duty cycle at 400 kHz must be >40%.



**Figure 5-22. I<sup>2</sup>C Protocol and Transmission Timing**  
**I<sup>2</sup>C Start Stop and Acknowledge Protocol**



**Figure 5-23. I<sup>2</sup>C Protocol and Transmission Timing**  
**I<sup>2</sup>C Data Transmission Timing**

## 5.4 Device Functional Modes

### 5.4.1 Modes of Operation

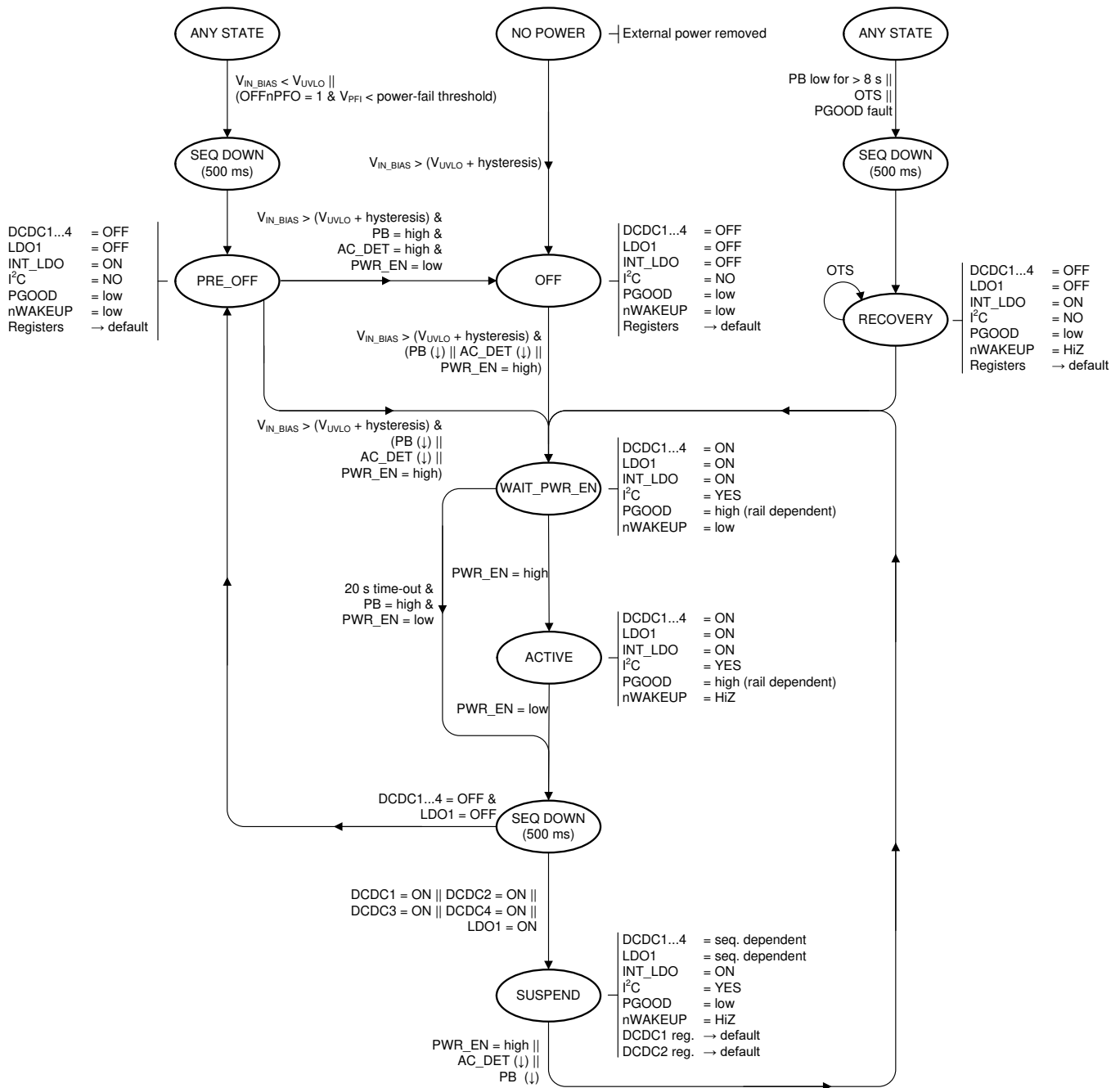


Figure 5-24. Modes of Operation Diagram

#### 5.4.2 OFF

In OFF mode, the PMIC is completely shut down with the exception of a few circuits to monitor the AC\_DET, PWR\_EN, and PB input. All power rails are turned off and the registers are reset to their default values. The I<sup>2</sup>C communication interface is turned off. This is the lowest-power mode of operation. To exit OFF mode  $V_{IN\_BIAS}$  must exceed the UVLO threshold and one of the following wake-up events must occur:

- The PB input is pulled low.

- THE AC\_DET input is pulled low.
- The PWR\_EN input is pulled high.

To enter OFF state, ensure that all power rails are assigned to the sequencer, then pull the PWR\_EN pin low. Additionally, if the OFFnPFO bit is set to 1b and the PFI input falls below the power fail threshold the device transitions to the OFF state. If a PGOOD or OTS fault occurs while in the ACTIVE state, TPS65216 will transition to the RESET state.

### 5.4.3 ACTIVE

This is the typical mode of operation when the system is up and running. All DCDC converters, LDOs, and load switch are operational and can be controlled through the I<sup>2</sup>C interface. After a wake-up event, the PMIC enables all rails controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device only enters ACTIVE state if the host asserts the PWR\_EN pin within 20 s after the wake-up event. Otherwise it will enter OFF state. The nWAKEUP pin returns to HiZ mode after the PWR\_EN pin is asserted. ACTIVE state can also be directly entered from SUSPEND state by pulling the PWR\_EN pin high. See SUSPEND state description for details. To exit ACTIVE mode, the PWR\_EN pin must be pulled low.

### 5.4.4 SUSPEND

SUSPEND state is a low-power mode of operation intended to support system standby. Typically all power rails are turned off with the exception of any rail with an SEQ register set to 0h. To enter SUSPEND state, pull the PWR\_EN pin low. All power rails controlled by the power-down sequencer are shut down, and after 500 ms the device enters SUSPEND state. All rails not controlled by the power-down sequencer will maintain state. Note that all register values are reset as the device enters the SUSPEND state. The device enters ACTIVE state after it detects a wake-up event as described in the previous sections.

### 5.4.5 RESET

The TPS65216 can be reset by holding the PB pin low for more than 8 or 15 s, depending on the value of the TRST bit. All rails are shut down by the sequencer and all register values reset to their default values. Rails not controlled by the sequencer are shut down additionally. Note that the RESET function power-cycles the device and only temporarily shuts down the output rails. Resetting the device does not lead to OFF state. If the PB\_IN pin is kept low for an extended amount of time, the device continues to cycle between ACTIVE and RESET state, entering RESET every 8 or 15 s.

The device is also reset if a PGOOD or OTS fault occurs. The TPS65216 remains in the recovery state until the fault is removed, at which time it transitions back to the ACTIVE state.

## 5.5 Register Maps

### 5.5.1 Password Protection

Registers 0x11h through 0x26h are protected against accidental write by a 8-bit password. The password must be written prior to writing to a protected register and automatically resets to 0x00h after the next I<sup>2</sup>C transaction, regardless of the register accessed or transaction type (read or write). The password is required for write access only and is not required for read access.

To write to a protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh), to the PASSWORD register (0x10h).
2. Write the data to the password protected register.
3. If the content of the PASSWORD register is XORed, with an address send that matches 0x7Dh, then the data transfers to the protected register. Otherwise, the transaction is ignored. In either case the PASSWORD register resets to 0x00 after the transaction.

The cycle must be repeated for any other register that is Level1 write protected.

### 5.5.2 FLAG Register

The FLAG register contains a bit for each power rail and GPO to keep track of the enable state of the rails while the system is suspended. The following rules apply to the FLAG register:

- The power-up default value for any flag bit is 0.
- Flag bits are read-only and cannot be written to.
- Upon entering a SUSPEND state, the flag bits are set to same value as their corresponding ENABLE bits. Rails and GPOs enabled in a SUSPEND state have flag bits set to 1, while all other flag bits are set to 0. Flag bits are not updated while in the SUSPEND state or when exiting the SUSPEND state.
- The FLAG register is static in WAIT\_PWR\_EN and ACTIVE state. The FLAG register reflects the enable state of DCDC1, DCDC2, DCDC3, DCDC4, and LDO1; and, reflects the enable state of GPO1, GPO2, and GPO3 during the last SUSPEND state.

The host processor reads the FLAG register to determine if the system powered up from the OFF or SUSPEND state. In the SUSPEND state, typically the DDR memory is kept in self refresh mode and therefore the DC3\_FLG or DC4\_FLG bits are set.



### 5.5.3 TPS65216 Registers

Table 5-5 lists the memory-mapped registers for the TPS65216. All register offset addresses not listed in Table 5-5 should be considered as reserved locations and the register contents should not be modified.

**Table 5-5. TPS65216 Registers**

SUBADDRESS	ACRONYM	REGISTER NAME	R/W	PASSWORD PROTECTED	SECTION
0x00	CHIPID	CHIP ID	R	No	<a href="#">Go</a>
0x01	INT1	INTERRUPT 1	R	No	<a href="#">Go</a>
0x02	INT2	INTERRUPT 2	R	No	<a href="#">Go</a>
0x03	INT_MASK1	INTERRUPT MASK 1	R/W	No	<a href="#">Go</a>
0x04	INT_MASK2	INTERRUPT MASK 2	R/W	No	<a href="#">Go</a>
0x05	STATUS	STATUS	R	No	<a href="#">Go</a>
0x06	CONTROL	CONTROL	R/W	No	<a href="#">Go</a>
0x07	FLAG	FLAG	R	No	<a href="#">Go</a>
0x10	PASSWORD	PASSWORD	R/W	No	<a href="#">Go</a>
0x11	ENABLE1	ENABLE 1	R/W	Yes	<a href="#">Go</a>
0x12	ENABLE2	ENABLE 2	R/W	Yes	<a href="#">Go</a>
0x13	CONFIG1	CONFIGURATION 1	R/W	Yes	<a href="#">Go</a>
0x14	CONFIG2	CONFIGURATION 2	R/W	Yes	<a href="#">Go</a>
0x15	CONFIG3	CONFIGURATION 3	R/W	Yes	<a href="#">Go</a>
0x16	DCDC1	DCDC1 CONTROL	R/W	Yes	<a href="#">Go</a>
0x17	DCDC2	DCDC2 CONTROL	R/W	Yes	<a href="#">Go</a>
0x18	DCDC3	DCDC3 CONTROL	R/W	Yes	<a href="#">Go</a>
0x19	DCDC4	DCDC4 CONTROL	R/W	Yes	<a href="#">Go</a>
0x1A	SLEW	SLEW RATE CONTROL	R/W	Yes	<a href="#">Go</a>
0x1B	LDO1	LDO1 CONTROL	R/W	Yes	<a href="#">Go</a>
0x20	SEQ1	SEQUENCER 1	R/W	Yes	<a href="#">Go</a>
0x21	SEQ2	SEQUENCER 2	R/W	Yes	<a href="#">Go</a>
0x22	SEQ3	SEQUENCER 3	R/W	Yes	<a href="#">Go</a>
0x23	SEQ4	SEQUENCER 4	R/W	Yes	<a href="#">Go</a>
0x24	SEQ5	SEQUENCER 5	R/W	Yes	<a href="#">Go</a>
0x25	SEQ6	SEQUENCER 6	R/W	Yes	<a href="#">Go</a>
0x26	SEQ7	SEQUENCER 7	R/W	Yes	<a href="#">Go</a>

Table 5-6 explains the common abbreviations used in this section.

**Table 5-6. Common Abbreviations**

Abbreviation	Description
R	Read
W	Write
R/W	Read and write capable
E2	Backed by EEPROM
h	Hexadecimal notation of a group of bits
b	Hexadecimal notation of a bit or group of bits
X	Do not care reset value

**5.5.3.1 CHIPID Register (subaddress = 0x00) [reset = 0x05]**

CHIPID is shown in [Figure 5-25](#) and described in [Table 5-7](#).

Return to [Summary Table](#).

**Figure 5-25. CHIPID Register**

7	6	5	4	3	2	1	0
CHIP					REV		
R-0h					R-5h		

**Table 5-7. CHIPID Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	CHIP	R	0h	Chip ID: 0h = TPS65216 1h = Future use ... 1Fh = Future use
2-0	REV	R	5h	Revision code: 0h = Revision 1.0 1h = Revision 1.1 2h = Revision 2.0 3h = Revision 2.1 4h = Revision 3.0 5h = Revision 4.0 (D0) 6h = Future use 7h = Future use

### 5.5.3.2 INT1 Register (subaddress = 0x01) [reset = 0x00]

INT1 is shown in [Figure 5-26](#) and described in [Table 5-8](#).

Return to [Summary Table](#).

**Figure 5-26. INT1 Register**

7	6	5	4	3	2	1	0
RESERVED	VPRG	AC	PB	HOT	RESERVED	PRGC	
R-00b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

**Table 5-8. INT1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	VPRG	R	0b	Programming voltage interrupt: 0b = No significance. 1b = Input voltage is too low for programming power-up default values.
4	AC	R	0b	AC_DET pin status change interrupt. Note: Status information is available in STATUS register. 0b = No change in status. 1b = AC_DET status change (AC_DET pin changed high to low or low to high).
3	PB	R	0b	Push-button status change interrupt. Note: Status information is available in STATUS register 0b = No change in status. 1b = Push-button status change (PB changed high to low or low to high).
2	HOT	R	0b	Thermal shutdown early warning: 0b = Chip temperature is below HOT threshold. 1b = Chip temperature exceeds HOT threshold.
1	RESERVED	R	0b	
0	PRGC	R	0b	EEPROM programming complete interrupt: 0b = No significance. 1b = Programming of power-up default settings has completed successfully.

### 5.5.3.3 INT2 Register (subaddress = 0x02) [reset = 0x00]

INT2 is shown in [Figure 5-27](#) and described in [Table 5-9](#).

Return to [Summary Table](#).

**Figure 5-27. INT2 Register**

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LS_F	RESERVED	RESERVED	LS_I	RESERVED	RESERVED
R-00b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

**Table 5-9. INT2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LS_F	R	0b	Load switch fault interrupt: 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit and is temporarily disabled.
4	RESERVED	R	0b	
3	RESERVED	R	0b	
2	LS_I	R	0b	Load switch current-limit interrupt: 0b = Load switch is disabled or not in current limit. 1b = Load switch is actively limiting the output current (output load is exceeding current limit value).
1	RESERVED	R	0b	
0	RESERVED	R	0b	

### 5.5.3.4 INT\_MASK1 Register (subaddress = 0x03) [reset = 0x00]

INT\_MASK1 is shown in [Figure 5-28](#) and described in [Table 5-10](#).

Return to [Summary Table](#).

**Figure 5-28. INT\_MASK1 Register**

7	6	5	4	3	2	1	0
RESERVED	VPRGM	ACM	PBM	HOTM	RESERVED	PRGCM	
R-00b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-10. INT\_MASK1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	VPRGM	R/W	0b	Programming voltage interrupt mask bit. Note: mask bit has no effect on monitoring function: 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
4	ACM	R/W	0b	AC_DET interrupt masking bit: 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin). Note: mask bit has no effect on monitoring function.
3	PBM	R/W	0b	PB interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
2	HOTM	R/W	0b	HOT interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
1	RESERVED	R/W	0b	
0	PRGCM	R/W	0b	PRGC interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).

### 5.5.3.5 INT\_MASK2 Register (subaddress = 0x04) [reset = 0x00]

INT\_MASK2 is shown in [Figure 5-29](#) and described in [Table 5-11](#).

Return to [Summary Table](#).

**Figure 5-29. INT\_MASK2 Register**

7	6	5	4	3	2	1	0
RESERVED	LS_FM	RESERVED	RESERVED	LS_IM	RESERVED	RESERVED	
R-00b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-11. INT\_MASK2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LS_FM	R/W	0b	LS fault interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
4	RESERVED	R/W	0b	
3	RESERVED	R/W	0b	
2	LS_IM	R/W	0b	LS current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
1	RESERVED	R/W	0b	
0	RESERVED	R/W	0b	

### 5.5.3.6 STATUS Register (subaddress = 0x05) [reset = 00XXXXXXb]

Register mask: C0h

STATUS is shown in [Figure 5-30](#) and is described in [Table 5-12](#).

Return to [Summary Table](#).

**Figure 5-30. STATUS Register**

7	6	5	4	3	2	1	0
RESERVED	EE	AC_STATE	PB_STATE	STATE		RESERVED	
R-0b	R-0b	R-X	R-X	R-X		R-X	

**Table 5-12. STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	
6	EE	R	0b	EEPROM status: 0b = EEPROM values have not been changed from factory default setting. 1b = EEPROM values have been changed from factory default settings.
5	AC_STATE	R	X	AC_DET input status bit: 0b = AC_DET input is inactive (AC_DET input pin is high). 1b = AC_DET input is active (AC_DET input is low).
4	PB_STATE	R	X	PB input status bit: 0b = Push Button input is inactive (PB input pin is high). 1b = Push Button input is active (PB input pin is low).
3-2	STATE	R	X	State machine STATE indication: 0h = PMIC is in transitional state. 1h = PMIC is in WAIT_PWR_EN state. 2h = PMIC is in ACTIVE state. 3h = PMIC is in SUSPEND state.
1-0	RESERVED	R	X	

### 5.5.3.7 CONTROL Register (subaddress = 0x06) [reset = 0x00]

CONTROL is shown in [Figure 5-31](#) and described in [Table 5-13](#).

Return to [Summary Table](#).

**Figure 5-31. CONTROL Register**

7	6	5	4	3	2	1	0
RESERVED						OFFnPFO	RESERVED
R-0000 00b						R/W-0b	R/W-0b

**Table 5-13. CONTROL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0000 00b	
1	OFFnPFO	R/W	0b	Power-fail shutdown bit: 0b = nPFO has no effect on PMIC state. 1b = All rails are shut down and PMIC enters OFF state when PFI comparator trips (nPFO is low).
0	RESERVED	R/W	0b	



### 5.5.3.8 FLAG Register (subaddress = 0x07) [reset = 0x00]

FLAG is shown in [Figure 5-32](#) and described in [Table 5-14](#).

Return to [Summary Table](#).

**Figure 5-32. FLAG Register**

7	6	5	4	3	2	1	0
GPO2_FLG	RESERVED	GPO1_FLG	LDO1_FLG	DC4_FLG	DC3_FLG	DC2_FLG	DC1_FLG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

**Table 5-14. FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GPO2_FLG	R	0b	GPO2 Flag bit: 0b = Device powered up from OFF or SUSPEND state and GPO2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO2 was enabled while in SUSPEND.
6	RESERVED	R	0b	
5	GPO1_FLG	R	0b	GPO1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and GPO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO1 was enabled while in SUSPEND.
4	LDO1_FLG	R	0b	LDO1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and LDO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and LDO1 was enabled while in SUSPEND.
3	DC4_FLG	R	0b	DCDC4 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC4 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC4 was enabled while in SUSPEND.
2	DC3_FLG	R	0b	DCDC3 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC3 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC3 was enabled while in SUSPEND.
1	DC2_FLG	R	0b	DCDC2 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC2 was enabled while in SUSPEND.
0	DC1_FLG	R	0b	DCDC1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GDCDC1PO3 was enabled while in SUSPEND.

**5.5.3.9 PASSWORD Register (subaddress = 0x10) [reset = 0x00]**

PASSWORD is shown in [Figure 5-33](#) and described in [Table 5-15](#).

Return to [Summary Table](#).

**Figure 5-33. PASSWORD Register**

7	6	5	4	3	2	1	0
PWRD							
R/W-00h							

**Table 5-15. PASSWORD Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PWRD	R/W	00h	Register is used for accessing password protected registers (see <a href="#">Section 5.5.1</a> for details). Breaking the freshness seal (see for details). Programming power-up default values (see for details). Read-back always yields 0x00.

### 5.5.3.10 ENABLE1 Register (subaddress = 0x11) [reset = 0x00]

ENABLE1 is shown in [Figure 5-34](#) and described in [Table 5-16](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-34. ENABLE1 Register**

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	DC4_EN	DC3_EN	DC2_EN	DC1_EN	
R-00b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-16. ENABLE1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	RESERVED	R/W	0b	
4	RESERVED	R/W	0b	
3	DC4_EN	R/W	0b	DCDC4 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
2	DC3_EN	R/W	0b	DCDC3 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
1	DC2_EN	R/W	0b	DCDC2 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
0	DC1_EN	R/W	0b	DCDC1 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled

### 5.5.3.11 ENABLE2 Register (subaddress = 0x12) [reset = 0x00]

ENABLE2 is shown in [Figure 5-35](#) and described in [Table 5-17](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-35. ENABLE2 Register**

7	6	5	4	3	2	1	0
RESERVED	GPIO2	RESERVED	GPIO1	LS_EN	RESERVED	RESERVED	LDO1_EN
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-17. ENABLE2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	
6	GPIO2	R/W	0b	General purpose output 3 / reset polarity. Note: If DC12_RST bit (register 0x14) is set to 1 this bit has no function. 0b = GPIO2 output is driven low. 1b = GPIO2 output is HiZ.
5	RESERVED	R/W	0b	
4	GPIO1	R/W	0b	General purpose output 1. Note: If IO_SEL bit (register 0x13) is set to 1 this bit has no function. 0b = GPO1 output is driven low. 1b = GPO1 output is HiZ.
3	LS_EN	R/W	0b	Load switch (LS) enable bit. 0b = Disabled 1b = Enabled
2	RESERVED	R/W	0b	
1	RESERVED	R/W	0b	
0	LDO1_EN	R/W	0b	LDO1 enable bit. 0b = Disabled 1b = Enabled  Note: At power-up and down this bit is automatically updated by the internal power sequencer.

### 5.5.3.12 CONFIG1 Register (subaddress = 0x13) [reset = 0x4C]

CONFIG1 is shown in [Figure 5-36](#) and described in [Table 5-18](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-36. CONFIG1 Register**

7	6	5	4	3	2	1	0
TRST	RESERVED	RESERVED	PGDLY		STRICT	UVLO	
R/W-0b	R/W-1b	R/W-0b	R/W-01b		R/W-1b	R/W-00b	

**Table 5-18. CONFIG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	TRST	R/W, E2	0b	Push-button reset time constant: 0b = 8 s 1b = 15 s
6	RESERVED	R/W	1b	
5	RESERVED	R/W	0b	
4-3	PGDLY	R/W, E2	01b	Power-Good delay. Note: Power-good delay applies to rising-edge only (power-up), not falling edge (power-down or fault). 00b = 10 ms 01b = 20 ms 10b = 50 ms 11b = 150 ms
2	STRICT	R/W, E2	1b	Supply Voltage Supervisor Sensitivity selection. See <a href="#">Section 4.5</a> for details. 0b = Power-good threshold (VOUT falling) has wider limits. Over-voltage is not monitored. 1b = Power-good threshold (VOUT falling) has tight limits. Over-voltage is monitored.
1-0	UVLO	R/W, E2	00b	UVLO setting 00b = 2.75 V 01b = 2.95 V 10b = 3.25 V 11b = 3.35 V

### 5.5.3.13 CONFIG2 Register (subaddress = 0x14) [reset = 0xC0]

CONFIG2 is shown in [Figure 5-37](#) and described in [Table 5-19](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-37. CONFIG2 Register**

7	6	5	4	3	2	1	0
DC12_RST	UVLOHYS	RESERVED		LSILIM		RESERVED	
R/W-1b	R/W-1b	R-00b		R/W-00b		R/W-00b	

**Table 5-19. CONFIG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DC12_RST	R/W, E2	1b	DCDC1 and DCDC2 reset-pin enable: 0b = GPIO2 is configured as general-purpose output. 1b = GPIO2 is configured as warm-reset input to DCDC1 and DCDC2.
6	UVLOHYS	R/W, E2	1b	UVLO hysteresis: 0b = 200 mV 1b = 400 mV
5-4	RESERVED	R	00b	
3-2	LSILIM	R/W	00b	Load switch (LS) current limit selection: 00b = 100 mA, (MIN = 98 mA) 01b = 200 mA, (MIN = 194 mA) 10b = 500 mA, (MIN = 475 mA) 11b = 1000 mA, (MIN = 900 mA) See the LS current limit specification in <a href="#">Section 4.5</a> for more details.
1-0	RESERVED	R/W	00b	

#### 5.5.3.14 CONFIG3 Register (subaddress = 0x15) [reset = 0x0]

CONFIG3 is shown in [Figure 5-38](#) and described in [Table 5-20](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-38. CONFIG3 Register**

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LSnPFO	RESERVED	RESERVED	LSDCHRG	RESERVED	RESERVED
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-20. CONFIG3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LSnPFO	R/W	0b	Load switch power-fail disable bit: 0b = Load switch status is not affected by power-fail comparator. 1b = Load switch is disabled if power-fail comparator trips (nPFO is low).
4	RESERVED	R/W	0b	
3	RESERVED	R/W	0b	
2	LSDCHRG	R/W	0b	Load switch discharge enable bit: 0b = Active discharge is disabled. 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF).
1	RESERVED	R/W	0b	
0	RESERVED	R/W	0b	

### 5.5.3.15 DCDC1 Register (offset = 0x16) [reset = 0x99]

DCDC1 is shown in [Figure 5-39](#) and described in [Table 5-21](#).

Return to [Summary Table](#).

Note 1: This register is password protected. For more information, see [Section 5.5.1](#).

Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC1 register.

Note 3: To change the output voltage of DCDC1, the GO bit or the GODSBL bit must be set to 1b in register 0x1A.

**Figure 5-39. DCDC1 Register**

7	6	5	4	3	2	1	0
PFM	RESERVED						DCDC1
R/W-1b	R-0b						R/W-19h

**Table 5-21. DCDC1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition.  0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	



**Table 5-21. DCDC1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-0	DCDC1	R/W, E2	19h	DCDC1 output voltage setting: 0h = 0.850 1h = 0.860 2h = 0.870 3h = 0.880 4h = 0.890 5h = 0.900 6h = 0.910 7h = 0.920 8h = 0.930 9h = 0.940 Ah = 0.950 Bh = 0.960 Ch = 0.970 Dh = 0.980 Eh = 0.990 Fh = 1.000 10h = 1.010 11h = 1.020 12h = 1.030 13h = 1.040 14h = 1.050 15h = 1.060 16h = 1.070 17h = 1.080 18h = 1.090 19h = 1.100 1Ah = 1.110 1Bh = 1.120 1Ch = 1.130 1Dh = 1.140 1Eh = 1.150 1Fh = 1.160 20h = 1.170 21h = 1.180 22h = 1.190 23h = 1.200

**Table 5-21. DCDC1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
				24h = 1.210
				25h = 1.220
				26h = 1.230
				27h = 1.240
				28h = 1.250
				29h = 1.260
				2Ah = 1.270
				2Bh = 1.280
				2Ch = 1.290
				2Dh = 1.300
				2Eh = 1.310
				2Fh = 1.320
				30h = 1.330
				31h = 1.340
				32h = 1.350
				33h = 1.375
				34h = 1.400
				35h = 1.425
				36h = 1.450
				37h = 1.475
				38h = 1.500
				39h = 1.525
				3Ah = 1.550
				3Bh = 1.575
				3Ch = 1.600
				3Dh = 1.625
				3Eh = 1.650
				3Fh = 1.675

### 5.5.3.16 DCDC2 Register (subaddress = 0x17) [reset = 0x99]

DCDC2 is shown in [Figure 5-40](#) and described in [Table 5-22](#).

Return to [Summary Table](#).

Note 1: This register is password protected. For more information, see [Section 5.5.1](#).

Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC2 register.

Note 3: To change the output voltage of DCDC2, the GO bit or the GODSBL bit must be set to 1b in register 0x1A.

**Figure 5-40. DCDC2 Register**

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC2					
R/W-1b	R-0b	R/W-19h					

**Table 5-22. DCDC2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse frequency modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition.  0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	

**Table 5-22. DCDC2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-0	DCDC2	R/W, E2	19h	DCDC2 output voltage setting: 0h = 0.850 1h = 0.860 2h = 0.870 3h = 0.880 4h = 0.890 5h = 0.900 6h = 0.910 7h = 0.920 8h = 0.930 9h = 0.940 Ah = 0.950 Bh = 0.960 Ch = 0.970 Dh = 0.980 Eh = 0.990 Fh = 1.000 10h = 1.010 11h = 1.020 12h = 1.030 13h = 1.040 14h = 1.050 15h = 1.060 16h = 1.070 17h = 1.080 18h = 1.090 19h = 1.100 1Ah = 1.110 1Bh = 1.120 1Ch = 1.130 1Dh = 1.140 1Eh = 1.150 1Fh = 1.160 20h = 1.170 21h = 1.180 22h = 1.190 23h = 1.200

**Table 5-22. DCDC2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
				24h = 1.210
				25h = 1.220
				26h = 1.230
				27h = 1.240
				28h = 1.250
				29h = 1.260
				2Ah = 1.270
				2Bh = 1.280
				2Ch = 1.290
				2Dh = 1.300
				2Eh = 1.310
				2Fh = 1.320
				30h = 1.330
				31h = 1.340
				32h = 1.350
				33h = 1.375
				34h = 1.400
				35h = 1.425
				36h = 1.450
				37h = 1.475
				38h = 1.500
				39h = 1.525
				3Ah = 1.550
				3Bh = 1.575
				3Ch = 1.600
				3Dh = 1.625
				3Eh = 1.650
				3Fh = 1.675

### 5.5.3.17 DCDC3 Register (subaddress = 0x18) [reset = 0x8C]

DCDC3 is shown in [Figure 5-41](#) and described in [Table 5-23](#).

Return to [Summary Table](#).

Note 1: This register is password protected. For more information, see [Section 5.5.1](#).

Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC3 register.

---

#### NOTE

Power-up default may differ depending on RSEL value. See [Section 5.3.1.10](#) for details.

---

**Figure 5-41. DCDC3 Register**

7	6	5	4	3	2	1	0
PFM	RESERVED						DCDC3
R/W-1b	R-0b						R/W-Ch

**Table 5-23. DCDC3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition.  0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	

**Table 5-23. DCDC3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-0	DCDC3	R/W, E2	Ch	DCDC3 output voltage setting: 0h = 0.900 1h = 0.925 2h = 0.950 3h = 0.975 4h = 1.000 5h = 1.025 6h = 1.050 7h = 1.075 8h = 1.100 9h = 1.125 Ah = 1.150 Bh = 1.175 Ch = 1.200 Dh = 1.225 Eh = 1.250 Fh = 1.275 10h = 1.300 11h = 1.325 12h = 1.350 13h = 1.375 14h = 1.400 15h = 1.425 16h = 1.450 17h = 1.475 18h = 1.500 19h = 1.525 1Ah = 1.550 1Bh = 1.600 1Ch = 1.650 1Dh = 1.700 1Eh = 1.750 1Fh = 1.800 20h = 1.850 21h = 1.900 22h = 1.950 23h = 2.000

**Table 5-23. DCDC3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
				24h = 2.050
				25h = 2.100
				26h = 2.150
				27h = 2.200
				28h = 2.250
				29h = 2.300
				2Ah = 2.350
				2Bh = 2.400
				2Ch = 2.450
				2Dh = 2.500
				2Eh = 2.550
				2Fh = 2.600
				30h = 2.650
				31h = 2.700
				32h = 2.750
				33h = 2.800
				34h = 2.850
				35h = 2.900
				36h = 2.950
				37h = 3.000
				38h = 3.050
				39h = 3.100
				3Ah = 3.150
				3Bh = 3.200
				3Ch = 3.250
				3Dh = 3.300
				3Eh = 3.350
				3Fh = 3.400



### 5.5.3.18 DCDC4 Register (subaddress = 0x19) [reset = 0xB2]

DCDC4 is shown in [Figure 5-42](#) and described in [Table 5-24](#).

Return to [Summary Table](#).

Note 1: This register is password protected. For more information, see [Section 5.5.1](#).

Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC4 register.

---

#### NOTE

Power-up default may differ depending on RSEL value. See [Section 5.3.1.10](#) for details. The Reserved setting should not be selected and the output voltage settings should not be modified while the converter is operating.

---

**Figure 5-42. DCDC4 Register**

7	6	5	4	3	2	1	0
PFM	RESERVED						DCDC4
R/W-1b	R-0b						R/W-32h

**Table 5-24. DCDC4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	

**Table 5-24. DCDC4 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-0	DCDC4	R/W, E2	32h	DCDC4 output voltage setting: 0h = 1.175 1h = 1.200 2h = 1.225 3h = 1.250 4h = 1.275 5h = 1.300 6h = 1.325 7h = 1.350 8h = 1.375 9h = 1.400 Ah = 1.425 Bh = 1.450 Ch = 1.475 Dh = 1.500 Eh = 1.525 Fh = 1.550 10h = 1.600 11h = 1.650 12h = 1.700 13h = 1.750 14h = 1.800 15h = 1.850 16h = 1.900 17h = 1.950 18h = 2.000 19h = 2.050 1Ah = 2.100 1Bh = 2.150 1Ch = 2.200 1Dh = 2.250 1Eh = 2.300 1Fh = 2.3500 20h = 2.400 21h = 2.450 22h = 2.500 23h = 2.550

**Table 5-24. DCDC4 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
				24h = 2.600
				25h = 2.650
				26h = 2.700
				27h = 2.750
				28h = 2.800
				29h = 2.850
				2Ah = 2.900
				2Bh = 2.950
				2Ch = 3.000
				2Dh = 3.050
				2Eh = 3.100
				2Fh = 3.150
				30h = 3.200
				31h = 3.250
				32h = 3.300
				33h = 3.350
				34h = 3.400
				35h = reserved
				36h = reserved
				37h = reserved
				38h = reserved
				39h = reserved
				3Ah = reserved
				3Bh = reserved
				3Ch = reserved
				3Dh = reserved
				3Eh = reserved
				3Fh = reserved

### 5.5.3.19 SLEW Register (subaddress = 0x1A) [reset = 0x06]

SLEW is shown in [Figure 5-43](#) and described in [Table 5-25](#).

Return to [Summary Table](#).

#### NOTE

Slew-rate control applies to DCDC1 and DCDC2 only. If changing from a higher voltage to lower voltage while STRICT = 1 and converters are in a no load state, PFM bit for DCDC1 and DCDC2 must be set to 0.

**Figure 5-43. SLEW Register**

7	6	5	4	3	2	1	0
GO	GODSBL	RESERVED			SLEW		
R/W-0b	R/W-0b	R-000b			R/W-6h		

**Table 5-25. SLEW Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	GO	R/W	0b	Go bit. Note: Bit is automatically reset at the end of the voltage transition.  0b = No change  1b = Initiates the transition from present state to the output voltage setting currently stored in DCDC1 and DCDC2 register. SLEW setting does apply.
6	GODSBL	R/W	0b	Go disable bit  0b = Enabled  1b = Disabled; DCDC1 and DCDC2 output voltage changes whenever set-point is updated in DCDC1 and DCDC2 register without having to write to the GO bit. SLEW setting does apply.
5-3	RESERVED	R	000b	
2-0	SLEW	R/W	6h	Output slew rate setting:  0h = 160 $\mu\text{s}/\text{step}$ (0.0625 mV/ $\mu\text{s}$ at 10 mV per step) 1h = 80 $\mu\text{s}/\text{step}$ (0.125 mV/ $\mu\text{s}$ at 10 mV per step) 2h = 40 $\mu\text{s}/\text{step}$ (0.250 mV/ $\mu\text{s}$ at 10 mV per step) 3h = 20 $\mu\text{s}/\text{step}$ (0.500 mV/ $\mu\text{s}$ at 10 mV per step) 4h = 10 $\mu\text{s}/\text{step}$ (1.0 mV/ $\mu\text{s}$ at 10 mV per step) 5h = 5 $\mu\text{s}/\text{step}$ (2.0 mV/ $\mu\text{s}$ at 10 mV per step) 6h = 2.5 $\mu\text{s}/\text{step}$ (4.0 mV/ $\mu\text{s}$ at 10 mV per step)  7h = Immediate; slew rate is only limited by control loop response time. Note: The actual slew rate depends on the voltage step per code. Refer to DCDCx registers for details.

### 5.5.3.20 LDO1 Register (subaddress = 0x1B) [reset = 0x1F]

LDO1 is shown in [Figure 5-44](#) and described in [Table 5-26](#).

Return to [Summary Table](#).

Note 1: This register is password protected. For more information, see [Section 5.5.1](#).

Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the LDO1 register.

**Figure 5-44. LDO1 Register**

7	6	5	4	3	2	1	0
RESERVED			LDO1				
R-00b			R/W-1Fh				

**Table 5-26. LDO1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5-0	LDO1	R/W, E2	1Fh	LDO1 output voltage setting: 0h = 0.900 1h = 0.925 2h = 0.950 3h = 0.975 4h = 1.000 5h = 1.025 6h = 1.050 7h = 1.075 8h = 1.100 9h = 1.125 Ah = 1.150 Bh = 1.175 Ch = 1.200 Dh = 1.225 Eh = 1.250 Fh = 1.275 10h = 1.300 11h = 1.325 12h = 1.350 13h = 1.375 14h = 1.400 15h = 1.425 16h = 1.450 17h = 1.475 18h = 1.500 19h = 1.525

**Table 5-26. LDO1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
				1Ah = 1.550
				1Bh = 1.600
				1Ch = 1.650
				1Dh = 1.700
				1Eh = 1.750
				1Fh = 1.800
				20h = 1.850
				21h = 1.900
				22h = 1.950
				23h = 2.000
				24h = 2.050
				25h = 2.100
				26h = 2.150
				27h = 2.200
				28h = 2.250
				29h = 2.300
				2Ah = 2.350
				2Bh = 2.400
				2Ch = 2.450
				2Dh = 2.500
				2Eh = 2.550
				2Fh = 2.600
				30h = 2.650
				31h = 2.700
				32h = 2.750
				33h = 2.800
				34h = 2.850
				35h = 2.900
				36h = 2.950
				37h = 3.000
				38h = 3.050
				39h = 3.100
				3Ah = 3.150
				3Bh = 3.200
				3Ch = 3.250
				3Dh = 3.300
				3Eh = 3.350
				3Fh = 3.400

### 5.5.3.21 SEQ1 Register (subaddress = 0x20) [reset = 0x00]

SEQ1 is shown in [Figure 5-45](#) and described in [Table 5-27](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-45. SEQ1 Register**

7	6	5	4	3	2	1	0
DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**Table 5-27. SEQ1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DLY8	R/W, E2	0b	Delay8 (occurs after Strobe 8 and before Strobe 9.) 0b = 2 ms 1b = 5 ms
6	DLY7	R/W, E2	0b	Delay7 (occurs after Strobe 7 and before Strobe 8.) 0b = 2 ms 1b = 5 ms
5	DLY6	R/W, E2	0b	Delay6 (occurs after Strobe 6 and before Strobe 7.) 0b = 2 ms 1b = 5 ms
4	DLY5	R/W, E2	0b	Delay5 (occurs after Strobe 5 and before Strobe 6.) 0b = 2 ms 1b = 5 ms
3	DLY4	R/W, E2	0b	Delay4 (occurs after Strobe 4 and before Strobe 5.) 0b = 2 ms 1b = 5 ms
2	DLY3	R/W, E2	0b	Delay3 (occurs after Strobe 3 and before Strobe 4.) 0b = 2 ms 1b = 5 ms
1	DLY2	R/W, E2	0b	Delay2 (occurs after Strobe 2 and before Strobe 3.) 0b = 2 ms 1b = 5 ms
0	DLY1	R/W, E2	0b	Delay1 (occurs after Strobe 1 and before Strobe 2.) 0b = 2 ms 1b = 5 ms

### 5.5.3.22 SEQ2 Register (subaddress = 0x21) [reset = 0x00]

SEQ2 is shown in [Figure 5-46](#) and described in [Table 5-28](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-46. SEQ2 Register**

7	6	5	4	3	2	1	0
DLYFCTR	RESERVED					DLY9	
R/W -0b	R-000 000b					R/W -0b	

**Table 5-28. SEQ2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DLYFCTR	R/W, E2	0b	Power-down delay factor: 0b = 1x 1b = 10x (delay times are multiplied by 10x during power-down.) Note: DLYFCTR has no effect on power-up timing.
6-1	RESERVED	R	000 000b	
0	DLY9	R/W, E2	0b	Delay9 (occurs after Strobe 9 and before Strobe 10.) 0b = 2 ms 1b = 5 ms



**5.5.3.23 SEQ3 Register (subaddress = 0x22) [reset = 0x98]**

SEQ3 is shown in [Figure 5-47](#) and described in [Table 5-29](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-47. SEQ3 Register**

7	6	5	4	3	2	1	0
DC2_SEQ				DC1_SEQ			
R/W-9h				R/W-8h			

**Table 5-29. SEQ3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	DC2_SEQ	R/W, E2	9h	DCDC2 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

**Table 5-29. SEQ3 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	DC1_SEQ	R/W, E2	8h	DCDC1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

**5.5.3.24 SEQ4 Register (subaddress = 0x23) [reset = 0x75]**

SEQ4 is shown in [Figure 5-48](#) and described in [Table 5-30](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-48. SEQ4 Register**

7	6	5	4	3	2	1	0
DC4_SEQ				DC3_SEQ			
R/W-7h				R/W-5h			

**Table 5-30. SEQ4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	DC4_SEQ	R/W, E2	7h	DCDC4 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

**Table 5-30. SEQ4 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	DC3_SEQ	R/W, E2	5h	DCDC3 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

### 5.5.3.25 SEQ5 Register (subaddress = 0x24) [reset = 0x12]

SEQ5 is shown in [Figure 5-49](#) and described in [Table 5-31](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-49. SEQ5 Register**

7	6	5	4	3	2	1	0
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R/W-1h		R-0h		R/W-2h	

**Table 5-31. SEQ5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	RESERVED	R/W, E2	1h	
3-2	RESERVED	R	0h	
1-0	RESERVED	R/W, E2	2h	

**5.5.3.26 SEQ6 Register (subaddress = 0x25) [reset = 0x63]**

SEQ6 is shown in [Figure 5-50](#) and described in [Table 5-32](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-50. SEQ6 Register**

7	6	5	4	3	2	1	0
Reserved				LDO1_SEQ			
R/W-6h				R/W-3h			

**Table 5-32. SEQ6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	6h	Reserved
3-0	LDO1_SEQ	R/W, E2	3h	LDO1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

**5.5.3.27 SEQ7 Register (subaddress = 0x26) [reset = 0x03]**

SEQ7 is shown in [Figure 5-51](#) and described in [Table 5-33](#).

Return to [Summary Table](#).

Password protected.

**Figure 5-51. SEQ7 Register**

7	6	5	4	3	2	1	0
GPO2_SEQ				GPO1_SEQ			
R/W-0h				R/W-3h			

**Table 5-33. SEQ7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	GPO2_SEQ	R/W, E2	0h	GPO2 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

**Table 5-33. SEQ7 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	GPO1_SEQ	R/W, E2	3h	GPO1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.



## 6 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 6.1 Application Information

The TPS65216 is designed to pair with various application processors. For detailed information on using TPS65216 with Sitara™ AMIC110, AMIC120, AM335x or AM437x processors, refer to [.Powering AMIC110, AMIC120, AM335x, and AM437x with TPS65216](#). The typical application in [Section 6.2](#) is based on and uses terminology consistent with the Sitara™ family of processors.

## 6.2 Typical Application

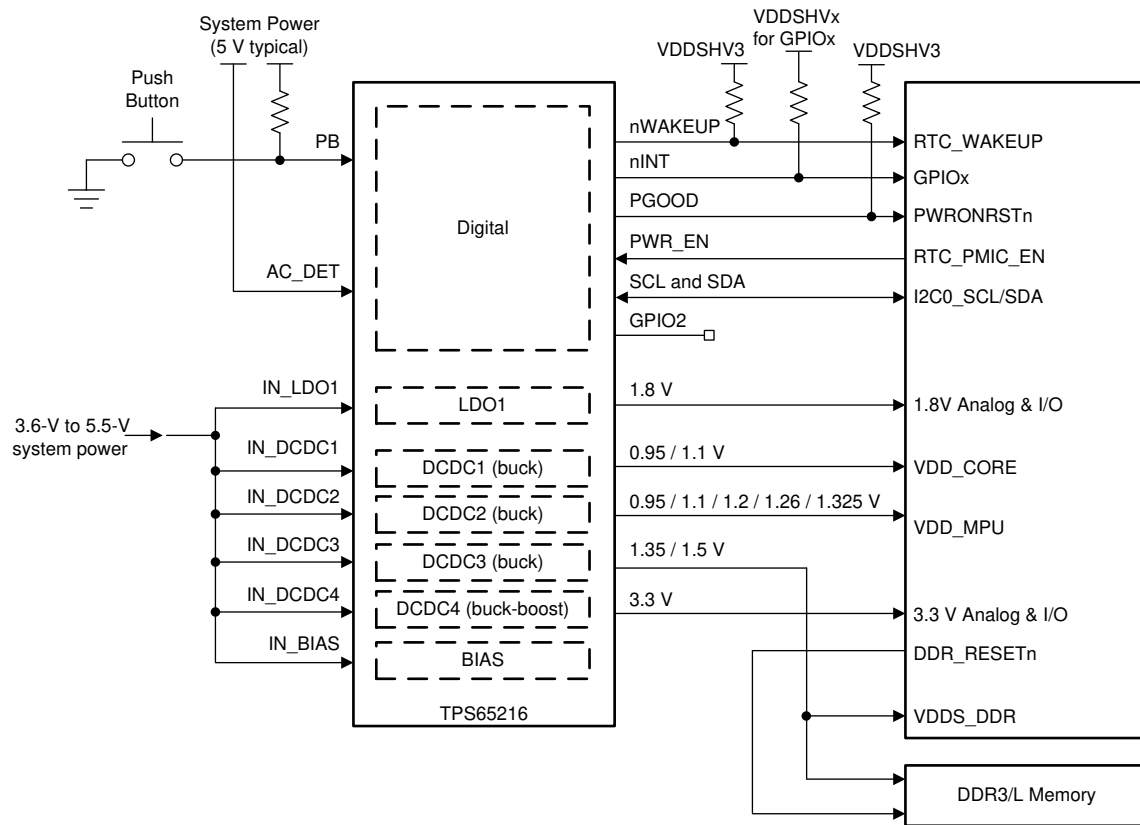


Figure 6-1. Typical Application Schematic

## 6.2.1 Design Requirements

Table 6-1 lists the design requirements.

**Table 6-1. Design Parameters**

	VOLTAGE	SEQUENCE
DCDC1	1.1 V	8
DCDC2	1.1 V	9
DCDC3	1.2 V	5
DCDC4	3.3 V	7
LDO1	1.8 V	3

## 6.2.2 Detailed Design Procedure

### 6.2.2.1 Output Filter Design

The step down converters (DCDC1, DCDC2, and DCDC3) on TPS65216 are designed to operate with effective inductance values in the range of 1 to 2.2  $\mu\text{H}$  and with effective output capacitance in the range of 10 to 100  $\mu\text{F}$ . The internal compensation is optimized to operate with an output filter of  $L = 1.5 \mu\text{H}$  and  $C_{\text{OUT}} = 10 \mu\text{F}$ .

The buck boost converter (DCDC4) on TPS65216 is designed to operate with effective inductance values in the range of 1.2 to 2.2  $\mu\text{H}$ . The internal compensation is optimized to operate with an output filter of  $L = 1.5 \mu\text{H}$  and  $C_{\text{OUT}} = 47 \mu\text{F}$ .

Larger or smaller inductor/capacitance values can be used to optimize performance of the device for specific operation conditions.

### 6.2.2.2 Inductor Selection for Buck Converters

The inductor value affects its peak to peak ripple current, the PWM to PFM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current ( $\Delta I_L$ ) decreases with higher inductance and increases with higher  $V_{\text{IN}}$  or  $V_{\text{OUT}}$ . Equation 1 calculates the maximum inductor current ripple under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended as during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{\text{OUT}} \times \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{L \times f} \quad (1)$$

$$I_{L\text{max}} = I_{\text{OUTmax}} + \frac{\Delta I_L}{2}$$

where

- F = Switching frequency
  - L = Inductor value
  - $\Delta I_L$  = Peak-to-peak inductor ripple current
  - $I_{L\text{max}}$  = Maximum inductor current
- (2)

The following inductors have been used with the TPS65216 (see Table 6-2).

**Table 6-2. List of Recommended Inductors**

PART NUMBER	VALUE	SIZE (mm) [L x W x H]	MANUFACTURER
<b>INDUCTORS FOR DCDC1, DCDC2, DCDC3, DCDC4</b>			

**Table 6-2. List of Recommended Inductors (continued)**

PART NUMBER	VALUE	SIZE (mm) [L x W x H]	MANUFACTURER
SPM3012T-1R5M	1.5 $\mu$ H, 2.8 A, 77 m $\Omega$	3.2 x 3.0 x 1.2	TDK
IHLP1212BZER1R5M11	1.5 $\mu$ H, 4.0 A, 28.5 m $\Omega$	3.6 x 3.0 x 2.0	Vishay

**6.2.2.3 Output Capacitor Selection**

The hysteretic PWM control scheme of the TPS65216 switching converters allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents the converter operates in power save mode, and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM mode.

The buck-boost converter requires additional output capacitance to help maintain converter stability during high load conditions. At least 40  $\mu$ F of output capacitance is recommended and an additional 100-nF capacitor can be added to further filter output ripple at higher frequencies.

Table 6-2 lists the recommended capacitors.

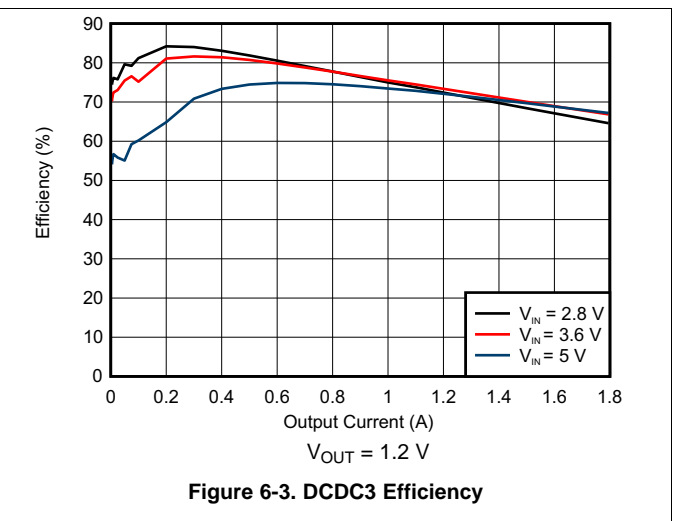
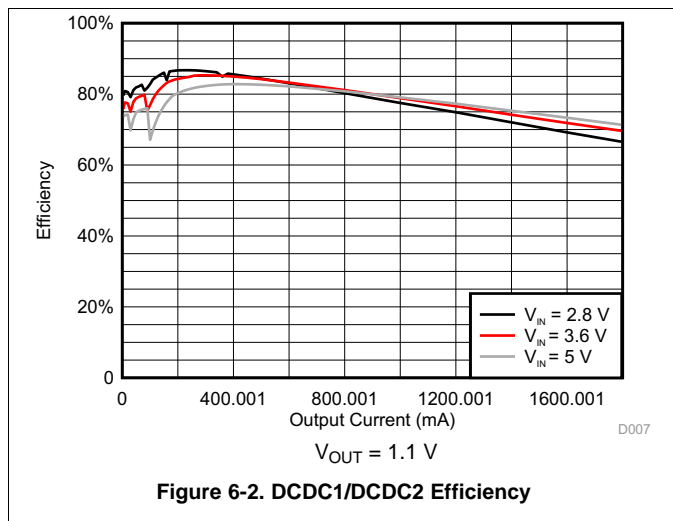
**Table 6-3. List of Recommended Capacitors**

PART NUMBER	VALUE	SIZE (mm) [L x W x H]	MANUFACTURER
<b>CAPACITORS FOR VOLTAGES UP TO 5.5 V<sup>(1)</sup></b>			
GRM188R60J105K	1 $\mu$ F	1608 / 0603 (1.6 x 0.8 x 0.8)	Murata
GRM21BR60J475K	4.7 $\mu$ F	2012 / 0805 (2.0 x 1.25 x 1.25)	Murata
GRM31MR60J106K	10 $\mu$ F	3216 / 1206 (3.2 x 1.6 x 1.6)	Murata
GRM31CR60J226K	22 $\mu$ F	3216 / 1206 (3.2 x 1.6 x 1.6)	Murata

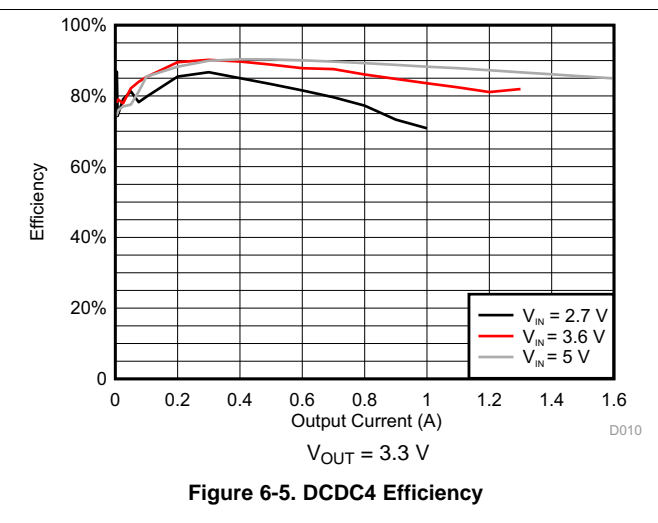
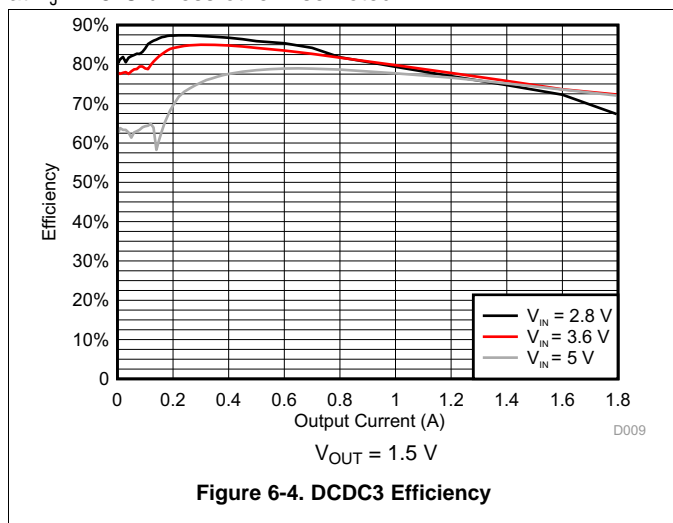
(1) The DC bias effect of ceramic capacitors must be considered when selecting a capacitor.

**6.2.3 Application Curves**

at  $T_J = 25^\circ\text{C}$  unless otherwise noted



at  $T_j = 25^\circ\text{C}$  unless otherwise noted



## 7 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 3.6 V and 5.5 V. This input supply can be from an externally regulated supply. If the input supply is located more than a few inches from the TPS65216 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47  $\mu\text{F}$  is a typical choice.

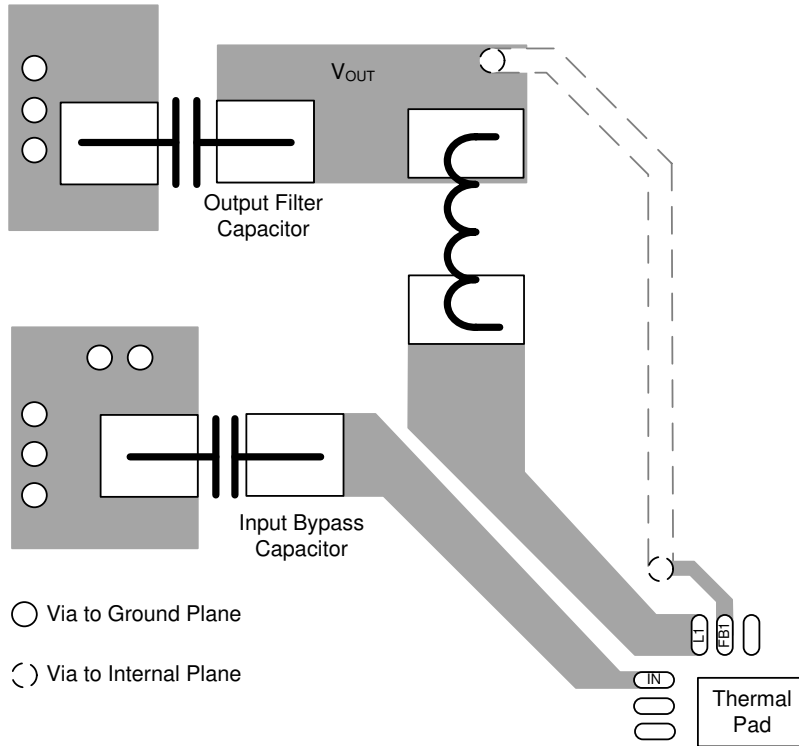
## 8 Layout

### 8.1 Layout Guidelines

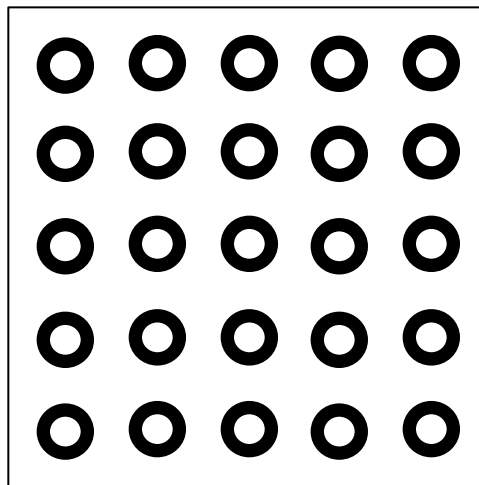
Follow these layout guidelines:

- The IN\_X pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 4.7- $\mu\text{F}$  with a X5R or X7R dielectric.
- The optimum placement is closest to the IN\_X pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the IN\_X pin, and the thermal pad of the device.
- The thermal pad should be tied to the PCB ground plane with a minimum of 25 vias. See [Figure 8-2](#) for an example.
- The LX trace should be kept on the PCB top layer and free of any vias.
- The FBX traces should be routed away from any potential noise source to avoid coupling.
- DCDC4 Output capacitance should be placed immediately at the DCDC4 pin. Excessive distance between the capacitance and DCDC4 pin may cause poor converter performance.

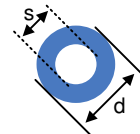
### 8.2 Layout Example



**Figure 8-1. Layout Recommendation**



Recommended Thermal Pad by size  
 Hole size (s) = 8 mil  
 Diameter (d) = 16 mil



**Figure 8-2. Thermal Pad Layout Recommendation**

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 *Third-Party Products Disclaimer*

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### 9.2 Documentation Support

#### 9.2.1 *Related Documentation*

For related documentation see the following:

- Texas Instruments, [Basic Calculation of a Buck Converter's Power Stage application report](#)
- Texas Instruments, [Design Calculations for Buck-Boost Converters application report](#)
- Texas Instruments, [Empowering Designs With Power Management IC \(PMIC\) for Processor Applications application report](#)
- Texas Instruments, [TPS65218EVM user's guide](#)
- Texas Instruments, [TPS65218 Power Management Integrated Circuit \(PMIC\) for Industrial Applications application report](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.5 Trademarks

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## 10.1 Package Option Addendum

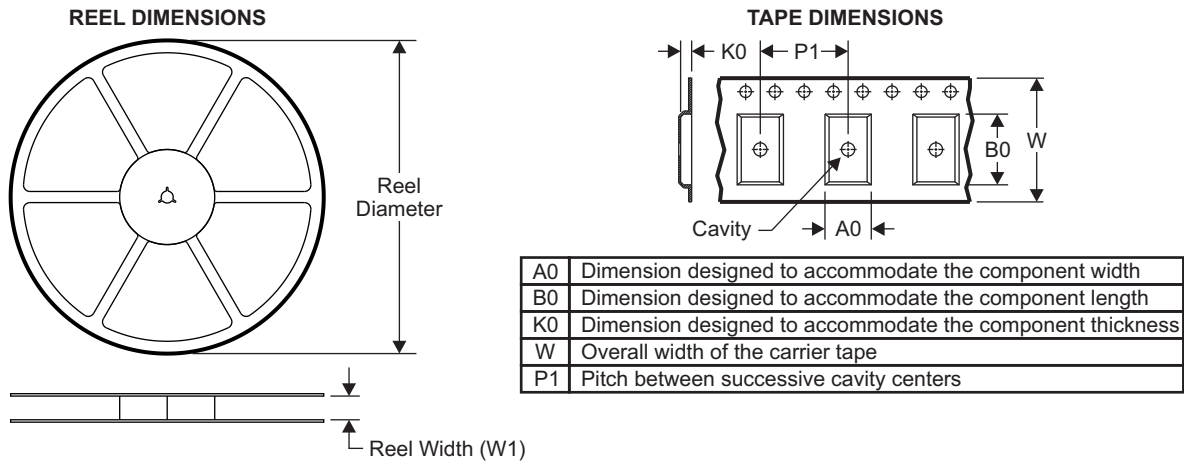
### 10.1.1 Packaging Information

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(3)</sup>	MSL Peak Temp <sup>(4)</sup>	Op Temp (°C)	Device Marking <sup>(5) (6)</sup>
TPS65216D0RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65216D0
TPS65216D0RSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65216D0

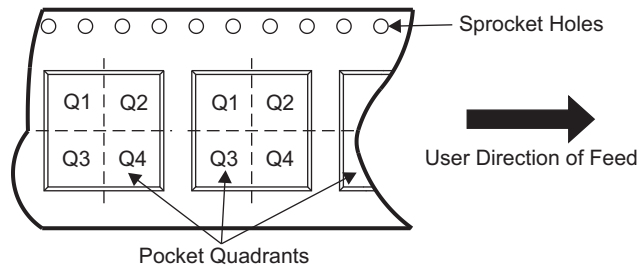
- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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### 10.1.2 Tape and Reel Information

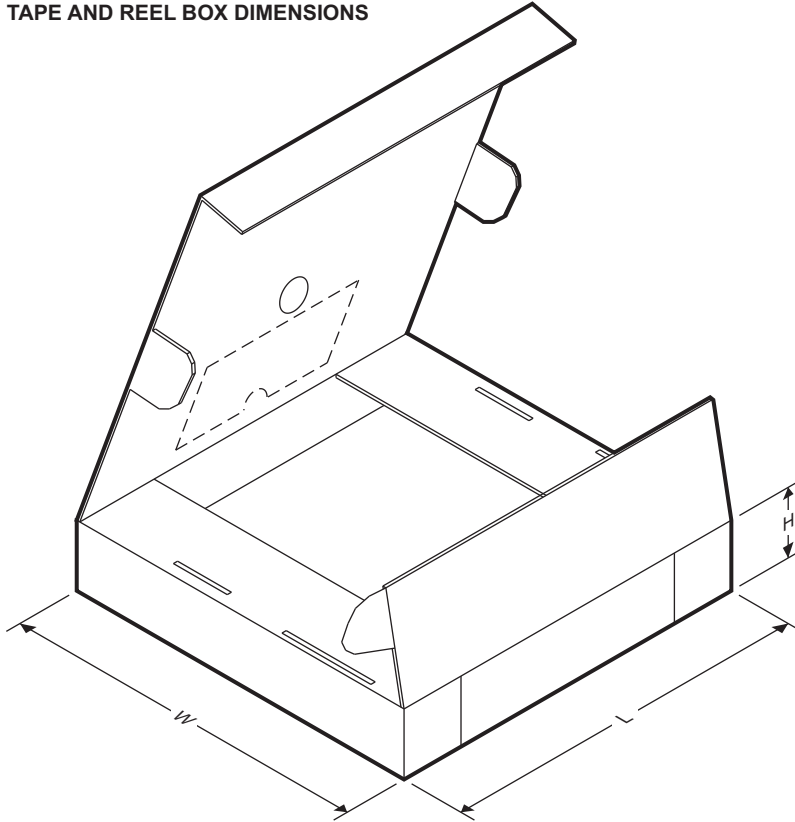


#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65216D0RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65216D0RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65216D0RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65216D0RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65216D0RSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	T65216D0	<a href="#">Samples</a>
TPS65216D0RSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	T65216D0	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65216D0RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65216D0RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

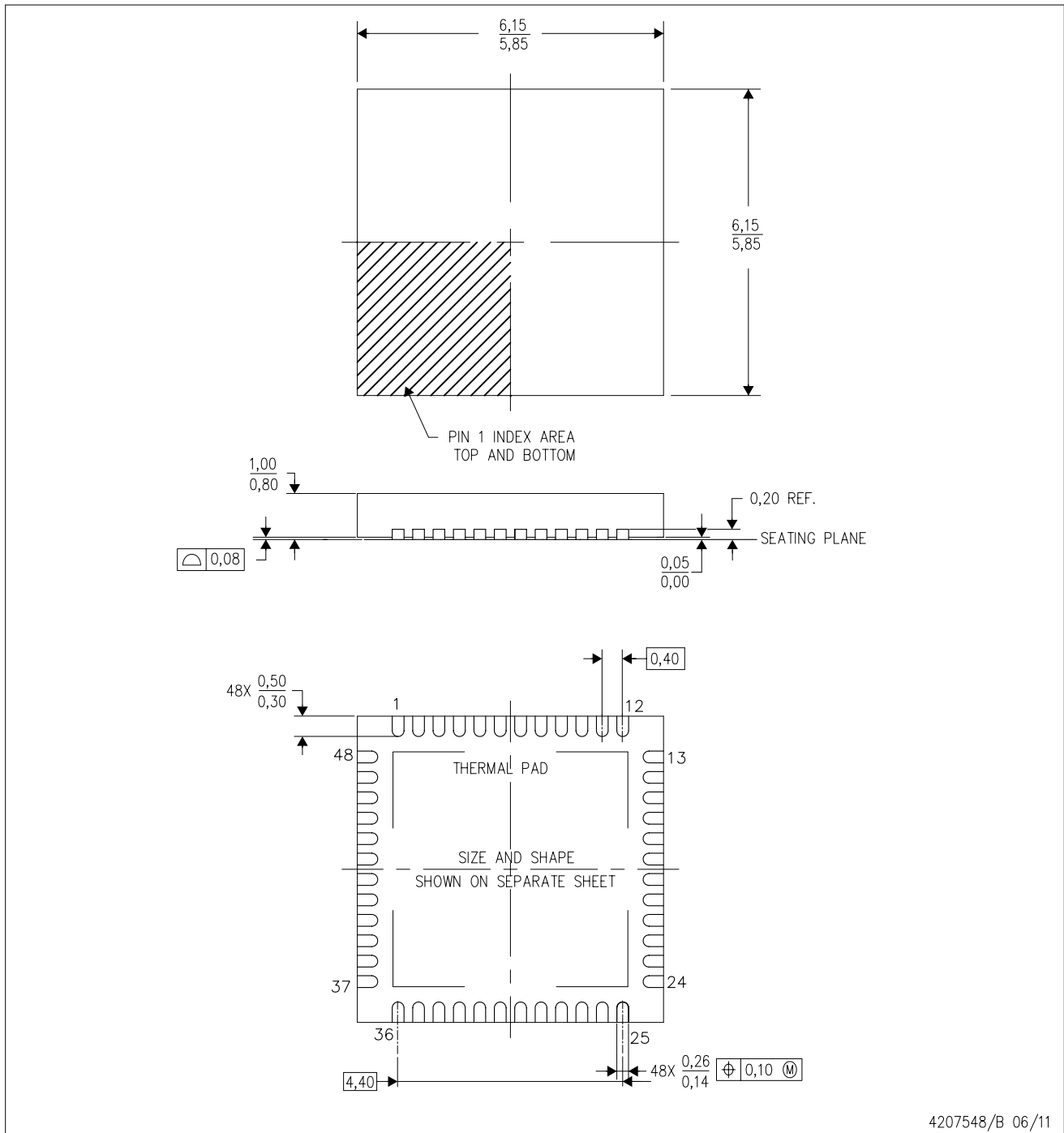

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65216D0RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65216D0RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

# MECHANICAL DATA

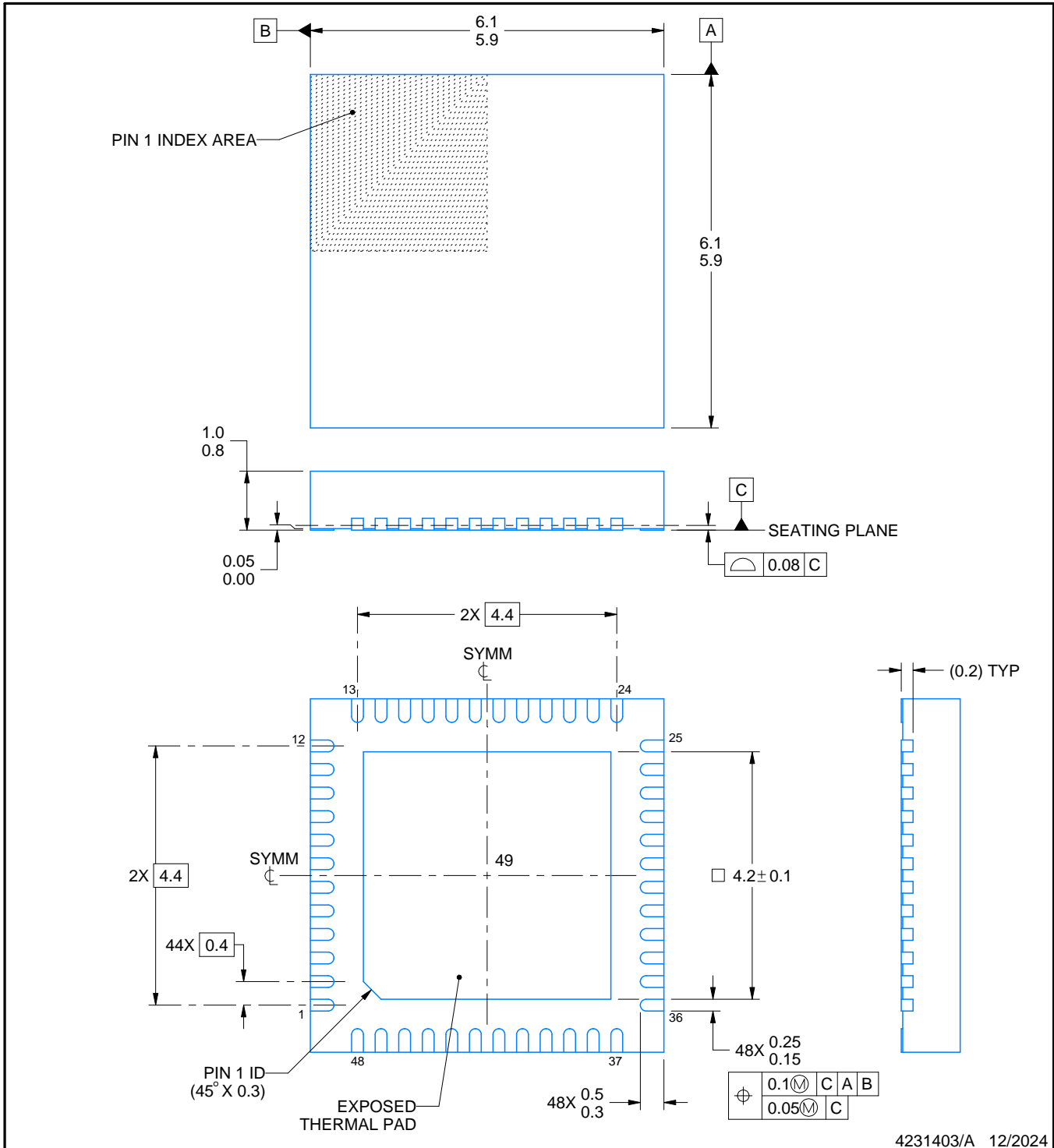
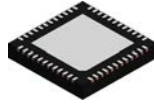
RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.





NOTES:

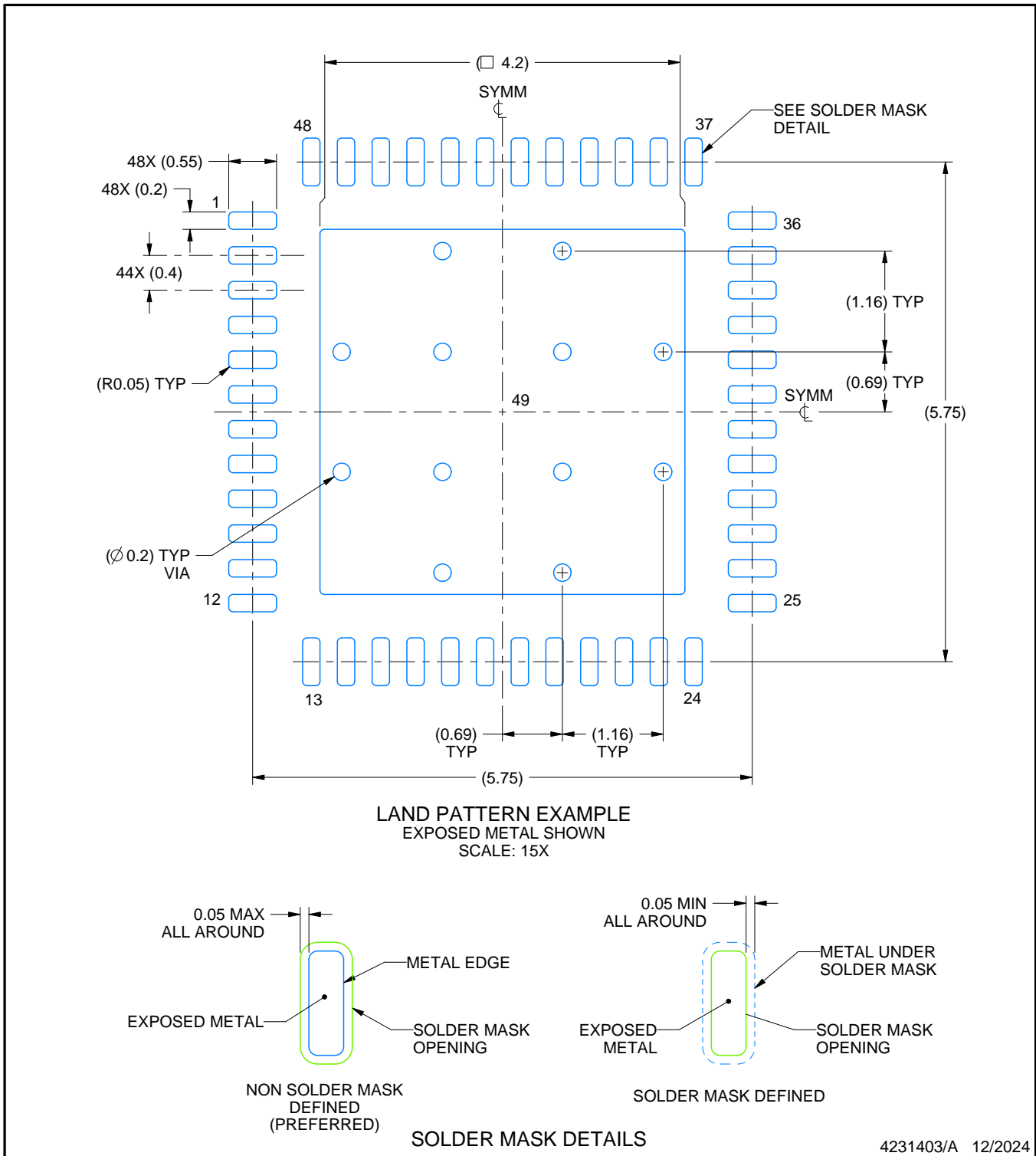
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

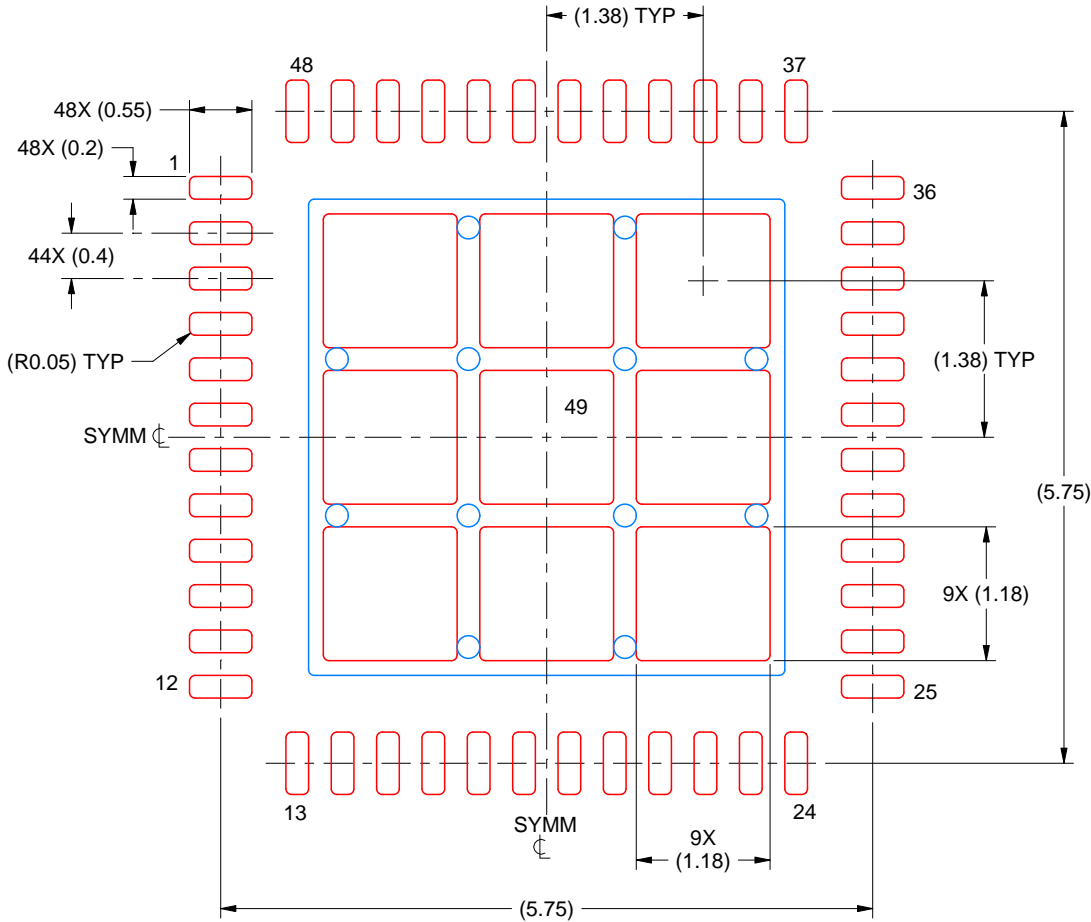
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 MM THICK STENCIL  
 SCALE: 15X

EXPOSED PAD 49  
 71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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