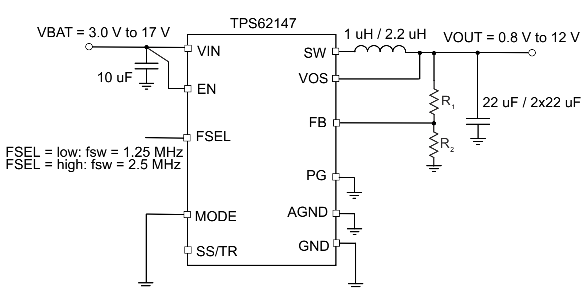
# TPS62147, TPS62148 High-Accuracy, 3-V to 17-V, 2-A Step-Down Converter with DCS-Control

## 1 Features

- Output voltage accuracy ± 1% over specified $T_J$ range (PWM mode)
- Input voltage range: 3 V to 17 V
- Quiescent current 18-µA typical
- Output voltage from 0.8 V to 12 V
- Adjustable soft start
- Forced PWM or PWM/PFM operation
- Switching frequency of 1.25 MHz or 2.5 MHz in forced PWM
- Precise ENABLE input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- 100% duty cycle mode
- Automatic efficiency enhancement AEE
- DCS-Control topology
- Active output discharge (TPS62148)
- HICCUP overcurrent protection (TPS62147)
- Power-good output
- Available in 2-mm × 3-mm VQFN package

## 2 Applications

- Standard 12-V rail supplies
- Mobile and embedded computers
- POL supply from multiple batteries
- Factory automation, PLC, industrial PC
- Building automation, video surveillance




**Simplified Schematic**

## 3 Description

The TPS62147 and TPS62148 are high efficiency and easy-to-use synchronous step-down DC/DC converters, based on the DCS-Control Topology. The wide input voltage range of 3-V to 17-V make the devices suitable for multi-cell Li-Ion as well as 12-V intermediate supply rails. The devices provide 2-A continuous output current. The devices automatically enter Power Save Mode at light loads to maintain high efficiency across the whole load range. With that, the devices are well suited for applications that require connected standby performance, like industrial PC and video surveillance. With the MODE pin set to low, the switching frequency is adapted automatically based on the output current and also on input and output voltage. This technique is called Automatic Efficiency Enhancement (AEE) and maintains high conversion efficiency over the whole operation range. TPS62147, TPS62148 provide a 1% output voltage accuracy in PWM mode and therefore enable the design of a power supply with high output voltage accuracy. The FSEL pin allows to set a switching frequency in forced PWM mode of 1.25 MHz or 2.5 MHz, respectively.

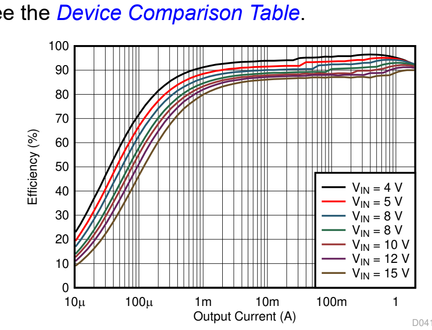
The typical quiescent current is 18 µA. In shutdown mode, the current is typically 1 µA.

The devices are available as an adjustable version, packaged in a 3-mm × 2-mm VQFN package.

**Device Information**

| PART NUMBER[2] | PACKAGE[1] | BODY SIZE (NOM) |
|---|---|---|
| TPS62147 | RGX (VQFN, 11) | 3.00 mm × 2.00 mm |
| TPS62148 | | 3.00 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See the *Device Comparison Table*.




**Efficiency vs Output Current for Vo = 3.3 V; fsw = 1.25 MHz; PFM**

## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (January 2023) to Revision B (February 2023)** **Page**

- Revision B expanded the listings shown in revision A ... 20
- Updated Figure 10-7 to the correct graph ... 20

**Changes from Revision * (April 2018) to Revision A (January 2023)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Removed trademarks from DCS-Control and AEE ... 1
- Updated Absolute Maximum Ratings table note ... 4
- Updated Figure 10-4 Efficiency vs Output current graph on page 20 ... 20
- Updated Figure 10-8 Efficiency vs Output current graph on page 21 ... 20
- Updated Figure 10-66 Switching Frequency vs Input Voltage graph on page 30 ... 20
- Updated Figure 10-68 Switching Frequency vs Input Voltage graph on page 31 ... 20
- Removed the graph “Switching Frequency vs Junction Temperature (Vout = 1.2 V, 1.8 V, PWM, FSEL= high)" on page 30 ... 20

## 5 Device Comparison Table

| DEVICE NUMBER | FEATURES | OUTPUT VOLTAGE | MARKING |
|---|---|---|---|
| TPS62147 | frequency selection on FSEL<br>HICCUP current limit | adjustable | 62147 |
| TPS62148 | frequency selection on FSEL<br>output voltage discharge | adjustable | 62148 |

## 6 Pin Configuration and Functions

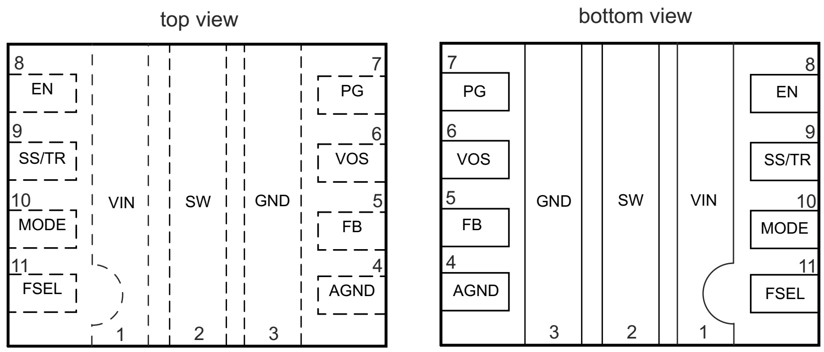



**Figure 6-1. RGX Package 11-Pin VQFN**

**Table 6-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NUMBER | NAME | | |
| 1 | VIN | I | Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN and GND. |
| 2 | SW | | Switch pin of the converter connected to the internal Power MOSFETs. |
| 3 | GND | I | Ground pin. |
| 4 | AGND | I | Connect to GND. |
| 5 | FB | I | Voltage feedback input. Connect resistive output voltage divider to this pin. |
| 6 | VOS | I | Output voltage sense pin. Connect directly to the positive pin of the output capacitor. |
| 7 | PG | O | Open drain power good output. Leave open or tie to GND if not used. |
| 8 | EN | I | Enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected. |
| 9 | SS/TR | I | Soft-start / Tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing - see *Detailed Description* section in this document. |
| 10 | MODE | I | The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. |
| 11 | FSEL | I | Switching frequency setting pin. Pull to logic low for a switching frequency of 1.25 MHz. Pull to logic high for a switching frequency of 2.5 MHz. Do not leave FSEL unconnected. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over junction temperature range of –40°C to 150°C (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage range[2] | VIN | –0.3 | 20 | V |
| | SW, VOS | –0.3 | $V_{IN}$+0.3 | V |
| | SW (transient for t<10ns)[2] | –2 | 25.5 | V |
| | EN, MODE, FSEL, PG, FB, , SS/TR | –0.3 | $V_{IN}$+0.3 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) While switching

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human Body Model - (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charge Device Model - (CDM), per JEDEC specification JESD22-C101[2] | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VIN | Supply voltage | 3 | | 17 | V |
| VOUT | Output voltage | 0.7 | | 12 | V |
| L | Effective inductance for fsw = 2.5 MHz | 0.6 | 1 | 2.9 | µH |
| L | Effective inductance for fsw = 1.25 MHz | 0.7 | 1.5 or 2.2 | 2.9 | µH |
| $C_O$ | Effective output capacitance for fsw = 2.5 MHz[1] | 6 | 22 | 200[3] | µF |
| $C_O$ | Effective output capacitance for fsw = 1.25 MHz[1] | 12 | 47 | 200[3] | µF |
| $C_I$ | Effective input capacitance[1] [2] | 3 | 10 | | µF |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) The values given for all the capacitors are effective capacitance, which includes the dc bias effect. Please check the manufacturer´s dc bias curves for the effective capacitance vs dc bias voltage applied.
(2) Larger values can be required if the source impedance can not support the transient requirements of the load.
(3) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitors. See also the systems examples *Section 10.3.2* for applications with many distributed capacitors on the output.

## 7.4 Thermal Information

| THERMAL METRIC[1] | | TPS62147, TPS62148 | UNIT |
|---|---|---|---|
| | | RGX (VQFN) | |
| | | 11 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 38.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 2.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.6 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 7.6 | °C/W |

| THERMAL METRIC[(1)] | | TPS62147, TPS62148 RGX (VQFN) 11 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

$T_J$ = –40 °C to +125 °C and $V_{IN}$ = 3 V to 17 V. Typical values at $V_{IN}$ = 12 V and $T_A$ = 25 °C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Operating Quiescent Current | EN = high, $I_{OUT}$= 0 mA, Device not switching, $T_J$= 85 °C | | | 35 | µA |
| $I_Q$ | Operating Quiescent Current | EN = high, $I_{OUT}$= 0 mA, Device not switching | | 18 | 46 | µA |
| $I_{SD}$ | Shutdown Current | EN = 0 V, Nominal value at $T_J$= 25 °C, Max value at $T_J$= 85 °C | | 1 | 8 | µA |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | Rising Input Voltage | 2.8 | 2.9 | 3.0 | V |
| | | Falling Input Voltage | 2.5 | 2.6 | 2.7 | V |
| $T_{SD}$ | Thermal Shutdown Temperature | Rising Junction Temperature | | 160 | | °C |
| | Thermal Shutdown Hysteresis | | | 20 | | |
| **CONTROL (EN, SS/TR, PG, MODE, FSEL)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage for FSEL, MODE pin | | 0.9 | | | V |
| $V_{IL}$ | Low Level Input Voltage for FSEL, MODE pin | | | | 0.3 | V |
| $V_{IH}$ | Input Threshold Voltage for EN pin; rising edge | | 0.77 | 0.8 | 0.83 | V |
| $V_{IL}$ | Input Threshold Voltage for EN pin; falling edge | | 0.67 | 0.7 | 0.73 | V |
| $I_{LKG\_EN}$ | Input Leakage Current for EN, FSEL, MODE | $V_{IH}$ = VIN or $V_{IL}$= GND | | | 100 | nA |
| $V_{TH\_PG}$ | Power Good Threshold Voltage; dc level | Rising (%$V_{OUT}$) | 93% | 96% | 98% | |
| | Hysteresis | Falling (%$V_{OUT}$) | 3% | | 4.5% | |
| $V_{OL\_PG}$ | Power Good Output Low Voltage | $I_{PG}$ = -2 mA | | 0.07 | 0.3 | V |
| $I_{LKG\_PG}$ | Input Leakage Current (PG) | $V_{PG}$ = 5 V | | | 100 | nA |
| $I_{SS/TR}$ | SS/TR pin source current | | | 2.5 | | µA |
| | $I_{SS/TR}$ tolerance | $T_J$= –40 °C to +125 °C | | ±0.2 | | µA |
| | Tracking gain | $V_{FB}$ / $V_{SS/TR}$ | | 1 | | |
| | Tracking offset | feedback voltage with $V_{SS/TR}$ = 0 V | | 11 | | mV |

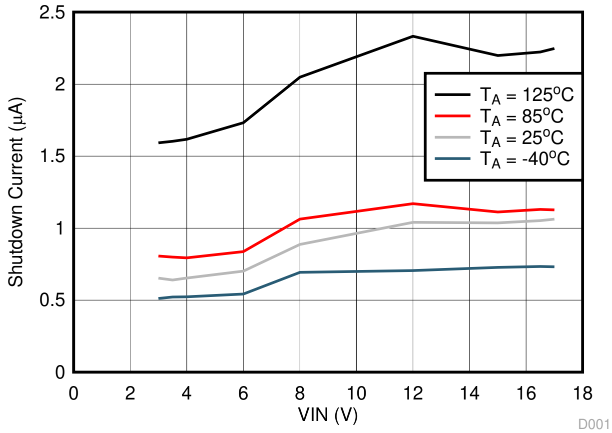
## 7.5 Electrical Characteristics (continued)

$T_J$ = –40 °C to +125 °C and $V_{IN}$ = 3 V to 17 V. Typical values at $V_{IN}$ = 12 V and $T_A$ = 25 °C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | |
| $R_{DS(ON)}$ | High-Side MOSFET ON-Resistance | $V_{IN}$ ≥ 4 V | | | 100 | 180 | mΩ |
| | Low-Side MOSFET ON-Resistance | $V_{IN}$ ≥ 4 V | | | 39 | 67 | mΩ |
| $I_{LIMH}$ | High-Side MOSFET Current Limit | dc value(2) | | 2.8 | 3.5 | 4.2 | A |
| $I_{LIML}$ | Low-Side MOSFET Current Limit | dc value(2) | | 2.8 | 3.5 | 4.2 | A |
| $I_{LIMNEG}$ | Negative current limit; average value | dc value | | | 1.5 | | A |
| **OUTPUT** | | | | | | | |
| $V_{FB}$ | Feedback Voltage | | | | 0.7 | | V |
| $I_{LKG\_FB}$ | Input Leakage Current (FB) | $V_{FB}$= 0.7 V | | | 1 | 70 | nA |
| $V_{FB}$ | Feedback Voltage Accuracy(1) | $V_{IN}$ ≥ $V_{OUT}$ +1 V | PWM mode | -1% | | 1% | |
| | | $V_{IN}$ ≥ $V_{OUT}$ +1 V; $V_{OUT}$ ≥ 1.5 V | PFM mode; Co,eff ≥ 47 µF, L = 1 µH for FSEL = high, L = 1.5 µH for FSEL = low | -1% | | 2% | |
| | | 1 V ≤ $V_{OUT}$ < 1.5 V | PFM mode; Co,eff ≥ 47 µF, L = 1 µH for FSEL = high, Co,eff ≥ 60 µF, L = 1.5 µH for FSEL = low | -1% | | 2.5% | |
| | | $V_{OUT}$ < 1 V | PFM mode; Co,eff ≥ 75 µF, L = 1 µH for FSEL = high, L = 1.5 µH for FSEL = low | -1% | | 2.5% | |
| $V_{FB}$ | Feedback Voltage Accuracy with Voltage Tracking | $V_{IN}$ ≥ $V_{OUT}$ +1 V; $V_{SS/TR}$ = 0.35 V | PWM mode | -2% | | 7.5% | |
| | Load Regulation | PWM mode operation | | | 0.05 | | %/A |
| | Line Regulation | PWM mode operation, $I_{OUT}$= 1 A, VIN ≥ Vout + 1 V or VIN ≥ 3.5 V whichever is larger | | | 0.02 | | %/V |
| | Output Discharge Resistance | | | | 100 | | Ω |
| $t_{delay}$ | Start-up Delay time | $I_O$= 0 mA, Time from EN=high to start switching; VIN applied already | | | 200 | 300 | µs |
| $t_{ramp}$ | Ramp time; SS/TR pin open | $I_O$= 0 mA, Time from first switching pulse until 95% of nominal output voltage; device not in current limit | | | 150 | | µs |

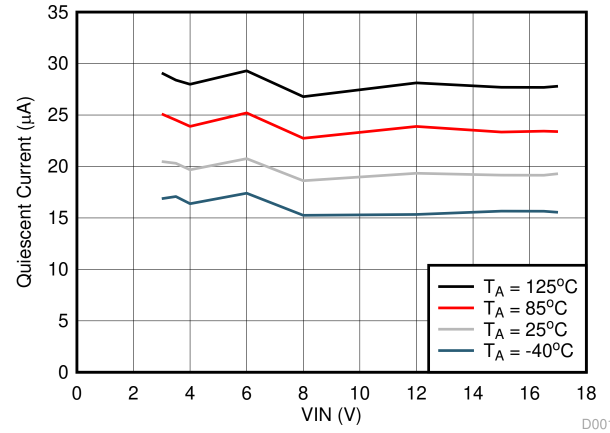
(1) The output voltage accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple (see *Pulse Width Modulation (PWM) Operation*).
(2) See also *Section 9.4.5*.

### 7.6 Typical Characteristics




EN = low

**Figure 7-1. Shutdown Current vs Input Voltage**




EN = high device not switching

**Figure 7-2. Quiescent Supply Current vs Input Voltage**

## 8 Parameter Measurement Information

### 8.1 Schematic

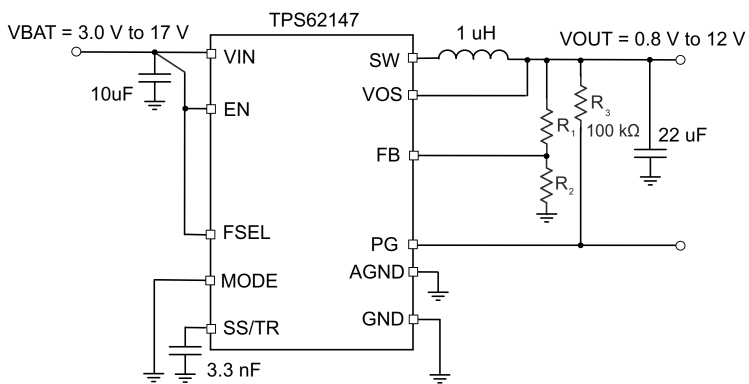



**Figure 8-1. Measurement Setup with FSEL = high**

**Table 8-1. List of Components for FSEL = high (fsw = 2.5 MHz)**

| REFERENCE | DESCRIPTION | MANUFACTURER |
|---|---|---|
| IC | 17 V, 2 A Step-Down Converter | TPS62147; Texas Instruments |
| L | 1 µH inductor | XFL4020-102; Coilcraft |
| CIN | 10 µF, 25 V, Ceramic, 0805 | TMK212BBJ106MG-T; Taiyo Yuden |
| COUT | 2 × 10 µF, 16 V, Ceramic, 0805; all VOUT except 9 V and 1.2 V | EMK212BBJ106MG-T; Taiyo Yuden |
| COUT | 3 × 10 µF, 16 V, Ceramic, 0805 for VOUT = 1.2 V | EMK212BBJ106MG-T; Taiyo Yuden |
| COUT | 4 × 10 µF, 16 V, Ceramic, 0805 for VOUT = 9 V | EMK212BBJ106MG-T; Taiyo Yuden |
| CSS | 3.3 nF, 10 V, Ceramic, X7R | - |
| R1 | Depending on Vout; see Table 10-4 | Standard 1% metal film |
| R2 | Depending on Vout; see Table 10-4 | Standard 1% metal film |
| R3 | 470 kΩ, Chip, 0603, 1/16 W, 1% | Standard 1% metal film |

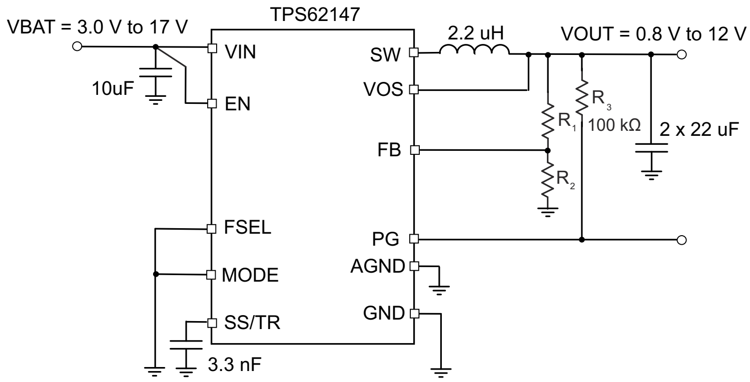



**Figure 8-2. Measurement Setup with FSEL = low**

**Table 8-2. List of Components for FSEL = low (fsw = 1.25 MHz)**

| REFERENCE | DESCRIPTION | MANUFACTURER[(1)] |
|---|---|---|
| IC | 17 V, 2 A Step-Down Converter | TPS62147; Texas Instruments |
| L | 2.2 µH inductor | XFL4020-222; Coilcraft |
| CIN | 10 µF, 25 V, Ceramic, 0805 | TMK212BBJ226MG-T; Taiyo Yuden |
| COUT | 2 × 22 µF, 16 V, Ceramic, 0805; all VOUT except 9 V and 1.2 V | EMK212BBJ226MG-T; Taiyo Yuden |
| COUT | 3 × 22 µF, 16 V, Ceramic, 0805 for VOUT = 1.2 V and VOUT = 9 V | EMK212BBJ226MG-T; Taiyo Yuden |
| CSS | 3.3 nF, 10 V, Ceramic, X7R | - |
| R1 | Depending on Vout; see Table 10-4 | Standard 1% metal film |
| R2 | Depending on Vout; see Table 10-4 | Standard 1% metal film |
| R3 | 470 kΩ, Chip, 0603, 1/16 W, 1% | Standard 1% metal film |

(1) See *Third-party Products Disclaimer*

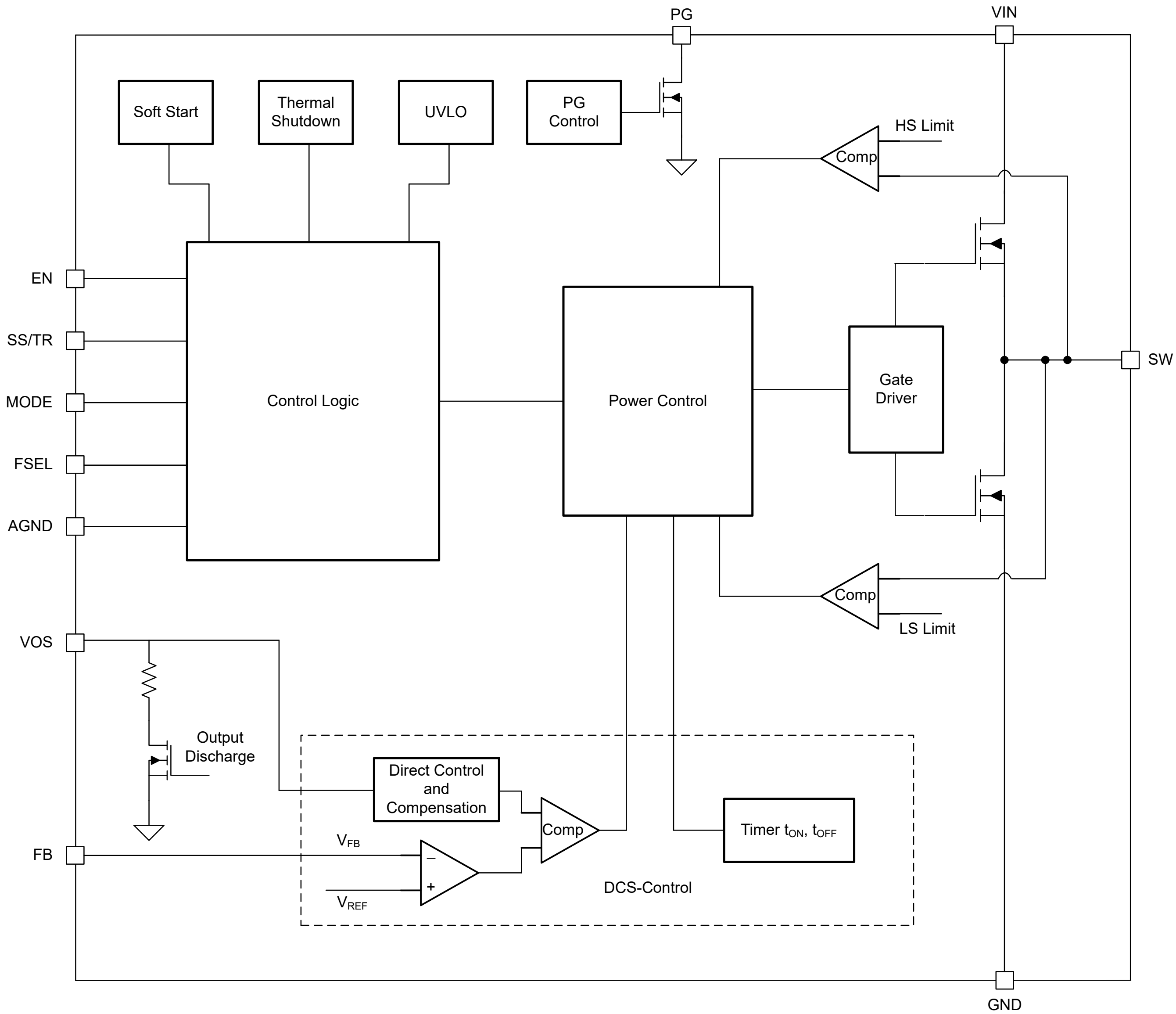
# 9 Detailed Description

## 9.1 Overview

The TPS62147, TPS62148 synchronous switched mode power converters are based on DCS-Control (Direct Control with Seamless Transition into Power Save Mode), an advanced regulation topology that combines the advantages of hysteretic, voltage mode and current mode control. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate dc load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 1.25 MHz or 2.5 MHz, depending on the setting of the FSEL pin, with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless. An internal current limit supports nominal output currents of up to 2 A. The TPS62147, TPS62148 offer both excellent dc voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

## 9.2 Functional Block Diagram




The discharge switch on the VOS pin is not available in the TPS62147.

## 9.3 Feature Description

### 9.3.1 Precise Enable

The voltage applied at the Enable pin of the TPS62147, TPS62148 is compared to a fixed threshold of 0.8 V for a rising voltage. This allows to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input allows the use as a user programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62147, TPS62148 start operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 1 µA. In this mode, the internal high side and low side MOSFETs are turned off and the entire internal control circuitry is switched off.

### 9.3.2 Power Good (PG)

The built-in power good (PG) function indicates whether the output voltage has reached its target. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor to any voltage up to a voltage level of the input voltage at VIN. It can sink 2 mA of current and maintain its specified logic low level. PG is low when the device is turned off due to EN, UVLO or thermal shutdown, so it can be used to actively discharge Vout. VIN must remain present for the PG pin to stay low.

The power good threshold in transient operation can be slightly different from the dc values given in the electrical specification in case a feed forward capacitor is used on the output voltage divider. Due to the capacitive coupling, power good can go high for a short time after a release of a short circuit on the output.

If the power good output is not used, it is recommended to tie to GND or leave open.

### 9.3.3 MODE

When MODE is set low, the device operates in PWM or PFM mode depending on the output current. Automatic Efficiency Enhancement (AEE), which scales the switching frequency based on the input voltage and the output voltage, is enabled for highest efficiency over a wide input voltage, output voltage and output current range. The MODE pin allows to force PWM mode when set high. In forced PWM mode, AEE is disabled. See also *Power Save Mode Operation (PWM/PFM)*.

### 9.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

### 9.3.5 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. If $T_J$ exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When $T_J$ decreases below the hysteresis amount of typically 20°C, the converter resumes normal operation, beginning with soft-start. During a PFM skip pause, the thermal shutdown is not active. See also *Power Save Mode Operation (PWM/PFM)*.

## 9.4 Device Functional Modes

### 9.4.1 Pulse Width Modulation (PWM) Operation

TPS62147, TPS62148 have two operating modes: Forced PWM mode discussed in this section and PWM/PFM as discussed in *Power Save Mode Operation (PWM/PFM)*.

With the MODE pin set to high, the TPS62147, TPS62148 operate with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz for FSEL = high and 1.25 MHz for FSEL = low. The frequency variation in PWM is controlled and depends on VIN, VOUT and the inductance. The on-time (TON) in forced PWM mode depends on the setting of FSEL.

For FSEL = high (2.5 MHz):

$$TON = \frac{VOUT}{VIN} \times 400[ns] \tag{1}$$

For FSEL = low (1.25 MHz):

$$TON = \frac{VOUT}{VIN} \times 800[ns] \tag{2}$$

### 9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE pin is low, Power Save Mode is allowed. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current. For improved transient response, PWM mode is forced for 8 switching cycles if the output voltage is above target due to a load release. The Power Save Mode is entered seamlessly, if the load current decreases and the MODE pin is set low. This ensures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode is seamless in both directions.

The AEE function in TPS62147, TPS62148 adjusts the on-time (TON) in power save mode depending on the input voltage and the output voltage to maintain highest efficiency. The on-time, in steady-state operation, can be estimated as follows.

For FSEL = high (2.5MHz):

$$TON = 100 \times \frac{VIN}{VIN - VOUT}[ns] \tag{3}$$

For FSEL = low (1.25MHz):

$$TON = 200 \times \frac{VIN}{VIN - VOUT}[ns] \tag{4}$$

For very small output voltages, an absolute minimum on-time of about 50 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Using TON, the typical peak inductor current in Power Save Mode is approximated by:

$$ILPSM_{(peak)} = \frac{(VIN - VOUT)}{L} \times TON \tag{5}$$

There is a minimum off-time which limits the duty cycle of the TPS62147, TPS62148. When VIN decreases to typically 15% above VOUT, the TPS62147, TPS62148 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

The output voltage ripple in power save mode is given by Equation 6:

$$\Delta V = \frac{L \times VIN^2}{200 \times C}\left(\frac{1}{VIN - VOUT} + \frac{1}{VOUT}\right) \tag{6}$$

### 9.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = VOUT / VIN and increases as the input voltage comes close to the output voltage. The minimum off-time is about 80 ns. When the minimum off-time is reached, TPS62147, TPS62148 scale down the switching frequency while they approach 100% mode. In 100% mode the high-side switch is on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences, for example for longest operation time of battery-powered applications. In 100% duty-cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$VIN_{(\min)} = VOUT + IOUT\left(R_{DS(on)} + R_L\right) \tag{7}$$

where

- IOUT is the output current,
- $R_{DS(on)}$ is the on-state resistance of the high-side FET and
- $R_L$ is the dc resistance of the inductor used.

### 9.4.4 Current Limit And Short Circuit Protection (for TPS62148)

The TPS62148 is protected against overload and short circuit events. If the inductor current exceeds the current limit I(LIMF), the high side switch is turned off and the low side switch is turned on to ramp down the inductor current. This allows it to provide the maximum current, for example, charging a large output capacitance without the must increase the soft-start time.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \tag{8}$$

where

- $I_{LIMF}$ is the static current limit as specified in the electrical characteristics
- L is the effective inductance at the peak current
- $V_L$ is the voltage across the inductor ($V_{IN}$ - $V_{OUT}$) and
- $t_{PD}$ is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{VIN - VOUT}{L} \times 50ns \tag{9}$$

### 9.4.5 HICCUP Current Limit And Short Circuit Protection (for TPS62147)

The TPS62147 is protected against overload and short circuit events. If the inductor current exceeds the current limit I(LIMF), the high side switch is turned off and the low side switch is turned on to ramp down the inductor current. After the switch current limit is triggered for 512 switching cycles, the device stops switching. After a typical delay of 800 µs, the device begins a new soft-start cycle. This is called HICCUP short circuit protection. TPS62147 repeats this mode until the short circuit condition disappears.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The equations given under *Current Limit And Short Circuit Protection (for TPS62148)* also apply.

### 9.4.6 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs then the internal reference and hence VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving SS/TR pin unconnected provides fastest startup ramp with 150 µs typically.

If the device is set to shutdown (EN = GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin of several devices must not be connected with each other.

### 9.4.7 Output Discharge Function (TPS62148 only)

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once TPS62148 has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled, in thermal shutdown or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.

### 9.4.8 Starting into a Pre-Biased Load

The TPS62147 is capable of starting into a pre-biased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS62147 does not start switching unless the voltage at the feedback pin drops to the target.

This functionality actually also applies to TPS62148 but the discharge function in TPS62148 keeps the voltage close to 0 V, so starting into a pre-biased output does not apply.

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Programming the Output Voltage

The output voltage is adjustable. It can be programmed for output voltages from 0.8 V to 12 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 0.7 V. The value of the output voltage is set by the selection of the resistor divider from Equation 10. It is recommended to choose resistor values which allow a current of at least 2 uA, meaning the value of R2 must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \times \left( \frac{VOUT}{VFB} - 1 \right) \tag{10}$$

### 10.1.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the device´s control loop. The TPS62147, TPS62148 are optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability*). Table 10-1 can be used to simplify the output filter component selection.

**Table 10-1. Recommended LC Output Filter Combinations**(1)

| | 4.7 µF | 10 µF | 22 µF | 47 µF | 100 µF | 200 µF | ≥ 400 µF |
|---|---|---|---|---|---|---|---|
| 0.68 µH | | √ | √ | √ | | | |
| 1 µH | | √ | √(2) | √ | √ | √ | √(4) |
| 1.5 µH | | √ | √ | √ | √ | √ | √(4) |
| 2.2 µH | | √ | √ | √(3) | √ | √ | √(4) |
| 3.3 µH | | | | | | | |

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications with FSEL = high.
(3) This LC combination is the standard value and recommended for most applications with FSEL = low.
(4) Output capacitance must have a ESR of ≥ 10 mΩ for stable operation, see also *Powering Multiple Loads*.

### 10.1.3 Inductor Selection

The TPS62147, TPS62148 are designed for a nominal 1-µH inductor if FSEL = high and a 1.5-uH or 2.2-uH inductor if FSEL = low. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 1 µH cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. Therefore they are not recommended at large voltages across the inductor as it is the case for high input voltages and low output voltages. With low output current in forced PWM mode this causes a larger negative inductor current peak which can exceed the negative current limit.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and dc resistance (DCR). Equation 11 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \quad (11)$$

$$\Delta I_{L(\max)} = \frac{VIN_{(\max)}}{L_{(\min)}} \times 100ns \quad (12)$$

where

- $I_L$(max) is the maximum inductor current
- $\Delta I_L$ is the Peak to Peak Inductor Ripple Current
- L(min) is the minimum effective inductor value.

Above equation is valid for FSEL = high. With FSEL = low, the ON-time is doubled from 100 ns to 200 ns so the peak inductor current doubles given the same input voltage and inductor.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS62147, TPS62148 and are recommended for use:

**Table 10-2. List of Inductors**[1]

| TYPE | INDUCTANCE [µH] | CURRENT [A][2] | DIMENSIONS [LxBxH] mm | MANUFACTURER[1] |
|---|---|---|---|---|
| XFL3012-102ME | 1.0 µH, ±20% | 2.3 | 3 x 3 x 1.3 | Coilcraft |
| XFL4015-122ME | 1.2µH, ±20% | 4.5 | 4 x 4 x 1.6 | Coilcraft |
| XFL4020-102ME | 1.0 µH, ±20% | 5.4 | 4 × 4 x 2.1 | Coilcraft |
| XFL4020-152ME | 1.5 µH, ±20% | 4.6 | 4 x 4 x 2.1 | Coilcraft |
| XFL4020-222ME | 2.2 µH, ±20% | 3.7 | 4 x 4 x 2.1 | Coilcraft |
| DFE322512F-2R2M | 2.2 µH, ±20% | 2.6 | 3.2 x 2.5 x 1.2 | Murata |
| DFE322512F-1R5M | 1.5 µH, ±20% | 3.0 | 3.2 x 2.5 x 1.2 | Murata |
| DFE322512F-1R0M | 1.0 µH, ±20% | 3.8 | 3.2 x 2.5 x 1.2 | Murata |

(1) See *Third-Party Products Disclaimer*
(2) Lower of $I_{RMS}$ at 40°C rise or $I_{SAT}$ at 30% drop.

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (13)$$

### 10.1.4 Capacitor Selection

#### *10.1.4.1 Output Capacitor*

The recommended value for the output capacitor is 22 µF with FSEL = high (fsw = 2.5 MHz) and 2 x 22 µF with FSEL = low (fsw = 1.25 MHz). The architecture of the TPS62147, TPS62148 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter dc output accuracy in Power Save Mode.

In Power Save Mode, the output voltage ripple depends on the output capacitance, its ESR, ESL and the peak inductor current. Using ceramic capacitors provides small ESR, ESL and low ripple. The output capacitor must be as close as possible to the device.

For large output voltages the dc bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

#### 10.1.4.2 Input Capacitor

For most applications, 10 µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins.

**Table 10-3. List of Capacitors**(1)

| TYPE | NOMINAL CAPACITANCE [µF] | VOLTAGE RATING [V] | SIZE | MANUFACTURER(1) |
|---|---|---|---|---|
| TMK212BBJ106MG-T | 10 | 25 | 0805 | Taiyo Yuden |
| EMK212BBJ226MG-T | 22 | 16 | 0805 | Taiyo Yuden |

(1) See *Third-Party Products Disclaimer*

#### 10.1.4.3 Soft-Start Capacitor

A capacitor connected between SS/TR pin and GND sets user programmable start-up slope of the output voltage. A constant current source provides typically 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time is given by:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{0.7V} \; [F] \tag{14}$$

where

- $C_{SS}$ is the capacitance required at the SS/TR pin and
- $t_{SS}$ is the desired soft-start ramp time

The fastest achievable typical ramp time is 150 µs even if the external $C_{ss}$ capacitance is lower than 680 pF or the pin is open.

### 10.1.5 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage with the typical gain and offset as specified in the electrical characteristics.

$$V_{FB} \approx V_{SS/TR} \tag{15}$$

When the SS/TR pin voltage is above 0.7 V, the internal voltage is clamped and the device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage in PFM mode, the device does not sink current from the output. The resulting decrease of the output voltage can therefore be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is $V_{IN}$ + 0.3 V. The SS/TR pin is internally connected with a resistor to GND when EN = 0.

If the input voltage drops below undervoltage lockout, the output voltage goes to zero, independent of the tracking voltage. Figure 10-1 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function. See also *Section 10.3.3* in the systems examples. SS/TR is internally clamped to approximately 3 V.

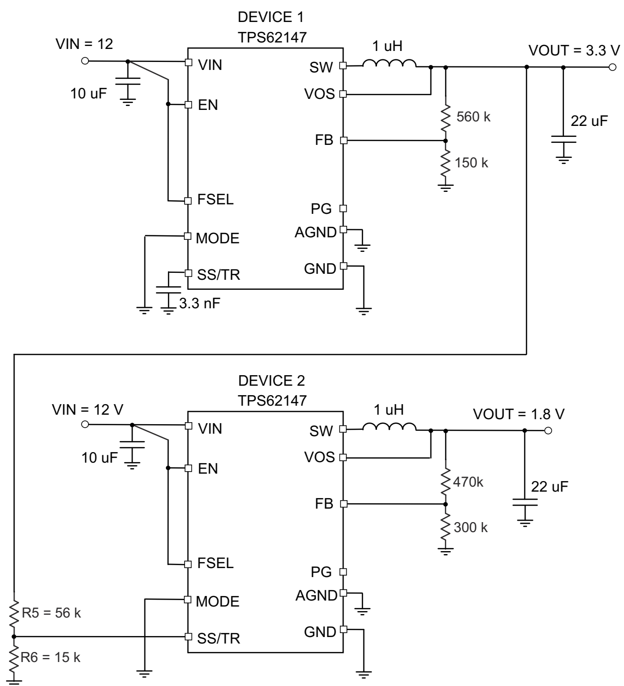



**Figure 10-1. Schematic for Ratiometric and Simultaneous Startup**

The resistive divider of R5 and R6 can be used to change the ramp rate of VOUT2 to be faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT of DEVICE 1 to the EN pin of DEVICE2. PG requires a pull-up resistor. Ratiometric start up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 14 gives the soft-start time, though the SS/TR current has to be doubled.

Note: If the voltage at the FB pin is below its typical value of 0.7 V, the output voltage accuracy can have a wider tolerance than specified. The current of 2.5 µA out of the SS/TR pin also has an influence on the tracking function, especially for high resistive external voltage dividers on the SS/TR pin.

### 10.1.6 Output Filter and Loop Stability

The TPS62147, TPS62148 are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 16:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (16)$$

Proven nominal values for inductance and ceramic capacitance are given in Table 10-1 and are recommended for use. Different values can work, but care has to be taken for the loop stability which is affected.

The TPS62147, TPS62148 include an internal 15 pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 17 and Equation 18:

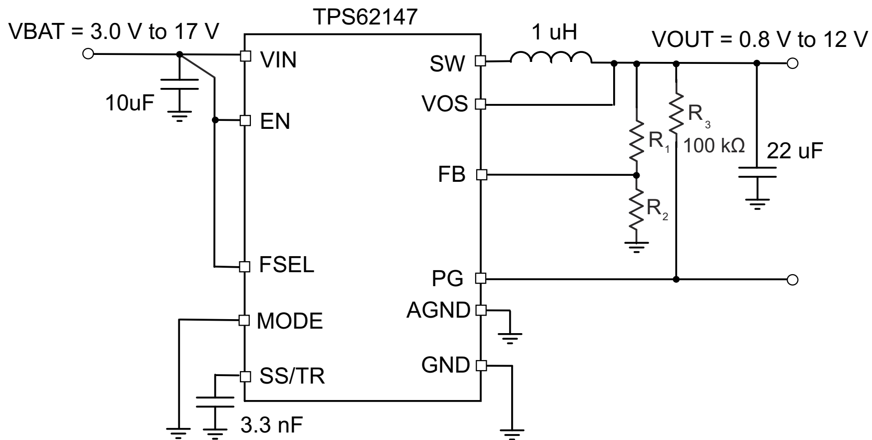
$$f_{zero} = \frac{1}{2\pi \times R_1 \times 15\,pF} \quad (17)$$

$$f_{pole} = \frac{1}{2\pi \times 15\,pF}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \quad (18)$$

Though the TPS62147, TPS62148 are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in SLVA289 and SLVA466.

## 10.2 Typical Applications

### 10.2.1 Typical Application with Adjustable Output Voltage




#### *10.2.1.1 Design Requirements*

The design guideline provides a component selection to operate the device within the recommended operating conditions. See Table 8-1 for the Bill of Materials used to generate the application curves.

#### *10.2.1.2 Detailed Design Procedure*

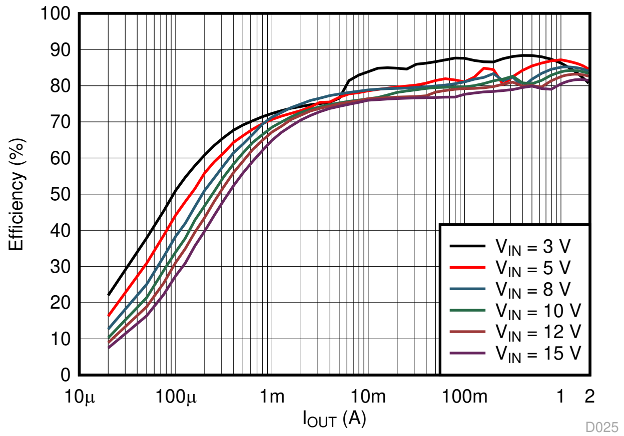
$$R_1 = R_2 \times \left( \frac{VOUT}{VFB} - 1 \right) \tag{19}$$

With VFB = 0.7 V:

**Table 10-4. Setting the Output Voltage**

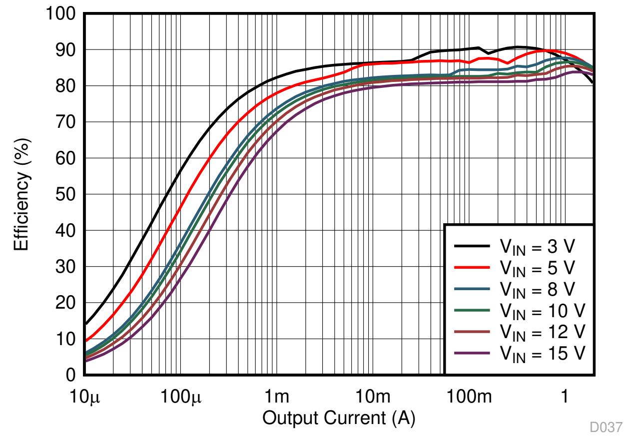
| NOMINAL OUTPUT VOLTAGE | R1 | R2 | EXACT OUTPUT VOLTAGE |
|---|---|---|---|
| 0.8 V | 51 kΩ | 360 kΩ | 0.799 V |
| 1.2 V | 130 kΩ | 180 kΩ | 1.206 V |
| 1.5 V | 150 kΩ | 130 kΩ | 1.508 V |
| 1.8 V | 470 kΩ | 300 kΩ | 1.797 V |
| 2.5 V | 620 kΩ | 240 kΩ | 2.508 V |
| 3.3 V | 560 kΩ | 150 kΩ | 3.313 V |
| 5 V | 510 kΩ | 82 kΩ | 5.054 V |
| 9 V | 510 kΩ | 43 kΩ | 9.002 V |
| 12 V | 1000 kΩ | 62 kΩ | 11.99 V |

### *10.2.1.3 Application Curves*



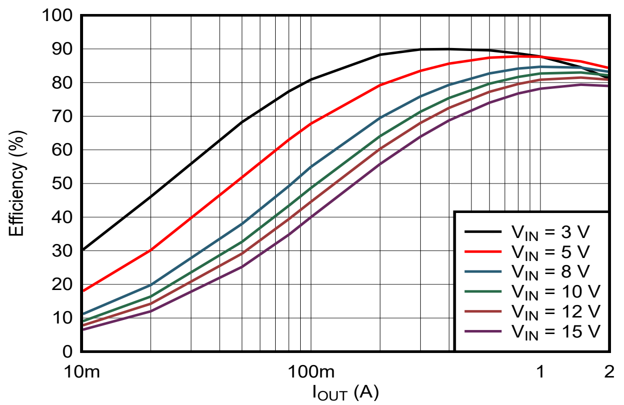

Vout = 1.2 V PFM FSEL = high $T_A$ = 25°C

**Figure 10-2. Efficiency vs Output Current**



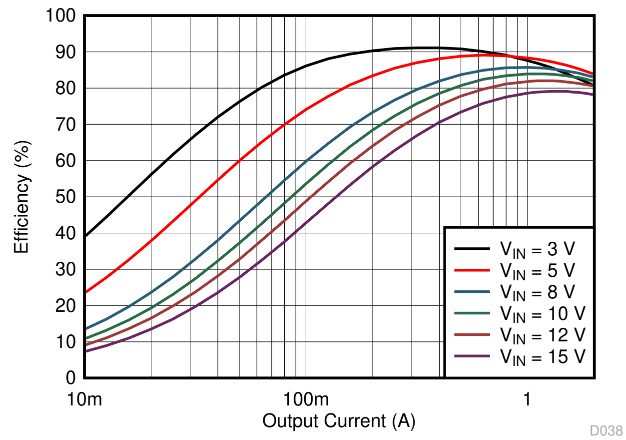

Vout = 1.2 V PFM FSEL = low $T_A$ = 25°C

**Figure 10-3. Efficiency vs Output Current**



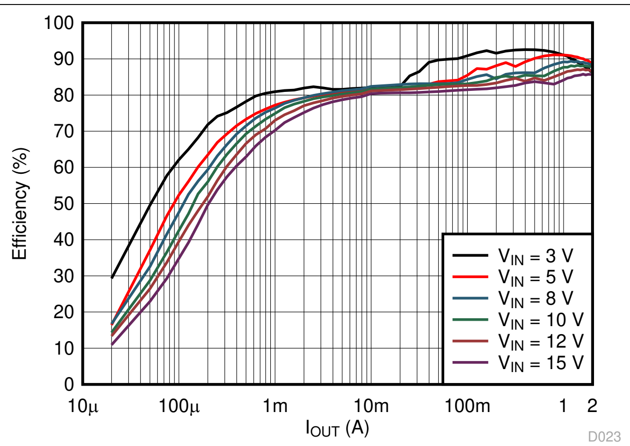

Vout = 1.2 V PWM FSEL = high $T_A$ = 25°C

**Figure 10-4. Efficiency vs Output Current**



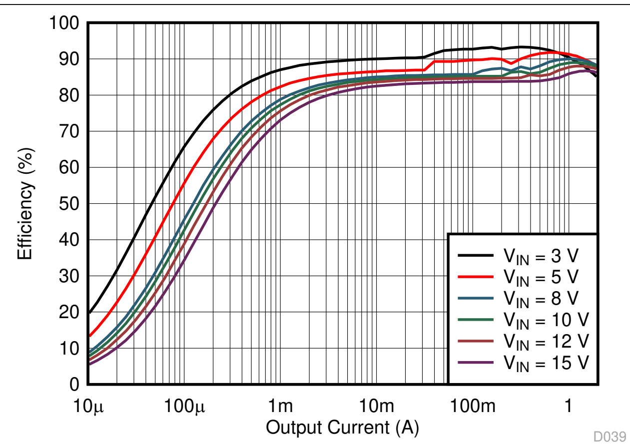

Vout = 1.2 V PWM FSEL = low $T_A$ = 25°C

**Figure 10-5. Efficiency vs Output Current**



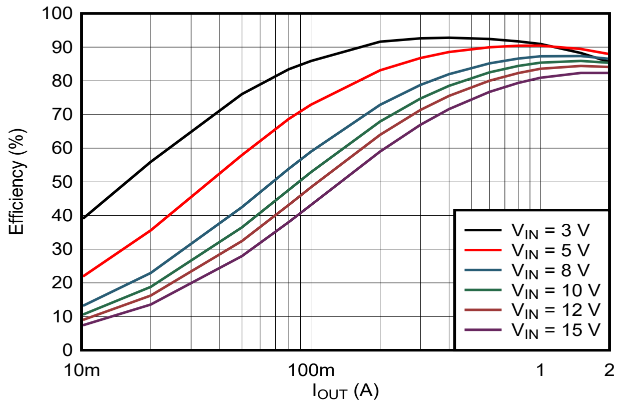

Vout = 1.8 V PFM FSEL = high $T_A$ = 25°C

**Figure 10-6. Efficiency vs Output Current**



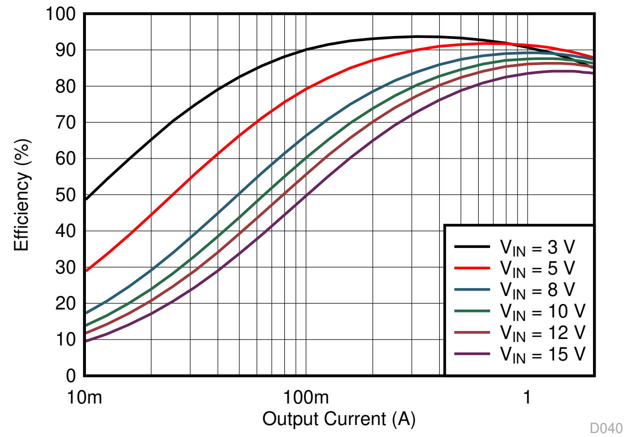

Vout = 1.8 V PFM FSEL = low $T_A$ = 25°C

**Figure 10-7. Efficiency vs Output Current**



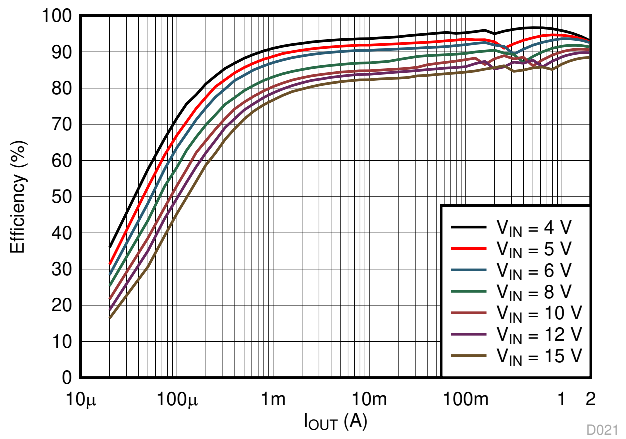

Vout = 1.8 V PWM FSEL = high $T_A$ = 25°C

**Figure 10-8. Efficiency vs Output Current**



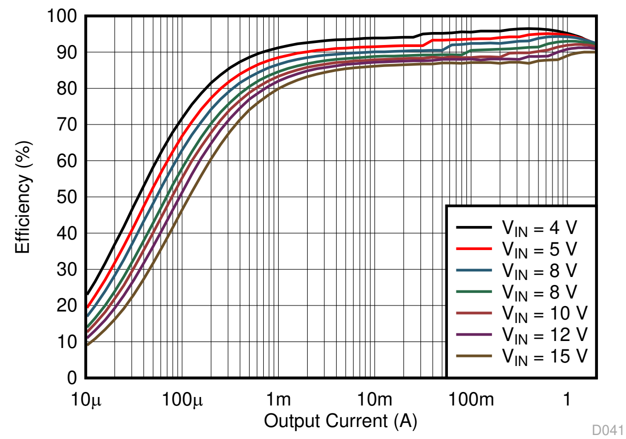

Vout = 1.8 V PWM FSEL = low $T_A$ = 25°C

**Figure 10-9. Efficiency vs Output Current**



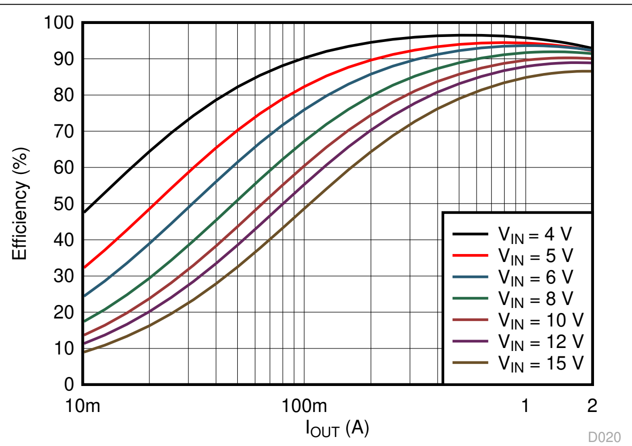

Vout = 3.3 V PFM FSEL = high $T_A$ = 25°C

**Figure 10-10. Efficiency vs Output Current**



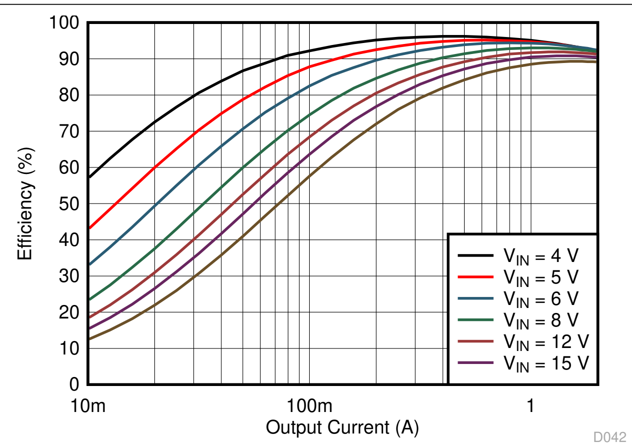

Vout = 3.3 V PFM FSEL = low $T_A$ = 25°C

**Figure 10-11. Efficiency vs Output Current**



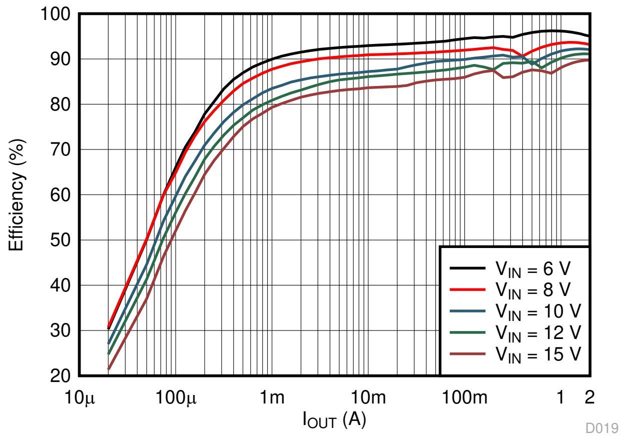

Vout = 3.3 V PWM FSEL = high $T_A$ = 25°C

**Figure 10-12. Efficiency vs Output Current**



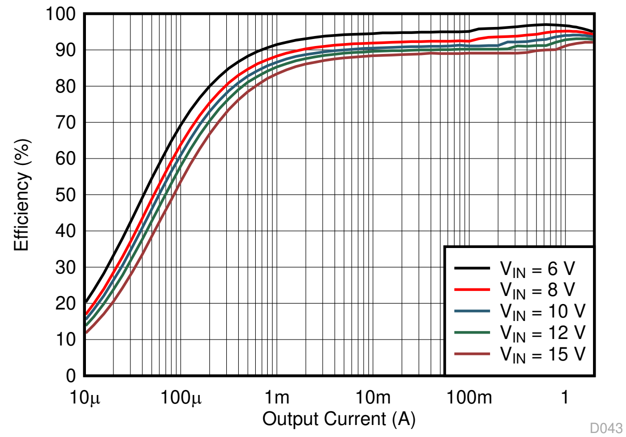

Vout = 3.3 V PWM FSEL = low $T_A$ = 25°C

**Figure 10-13. Efficiency vs Output Current**



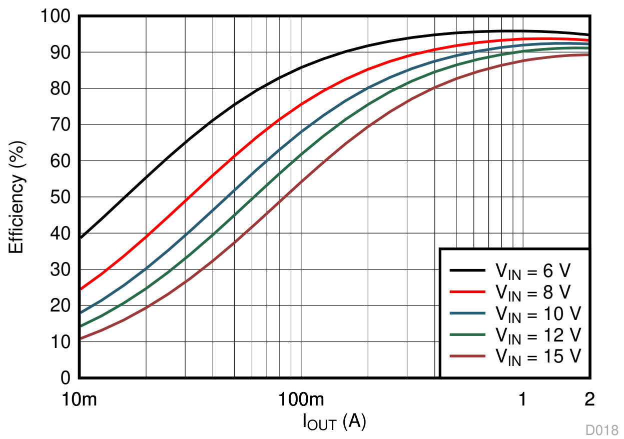

Vout = 5 V PFM FSEL = high $T_A$ = 25°C

**Figure 10-14. Efficiency vs Output Current**



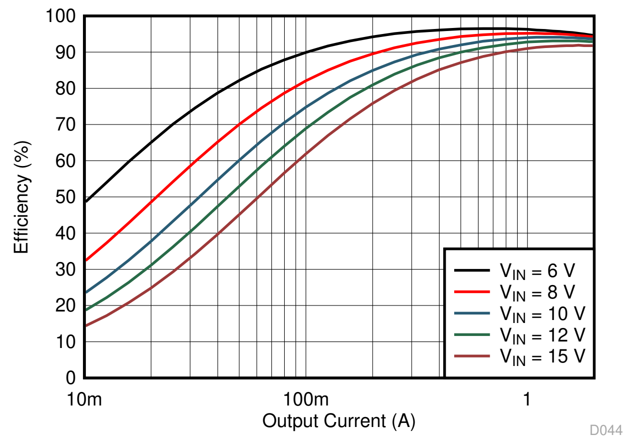

Vout = 5 V PFM FSEL = low $T_A$ = 25°C

**Figure 10-15. Efficiency vs Output Current**



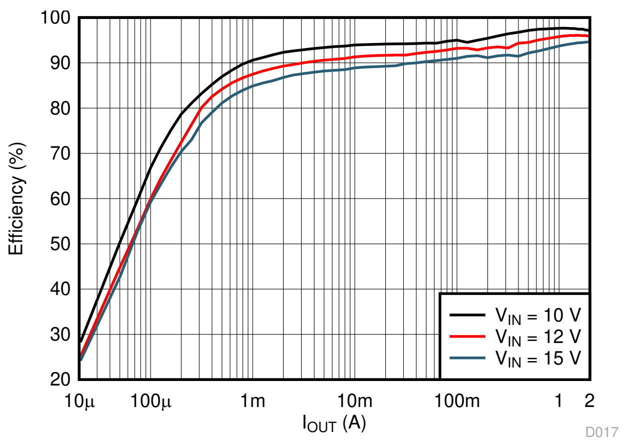

Vout = 5 V PWM FSEL = high $T_A$ = 25°C

**Figure 10-16. Efficiency vs Output Current**



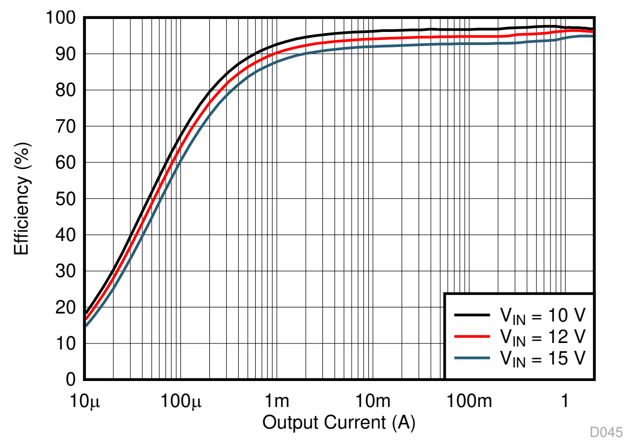

Vout = 5 V PWM FSEL = low $T_A$ = 25°C

**Figure 10-17. Efficiency vs Output Current**



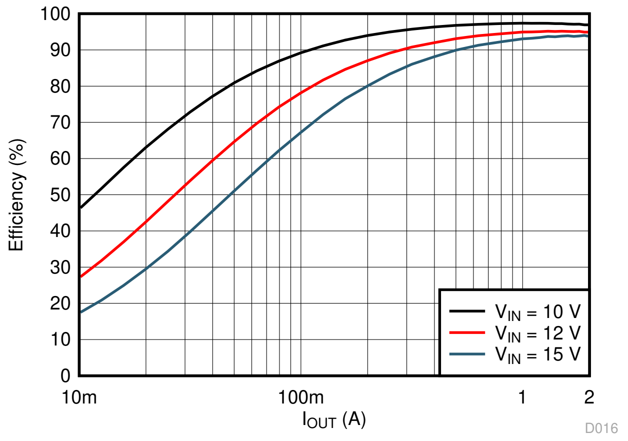

Vout = 9 V PFM FSEL = high $T_A$ = 25°C

**Figure 10-18. Efficiency vs Output Current**



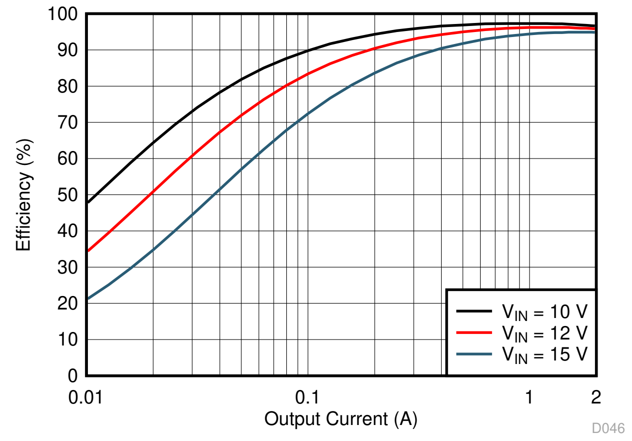

Vout = 9 V PFM FSEL = low $T_A$ = 25°C

**Figure 10-19. Efficiency vs Output Current**



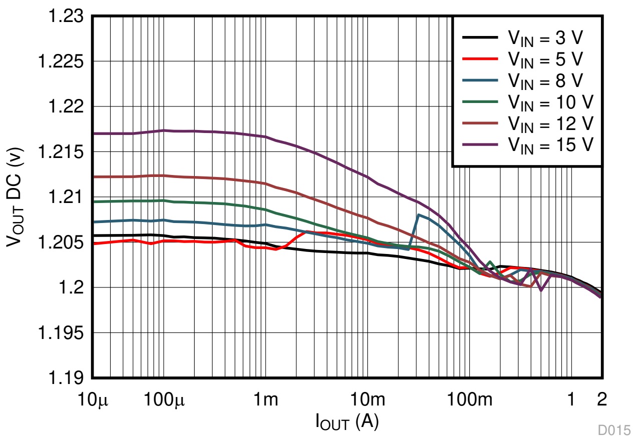

Vout = 9 V PWM FSEL = high $T_A$ = 25°C

**Figure 10-20. Efficiency vs Output Current**



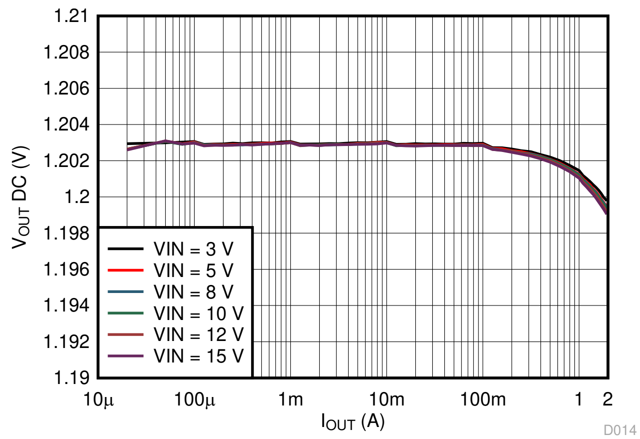

Vout = 9 V PWM FSEL = low $T_A$ = 25°C

**Figure 10-21. Efficiency vs Output Current**



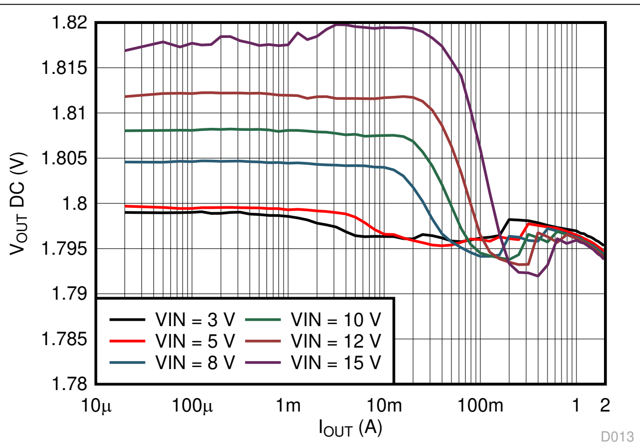

Vout = 1.2 V PFM $T_A$ = 25°C

**Figure 10-22. Output Voltage vs Output Current**



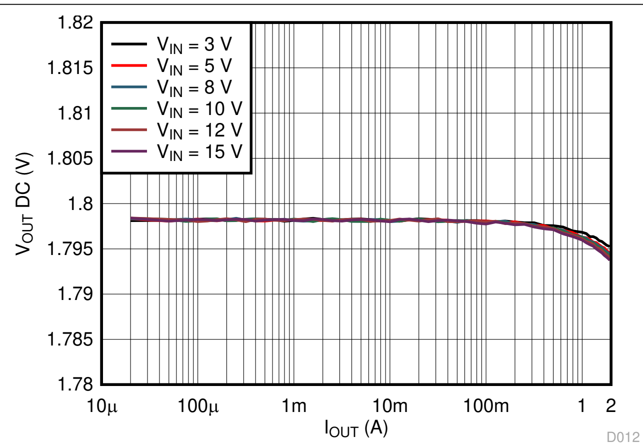

Vout = 1.2 V PWM $T_A$ = 25°C

**Figure 10-23. Output Voltage vs Output Current**



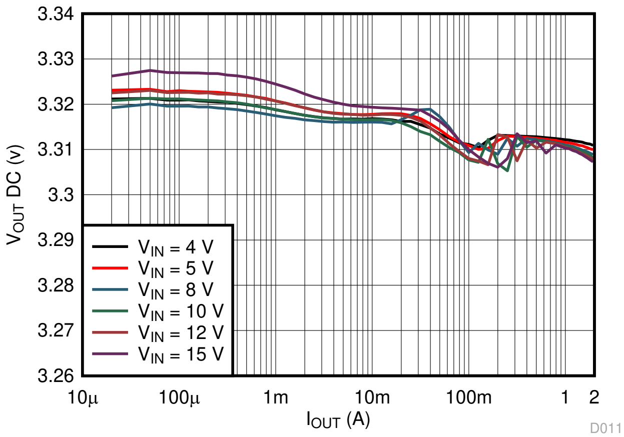

Vout = 1.8 V PFM $T_A$ = 25°C

**Figure 10-24. Output Voltage vs Output Current**



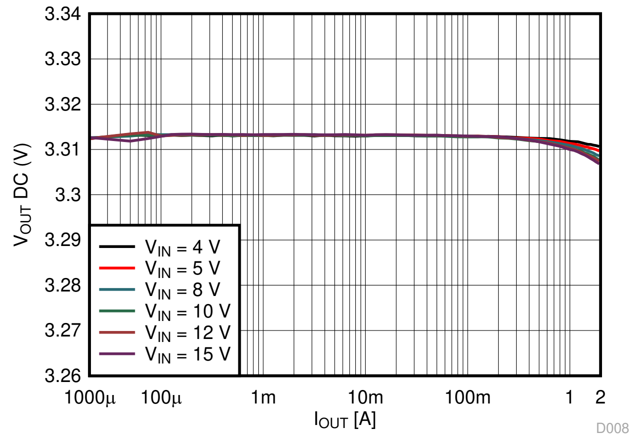

Vout = 1.8 V PWM $T_A$ = 25°C

**Figure 10-25. Output Voltage vs Output Current**



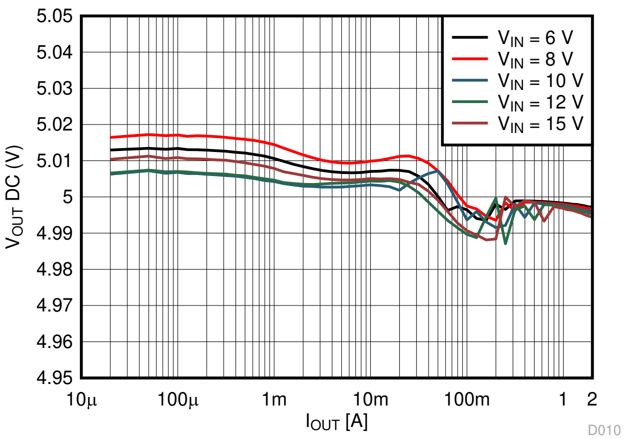

Vout = 3.3 V PFM $T_A$ = 25°C

**Figure 10-26. Output Voltage vs Output Current**



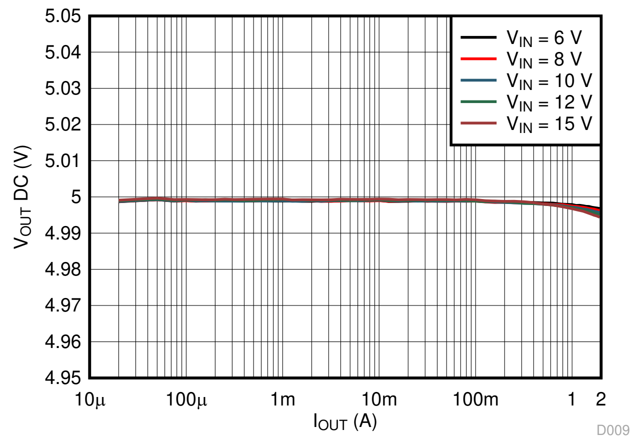

Vout = 3.3 V PWM $T_A$ = 25°C

**Figure 10-27. Output Voltage vs Output Current**



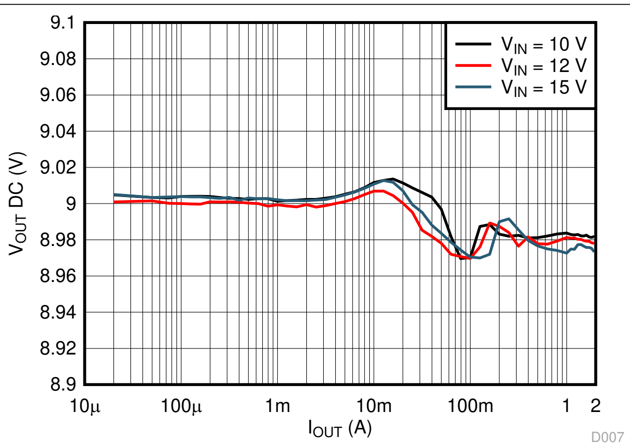

Vout = 5 V PFM $T_A$ = 25°C

**Figure 10-28. Output Voltage vs Output Current**



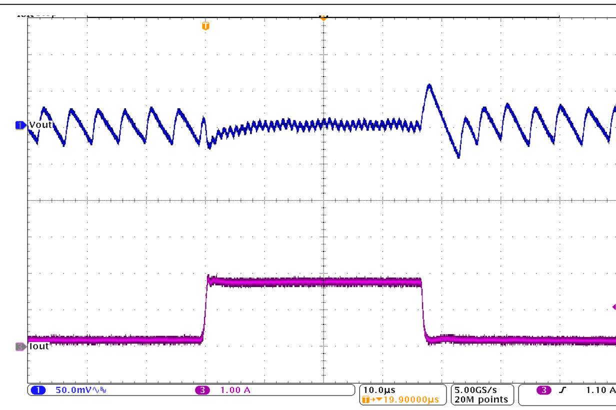

Vout = 5 V PWM $T_A$ = 25°C

**Figure 10-29. Output Voltage vs Output Current**



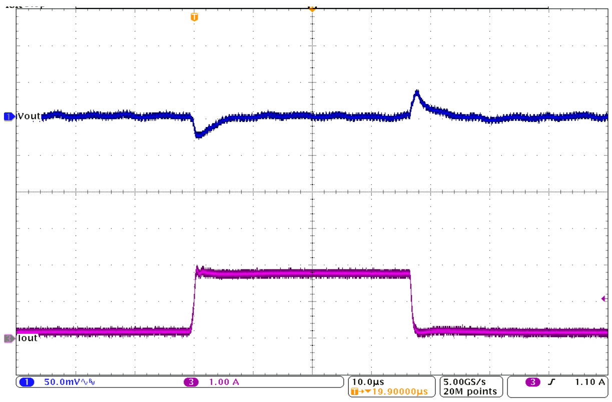

Vout = 9 V PFM $T_A$ = 25°C

**Figure 10-30. Output Voltage vs Output Current**



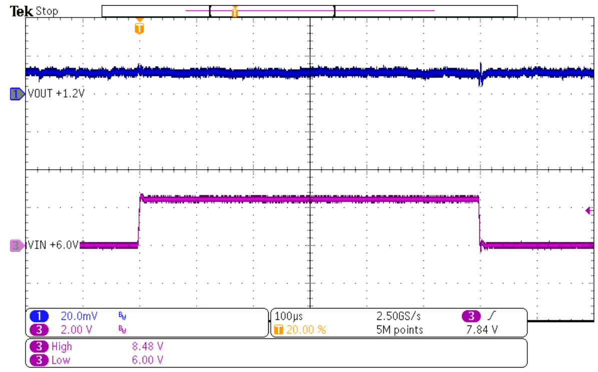

Vin = 12 V; PFM Io = 200 mA to 1.8 A;
Vout = 1.2 V; FSEL = high $T_A$= 25 °C

**Figure 10-31. Load Transient Response**



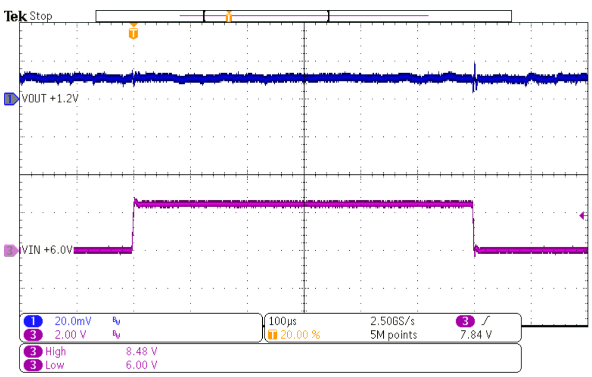

Vin = 12 V; PWM Io = 200 mA to 1.8 A
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-32. Load Transient Response**



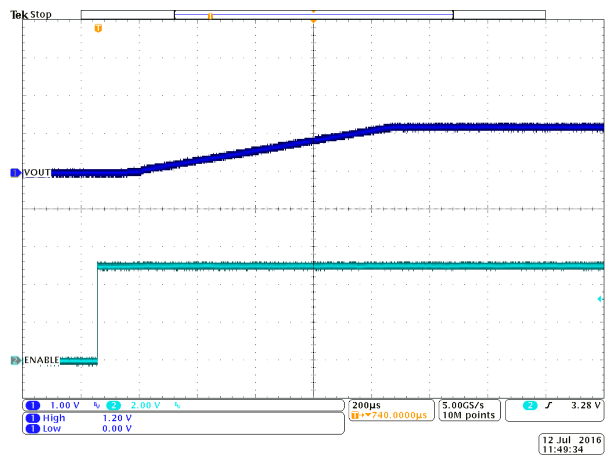

Vin = 6 V to 8.4 V; PFM Io = 1 A
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-33. Line Transient Response**



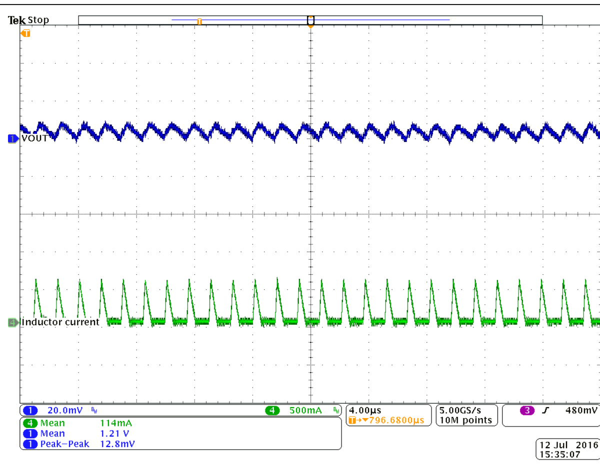

Vin = 6 V to 8.4 V; PWM Io = 1 A
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-34. Line Transient Response**



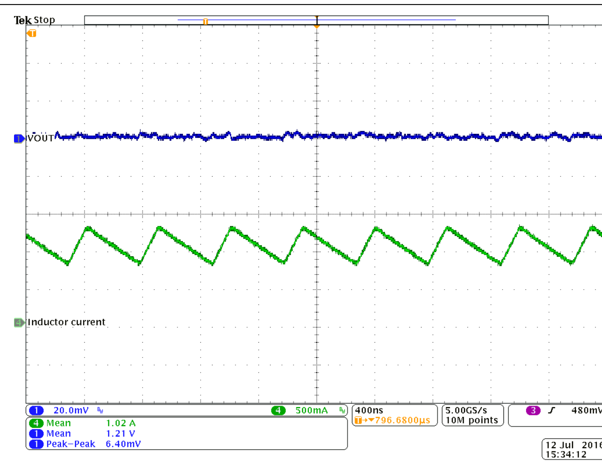

Vin = 5 V; PFM Rload = 1 kΩ
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-35. Start-Up Timing**



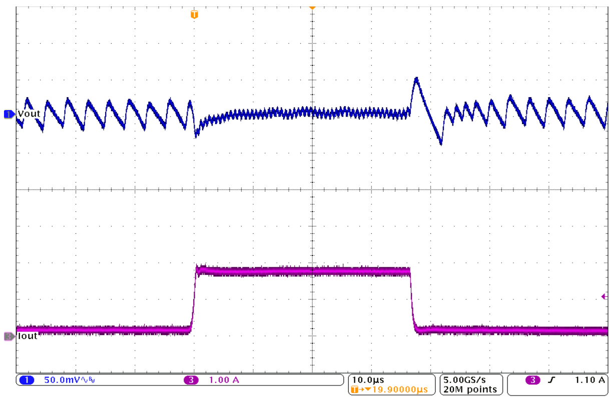

Vin = 5 V; PFM Io = 0.1 A
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-36. Output Voltage Ripple**



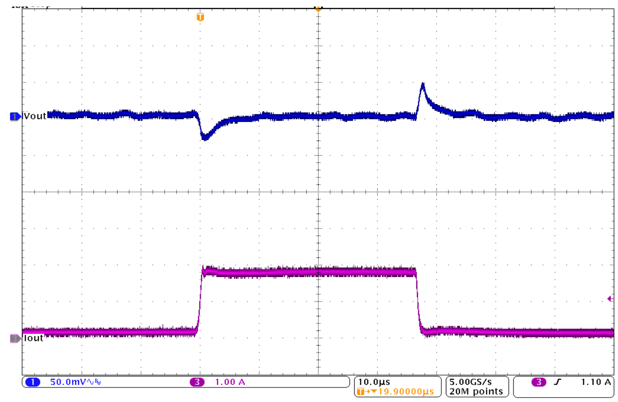

Vin = 5 V; PWM Io = 1 A
Vout = 1.2 V FSEL = high $T_A$= 25 °C

**Figure 10-37. Output Voltage Ripple**



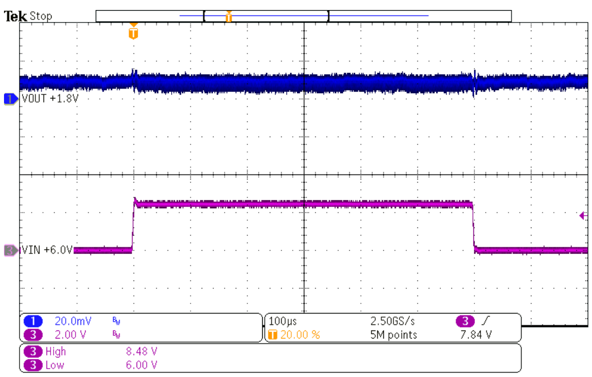

Vin = 12 V PFM Io = 200 mA to 1.8 A
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-38. Load Transient Response**



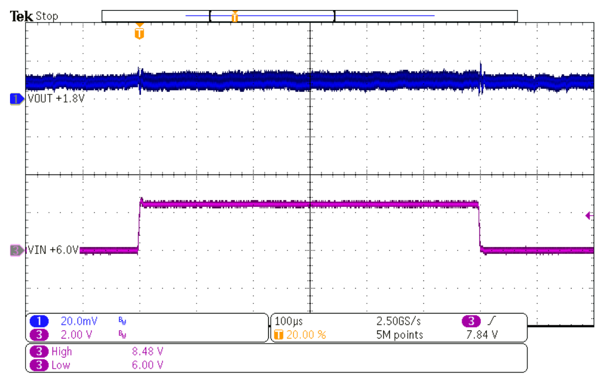

Vin = 12 V PWM Io = 200 mA to 1.8 A
Vout = 1.8 V FSEL = high $T_A$= 25°C

**Figure 10-39. Load Transient Response**



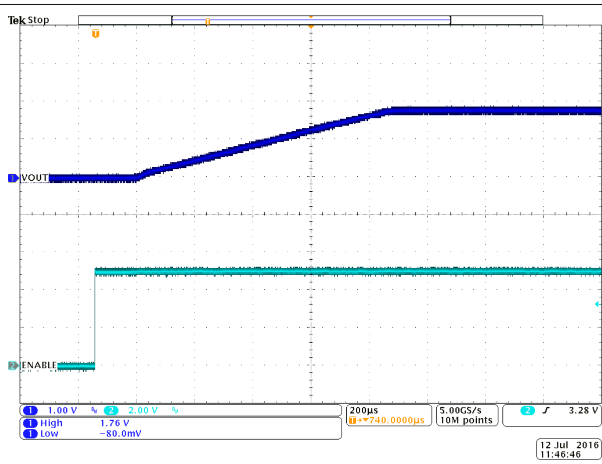

Vin = 6 V to 8.4 V; PFM Io = 1 A
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-40. Line Transient Response**



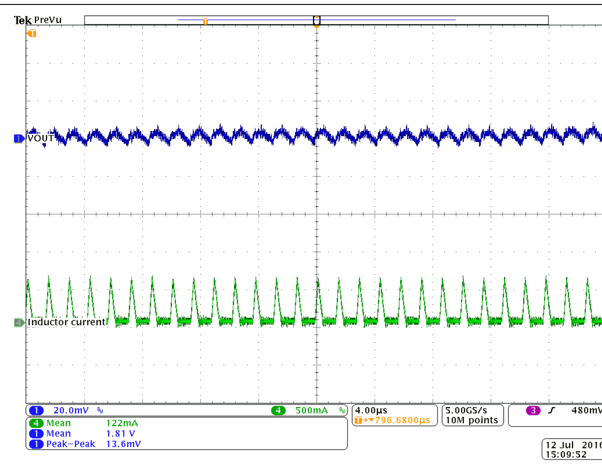

Vin = 6 V to 8.4 V; PWM Io = 1 A
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-41. Line Transient Response**



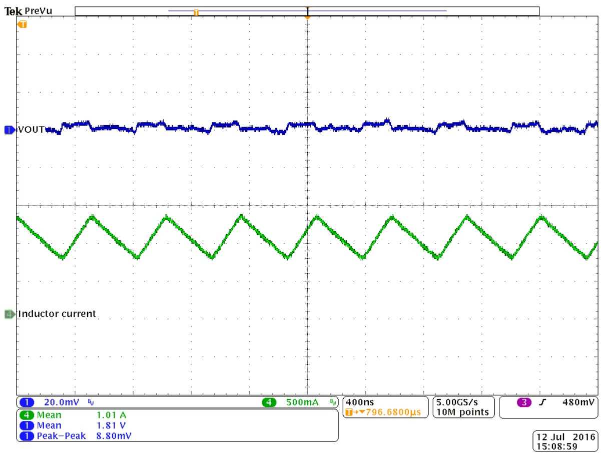

Vin = 5 V PWM Rload = 1 kΩ
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-42. Start-Up Timing**



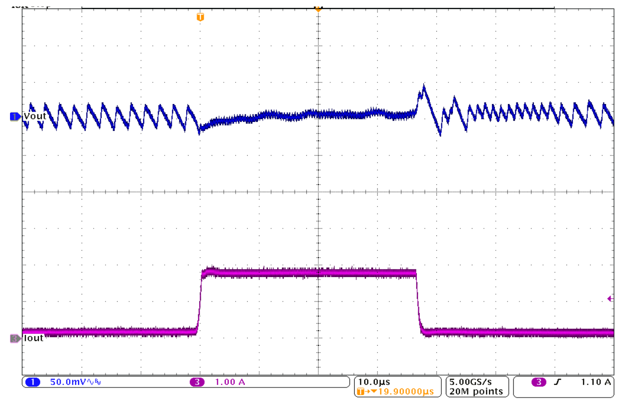

Vin = 5 V PFM Io = 0.1 A
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-43. Output Voltage Ripple**



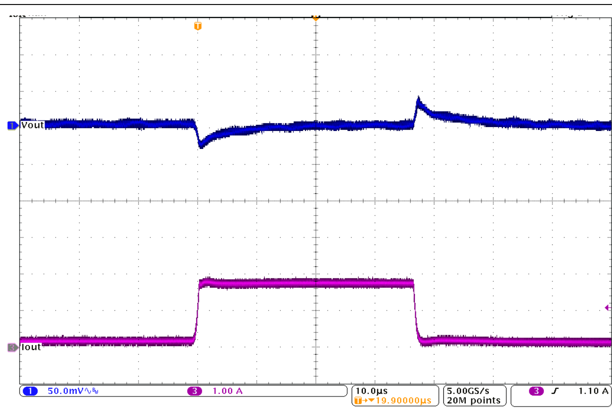

Vin = 5 V PWM Io = 1 A
Vout = 1.8 V FSEL = high $T_A$= 25 °C

**Figure 10-44. Output Voltage Ripple**



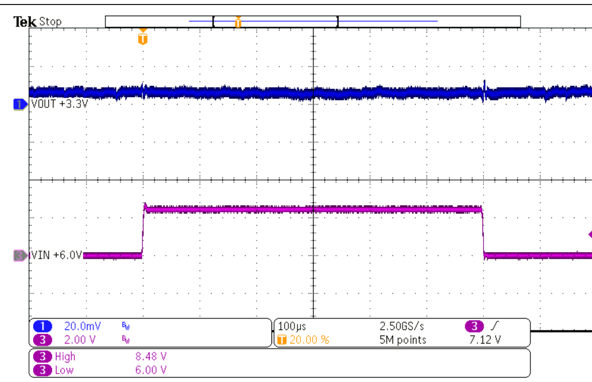

Vin = 12 V PFM Io = 200 mA to 1.8 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-45. Load Transient Response**



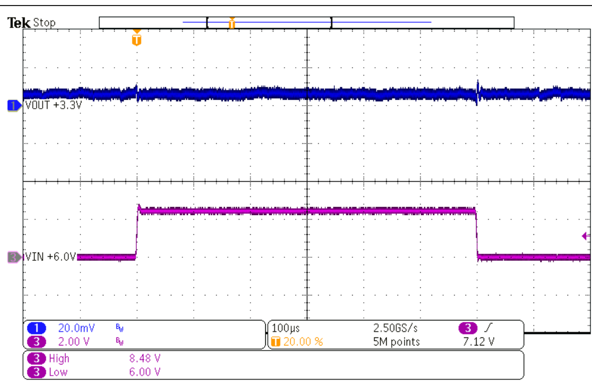

Vin = 12 V PWM Io = 200 mA to 1.8 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-46. Load Transient Response**



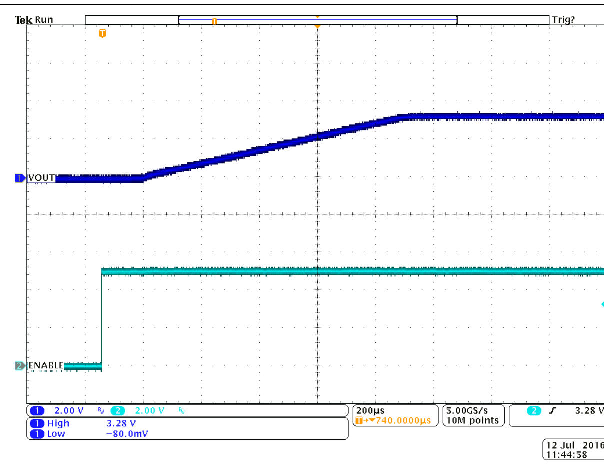

Vin = 6 V to 8.4 V; PFM Io = 1 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-47. Line Transient Response**



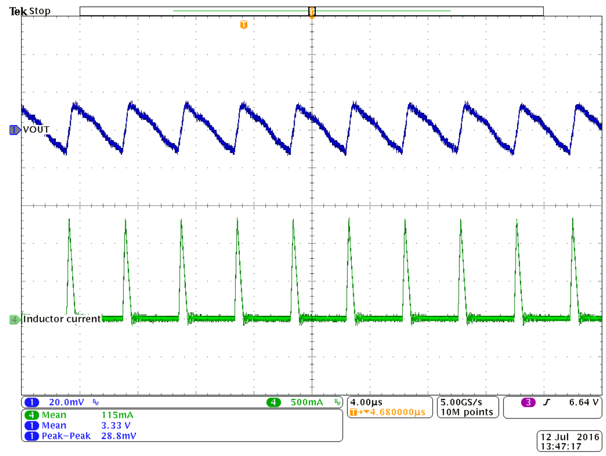

Vin = 6 V to 8.4 V; PWM Io = 1 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-48. Line Transient Response**



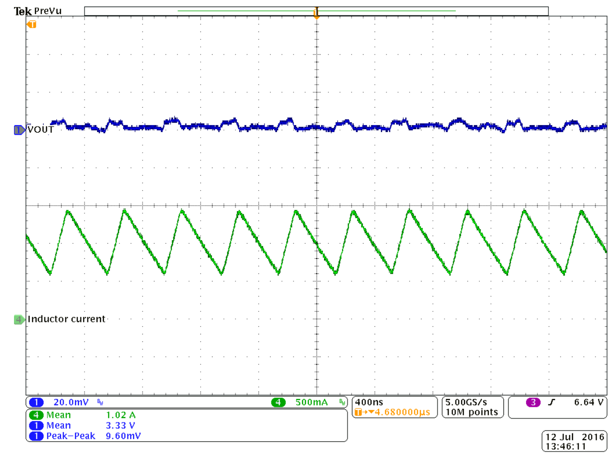

Vin = 5V PWM Rload = 1 kΩ
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-49. Start-Up Timing**



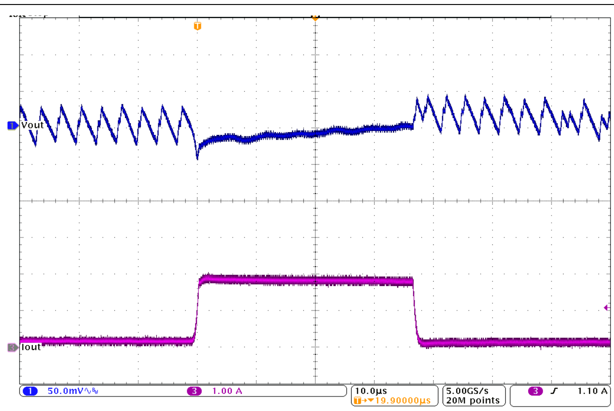

Vin = 12 V PFM Io = 0.1 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-50. Output Voltage Ripple**



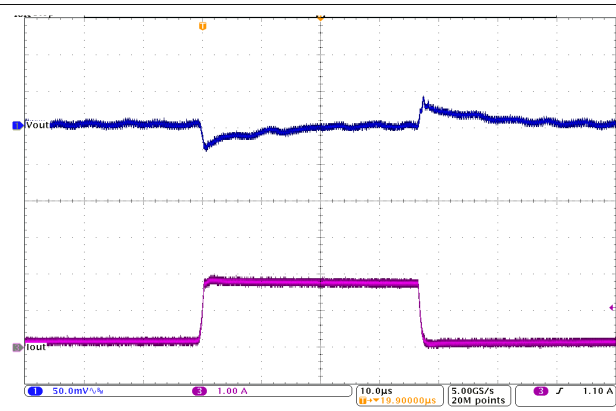

Vin = 12 V PWM Io = 1 A
Vout = 3.3 V FSEL = high $T_A$= 25 °C

**Figure 10-51. Output Voltage Ripple**



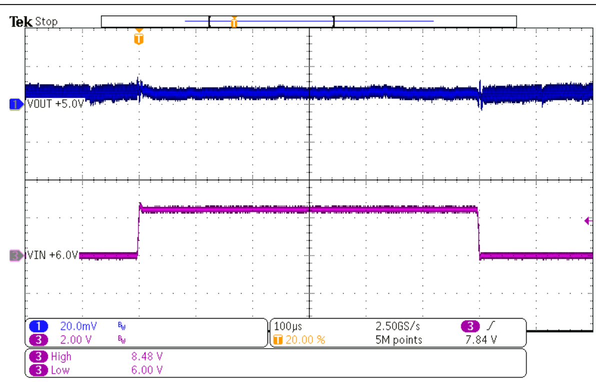

Vin = 12 V PFM Io = 200 mA to 1.8 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-52. Load Transient Response**



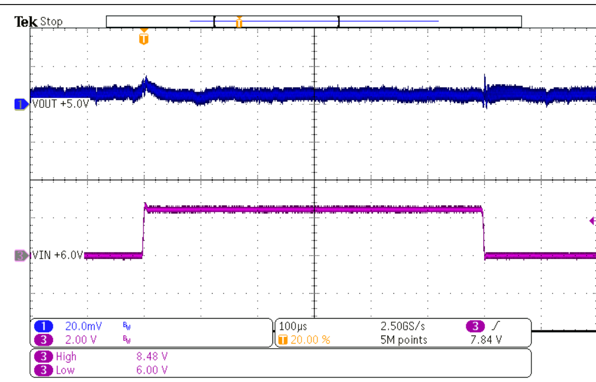

Vin = 12 V PWM Io = 200 mA to 1.8 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-53. Load Transient Response**



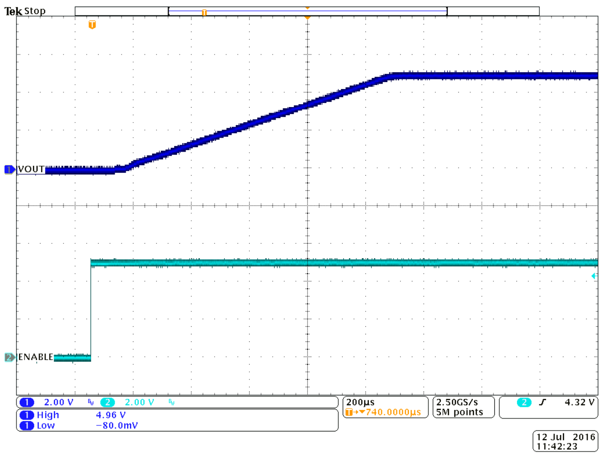

Vin = 6 V to 8.4 V; PFM Io = 1 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-54. Line Transient Response**



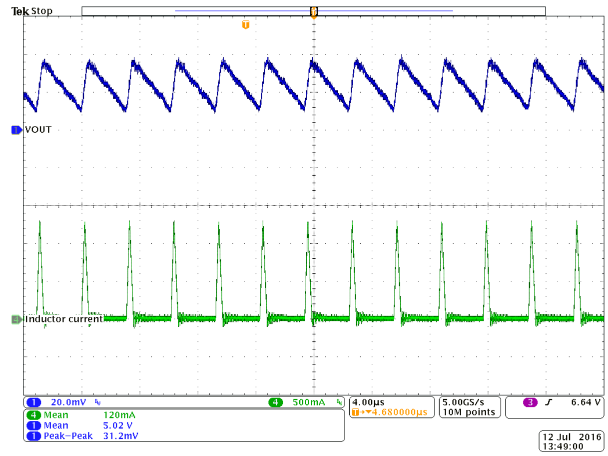

Vin = 6 V to 8.4 V; PWM Io = 1 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-55. Line Transient Response**



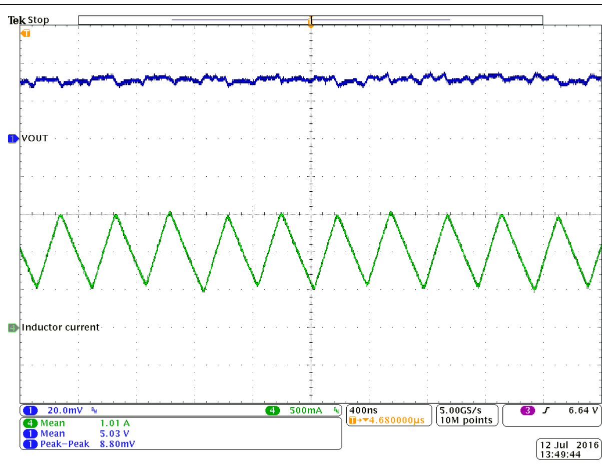

Vin = 12 V PWM Rload = 1 kΩ
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-56. Start-Up Timing**



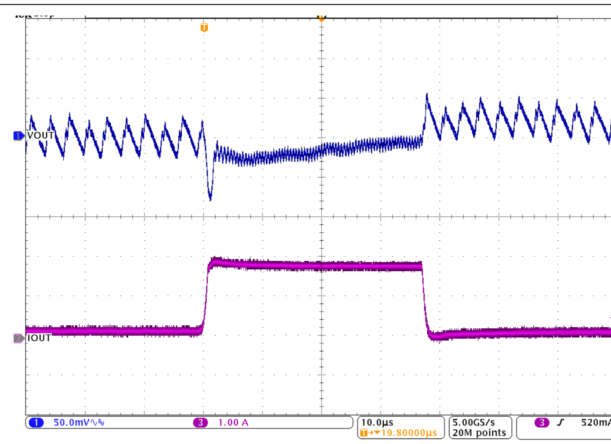

Vin = 12 V PFM Io = 0.1 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-57. Output Voltage Ripple**



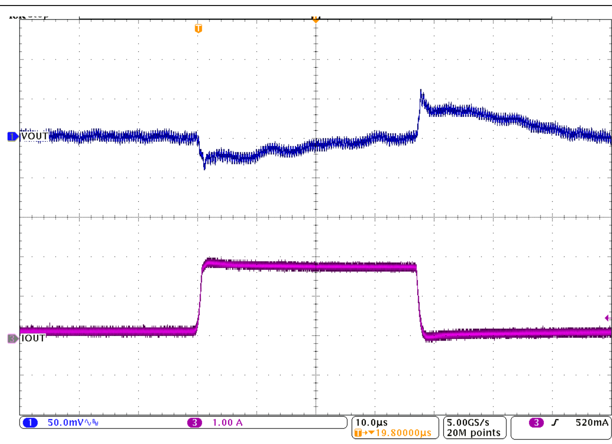

Vin = 12 V PWM Io = 1 A
Vout = 5 V FSEL = high $T_A$= 25 °C

**Figure 10-58. Output Voltage Ripple**



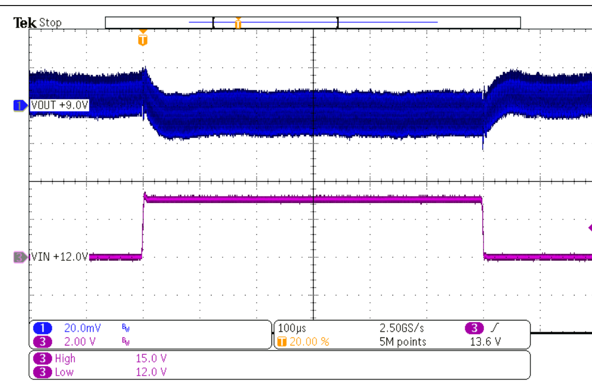

Vin = 12 V PFM Io = 200 mA to 1.8 A
Vout = 9 V FSEL = high $T_A$= 25 °C

**Figure 10-59. Load Transient Response**



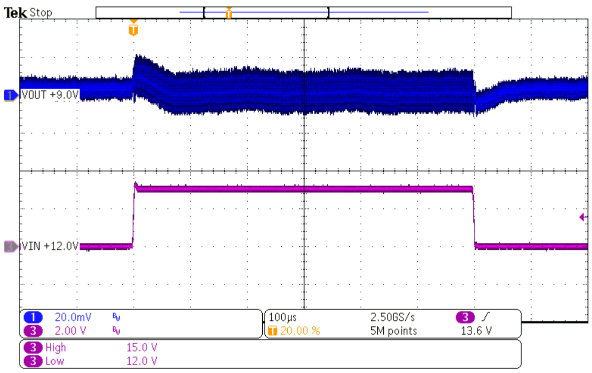

Vin = 12 V PWM Io = 200 mA to 1.8 A
Vout = 9 V FSEL = high $T_A$= 25 °C

**Figure 10-60. Load Transient Response**



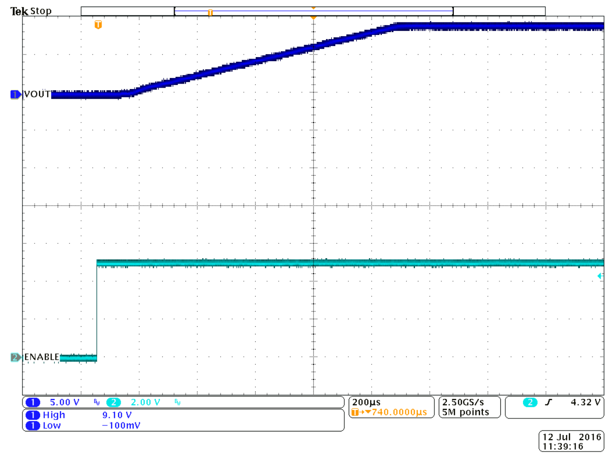

Vin = 12 V to 15 V; PFM Io = 1 A
Vout = 9 V FSEL = high $T_A$= 25 °C

**Figure 10-61. Line Transient Response**



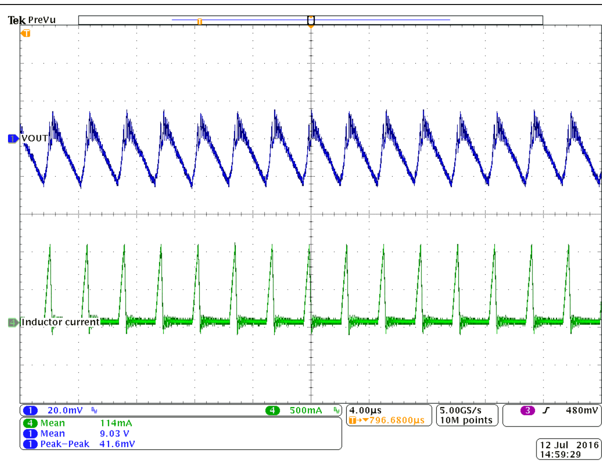

Vin = 12 V to 15 V; Vout = 9 V | PWM FSEL = high | Io = 1 A $T_A$= 25 °C

**Figure 10-62. Line Transient Response**



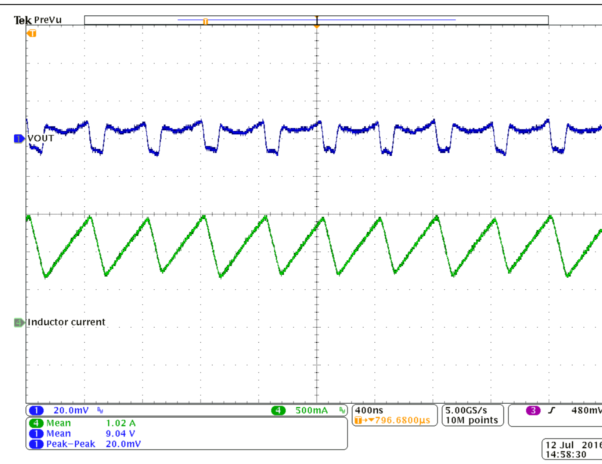

Vin = 12 V Vout = 9 V | PWM FSEL = high | Rload = 1 kΩ $T_A$= 25 °C

**Figure 10-63. Start-Up Timing**



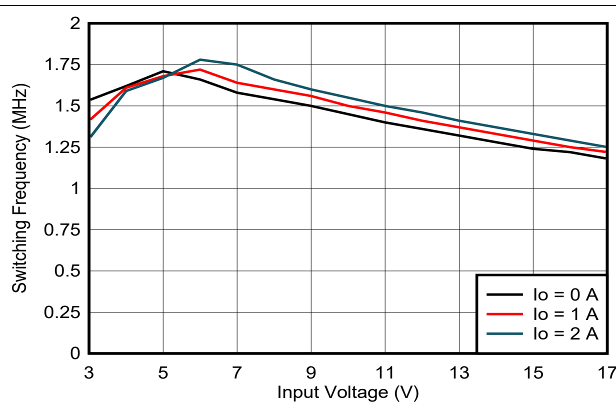

Vin = 12 V Vout = 9 V | PFM FSEL = high | Io = 0.1 A $T_A$= 25 °C

**Figure 10-64. Output Voltage Ripple**



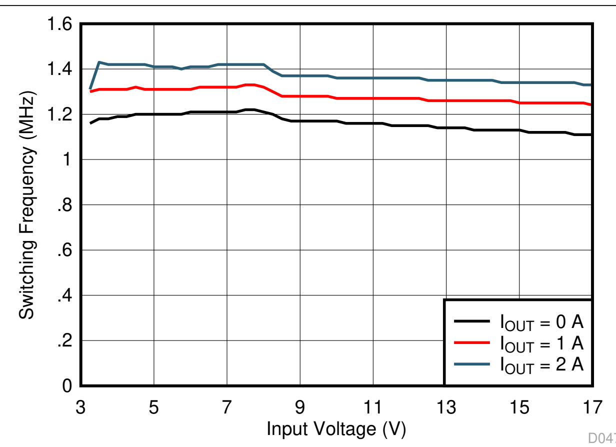

Vin = 12 V Vout = 9 V | PWM FSEL = high | Io = 1 A $T_A$= 25 °C

**Figure 10-65. Output Voltage Ripple**



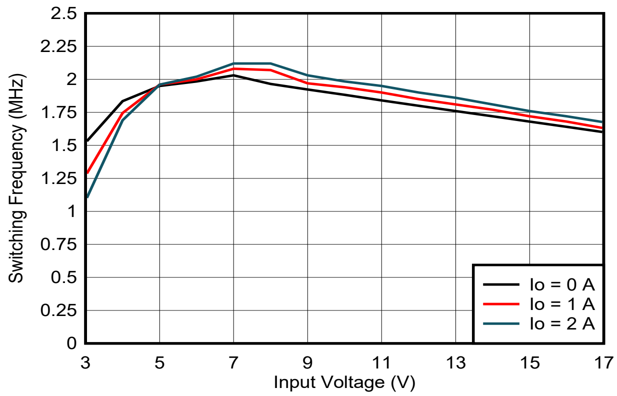

Vout = 1.2 V | PWM FSEL = high | $T_A$= 25 °C

**Figure 10-66. Switching Frequency vs Input Voltage**



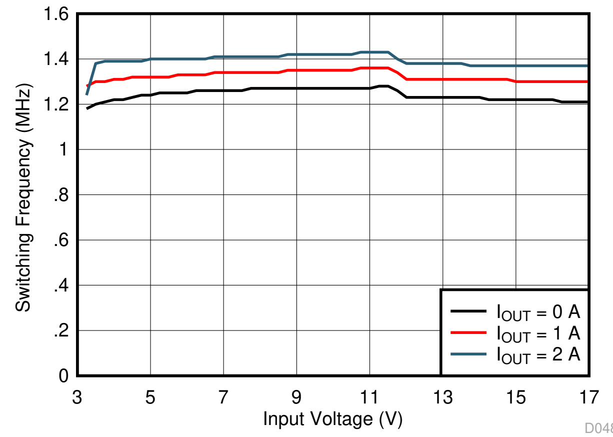

Vout = 1.2 V | PWM FSEL = low | $T_A$= 25 °C

**Figure 10-67. Switching Frequency vs Input Voltage**



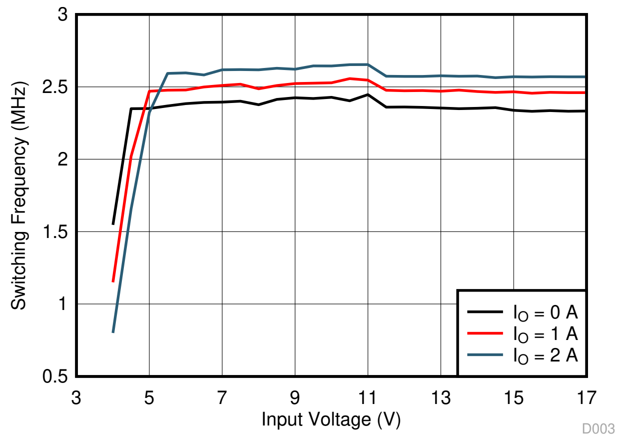

Vout = 1.8 V PWM FSEL = high $T_A$= 25 °C

**Figure 10-68. Switching Frequency vs Input Voltage**



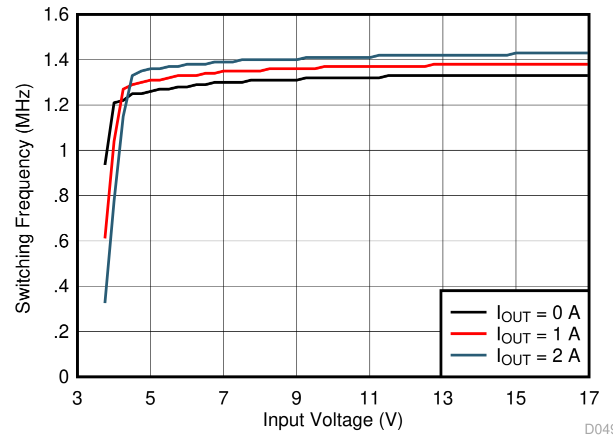

Vout = 1.8 V PWM FSEL = low $T_A$= 25 °C

**Figure 10-69. Switching Frequency vs Input Voltage**



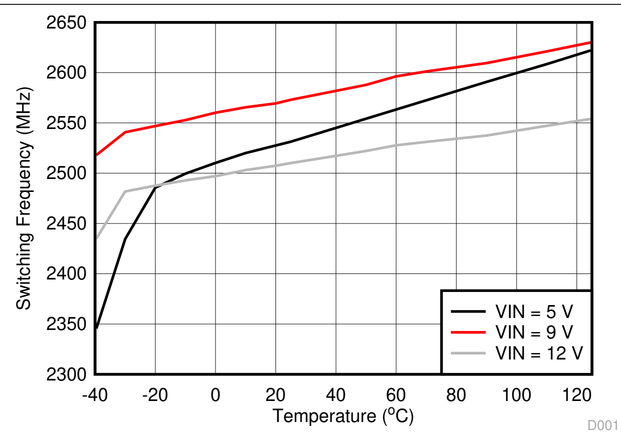

Vout = 3.3 V PWM FSEL = high $T_A$= 25 °C

**Figure 10-70. Switching Frequency vs Input Voltage**



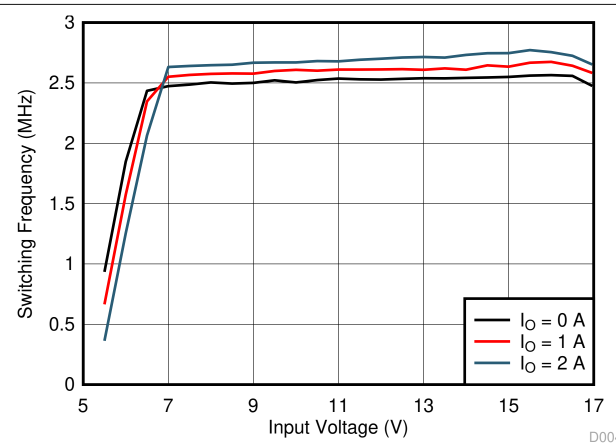

Vout = 3.3 V PWM FSEL = low $T_A$= 25 °C

**Figure 10-71. Switching Frequency vs Input Voltage**



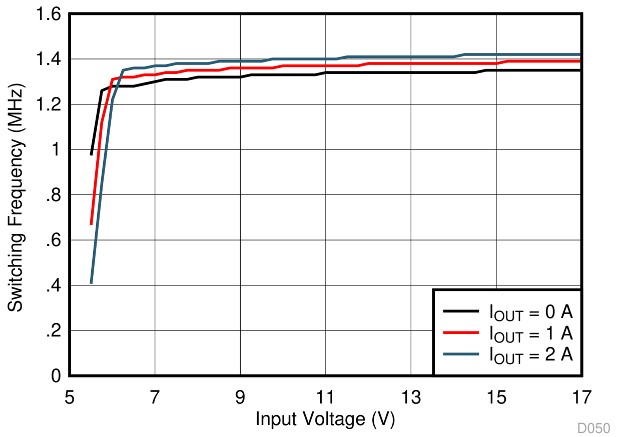

Vout = 3.3 V PWM FSEL = high Iout = 1 A

**Figure 10-72. Switching Frequency vs Junction Temperature**



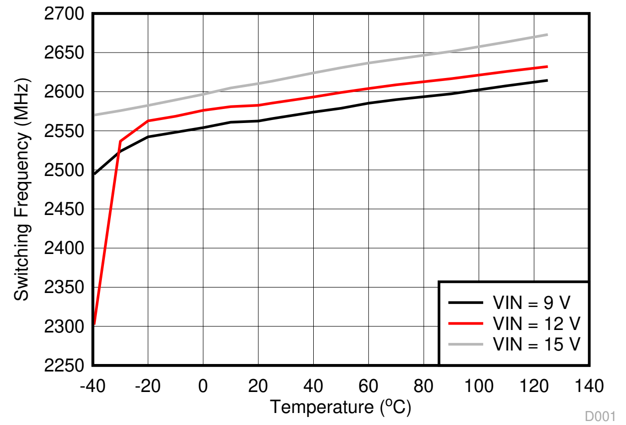

Vout = 5 V PWM FSEL = high $T_A$= 25 °C

**Figure 10-73. Switching Frequency vs Input Voltage**



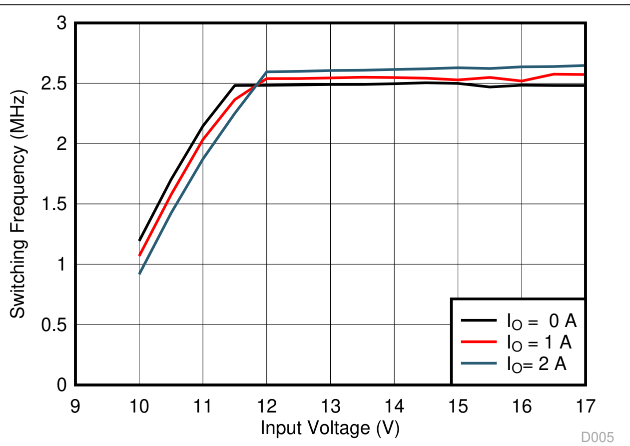

Vout = 5 V PWM FSEL = low $T_A$= 25 °C

**Figure 10-74. Switching Frequency vs Input Voltage**



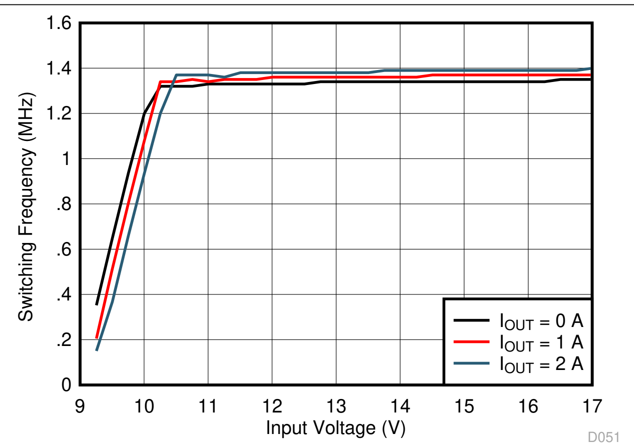

Vout = 5 V PWM FSEL = high Iout = 1 A

**Figure 10-75. Switching Frequency vs Junction Temperature**



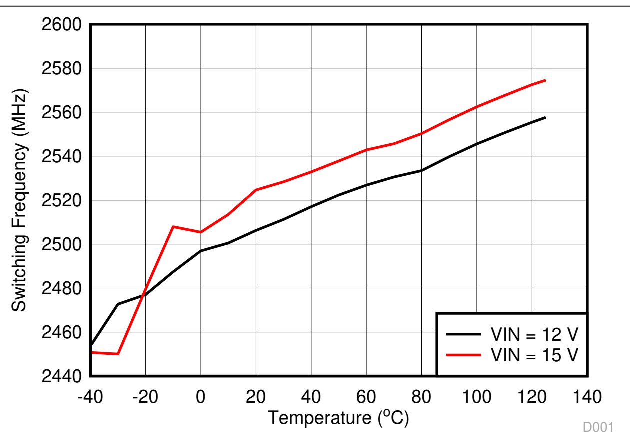

Vout = 9 V PWM FSEL = high $T_A$= 25 °C

**Figure 10-76. Switching Frequency vs Input Voltage**




Vout = 9 V PWM FSEL = low $T_A$= 25 °C

**Figure 10-77. Switching Frequency vs Input Voltage**




Vout = 9.0 V PWM FSEL = high Iout = 1 A

**Figure 10-78. Switching Frequency vs Junction Temperature**

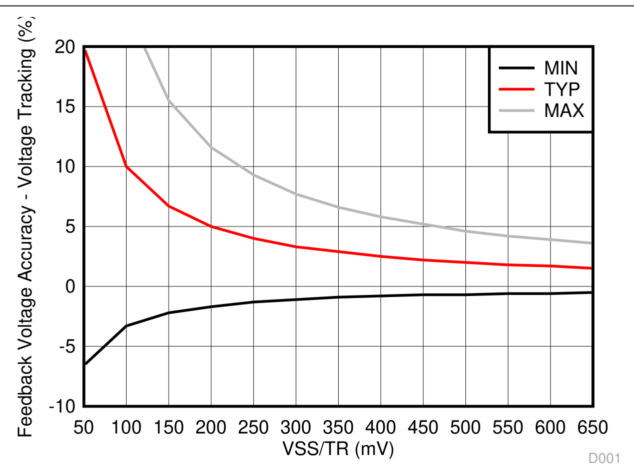



**Figure 10-79. Feedback Voltage Accuracy with Voltage Tracking vs Voltage at VSS/TR**

## 10.3 System Examples

### 10.3.1 LED Power Supply

The TPS62147, TPS62148 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Because this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 20. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62147, TPS62148.

Figure 10-80 shows an application circuit, tested with analog dimming:

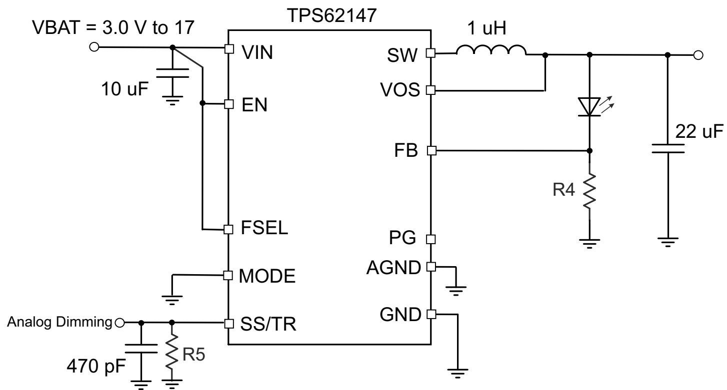



**Figure 10-80. Single Power LED Supply**

The resistor at SS/TR defines the FB voltage. It is set to 350 mV by R5 = 140 kΩ using Equation 20. This cuts the losses on R4 to half from the nominal 0.7 V of feedback voltage while it still provides good accuracy.

$$V_{FB} = 2.5\mu A \times R_{SS/TR} + 11mV \tag{20}$$

The device supplies a constant current set by resistor R4 from FB to GND. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

### 10.3.2 Powering Multiple Loads

In applications where TPS62147, TPS62148 are used to power multiple load circuits, it can be the case that the total capacitance on the output is very large. To properly regulate the output voltage, there must be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low ESR ceramic capacitors, the output voltage ripple can get very low, so it is not recommended to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a pcb, these loads are typically distributed across the board. This adds enough trace resistance ($R_{trace}$) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is 10 mΩ. The total capacitance n × Cin in the use case below was 32 × 47 uF of ceramic X7R capacitors.

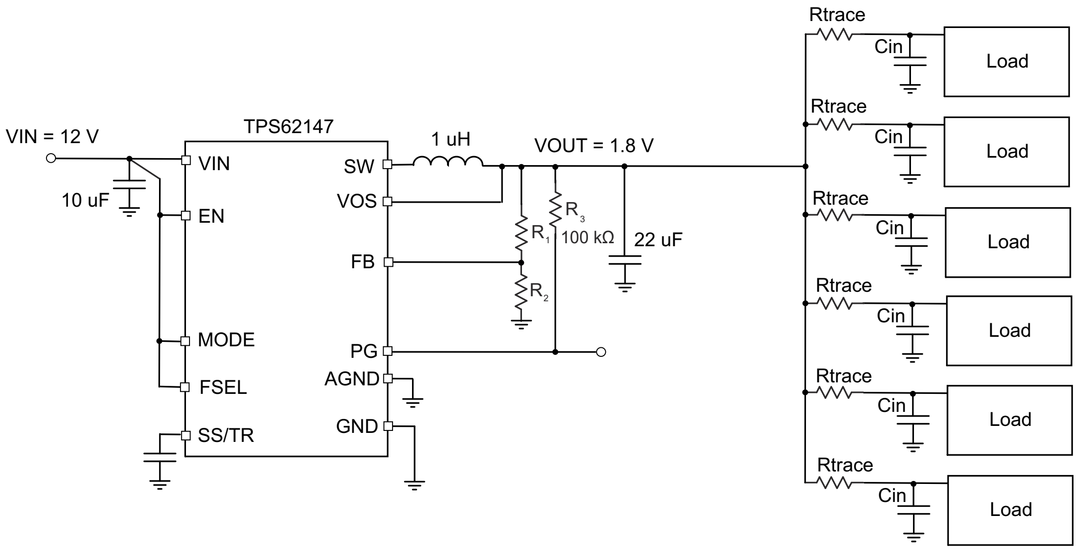



**Figure 10-81. Multiple Loads**

### 10.3.3 Voltage Tracking

DEVICE 2 follows the voltage applied to the SS/TR pin. A ramp on SS/TR to 0.7 V ramps the output voltage according to the 0.7 V reference.

Tracking the 3.3 V of DEVICE 1 requires a resistor divider on SS/TR of DEVICE 2 equal to the output voltage divider of DEVICE 1.

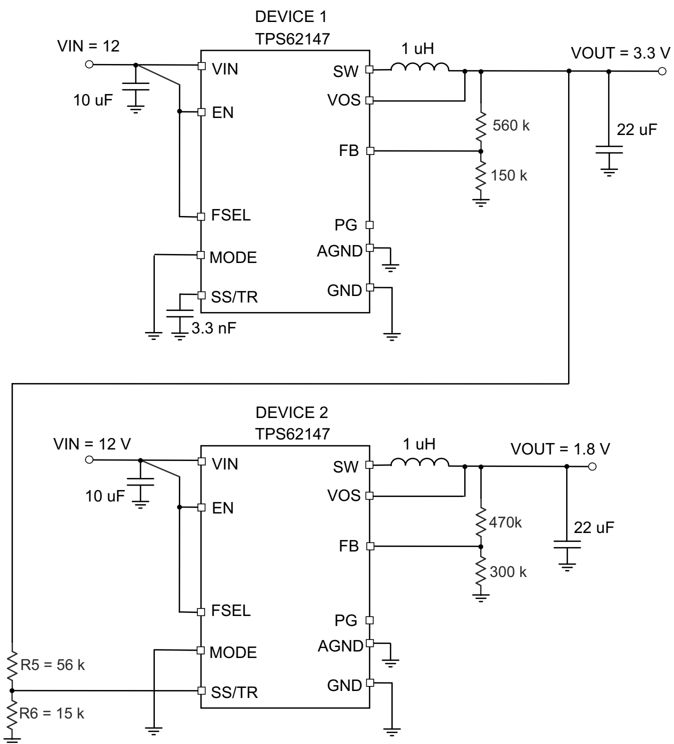



**Figure 10-82. Tracking Example**

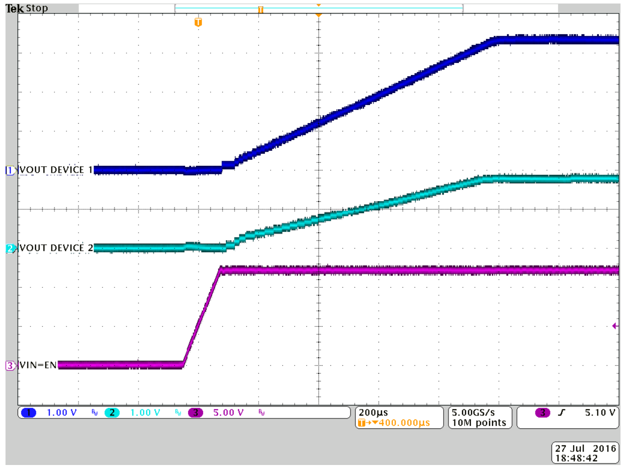



Figure 10-83. Tracking

### 10.3.4 Precise Soft-Start Timing

The SS/TR pin of the TPS62147, TPS62148 can be used for tracking as well as for setting the soft-start time. The TPS62147, TPS62148 has one GND terminal which is used for the power ground as well as for the analog ground connection. While starting the device with a load current above approximately 1 A, the noise on the GND connection can lead to a soft-start time shorter than calculated. There is an external work around as given below.

Adding a 10 kΩ resistor filters the noise on the GND connection and keeps the soft-start time at the value calculated.

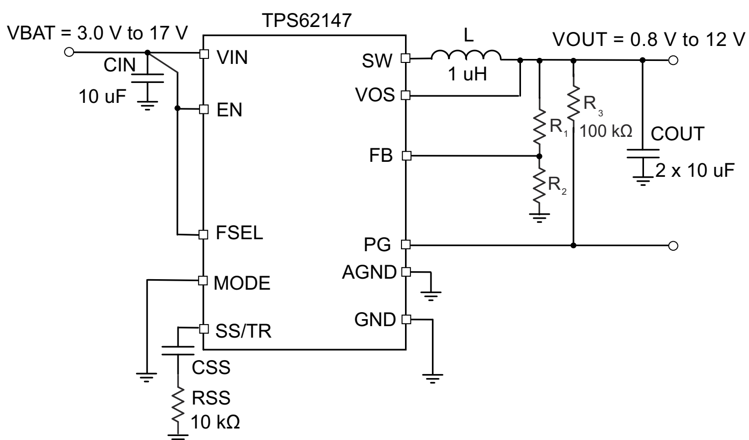



Figure 10-84. Adding a Series Resistor to CSS

## 10.4 Power Supply Recommendations

The power supply to the TPS62147, TPS62148 must have a current rating according to the supply voltage, output voltage, and output current of the TPS62147, TPS62148.

## 10.5 Layout

### 10.5.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS62147, TPS62148 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

See Section 10.5.2 for the recommended layout of the TPS62147, TPS62148, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and

GND pin of TPS62147, TPS62148. Also connect the VOS pin in the shortest way to VOUT at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops which conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS must be connected with short wires and not nearby high dv/dt signals (for example SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R1 and R2, must be kept close to the IC and connect directly to those pins and the system ground plane. The same applies to R3 if FB2 is used to scale the output voltage.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND and SW pins help to spread the heat through the pcb.

In case any of the digital inputs EN, FSEL or MODE must be tied to the input supply voltage at VIN, the connection must be made directly at the input capacitor as indicated in the schematics. Please also see the EVM User´s Guide SLVUBE9.

### 10.5.2 Layout Example

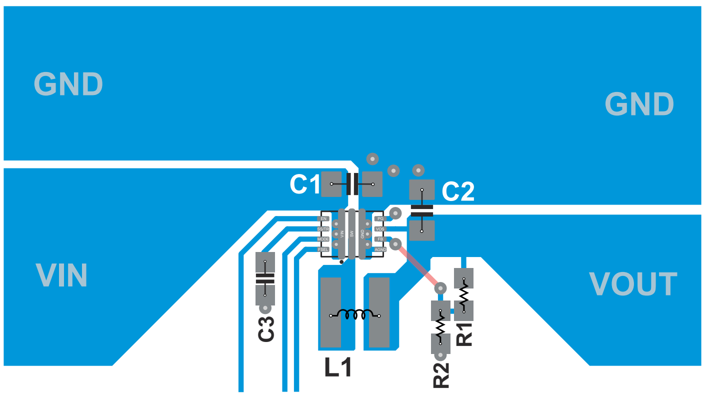



**Figure 10-85. Layout**

### 10.5.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design, for example, increasing copper thickness, thermal vias, number of layers
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (*Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*), and (*Semiconductor and IC Package Thermal Metrics application report*).

The TPS62147, TPS62148 are designed for a maximum operating junction temperature ($T_J$) of 125 °C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62147RGXR | ACTIVE | VQFN-HR | RGX | 11 | 3000 | RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 125 | 62147 | Samples |
| TPS62147RGXT | ACTIVE | VQFN-HR | RGX | 11 | 250 | RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 125 | 62147 | Samples |
| TPS62148RGXR | ACTIVE | VQFN-HR | RGX | 11 | 3000 | RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 125 | 62148 | Samples |
| TPS62148RGXT | ACTIVE | VQFN-HR | RGX | 11 | 250 | RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 125 | 62148 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

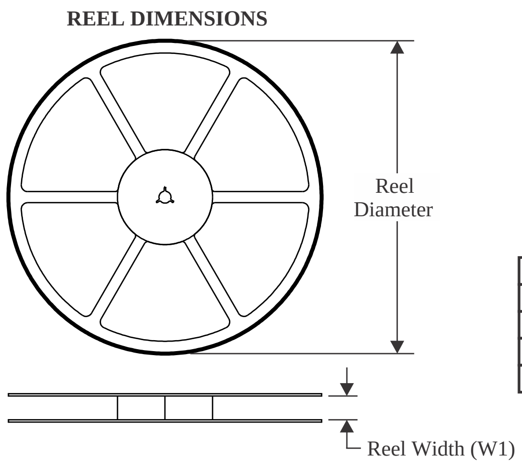
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

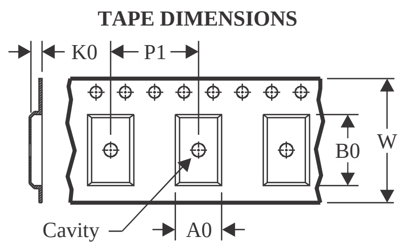
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

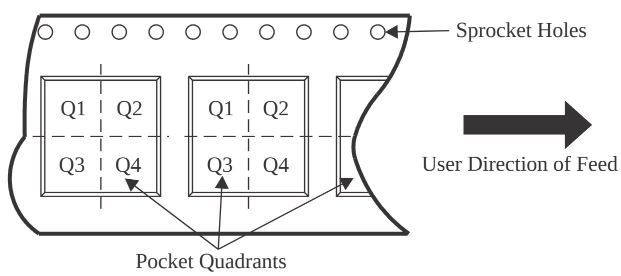
## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

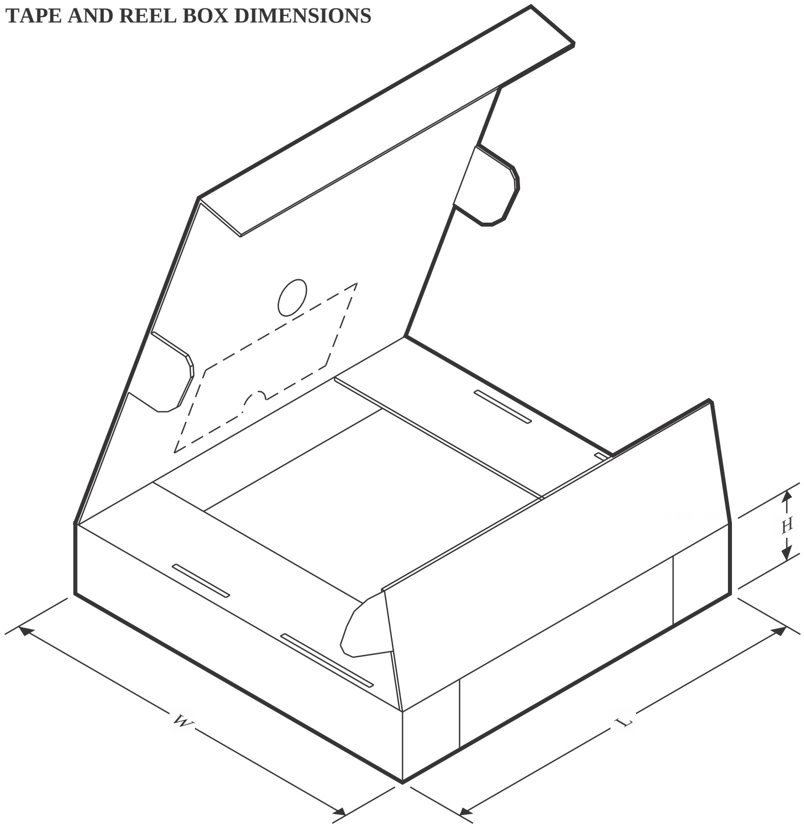
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

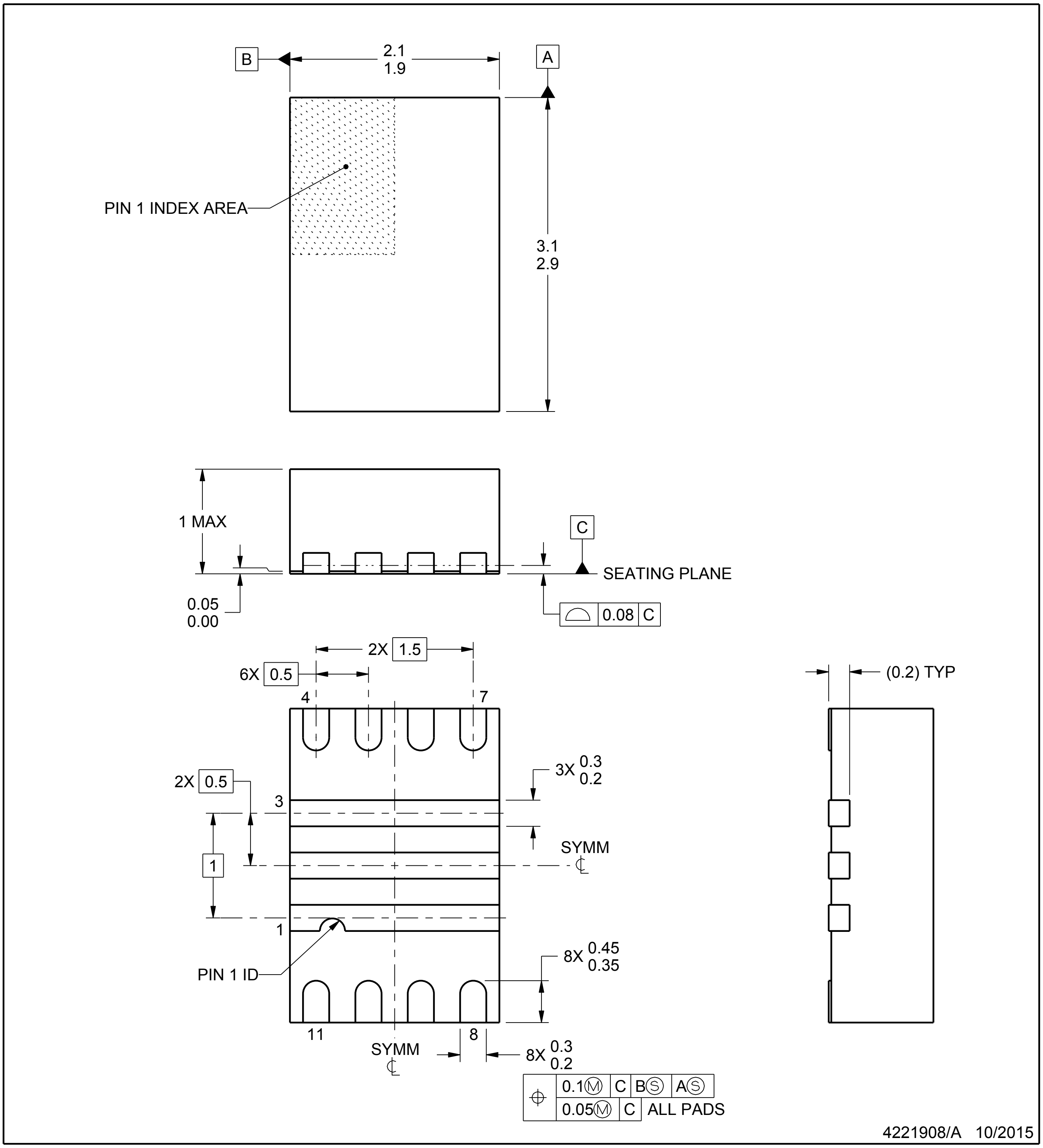
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62147RGXR | VQFN-HR | RGX | 11 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62147RGXT | VQFN-HR | RGX | 11 | 250 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62148RGXR | VQFN-HR | RGX | 11 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS62148RGXT | VQFN-HR | RGX | 11 | 250 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



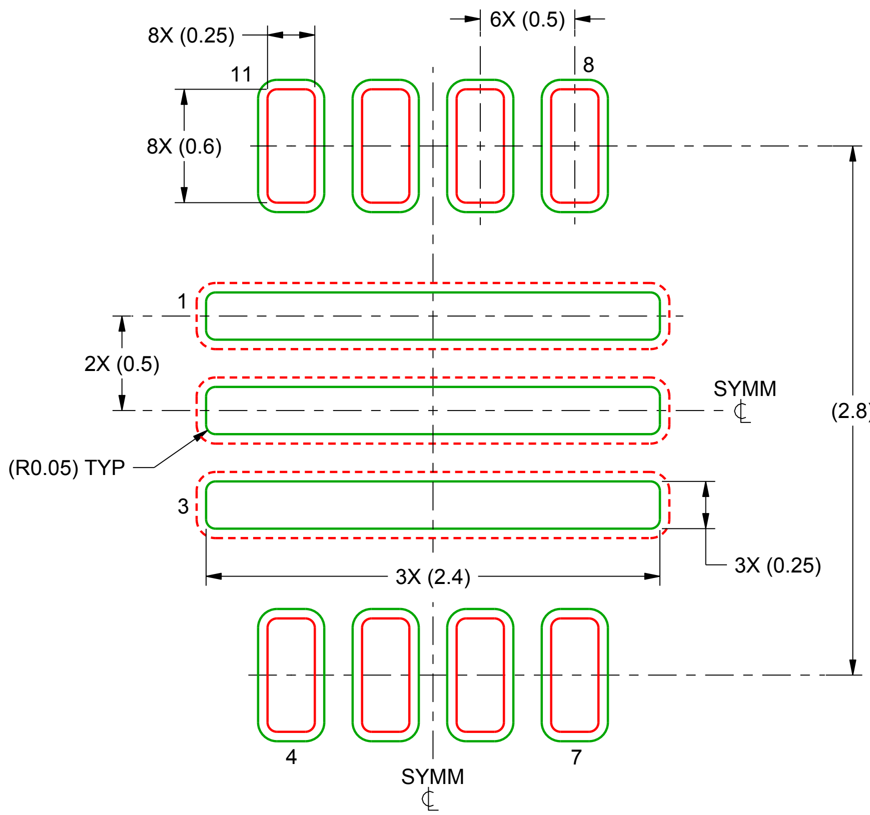

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62147RGXR | VQFN-HR | RGX | 11 | 3000 | 341.0 | 182.0 | 80.0 |
| TPS62147RGXT | VQFN-HR | RGX | 11 | 250 | 341.0 | 182.0 | 80.0 |
| TPS62148RGXR | VQFN-HR | RGX | 11 | 3000 | 341.0 | 182.0 | 80.0 |
| TPS62148RGXT | VQFN-HR | RGX | 11 | 250 | 341.0 | 182.0 | 80.0 |

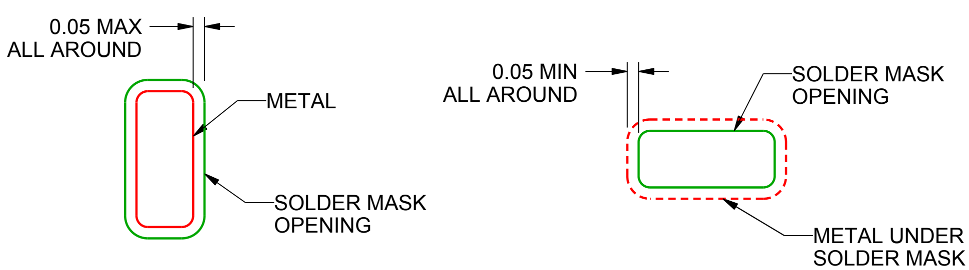



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:25X




NON SOLDER MASK DEFINED PADS 4-7 & 8-11

SOLDER MASK DEFINED PADS 1-3

SOLDER MASK DETAILS

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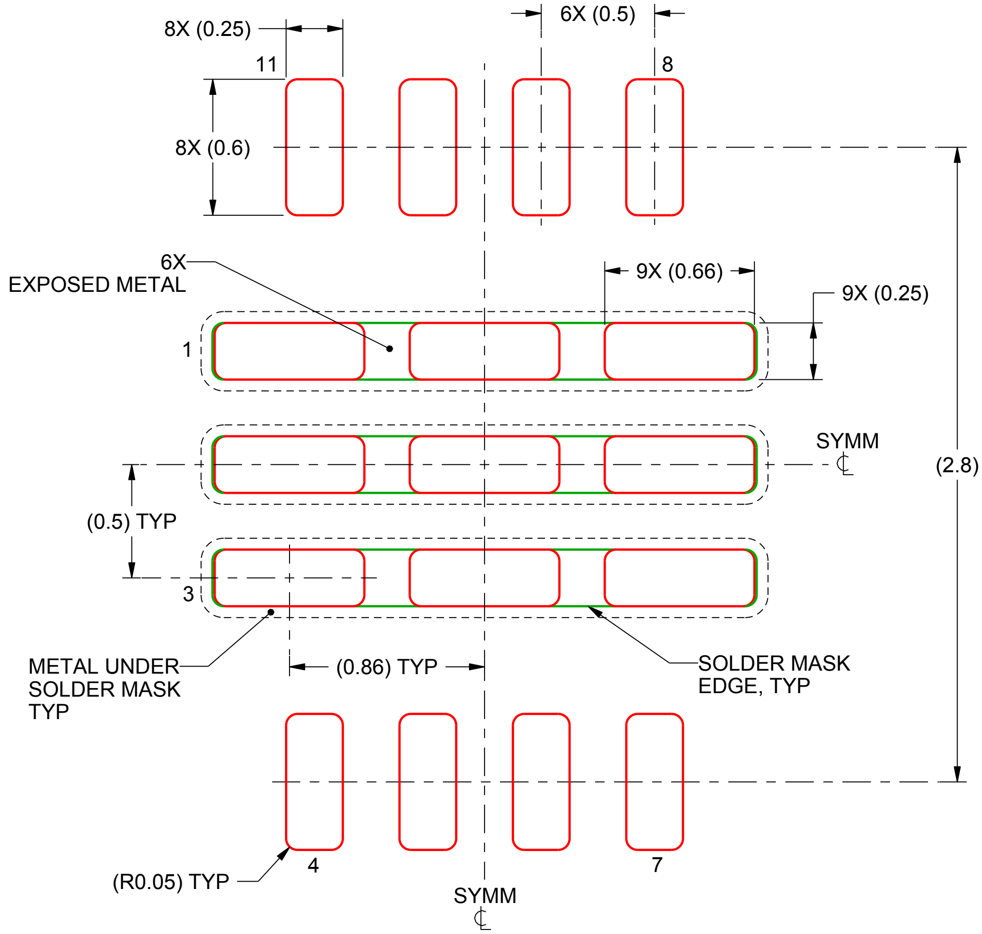
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 1-3
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.