BACKUP-BATTERY SUPERVISORS FOR RAM RETENTION

Check for Samples: TPS3619-33-EP, TPS3619-50-EP, TPS3620-33-EP, TPS3620-50-EP

FEATURES

- **Supply Current of 40 μA (Max)**
- **Battery-Supply Current of 100 nA (Max)**
- **Precision Supply-Voltage Monitor 3.3 V, 5 V, and Other Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Power-On Reset Generator with Fixed 100-ms Reset Delay Time**
- **Voltage Monitor for Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal (TPS3619)**
- **Pin-to-Pin Compatible With MAX819, MAX703, and MAX704**
- **8-Pin Mini Small-Outline Package (MSOP) Package**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice-Mail Systems**
- **Portable Battery-Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

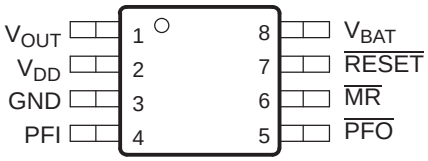
DESCRIPTION

The TPS3619 and TPS3620 families of supervisory circuits monitor and control processor activity by providing backup-battery switchover for data retention of CMOS RAM.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above V_{IT}. When the supply voltage drops below V_{IT}, the output becomes active (low) again.

The product spectrum is designed for supply voltages of 3.3 V and 5 V. The TPS3619 and TPS3620 are available in an 8-pin MSOP package and are characterized for operation over a temperature range of –55°C to 125°C.

DGK PACKAGE
(TOP VIEW)

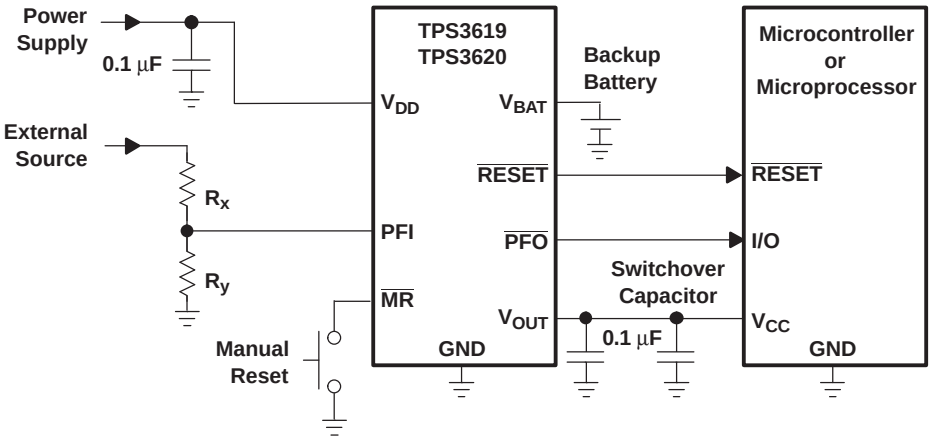


ACTUAL SIZE
3,05 mm x 4,98 mm

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL OPERATING CIRCUIT

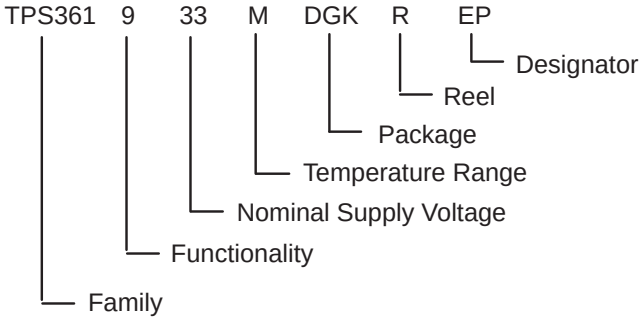


PACKAGE INFORMATION(1)

T_A	PRODUCT	PACKAGE MARKING	ORDERABLE PART NUMBER	TRANSPORT MEDIA, QUANTITY
–55°C to 125°C	TPS3619-33	BZP	TPS3619-33MDGKEP(2)	Tube, 80
			TPS3619-33MDGKREP	Tape and reel, 2500
	TPS3619-50	TBD	TPS3619-50MDGK(2)	Tube, 80
			TPS3619-50MDGKREP(2)	Tape and reel, 2500
	TPS3620-33	BTY	TPS3620-33MDGKTEP	Tape and reel, 250
			TPS3620-33MDGKREP	Tape and reel, 2500
	TPS3620-50	TBD	TPS3620-50MDGKTEP(2)	Tape and reel, 250
			TPS3620-50MDGKREP(2)	Tape and reel, 2500

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or see the TI web site at www.ti.com.
(2) Product Preview. Parameters in electrical characteristics are subject to change.

Standard and Application-Specific Versions



DEVICE NAME	NOMINAL VOLTAGE(1), V_{NOM}
TPS3619-33 DGK	3.3 V
TPS3619-50 DGK	5 V
TPS3620-33 DGK	3.3 V
TPS3620-50 DGK	5 V

(1) For other threshold voltage versions, contact the local TI sales office for availability and lead time.

Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		UNIT
Supply voltage	V_{DD} (2)	7 V
	$\overline{MR}$ and PFI pins(2)	–0.3 V to (V_{DD} + 0.3 V)
Continuous output current, I_O	V_{OUT}	400 mA
	All other pins(2)	±10 mA
Continuous total power dissipation		See Dissipation Ratings Table
Operating free-air temperature range, T_A		–55°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 in) from case for 10 s		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be continuously operated at 7 V for more than t = 1000 h.

Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW	93.98 mW

Recommended Operating Conditions

at specified temperature range

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.65	5.5	V
V_{BAT}	Battery supply voltage	1.5	5.5	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}		V
V_{IL}	Low-level input voltage		0.3 × V_{DD}	V
I_O	Continuous output current at V_{OUT}		300	mA
	Input transition rise and fall rate at $\overline{MR}$		100	ns/V
$\Delta t/\Delta V$	Slew rate at V_{DD} or V_{BAT}		1	V/µs
T_A	Operating free-air temperature	–55	125	°C

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 3.3 V, I_{OH} = –2 mA		V_{DD} – 0.4			V
			V_{DD} = 5 V, I_{OH} = –3 mA		V_{DD} – 0.4			
		$\overline{PFO}$	V_{DD} = 1.8 V, I_{OH} = –20 μA		V_{DD} – 0.3			
			V_{DD} = 3.3 V, I_{OH} = –80 μA		V_{DD} – 0.4			
			V_{DD} = 5 V, I_{OH} = –120 μA		V_{DD} – 0.4			
V_{OL}	Low-level output voltage	$\overline{RESET}$, $\overline{PFO}$	V_{DD} = 1.8 V, I_{OL} = –400 μA				0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA				0.4	
			V_{DD} = 5 V, I_{OL} = 3 mA				0.4	
V_{res}	Power-up reset voltage(1)		I_{OL} = 20 μA, V_{BAT} > 1.1 V or V_{DD} > 1.1 V				0.4	V
V_{OUT}	Normal mode		I_{OUT} = 8.5 mA, V_{BAT} = 0 V, V_{DD} = 1.8 V		V_{DD} – 50			mV
			I_{OUT} = 125 mA, V_{BAT} = 0 V, V_{DD} = 3.3 V		V_{DD} – 150			
			I_{OUT} = 190 mA, V_{BAT} = 0 V, V_{DD} = 5 V		V_{DD} – 200			
	Battery-backup mode		I_{OUT} = 0.5 mA, V_{BAT} = 1.5 V, V_{DD} = 0 V		V_{BAT} – 50			
			I_{OUT} = 7.5 mA, V_{BAT} = 3.3 V		V_{BAT} – 150			
$r_{DS(on)}$	V_{DD} to V_{OUT} on resistance		V_{DD} = 5 V			0.6	1	Ω
	V_{BAT} to V_{OUT} on resistance		V_{DD} = 3.3 V			8	20	
$V_{IT–}$	Negative-going input threshold voltage(2)	TPS36XX-33	T_A = –55°C to 125°C		2.88	2.93	3.05	V
		TPS36XX-50			4.46	4.55	4.64	
V_{PFI}			T_A = –55°C to 125°C		1.13	1.15	1.185	V
V_{hys}	Hysteresis	V_{IT}	1.65 V < V_{IT} < 2.5 V			20		mV
			2.5 V < V_{IT} < 3.5 V			40		
			3.5 V < V_{IT} < 5.5 V			60		
		PFI				12		
		VBSW(3)	V_{DD} = 1.8 V			55		
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD},	V_{DD} = 5 V	–30		–76	μA
I_{IL}	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0 V,	V_{DD} = 5 V	–110		–255	μA
I_I	Input current	PFI			–25		25	nA
I_{OS}	Short-circuit current	$\overline{PFO}$	$\overline{PFO}$ = 0 V	V_{DD} = 1.8 V			–0.3	mA
				V_{DD} = 3.3 V			–1.1	
				V_{DD} = 5 V			–2.4	
I_{DD}	V_{DD} supply current		V_{OUT} = V_{DD}				40	μA
			V_{OUT} = V_{BAT}				40	
$I_{(BAT)}$	V_{BAT} supply current		V_{OUT} = V_{DD}		–0.1		0.1	μA
			V_{OUT} = V_{BAT}				0.5	
C_I	Input capacitance		V_I = 0 V to 5 V			5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,VDD}$ ≥ 15 μs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.
(3) For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT}, regardless of V_{BAT}.

Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} – 0.2$ V	6		µs
		at $\overline{MR}$	$V_{DD} = V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100		ns

Switching Characteristics

at R_L = 1 MΩ, C_L= 50 pF, T_A= –55°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram	60	100	140	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT} – 0.4$ V, $V_{IH} = V_{IT} + 0.4$ V		2	5	µs
		PFI to $\overline{PFO}$ delay	$V_{IL} = V_{PFI} – 0.35$ V, $V_{IH} = V_{PFI} + 0.35$ V		3	5	
		$\overline{MR}$ to $\overline{RESET}$	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$		0.1	1	

Timing Diagram

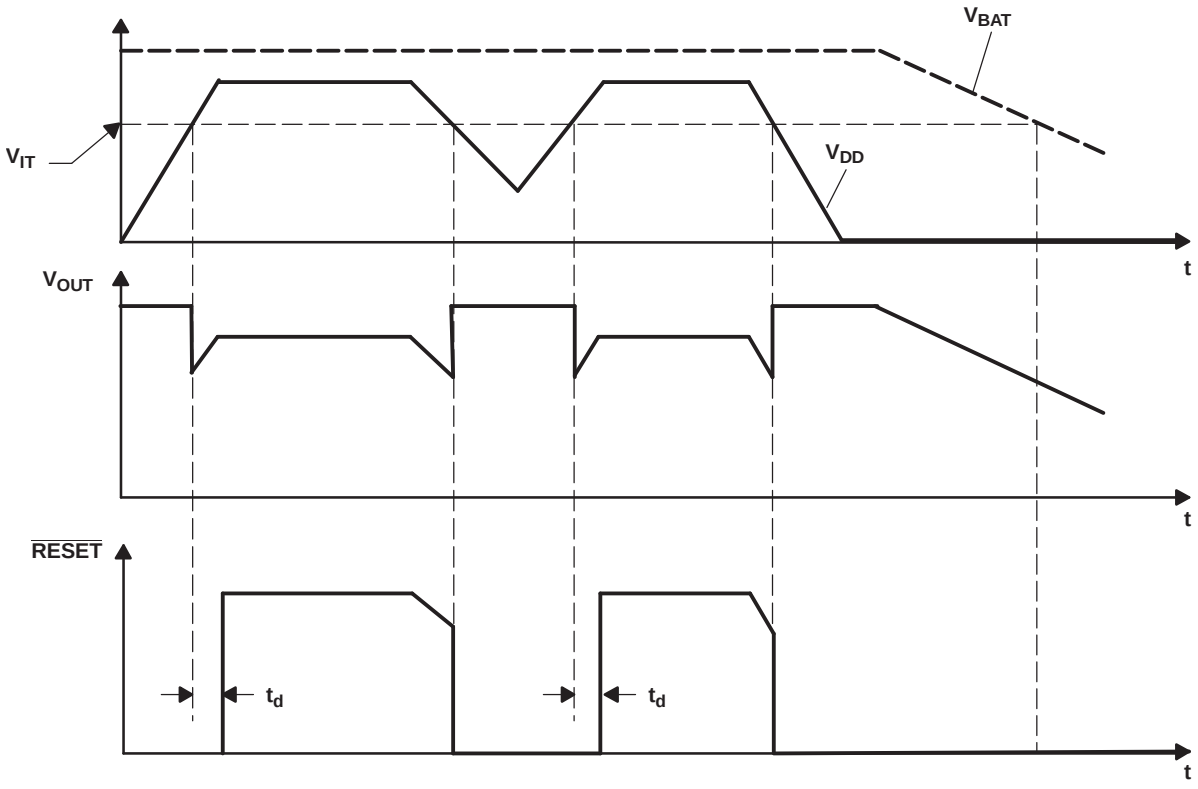


Table 1. FUNCTION TABLE

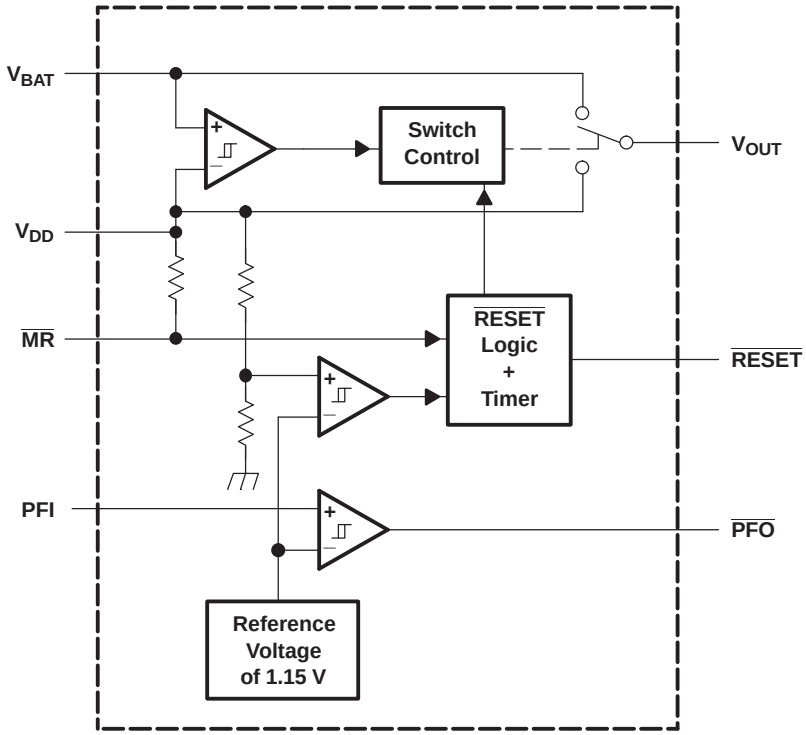
$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	$\overline{MR}$	V_{OUT}	$\overline{RESET}$
0	0	L	V_{BAT}	L
0	0	H	V_{BAT}	L
0	1	L	V_{DD}	L
0	1	H	V_{DD}	L
1	0	L	V_{DD}	L
1	0	H	V_{DD}	H
1	1	L	V_{DD}	L
1	1	H	V_{DD}	H

$PFI > V_{PFI}$	$\overline{PFO}$
0	L
1	H
CONDITION: $V_{DD} > V_{DD}$(MIN)	

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	3	I	Ground
$\overline{MR}$	6	I	Manual reset
PFI	4	I	Power-fail comparator input
$\overline{PFO}$	5	O	Power-fail comparator output
$\overline{RESET}$	7	O	Active-low reset
V_{BAT}	8	I	Backup battery
V_{DD}	2	I	Supply input voltage
V_{OUT}	1	O	Supply output voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

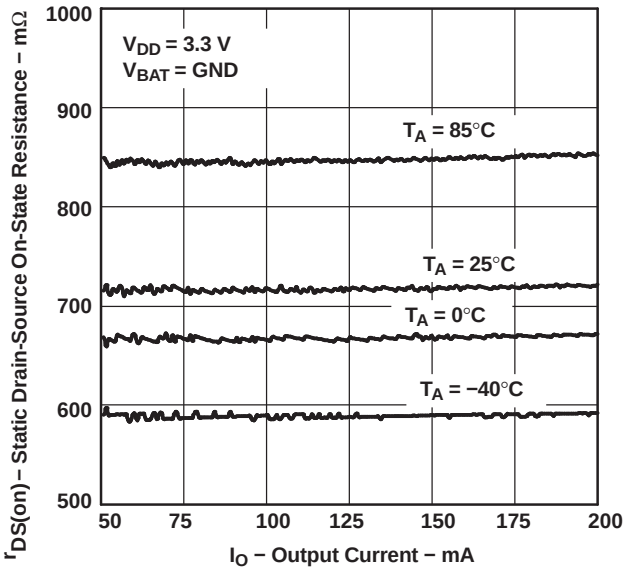


Figure 1.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

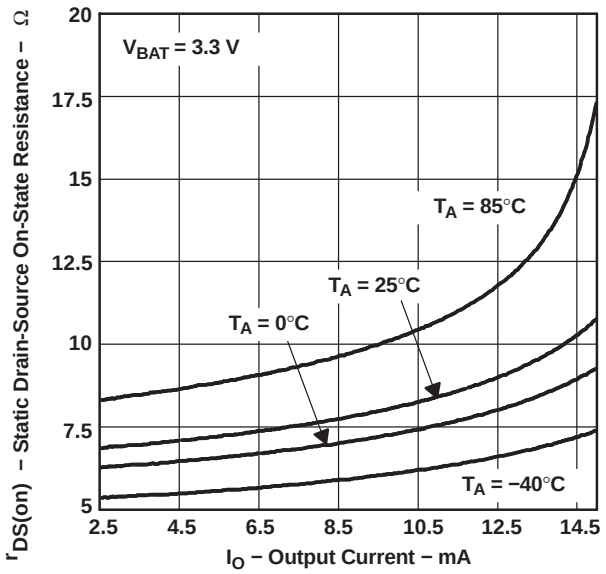


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

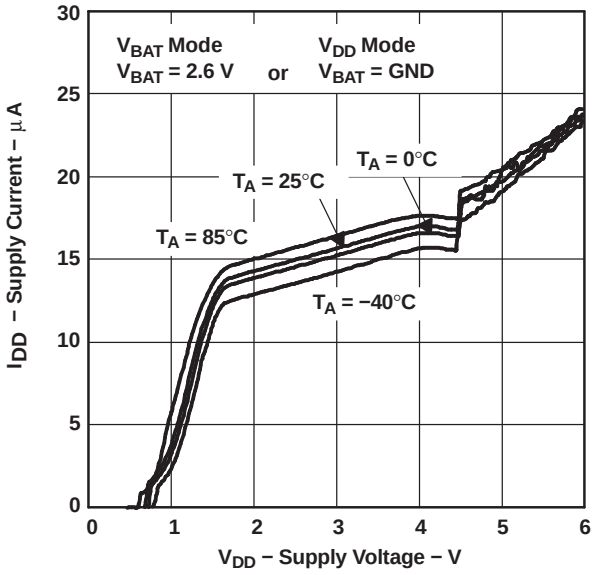


Figure 3.

NORMALIZED THRESHOLD AT $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

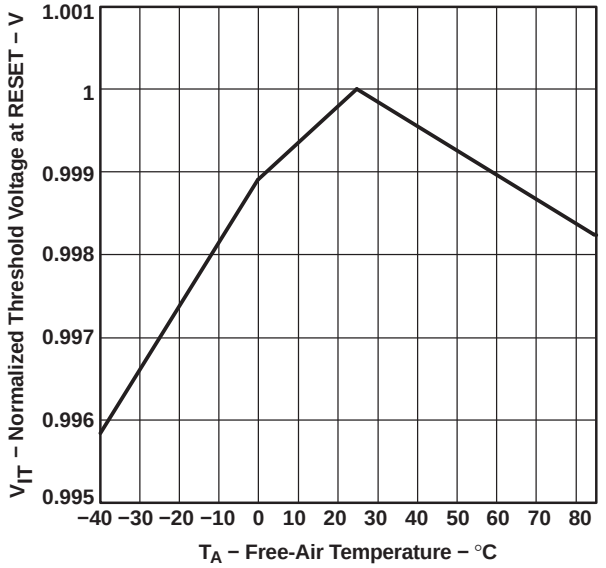


Figure 4.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs HIGH-LEVEL OUTPUT CURRENT

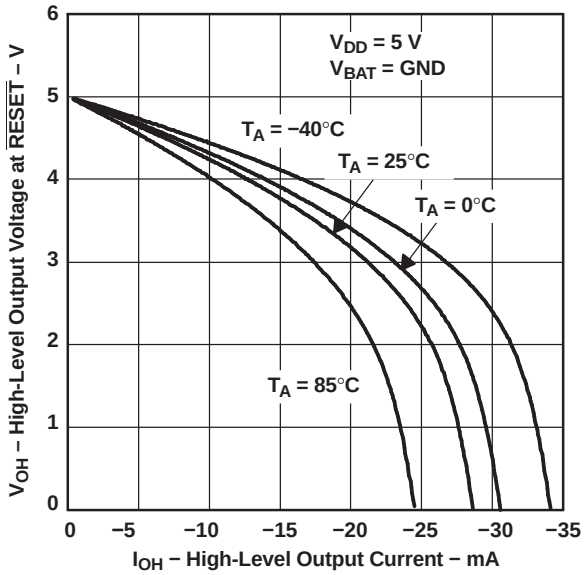


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs HIGH-LEVEL OUTPUT CURRENT

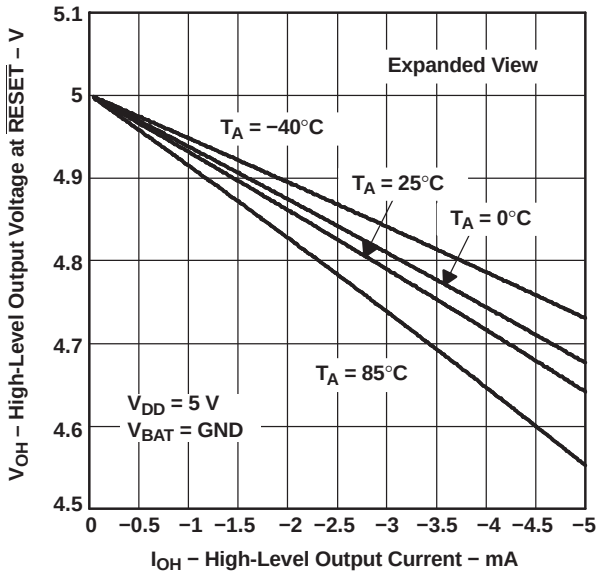


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$ vs HIGH-LEVEL OUTPUT CURRENT

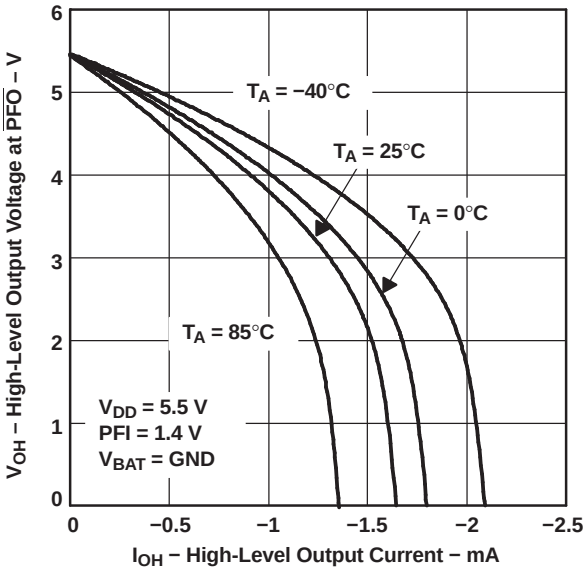


Figure 7.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$ vs HIGH-LEVEL OUTPUT CURRENT

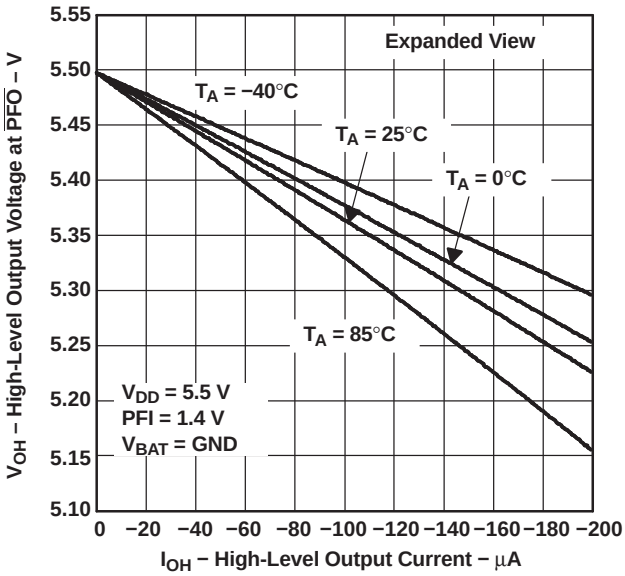


Figure 8.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs LOW-LEVEL OUTPUT CURRENT

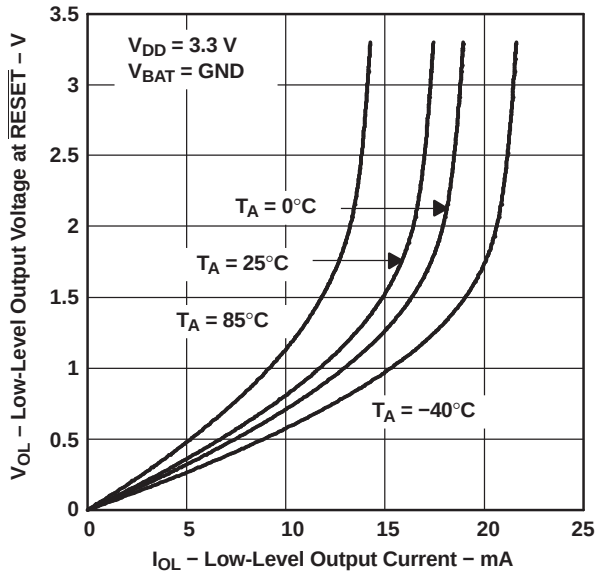


Figure 9.

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$ vs LOW-LEVEL OUTPUT CURRENT

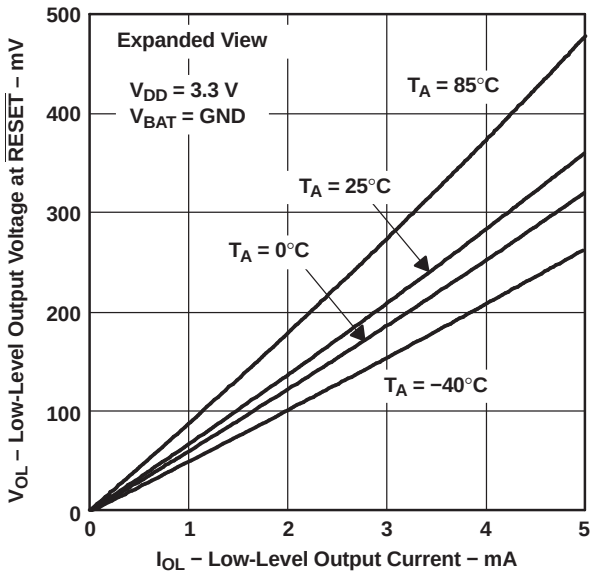


Figure 10.

MINIMUM PULSE DURATION AT V_{DD} vs THRESHOLD OVERDRIVE AT V_{DD}

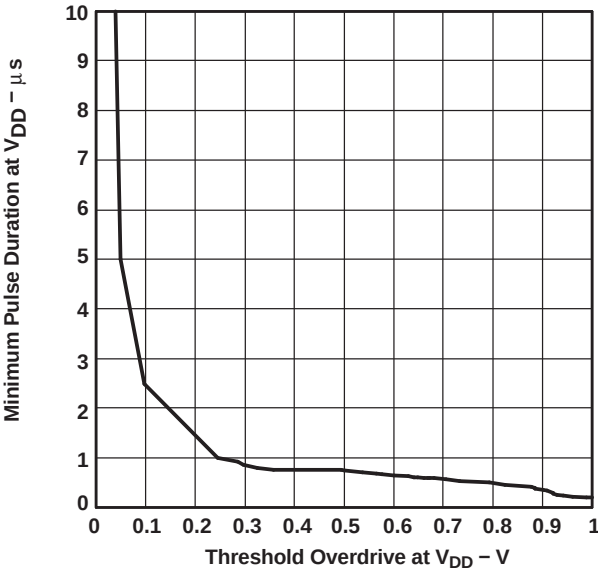


Figure 11.

MINIMUM PULSE DURATION AT PFI vs THRESHOLD OVERDRIVE AT PFI

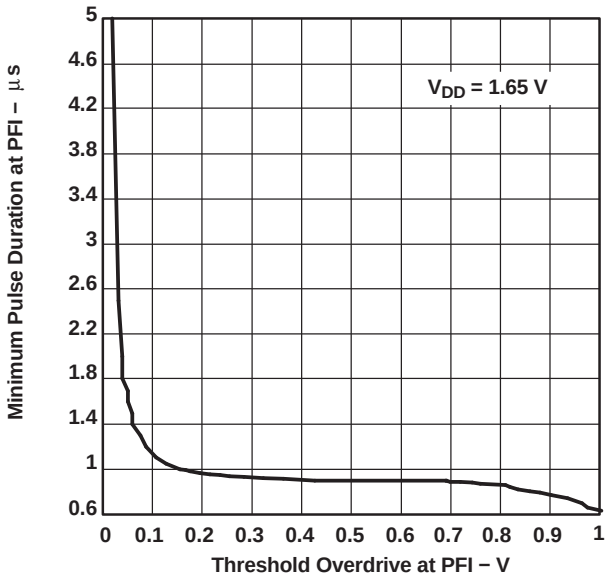


Figure 12.

DETAILED DESCRIPTION

Battery Freshness Seal (TPS3619)

The battery freshness seal of the TPS3619 family disconnects the backup battery from internal circuitry until it is needed. This function prevents the backup battery from being discharged until the final product is put to use. The following steps explain how to enable the freshness seal mode.

1. Connect V_{BAT} ($V_{BAT} > V_{BAT}$ min)
2. Ground $\overline{PFO}$
3. Connect PFI to V_{DD} (PFI = V_{DD})
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and retain for 5 ms < t < 35 ms

The battery freshness seal mode is removed automatically by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

Power-Fail Input/Output Comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The PFI is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ($V_{IT(PFI)}$) of 1.15 V (typ), the $\overline{PFO}$ goes low. If $V_{IT(PFI)}$ goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be ignored, compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1%, to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, PFI should be connected to ground and $\overline{PFO}$ left unconnected.

Backup-Battery Switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors do not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below the V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred, either until V_{DD} crosses V_{BAT} or until V_{DD} rises above V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

Table 2. FUNCTION TABLE

$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

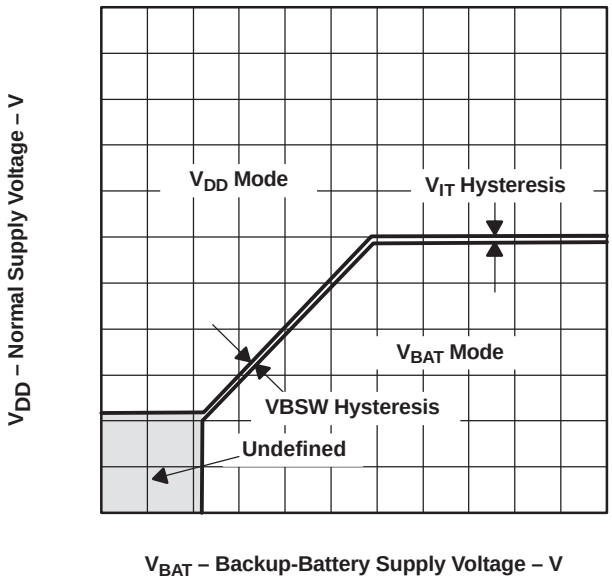


Figure 13. Normal Supply Voltage vs Backup-Battery Supply Voltage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3620-33MDGKREP	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTY	Samples
TPS3620-33MDGKTEP	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTY	Samples
V62/06670-03XE	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

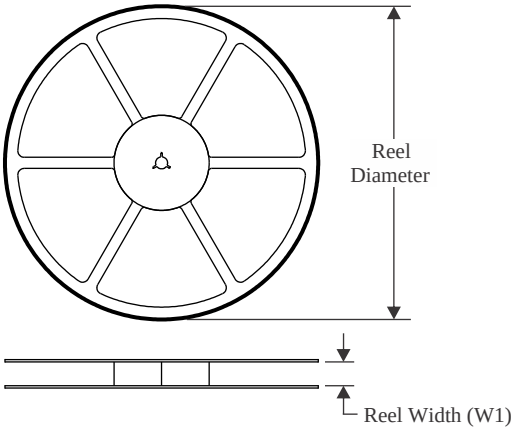
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

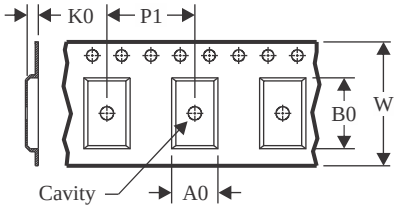
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

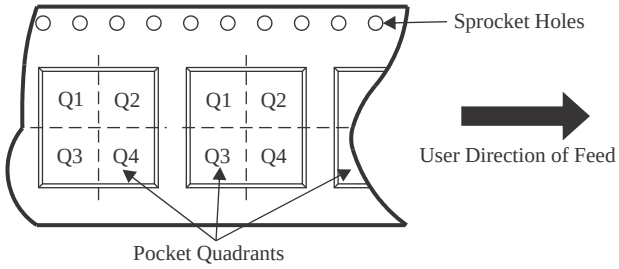


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

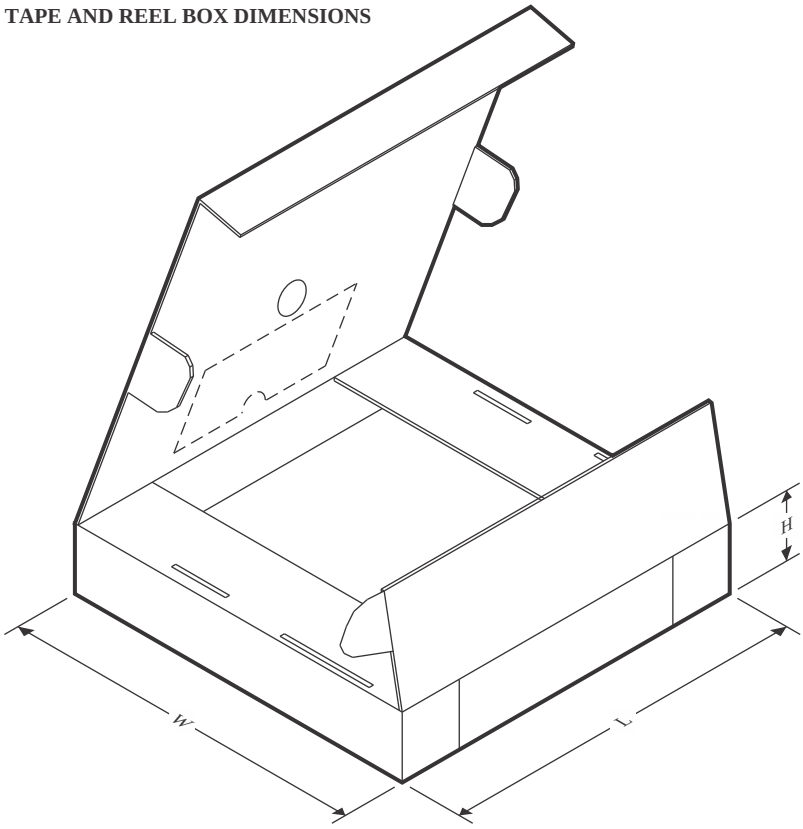
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3620-33MDGKREP	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3620-33MDGKTEP	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

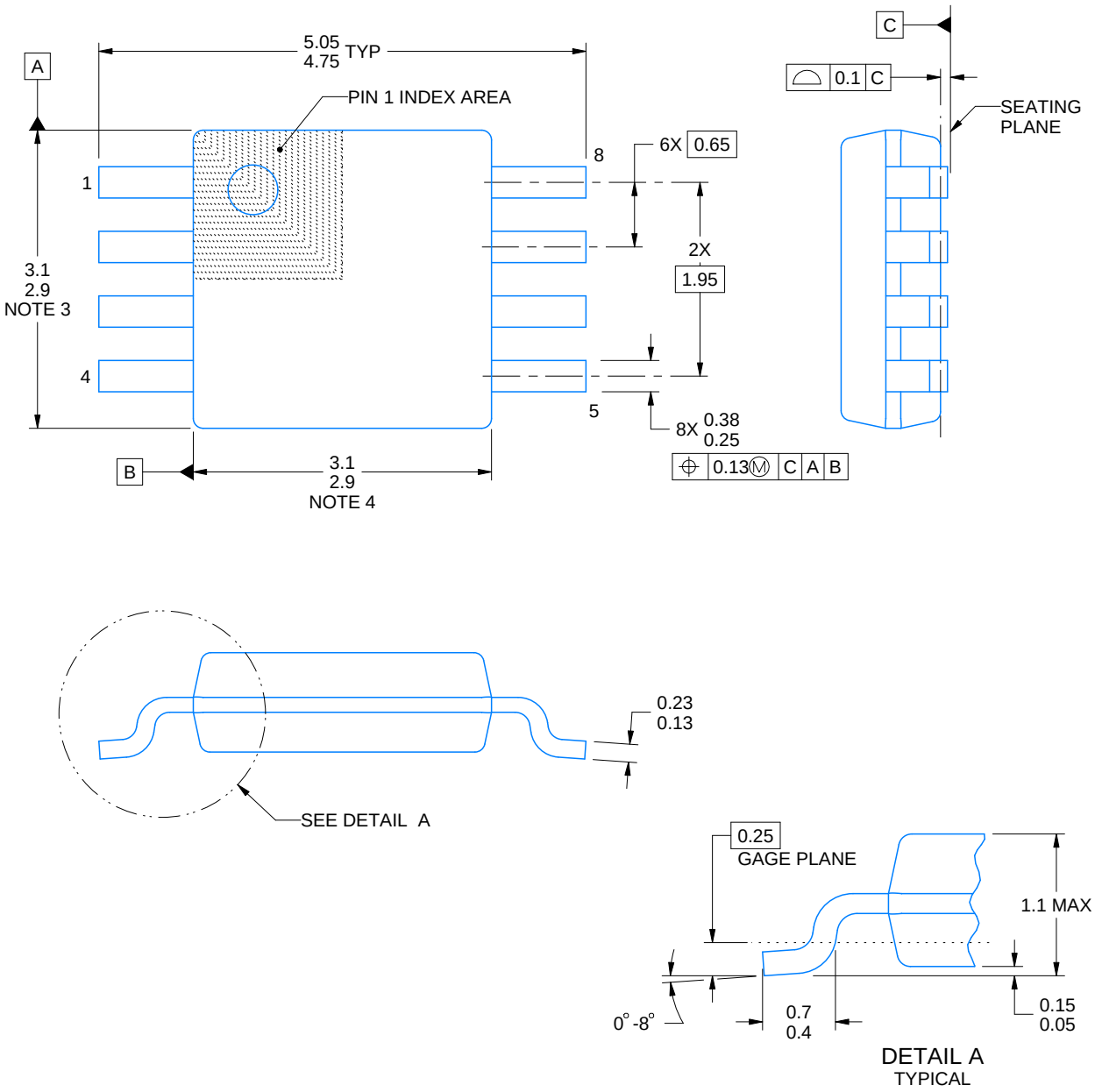
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3620-33MDGKREP	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3620-33MDGKTEP	VSSOP	DGK	8	250	202.0	201.0	28.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

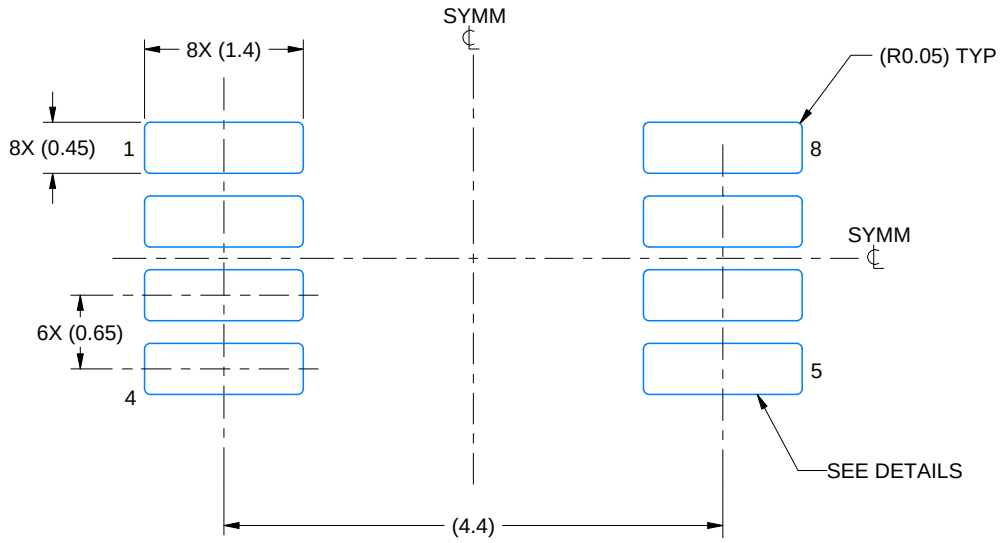
SMALL OUTLINE PACKAGE



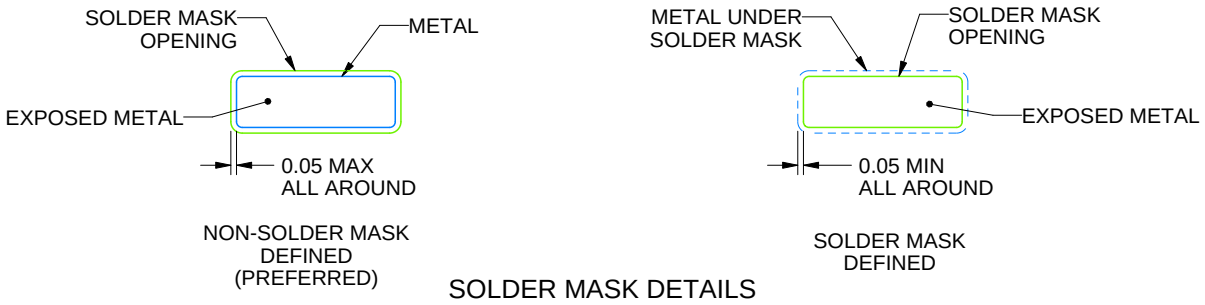
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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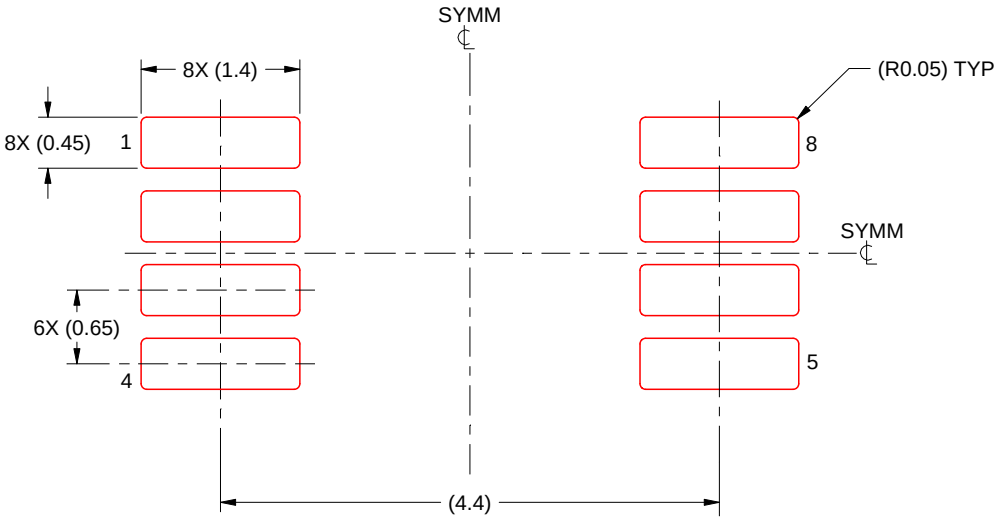
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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