

# TPS22996H-Q1 5.5V, 4A, 13mΩ On-Resistance Dual-Channel Automotive Load Switch

## 1 Features

- Integrated dual-channel load switch
- Input voltage range: 0.6V to  $V_{BIAS}$
- $V_{BIAS}$  voltage range: 2.5V to 5.5V
- ON-Resistance
  - $R_{ON} = 13m\Omega$  (typical)  
at  $V_{IN} = 0.6V$  to  $5V$ ,  $V_{BIAS} = 5V$
- 4A maximum continuous switch current per channel
- Quiescent current:
  - 18 $\mu A$  (typical, both channels)  
at  $V_{IN} = V_{BIAS} = 5V$
  - 13 $\mu A$  (typical, single channel)  
at  $V_{IN} = V_{BIAS} = 5V$
- Humidity resistant:
  - Device keeps functionality (ON, OFF, protection), but timing specification is affected under the following conditions:
    - 100k $\Omega$  short to GND
    - 100k $\Omega$  short to power
- Control input threshold enables use of 1.2V, 1.8V, 2.5V, and 3.3V logic
- Configurable rise time
- Thermal shutdown
- Quick output discharge (QOD)

## 2 Applications

- [Infotainment](#)
- [Cluster](#)
- [ADAS](#)

## 3 Description

TPS22996H-Q1 is a dual-channel load switch with controlled turnon. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.6V to 5.5V, and can support a maximum continuous current of 4A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The device is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range. The device also offers an integrated 230 $\Omega$  on-chip load resistor for quick output discharge when the switch is turned off.

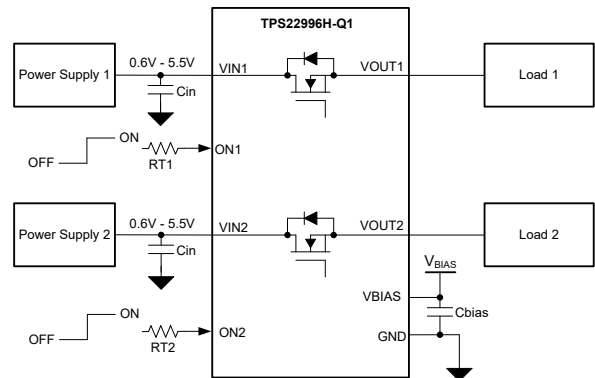
The pins of the TPS22996H-Q1 are resistant to high humidity conditions, meaning that the device is able to function with a 100k $\Omega$  short from any pin to GND or power.

The TPS22996H-Q1 is available in a small, space-saving 2.1mm × 1.2mm 8-DYC package. The device is characterized for operation over the free-air temperature range of –40°C to 125°C.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPS22996H	DYC (SOT, 8)	2.1mm × 1.2mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



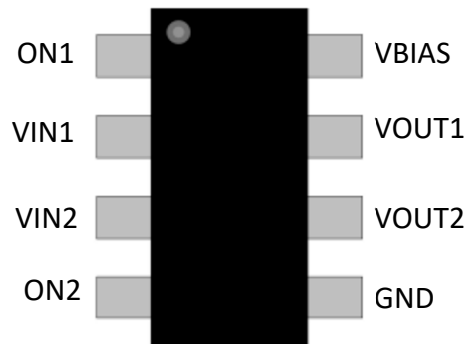
**Application Circuit**



## Table of Contents

<b>1 Features</b> .....	1	7.3 Feature Description.....	14
<b>2 Applications</b> .....	1	7.4 Device Functional Modes.....	16
<b>3 Description</b> .....	1	<b>8 Application and Implementation</b> .....	17
<b>4 Pin Configuration and Functions</b> .....	3	8.1 Application Information.....	17
<b>5 Specifications</b> .....	4	8.2 Typical Application.....	17
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	20
5.2 ESD Ratings.....	4	8.4 Layout.....	20
5.3 Recommended Operating Conditions.....	4	<b>9 Device and Documentation Support</b> .....	22
5.4 Thermal Information.....	4	9.1 Receiving Notification of Documentation Updates....	22
5.5 Electrical Characteristics.....	5	9.2 Support Resources.....	22
5.6 Switching Characteristics.....	6	9.3 Trademarks.....	22
5.7 Typical DC Characteristics.....	7	9.4 Electrostatic Discharge Caution.....	22
5.8 Typical AC Characteristics.....	8	9.5 Glossary.....	22
<b>6 Parameter Measurement Information</b> .....	12	<b>10 Revision History</b> .....	22
<b>7 Detailed Description</b> .....	13	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	22
7.1 Overview.....	13		
7.2 Functional Block Diagram.....	14		

## 4 Pin Configuration and Functions



**Figure 4-1. DYC Package, 8-Pin SOT (Top View)**

**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ON1	Input	Active-high switch 1 control input. Connect series resistor to set Slew Rate. Do not leave floating. See <a href="#">Section 7.3.7</a> for more information.
2	VIN1	Input	Switch 1 input. Recommended voltage range for these pins for optimal $R_{ON}$ performance is 0.6V to $V_{BIAS}$ . Place an optional decoupling capacitor between these pins and GND to reduce $V_{IN1}$ dip during turnon of the channel. See <a href="#">Section 8.2</a> for more information.
3	VIN2	Input	Switch 2 input. Recommended voltage range for these pins for optimal $R_{ON}$ performance is 0.6V to $V_{BIAS}$ . Place an optional decoupling capacitor between these pins and GND to reduce $V_{IN2}$ dip during turnon of the channel. See <a href="#">Section 8.2</a> for more information.
4	ON2	Input	Active-high switch 2 control input. Connect series resistor to set slew rate. Do not leave floating. See <a href="#">Section 7.3.7</a> for more information.
5	GND	—	Device ground.
6	VOUT2	Output	Switch 2 output.
7	VOUT1	Output	Switch 1 output.
8	VBIAS	Input	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V. See <a href="#">Section 8.1</a> .

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN1,2</sub>	Input Voltage	-0.3	6	V
V <sub>OUT1,2</sub>	Output Voltage	-0.3	6	V
V <sub>ON1,2</sub>	ON Pin Voltage	-0.3	6	V
V <sub>BIAS</sub>	Bias Voltage	-0.3	6	V
I <sub>MAX</sub>	Maximum continuous current per channel		4	A
I <sub>MAX,PLS</sub>	Maximum pulsed current switch per channel, pulse <300μs, 3% duty cycle		5.5	A
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD, VIN1,VIN2,VOUT1,VOUT2 pins	±500	
		Charged-device model (CDM), per AEC Q100-011 CDM ESD, ON1,ON2,VBIAS pins	±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN1,2</sub>	Input Voltage	0.6		V <sub>BIAS</sub>	V
V <sub>BIAS</sub>	Bias Voltage	2.5		5.5	V
V <sub>ON1,2</sub>	ON Pin Voltage	0		5.5	V
V <sub>OUT1,2</sub>	Output Voltage	0		V <sub>IN</sub>	V
V <sub>IH</sub>	High-Level Input Voltage, ON	1.2		5.5	V
V <sub>IL</sub>	Low-Level Input Voltage, ON	0		0.5	V
T <sub>A</sub>	Ambient Temperature	-40		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS22996H-Q1	
		DYC	
		8 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	108.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	73.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.3	°C/W

THERMAL METRIC <sup>(1)</sup>		TPS22996H-Q1		
		DYC		
		8 PINS		
UNIT				
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
<b>Power Supplies and Currents</b>								
$I_{Q,VBIAS}$	$V_{BIAS}$ Quiescent Current (Both channels)	$I_{OUT1} = I_{OUT2} = 0mA$ , $V_{IN1,2} = V_{ON1,2} = 5V$	25°C		18			μA
			-40°C to 85°C		18	22		μA
			-40°C to 125°C			25		μA
$I_{Q,VBIAS}$	$V_{BIAS}$ Quiescent Current (Single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$ , $V_{ON2} = 0V$ , $V_{IN1,2} = V_{IN1} = 5V$	25°C		13			μA
			-40°C to 85°C		13	17		μA
			-40°C to 125°C			19		μA
$I_{SD,VBIAS}$	$V_{BIAS}$ Shutdown Current	$V_{ON1,2} = 0V$ , $V_{OUT1,2} = 0V$	25°C		0.005	1		μA
			-40°C to 85°C		0.005	1		μA
			-40°C to 125°C		0.005	1		μA
$I_{SD,VIN}$	$V_{IN}$ Shutdown Current (per channel)	$V_{ON} = 0V$ , $V_{OUT} = 0V$	$V_{IN} = 5V$	25°C		0.002	0.8	μA
				-40°C to 85°C		0.002	0.8	μA
				-40°C to 125°C			1	μA
			$V_{IN} = 3.3V$	25°C		0.002	0.8	μA
				-40°C to 85°C		0.002	0.8	μA
				-40°C to 125°C			1	μA
			$V_{IN} = 1.8V$	25°C		0.002	0.8	μA
				-40°C to 85°C		0.002	0.8	μA
				-40°C to 125°C			1	μA
			$V_{IN} = 0.6V$	25°C		0.002	0.8	μA
				-40°C to 85°C		0.002	0.8	μA
				-40°C to 125°C			1	μA
$I_{ON}$	ON Pin Leakage Current	$V_{ON} = 5.5V$	-40°C to 125°C			0.1	μA	
<b>Resistance Characteristics</b>								
$R_{ON}$	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 5V$	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			$V_{IN} = 3.3V$	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			$V_{IN} = 1.8V$	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			$V_{IN} = 0.6V$	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
$V_{ON,VIH}$	VIH	$V_{IN} = 5V$	$V_{IN} = 5V$	-55°C to 125°C	1.2		V	

## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

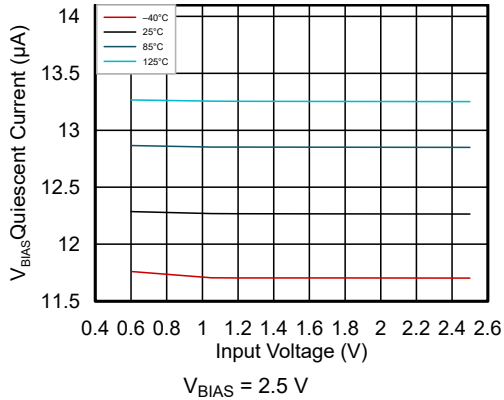
PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$V_{ON,VIL}$	VIL	$V_{IN} = 5V$	$V_{IN} = 5V$	-55°C to 125°C		0.65		V
$V_{ON,HYS}$	ON Pin Hysteresis	$V_{IN} = 5V$		-55°C to 125°C		90		mV
$R_i$	Internal On Pin Resistance	$V_{ON} = 5V$	$V_{ON} = 5V$	-55°C to 125°C		12.5		k $\Omega$
$R_{PD}$	Output Pulldown Resistance	$V_{IN} = V_{OUT} = 5V, V_{ON} = 0V$		-40°C to 125°C		230	300	$\Omega$
$T_{SD}$	Thermal Shutdown	Junction Temperature Rising		-		175		°C
$T_{SD,HYS}$	Thermal Shutdown Hysteresis	Junction Temperature Falling		-		20		°C

## 5.6 Switching Characteristics

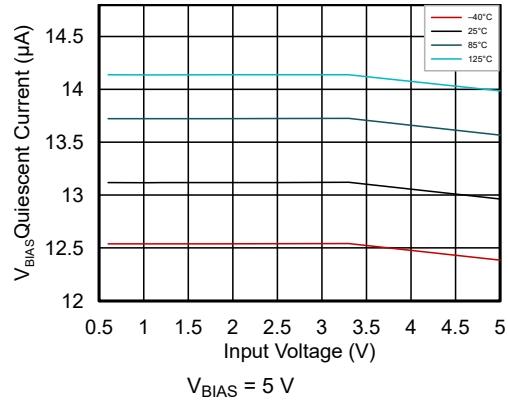
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b><math>V_{IN} = V_{ON} = V_{BIAS} = 5V</math></b>						
$t_{ON}$	Turn ON Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		946		$\mu s$
$t_{OFF}$	Turn OFF Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		2.1		$\mu s$
$t_R$	Rise Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		626		$\mu s$
$t_F$	Fall Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		2.1		$\mu s$
$t_D$	Delay Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		320		$\mu s$
<b><math>V_{IN} = 0.6V, V_{ON} = V_{BIAS} = 5V</math></b>						
$t_{ON}$	Turn ON Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A,$		587		$\mu s$
$t_{OFF}$	Turn OFF Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		2.1		$\mu s$
$t_R$	Rise Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		203		$\mu s$
$t_F$	Fall Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		2.52		$\mu s$
$t_D$	Delay Time	$R_L = 10\Omega, C_L = 0.1\mu F, I_{ON} = 100\mu A$		384		$\mu s$

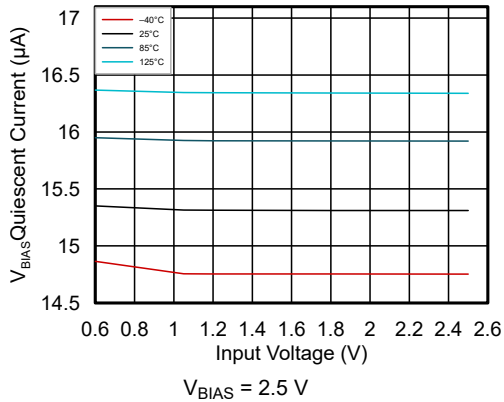
### 5.7 Typical DC Characteristics



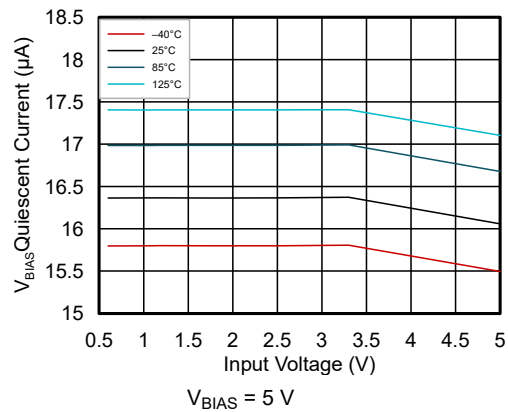
**Figure 5-1.  $V_{BIAS}$  Quiescent Current vs Input Voltage Single Channel**



**Figure 5-2.  $V_{BIAS}$  Quiescent Current vs Input Voltage Single Channel**



**Figure 5-3.  $V_{BIAS}$  Quiescent Current vs Input Voltage Both Channel**

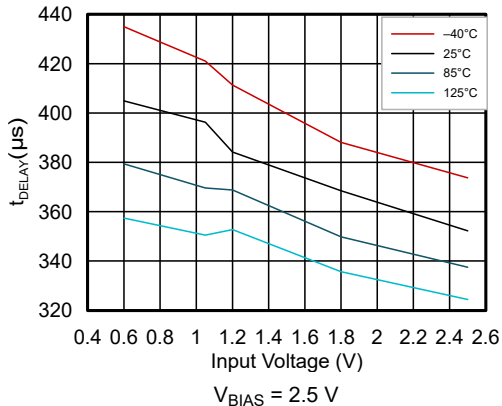


**Figure 5-4.  $V_{BIAS}$  Quiescent Current vs Input Voltage Both Channel**

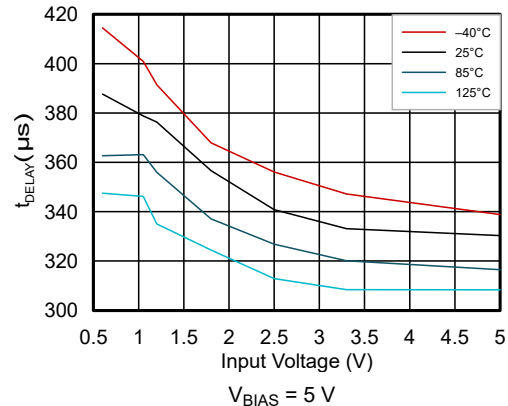
## 5.8 Typical AC Characteristics

### AC Characteristics

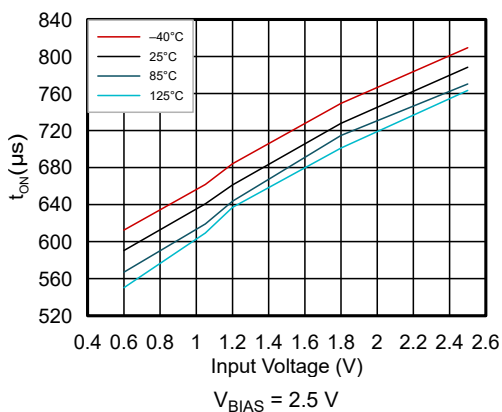
$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed



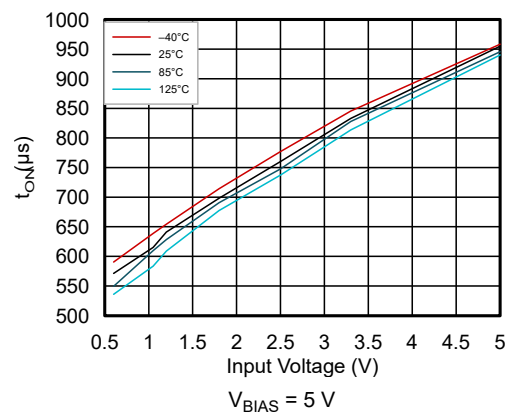
**Figure 5-5. Delay Time vs Input Voltage**



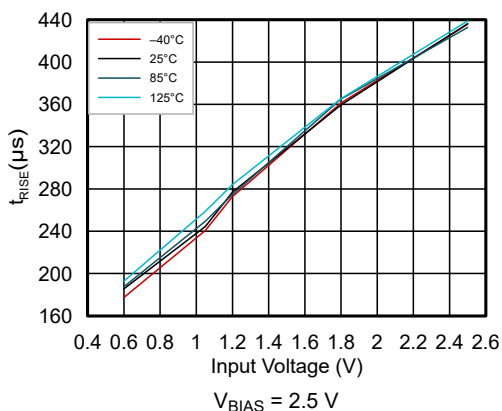
**Figure 5-6. Delay Time vs Input Voltage**



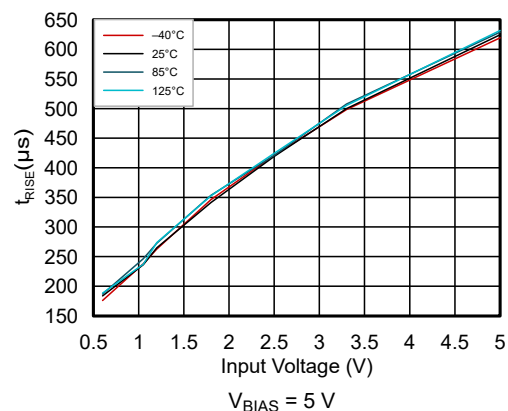
**Figure 5-7. Turnon Time vs Input Voltage**



**Figure 5-8. Turnon Time vs Input Voltage**



**Figure 5-9. Rise Time vs Input Voltage**



**Figure 5-10. Rise Time vs Input Voltage**



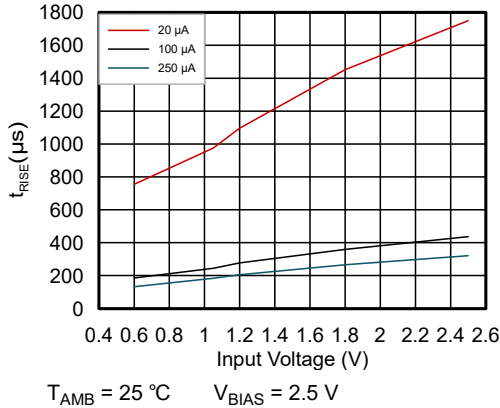


Figure 5-11. Rise Time vs Input Voltage with Different  $I_{ON}$

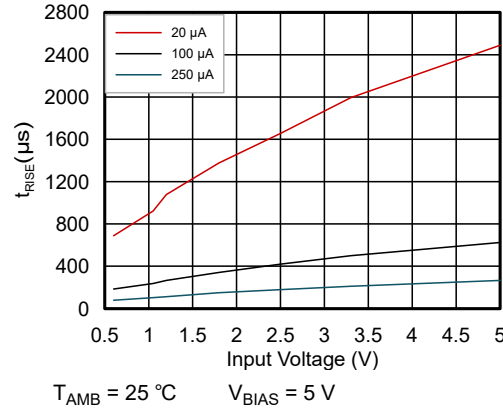


Figure 5-12. Rise Time vs Input Voltage with Different  $I_{ON}$

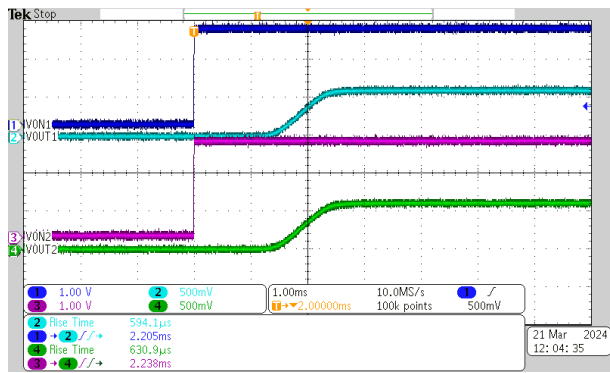


Figure 5-13. Turnon Response Time

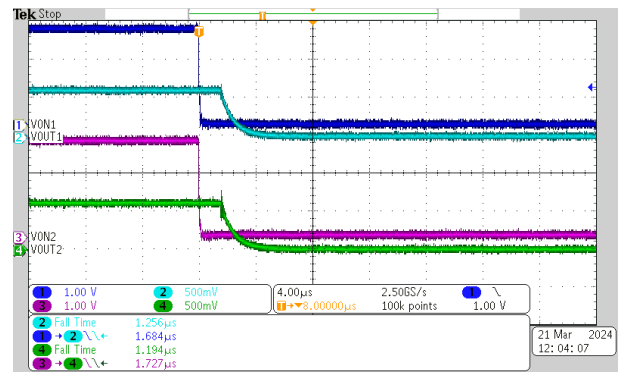


Figure 5-14. Turnoff Response Time

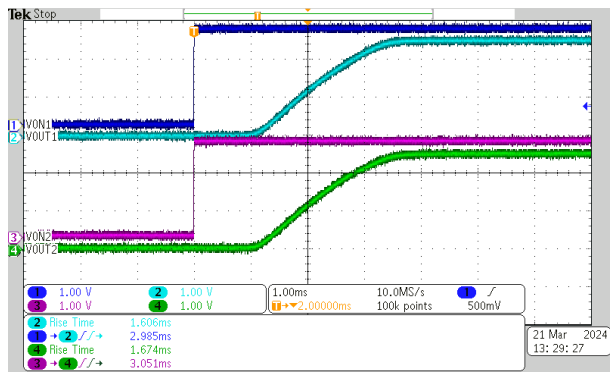


Figure 5-15. Turnon Response Time

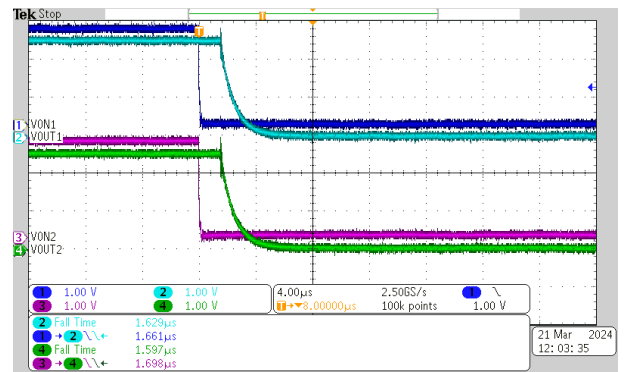


Figure 5-16. Turnoff Response Time

TPS22996H-Q1

SLVSHA3A – MARCH 2024 – REVISED OCTOBER 2024

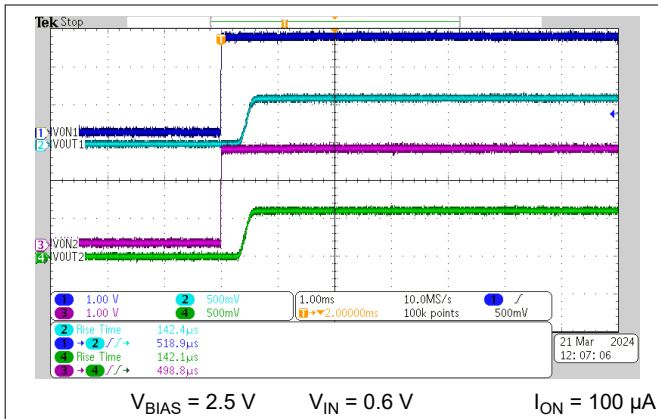


Figure 5-17. Turnon Response Time

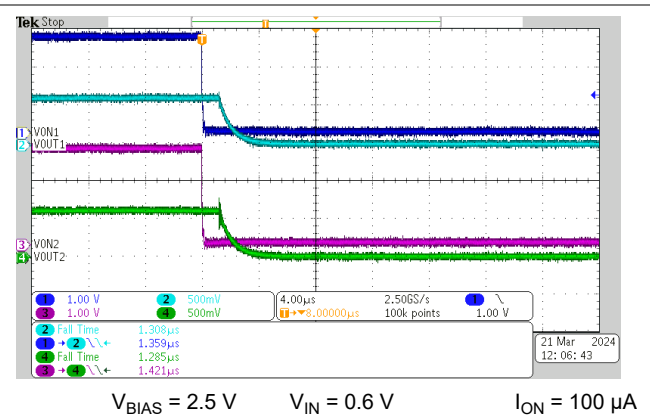


Figure 5-18. Turnoff Response Time

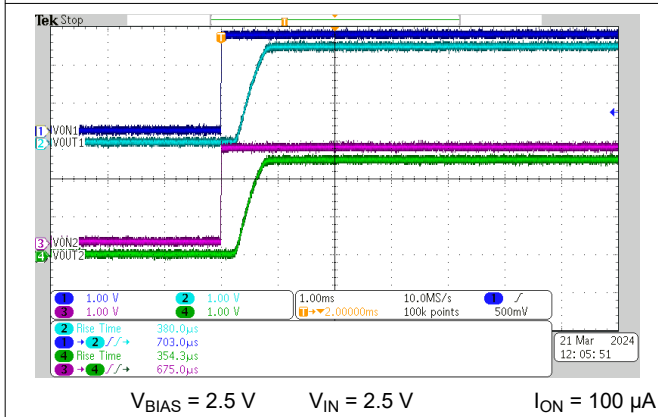


Figure 5-19. Turnon Response Time

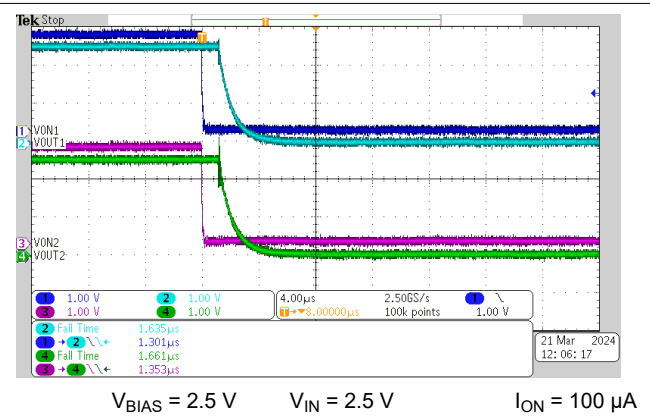


Figure 5-20. Turnoff Response Time

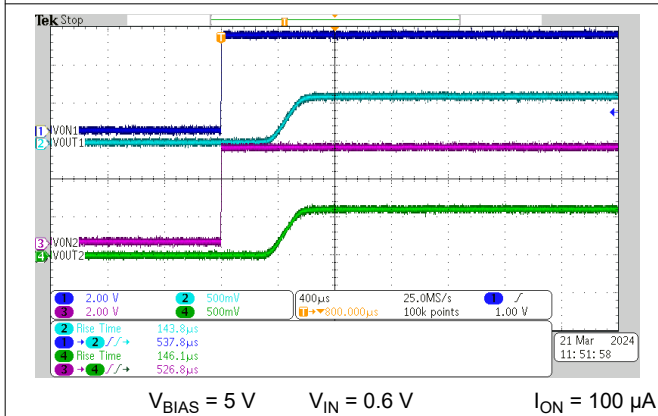


Figure 5-21. Turnon Response Time

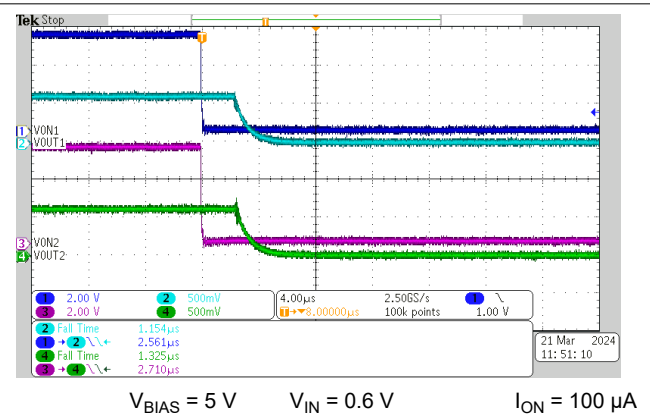
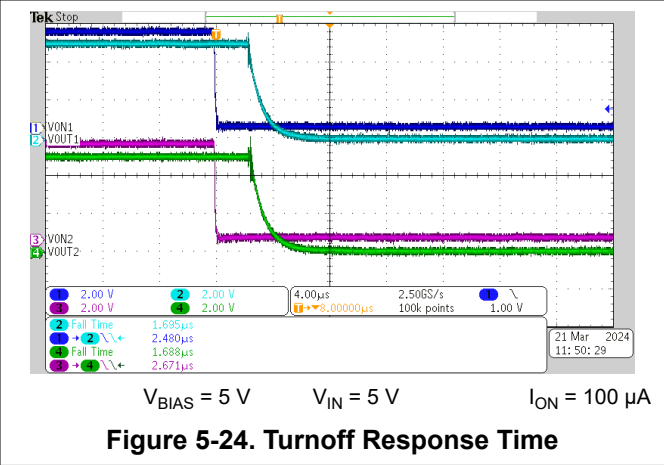
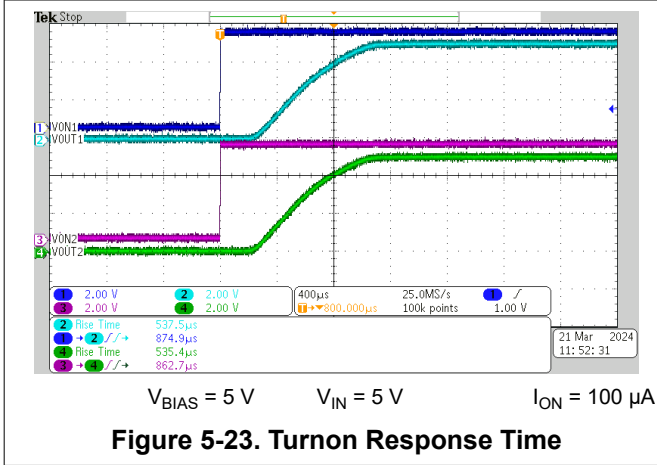


Figure 5-22. Turnoff Response Time



## 6 Parameter Measurement Information

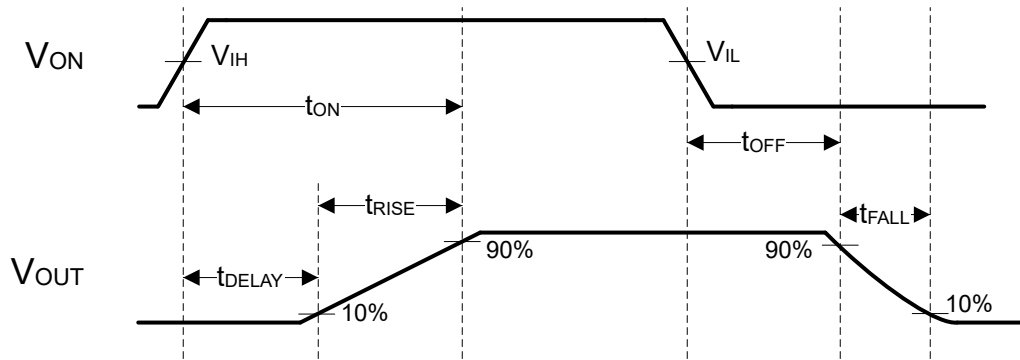


Figure 6-1.  $t_{ON}$  and  $t_{OFF}$  Waveforms

## 7 Detailed Description

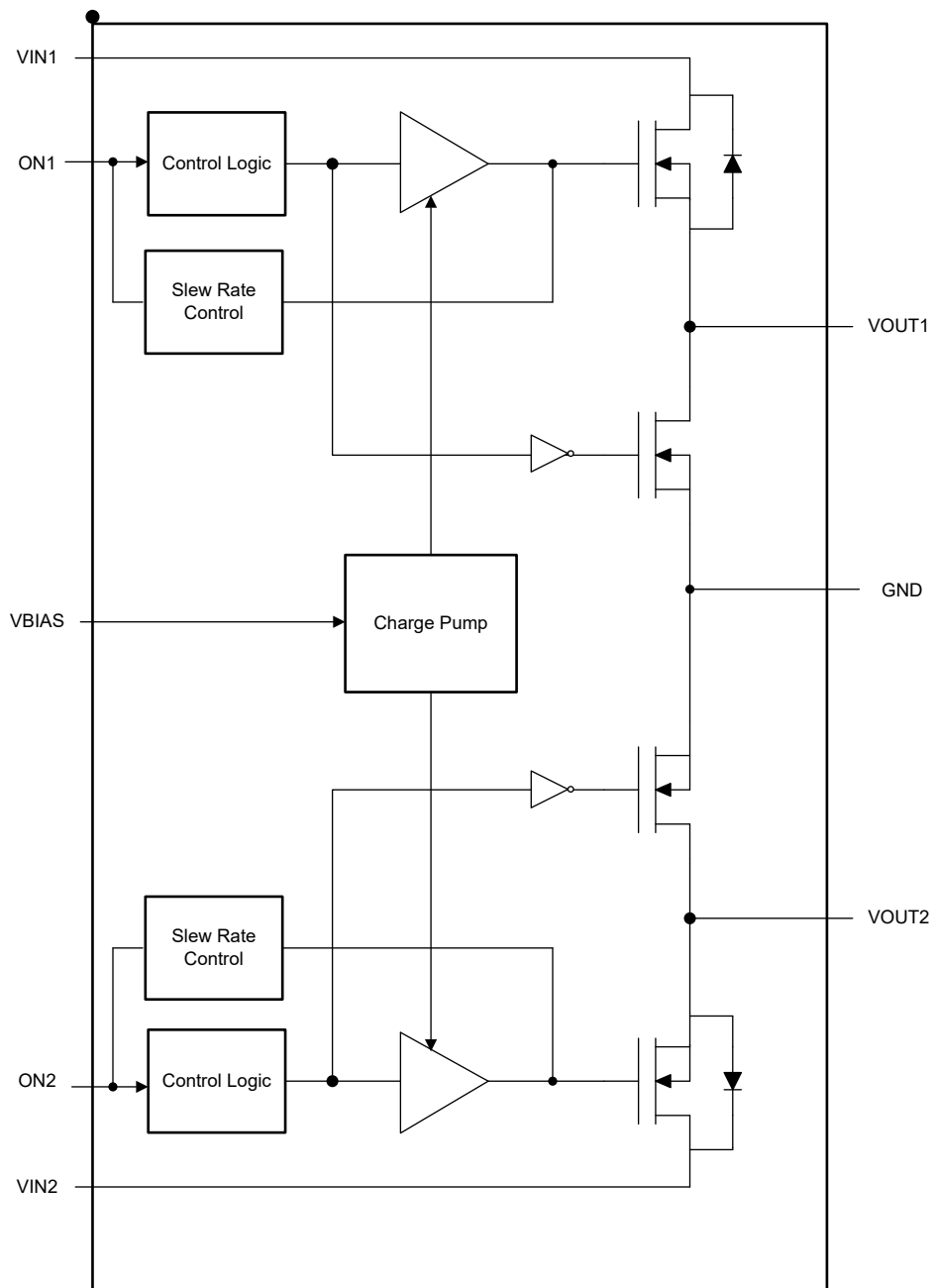
### 7.1 Overview

The TPS22996H-Q1 is a 5.5V, dual-channel, 13m $\Omega$  (typical)  $R_{ON}$  load switch in a 8-pin DYC package. Each channel can support a maximum continuous current of 4A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. Note that the ON pins must be connected and cannot be left floating. The device has a configurable slew rate for applications that require specific rise-time, which controls the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. Furthermore, the slew rate is proportional to the series resistor used on the ONx pin. See [Section 7.3.7](#) to determine the correct resistor value for a desired rise time.

The internal circuitry is powered by the  $V_{BIAS}$  pin, which supports voltages from 2.5V to 5.5V. This circuitry includes the charge pump, QOD, and control logic. When a voltage is applied to  $V_{BIAS}$ , and the ON<sub>1,2</sub> pins transition to a low state, the QOD functionality is activated. This connects  $V_{OUT1}$  and  $V_{OUT2}$  to ground through the on-chip resistor. The typical pulldown resistance ( $R_{PD}$ ) is 230 $\Omega$ .

During the off state, the device prevents downstream circuits from pulling high standby current from the supply. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, reducing solution size and bill of materials (BOM) count.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high with a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

### 7.3.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1µF ceramic capacitor,  $C_{IN}$ ,

placed close to the pins is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

### 7.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a  $C_{IN}$  greater than  $C_L$  is highly recommended. A  $C_L$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ . A  $C_{IN}$  to  $C_L$  ratio of 10 to 1 is recommended for minimizing  $V_{IN}$  dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more  $V_{IN}$  dip upon turnon due to inrush currents. This can be mitigated by increasing the  $R_T$  resistance on the ON pin for a longer rise time (see [Section 7.3.7](#)).

### 7.3.4 Quick Output Discharge

When the switch is disabled, an internal discharge resistance is connected between  $V_{OUT}$  and GND to remove the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before  $V_{BIAS}$  falls below the minimum recommended voltage.

### 7.3.5 Humidity Resistance

TPS22996H-Q1 is designed to be resistant to humidity, which is replicated by 100kΩ short between any pin to either GND or power. Under such humidity conditions, our device is able to function correctly with ON, OFF and thermal shutdown. However, the timing parameter will be affected by the short condition, and will deviate from the typical value listed in the *Electrical Characteristics* table (see [Section 5.5](#)).

### 7.3.6 Thermal Shutdown

Thermal shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds  $T_{SD}$ , the switch is turned off. The switch automatically turns on again if the temperature of the die drops  $T_{SD,HYS}$  below the  $T_{SD}$  threshold.

### 7.3.7 Adjustable Rise Time

TPS22996H-Q1 integrates a unique architecture for adjusting the rise time. The device senses the current flowing into the ON1 and ON2 ( $I_{ON}$ ) pins and utilizes the information to set the rise time. This allows the user to adjust the rise time by connecting a series resistance that is determined by the ON pin voltage. Refer to [Table 7-1](#) for reference on setting the resistor.

**Table 7-1. Typical Rise Time (VBIAS = 5V)**

$I_{ON}$	$V_{IN} = 0.6V$	$V_{IN} = 1.8V$	$V_{IN} = 2.5V$	$V_{IN} = 3.3V$	$V_{IN} = 5V$
20μA	764μs	1380μs	1700μs	1955μs	2350μs
100μA	203μs	343μs	426μs	500μs	626μs
250μA	85μs	148μs	180μs	208μs	265μs

**Table 7-2. Typical Rise Time (VBIAS = 3.3V)**

$I_{ON}$	$V_{IN} = 0.6V$	$V_{IN} = 1.8V$	$V_{IN} = 2.5V$	$V_{IN} = 3.3V$
20μA	738μs	1420μs	1735μs	2040μs
100μA	191μs	360μs	437μs	512μs
250μA	88μs	239μs	170μs	204μs

The following equation can be used to estimate the series resistance required to meet the desired rise time.

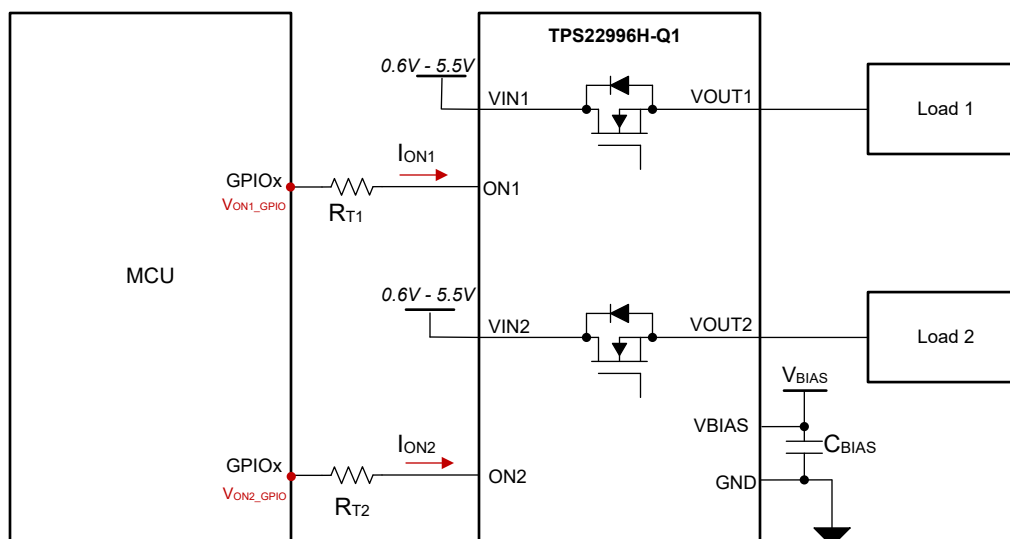
$$R_{Tx} = 1000 \times (V_{ONx\_GPIO} - 1.2V) / I_{ONx} - R_i \quad (1)$$

where:

**TPS22996H-Q1**

SLVSHA3A – MARCH 2024 – REVISED OCTOBER 2024

- $R_{Tx}$  = Channel  $\times$  series resistance in  $k\Omega$ .
- $R_i$  = Internal ON pin resistance  $k\Omega$ .
- $V_{ONx\_GPIO}$  = Channel  $\times$  GPIO voltage connected to ONx pin in V.
- $I_{ONx}$  = Current flowing into the ONx pin in  $\mu A$ .



**Figure 7-1. TPS22996H-Q1 Adjustable Rise Time Configuration**

## 7.4 Device Functional Modes

Table 7-3 lists the TPS22996H-Q1 functions.

**Table 7-3. TPS22996H-Q1 Functions Table**

ON	VIN to VOUT	VOUT
L	Off	GND
H	On	VIN



## 8 Application and Implementation

### Note

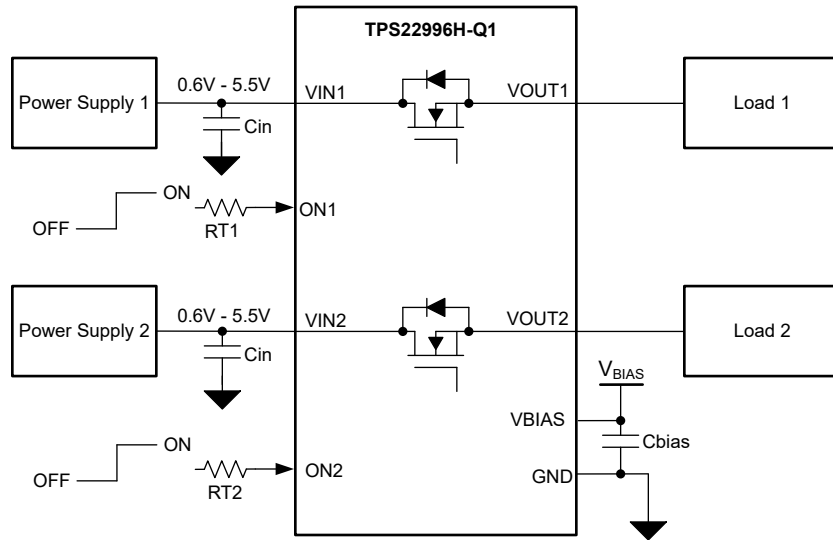
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

This section highlights some of the design considerations for implementing the device in various applications.

### 8.2 Typical Application

This application demonstrates how the TPS22996H-Q1 can be used to limit the inrush current when powering on downstream modules.



**Figure 8-1. Typical Application Circuit**

**Table 8-1. Component Descriptions**

DESIGN PARAMETER	TYPICAL VALUES	DESCRIPTION
$C_{IN}$	1 $\mu$ F	Filtering voltage transients
$C_{OUT}$	100nF	Filtering voltage transients
$C_{BIAS}$	0.1 $\mu$ F	Filtering voltage transients
RT1, RT2	10k $\Omega$	Series resistor for rise time control

### 8.2.1 Design Requirements

Table 8-2 shows the TPS22996H-Q1 design parameters.

**Table 8-2. Design Parameters**

DESIGN PARAMETER	VALUE
$V_{BIAS}$	5V
$V_{IN}$	5V
Rise Time	1000 $\mu$ s

### 8.2.2 Detailed Design Procedure

The design in this example is trying to achieve 1000µs rise time for power sequencing, with both  $V_{BIAS}$  and  $V_{IN}$  to be 5V. From [Table 7-1](#), the  $I_{ON}$  needs to be between 20µA and 100µA. To find the  $I_{ON}$  needed to achieve 1000µs rise time, linear interpolation can be used to estimate as below:

$$T_R = (T_{R2} - T_{R1}) / (I_{ON2} - I_{ON1}) * (I_{ON} - I_{ON1}) + T_{R1} \quad (2)$$

where:

- $T_R$  is the desired  $T_R$ , which is 1000µs
- $I_{ON}$  is the desired  $I_{ON}$
- $T_{R1}$  is the first  $T_R$  used for linear interpolation, which is 2350µs
- $T_{R2}$  is the second  $T_R$  used for linear interpolation, which is 626µs
- $I_{ON1}$  is the first  $I_{ON}$  used for linear interpolation, which is 20µA
- $I_{ON2}$  is the second  $I_{ON}$  used for linear interpolation, which is 100µA

$I_{ON}$  is calculated to be 82.6µA. To find the  $R_T$  value, plug in the parameters in [Equation 1](#).

$$R_T = 1000 \times (5V - 1.2V) / 82.6\mu A - 12.5k\Omega = 33.5k\Omega$$

By using the standard resistor value closest to 33.5kΩ, the typical rise time can be calculated for the actual resistor value used on board.

## 8.3 Power Supply Recommendations

The device is designed to operate from a  $V_{BIAS}$  range of 2.5V to 5.5V and a  $V_{IN}$  range of 0.6V to  $V_{BIAS}$ .

## 8.4 Layout

### 8.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for  $V_{IN}$ ,  $V_{OUT}$ , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

### 8.4.2 Layout Example

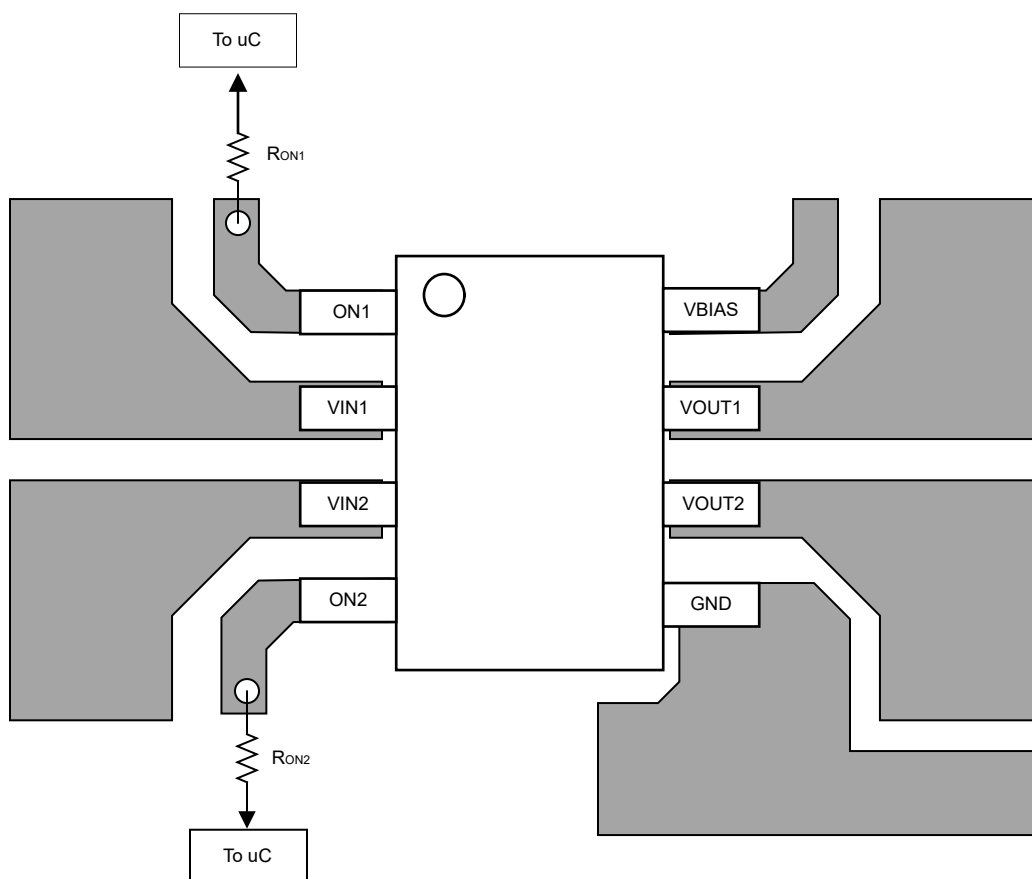


Figure 8-2. TPS22996H Layout Example

### 8.4.3 Power Dissipation

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation,  $P_{D(max)}$  for a given output current and ambient temperature, use Equation 3.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (3)$$

where

- $P_{D(max)}$  is the maximum allowable power dissipation.
- $T_{J(max)}$  is the maximum allowable junction temperature (150°C for the TPS22996H).

- $T_A$  is the ambient temperature of the device.
- $\theta_{JA}$  is the junction to air thermal impedance. See [Section 5.4](#). This parameter is highly dependent upon board layout.

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2024) to Revision A (October 2024)	Page
• Changed the document status From: <i>Advance Information</i> To: <i>Production Data</i> .....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22996HQDYCRQ1	ACTIVE	SOT-5X3	DYC	8	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	996HQ	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

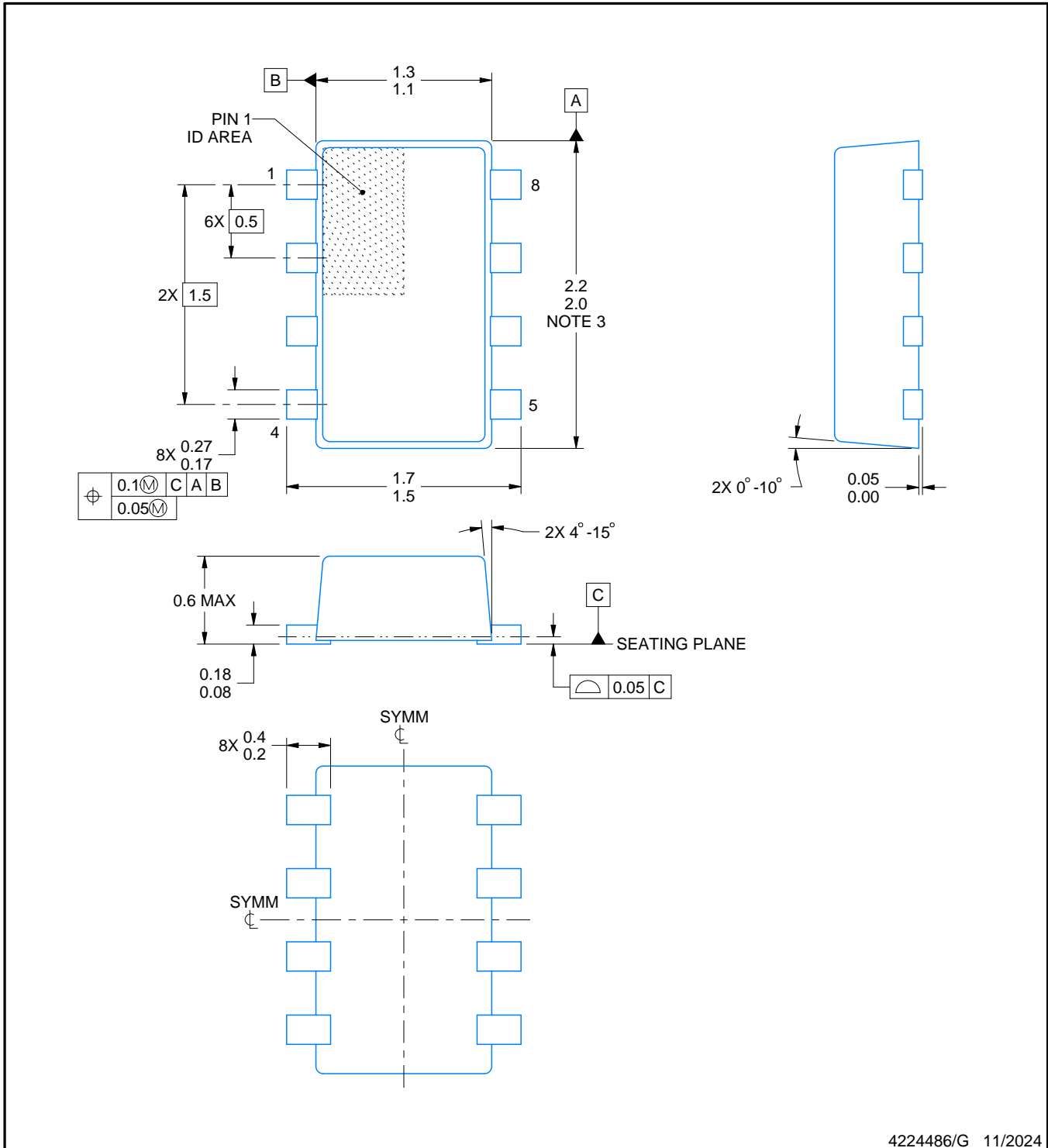
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22996HQDYCRQ1	SOT-5X3	DYC	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22996HQDYCRQ1	SOT-5X3	DYC	8	4000	210.0	185.0	35.0



4224486/G 11/2024

NOTES:

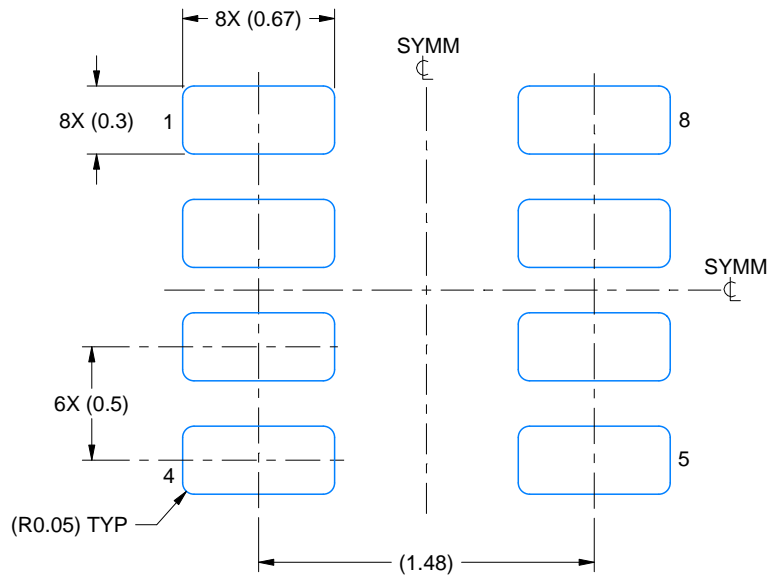
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

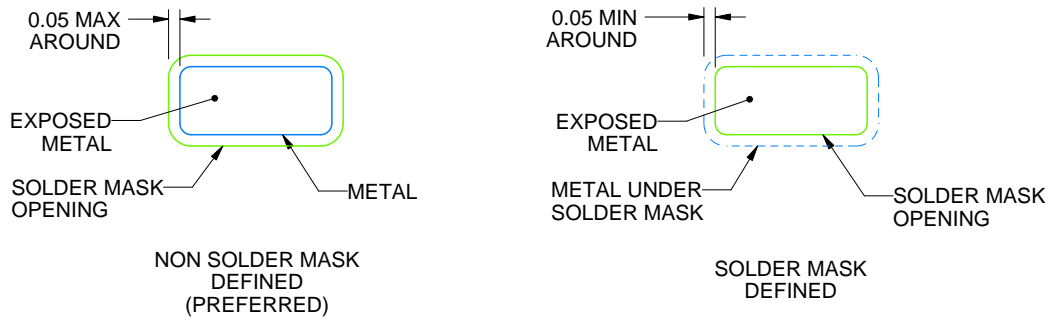
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

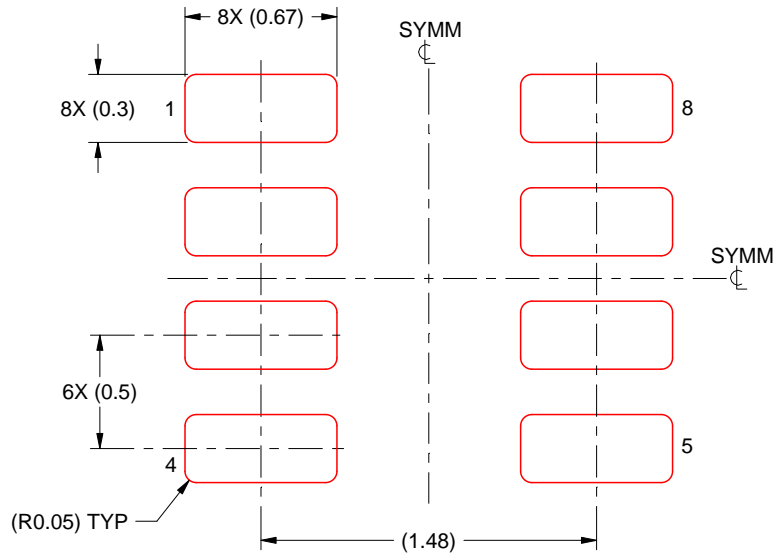
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

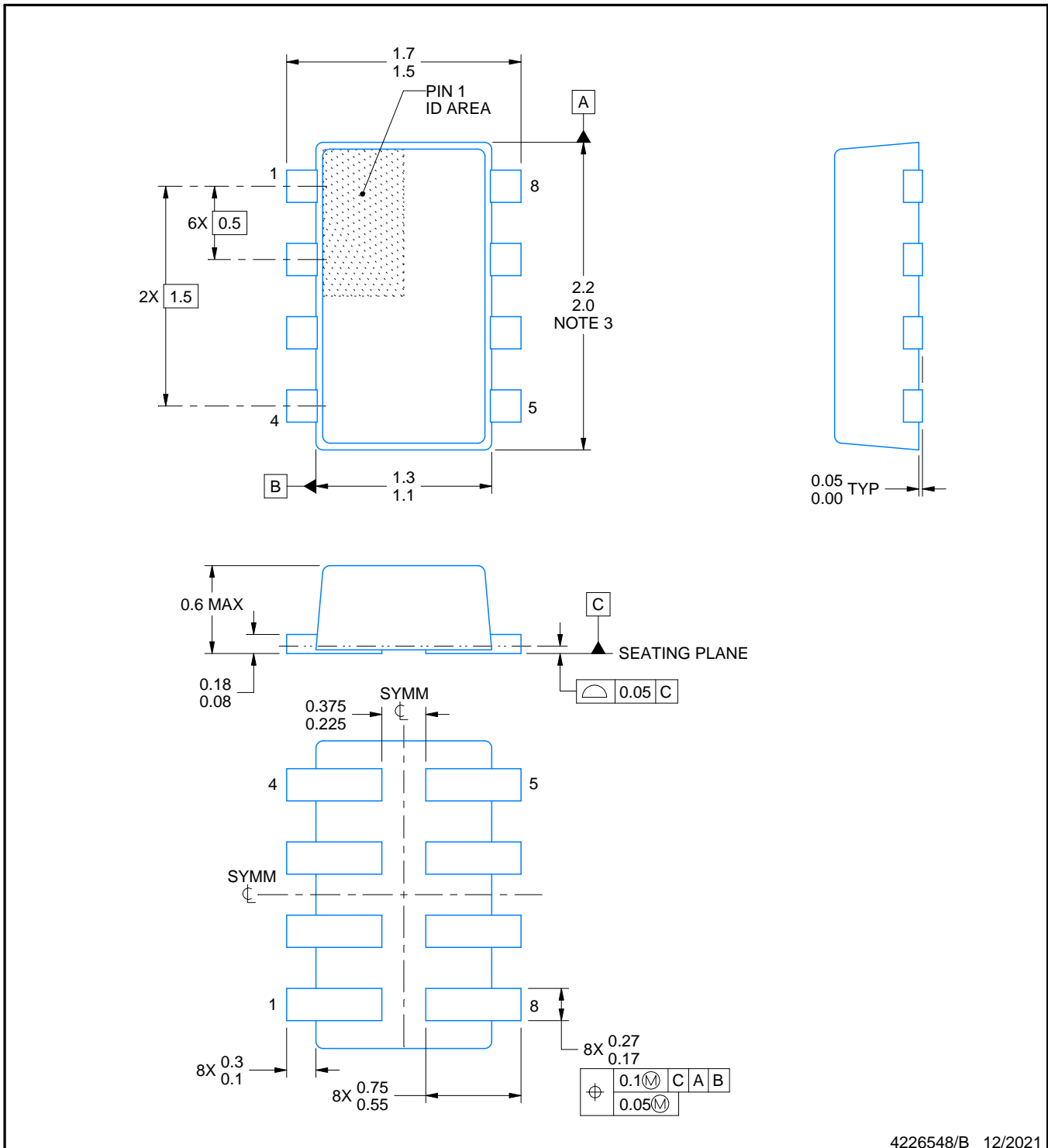
# DYC0008A



# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4226548/B 12/2021

### NOTES:

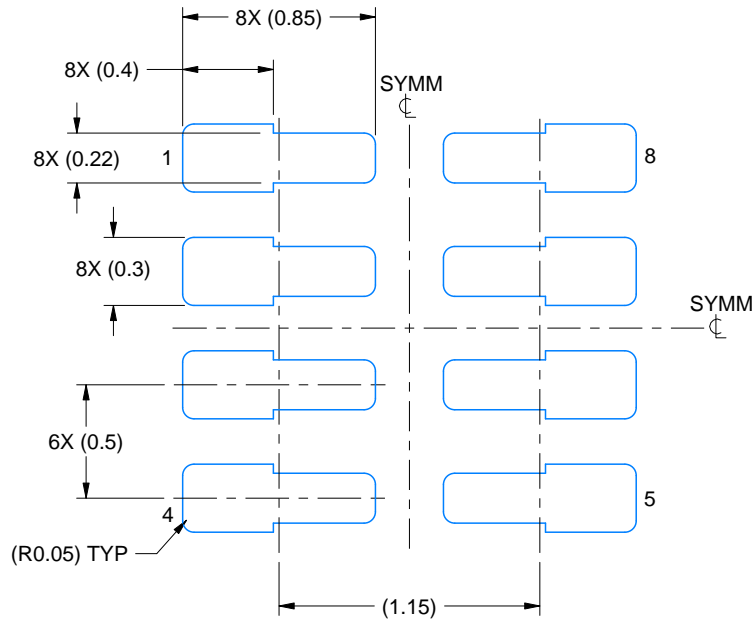
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

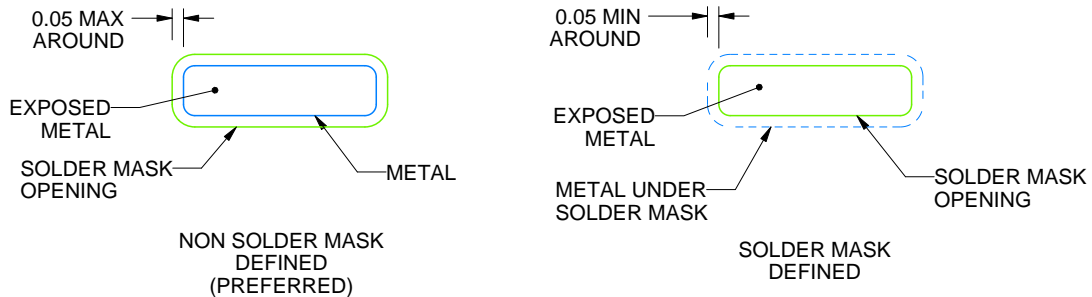
DYC0008A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

4226548/B 12/2021

NOTES: (continued)

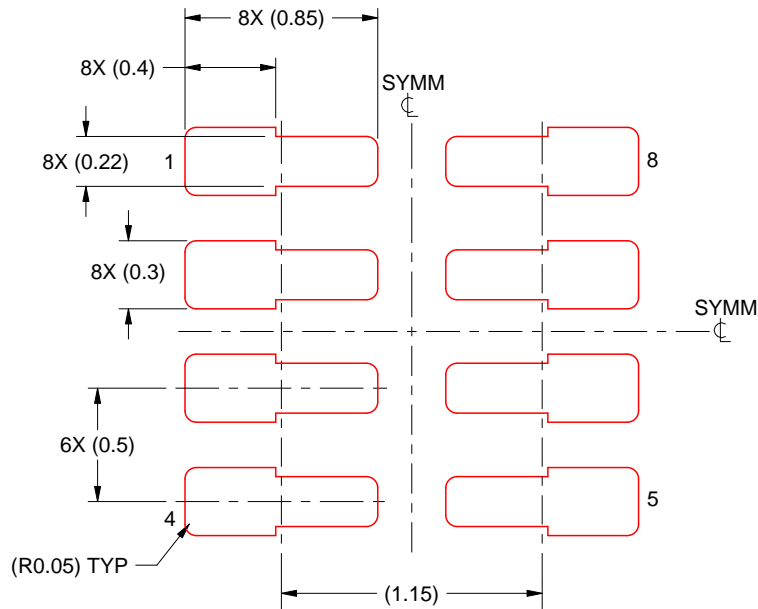
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DYC0008A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4226548/B 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated