TPS22991 5V, 3A, 25mΩ Load Switch Device With Small Plastic Package

1 Features

- Integrated single channel load switch
- Input voltage range: 1V to 5.5V
- 3A maximum continuous switch current
- 25mΩ typical ON-resistance
- Low quiescent current:
  - I_Q at 3.3V V_{IN} = 6µA (typ)
- Low shutdown current:
  - I_{SD} at 3.3V V_{IN} = 14nA (typ)
- Controlled slew rate:
  - Version B, BN: rise time (t_R) at 3.3V V_{IN} = 141µs
  - Version C, CN: rise time (t_R) at 3.3V V_{IN} = 662µs
- Quick output discharge (QOD) of 150Ω
- Thermal shutdown protection
- 0.85 × 0.75mm, 0.4mm pitch UQFN package

2 Applications

- PC and notebooks
- Wearables
- Solid state drive (SSD)
- Industrial PC

3 Description

The TPS22991 is a small, low R_{ON}, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.0V to 5.5V and can support a maximum continuous current of 3A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

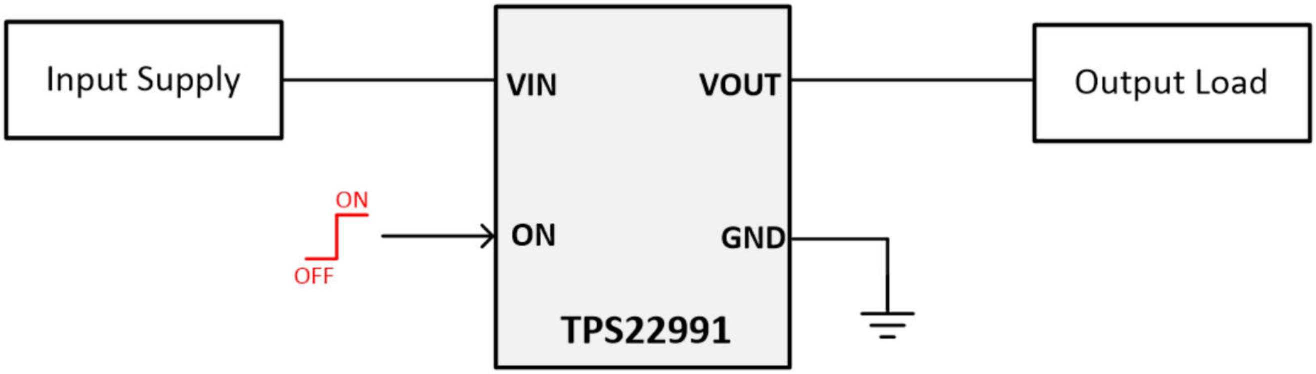
The small size and low R_{ON} makes the device ideal for being used in space constrained, battery powered applications. The wide input voltage range of the switch makes it a versatile solution for many different voltage rails. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS22991 further reduces the total solution size by integrating a 150Ω pulldown resistor for quick output discharge (QOD) when the switch is turned off.

The TPS22991 is available in a small, space saving 0.85mm × 0.75mm, 0.4mm pitch, 4-pin UQFN package. The device is characterized for operation over the free-air temperature range of –55°C to +125°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS22991	RAA (UQFN, 4)	0.85mm × 0.75mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS22991 Typical Application

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4 Device Comparison Table

Table 4-1. Functionality Comparison

PART NUMBER	QUICK OUTPUT DISCHARGE (QOD)	TURN ON TIME
TPS22991B	Yes	Fast
TPS22991BN(1)	No	Fast
TPS22991C	Yes	Slow
TPS22991CN(1)	No	Slow

(1) Device in preview. Please contact TI for more information.

5 Pin Configuration and Functions

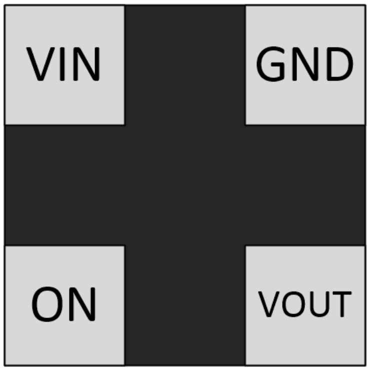


Figure 5-1. TPS22991 RAA Package, 4-Pin UQFN (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Switch input.
ON	2	I	Active high switch control input.
VOUT	3	O	Switch output.
GND	4	—	Device ground.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum input voltage range	–0.3	6	V
V_{OUT}	Maximum output voltage range	–0.3	6	V
V_{ON}	Maximum ON pin voltage range	–0.3	6	V
I_{MAX}	Maximum continuous current		3	A
I_{PLS}	Maximum pulsed current (2ms, 2% duty cycle)		4	A
T_J	Junction temperature	–55	150	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum lead temperature (10s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1750	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	1.0		5.5	V
V_{OUT}	Output voltage range	0		5.5	V
V_{IH}	ON pin high voltage Range	0.8		5.5	V
V_{IL}	ON pin low voltage range	0		0.35	V
T_A	Ambient temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS22991	UNIT
		4 PINS	
		RAA	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	214.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values at VIN = 3.3V unless otherwise specified

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)								
$I_{Q, VIN}$	VIN quiescent current	$V_{ON} \geq V_{IH}$, VOUT = Open		25°C		6		µA
				–40°C to 85°C			12	µA
				–55°C to 125°C			14	µA
$I_{SD, VIN}$	VIN shutdown current	$V_{ON} \leq V_{IL}$, VOUT = Open		25°C		14		nA
				–40°C to 85°C			20	µA
				–55°C to 125°C			67	µA
$I_{SD, VIN}$	VIN shutdown current	$V_{ON} \leq V_{IL}$, VOUT = GND	$V_{ON} \leq V_{IL}$, VOUT = GND	25°C		15		nA
				–40°C to 85°C			20	µA
				–55°C to 125°C			67	µA
ON-RESISTANCE (RON)								
R_{ON}	ON-state resistance	I_{OUT} = –200mA	V_{IN} = 5V	25°C		25		mΩ
				–40°C to 85°C			35	mΩ
				–40°C to 105°C			38	mΩ
				–55°C to 125°C			40	mΩ
			V_{IN} = 3.3V	25°C		25		mΩ
				–40°C to 85°C			35	mΩ
				–40°C to 105°C			38	mΩ
				–55°C to 125°C			40	mΩ
			V_{IN} = 1.8V	25°C		25		mΩ
				–40°C to 85°C			35	mΩ
				–40°C to 105°C			38	mΩ
				–55°C to 125°C			40	mΩ
			V_{IN} = 1V	25°C		35		mΩ
				–40°C to 85°C			48	mΩ
				–40°C to 105°C			52	mΩ
				–55°C to 125°C			60	mΩ
THERMAL SHUTDOWN (TSD)								
$T_{SD,R}$	Thermal shutdown			Rising		170		℃
$T_{SD,F}$	Thermal shutdown			Falling		150		℃
ENABLE PIN (ON)								
I_{ON}	ON pin leakage	$V_{ON} \geq V_{IH}$		–55°C to 125°C			100	nA
$R_{PD, ON}$	Smart pull down resistance	$V_{ON} \leq V_{IL}$		–55°C to 125°C		500		kΩ
$V_{IH,ON}$	ON pin threshold (VIH rising)			–55°C to 125°C			0.8	V
$V_{Hys,ON}$	ON pin threshold (hysteresis)			–55°C to 125°C		0.07		V
$V_{IL,ON}$	ON pin threshold (VIL falling)			–55°C to 125°C	0.35			V
QUICK OUTPUT DISCHARGE (QOD)								
R_{QOD}	QOD pin internal discharge resistance (Version B, C)	$V_{ON} \leq V_{IL}$	V_{IN} = 1V	–55°C to 125°C		190		Ω
			V_{IN} = 3.3V	–55°C to 125°C		150		Ω
			V_{IN} = 5V	–55°C to 125°C		140		Ω

6.6 Switching Characteristics (Version C, CN)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.3V, an ambient temperature of 25°C, and a load of CL = 0.1µF, RL = 10Ω. Timing parameter measurement details are shown in the timing diagram in the data sheet. Parameter not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON time	VIN = 5.0V		1119		µs
		VIN = 3.3V		996		µs
		VIN = 1.8V		853		µs
		VIN = 1.0V		774		µs
t_R	Output rise time	VIN = 5.0V		794		µs
		VIN = 3.3V		662		µs
		VIN = 1.8V		514		µs
		VIN = 1.0V		397		µs
t_D	Delay time	VIN = 5.0V		332		µs
		VIN = 3.3V		341		µs
		VIN = 1.8V		346		µs
		VIN = 1.0V		383		µs
t_{OFF}	Turn OFF time	VIN = 5.0V		6		µs
		VIN = 3.3V		4		µs
		VIN = 1.8V		2		µs
		VIN = 1.0V		4		µs
t_F	Output Fall time	VIN = 5.0V		5		µs
		VIN = 3.3V		5		µs
		VIN = 1.8V		5		µs
		VIN = 1.0V		5		µs

6.7 Switching Characteristics (Version B, BN)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.3V, an ambient temperature of 25°C, and a load of CL = 0.1µF, RL = 10Ω. Timing parameter measurement details are shown in the timing diagram in the data sheet. Parameter not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON time	VIN = 5.0V		302		µs
		VIN = 3.3V		259		µs
		VIN = 1.8V		216		µs
		VIN = 1.0V		198		µs
t_R	Output rise time	VIN = 5.0V		173		µs
		VIN = 3.3V		141		µs
		VIN = 1.8V		107		µs
		VIN = 1.0V		81		µs
t_D	Delay time	VIN = 5.0V		127		µs
		VIN = 3.3V		117		µs
		VIN = 1.8V		109		µs
		VIN = 1.0V		116		µs
t_{OFF}	Turn OFF time	VIN = 5.0V		6		µs
		VIN = 3.3V		4		µs
		VIN = 1.8V		2		µs
		VIN = 1.0V		4		µs

6.7 Switching Characteristics (Version B, BN) (continued)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.3V, an ambient temperature of 25°C, and a load of CL = 0.1µF, RL = 10Ω. Timing parameter measurement details are shown in the timing diagram in the data sheet. Parameter not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	Output fall time	VIN = 5.0V		5		µs
		VIN = 3.3V		5		µs
		VIN = 1.8V		5		µs
		VIN = 1.0V		5		µs

7 Typical Characteristics

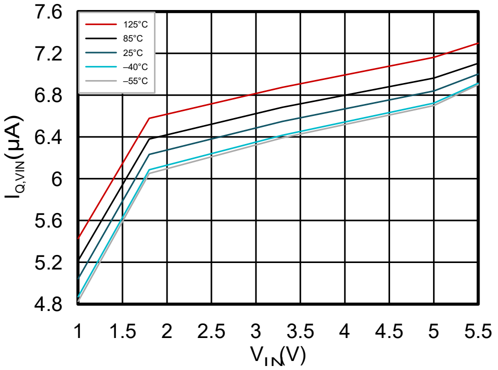
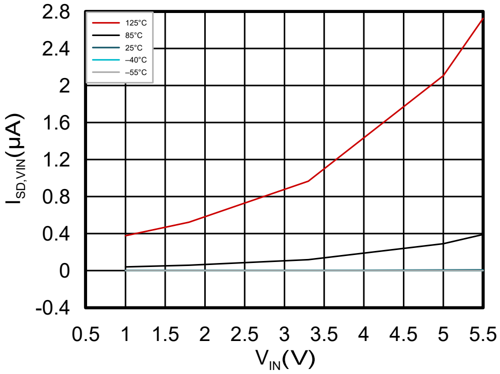
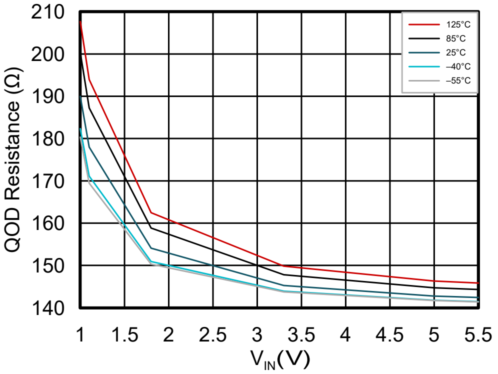


Figure 7-1. V_{IN} Quiescent Current vs Input Voltage



TPS22991B, TPS22991C

Figure 7-2. V_{IN} Shutdown Current vs Input Voltage



TPS22991B, TPS22991C

Figure 7-3. QOD Resistance vs Input Voltage

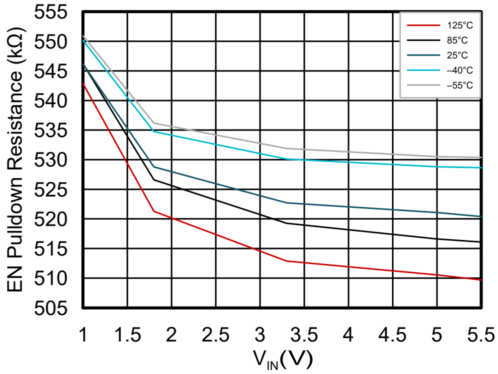


Figure 7-4. ON Pin Resistance $R_{PD,ON}$ vs Input Voltage

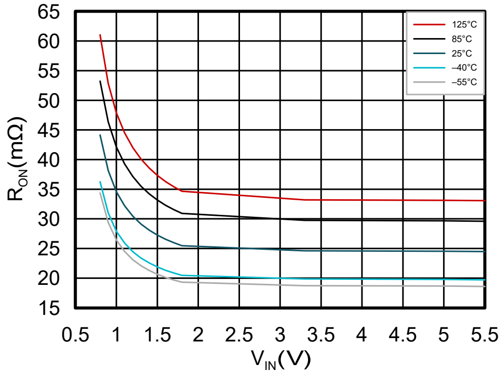
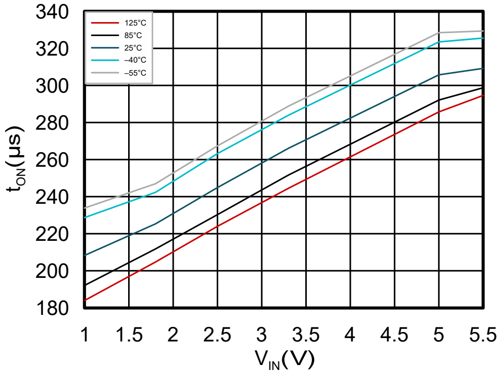


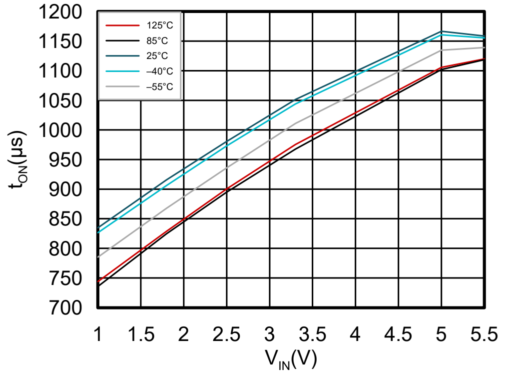
Figure 7-5. R_{ON} vs Input Voltage



C_L = 0.1µF R_L = 10Ω TPS22991B, TPS22991BN

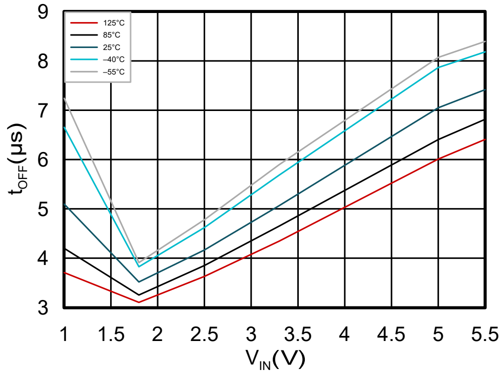
Figure 7-6. Turn ON Time vs Input Voltage

7 Typical Characteristics (continued)



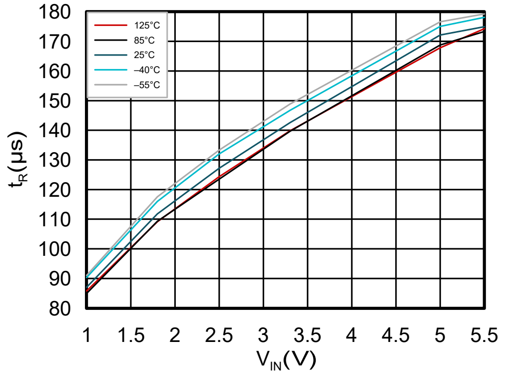
C_L = 0.1µF R_L = 10Ω TPS22991C, TPS22991CN

Figure 7-7. Turn ON Time vs Input Voltage



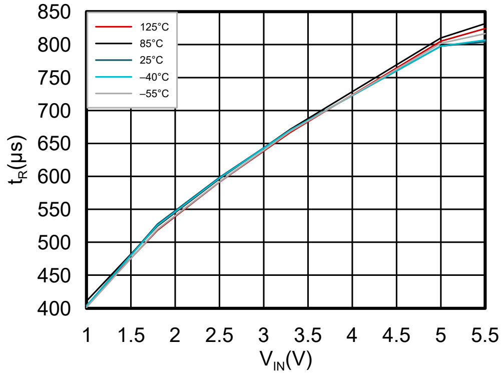
C_L = 0.1µF R_L = 10Ω

Figure 7-8. Turn OFF Time vs Input Voltage



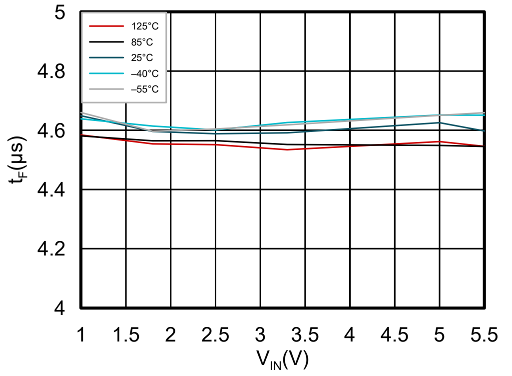
C_L = 0.1µF R_L = 10Ω TPS22991B, TPS22991BN

Figure 7-9. Rise Time vs Input Voltage



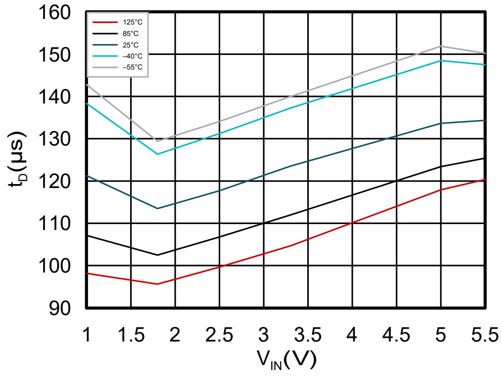
C_L = 0.1µF R_L = 10Ω TPS22991C, TPS22991CN

Figure 7-10. Rise Time vs Input Voltage



C_L = 0.1µF R_L = 10Ω

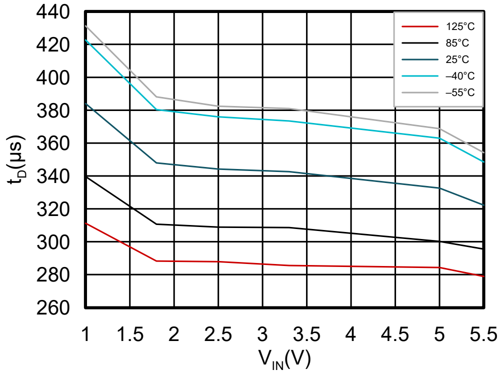
Figure 7-11. Fall Time vs Input Voltage



C_L = 0.1µF R_L = 10Ω TPS22991B, TPS22991BN

Figure 7-12. Delay Time vs Input Voltage

7 Typical Characteristics (continued)



C_L = 0.1µF R_L = 10Ω TPS22991C, TPS22991CN

Figure 7-13. Delay Time vs Input Voltage

8 Parameter Measurement Information

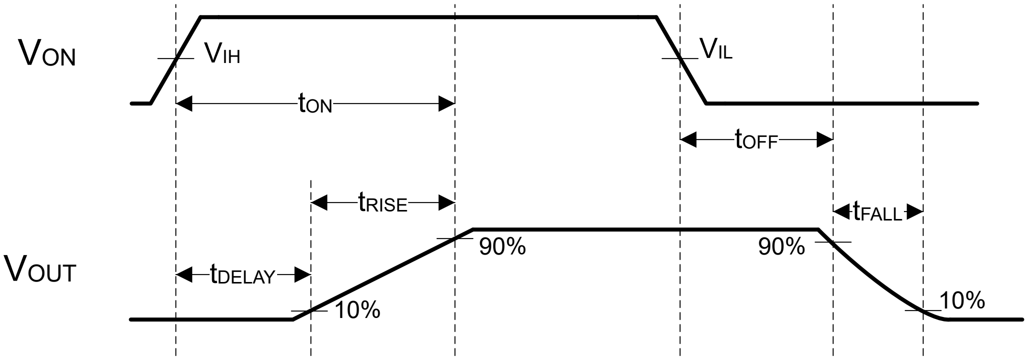


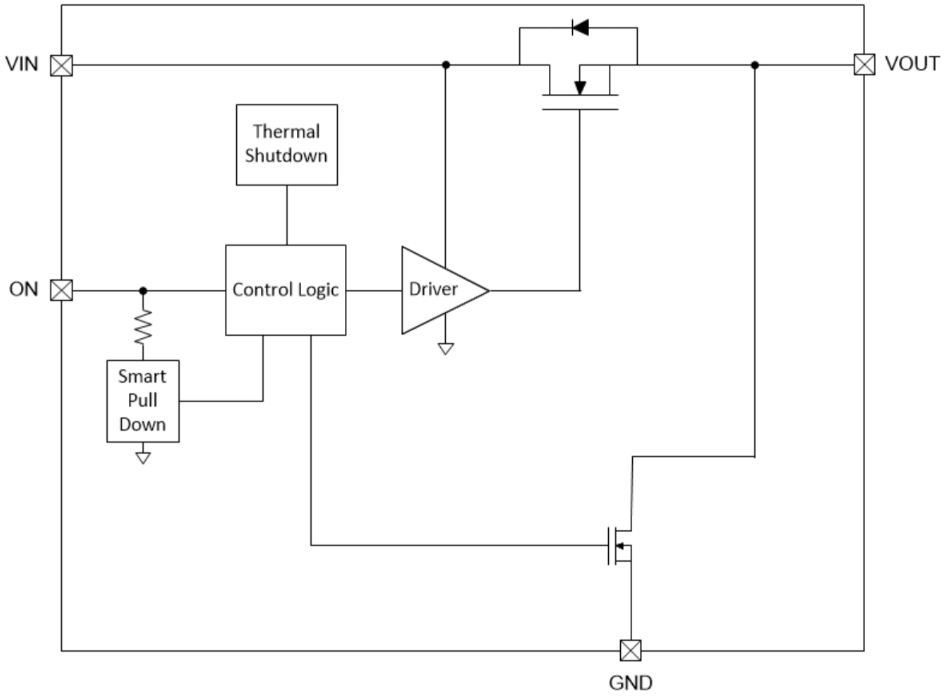
Figure 8-1. Timing Parameter Measurement Information

9 Detailed Description

9.1 Overview

The TPS22991 is a small, low R_{ON}, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1V to 5.5V and can support a maximum continuous current of 3A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to V_{IN}, a smart pulldown is used to keep the ON pin from floating until the system sequencing is complete. After the ON pin is deliberately driven high ($\geq V_{IH}$), the smart pulldown is disconnected to prevent unnecessary power loss. See Table 9-1 when the ON pin smart pulldown is active.

Table 9-1. On Pin Control

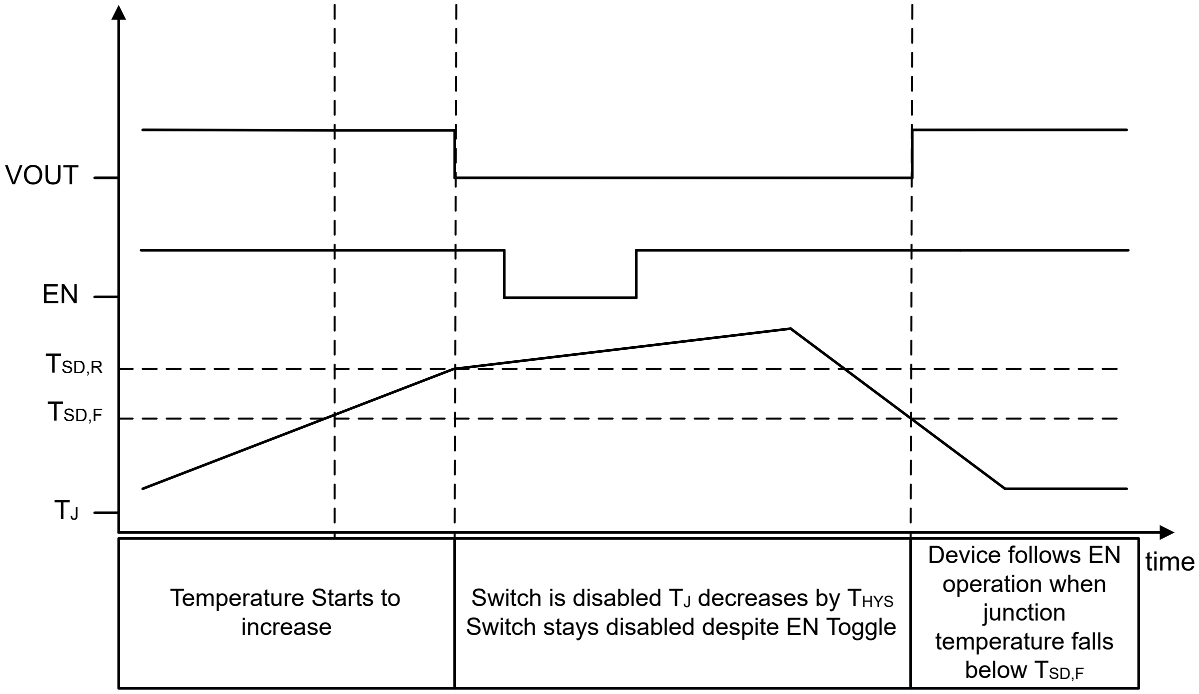
ON PIN VOLTAGE	ON PIN SMART PULLDOWN STATUS
$\leq V_{IL}$	Smart pulldown resistance active
$\geq V_{IH}$	Smart pulldown disconnected

9.3.2 Quick Output Discharge

TPS22991B and TPS22991C integrates quick output discharge. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 150Ω when V_{IN} = 3.3V, and prevents the output from floating while the switch is disabled.

9.3.3 Thermal Shutdown

When the device temperature reaches $T_{SD,\,R}$, the device shuts itself off to prevent thermal damage. After the device cools off to $T_{SD,F}$, it turns back on. If the device is kept in a thermally stressful environment, then the device oscillates between these two states until it can keep its temperature below the thermal shutdown point.



9.3.4 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.5 Output Capacitor (C_L)

Due to the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.4 Device Functional Modes

The table below describes the connection of the VOUT pin depending on the state of the ON pin.

ON	FAULT CONDITION	VOUT STATE
L	N/A	• Hi-Z for BN, CN • GND through QOD resistor for B, C
H	None	V_{IN} through R_{ON}
X	Thermal shutdown	• Hi-Z for BN, CN • GND through QOD resistor for B, C

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} condition of the device. After the R_{ON} of the device is determined based upon the V_{IN} condition, use the below equation to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{1}$$

where

- ΔV is the voltage drop from V_{IN} to V_{OUT}.
- I_{LOAD} is the load current.
- R_{ON} is the on-resistance of the device for a specific VIN and VBIAS.

10.2 Typical Application

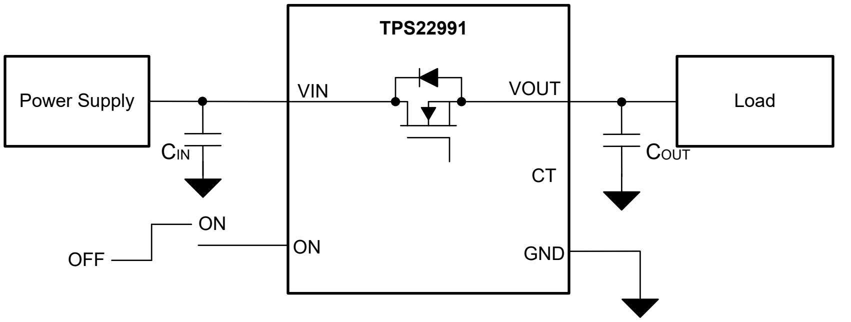


Figure 10-1. Typical Application Diagram

Table 10-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
C_{IN}	1µF	Filtering voltage transients
C_{OUT}	100nF	Filtering voltage transients

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-2.

Table 10-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5V
Load current	2A
Load capacitance	10µF

10.2.2 Detailed Design Procedure

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} condition of the device. After the R_{ON} of the device is determined based upon the V_{IN} condition, use the below equation to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{2}$$

where

- ΔV is the voltage drop from V_{IN} to V_{OUT}.
- I_{LOAD} is the load current.
- R_{ON} is the on-resistance of the device for a specific VIN and VBIAS.

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

To determine how much inrush current is caused by the load capacitance, use Equation 3.

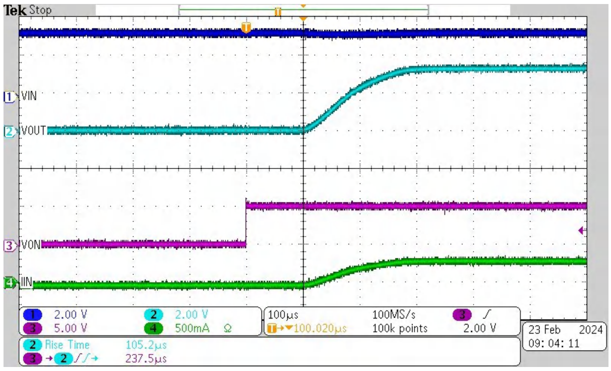
$$I_{INRUSH} = C_L \times dV_{OUT} / dt \tag{3}$$

where

- I_{INRUSH} is amount of inrush current caused by C_L
- C_L is the load capacitance on V_{OUT}
- dt is the rise time for V_{OUT} when the device is enabled
- dV_{OUT} is change in the V_{OUT} voltage after the device is enabled.

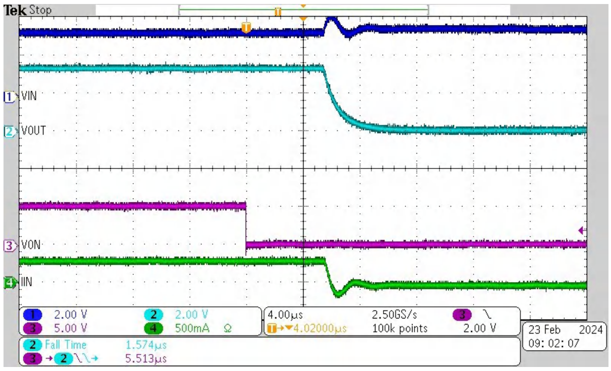
The slew rate of the device dV_{OUT}/dt at a given V_{IN} voltage can be found in the electrical characteristic table for a given version. I_{INRUSH} has to be within the I_{MAX} and I_{PLS} limits.

10.2.3 Application Curves



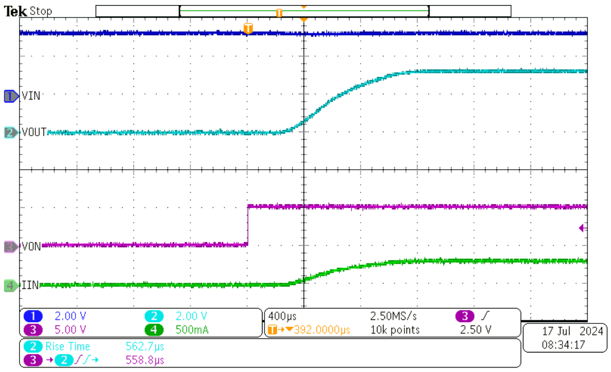
$C_L = 0.1\mu F$ $R_L = 10\Omega$ $V_{IN} = 3.3V$

Figure 10-2. Typical Turn On for TPS22991B



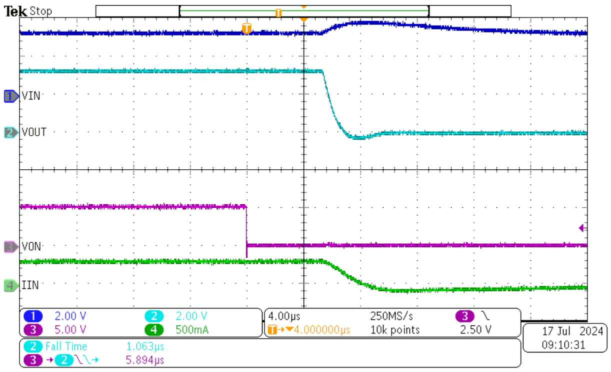
$C_L = 0.1\mu F$ $R_L = 10\Omega$ $V_{IN} = 3.3V$

Figure 10-3. Typical Turn Off for TPS22991B



C_L = 0.1µF R_L = 10Ω V_{IN} = 3.3V

Figure 10-4. Typical Turn On for TPS22991C



C_L = 0.1µF R_L = 10Ω V_{IN} = 3.3V

Figure 10-5. Typical Turn Off for TPS22991C

10.3 Power Supply Recommendations

The TPS22991 device is designed to operate with a V_{IN} range of 1V to 5.5V. Regulate the V_{IN} power supply well and place as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

10.4 Layout

10.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

10.4.2 Layout Example

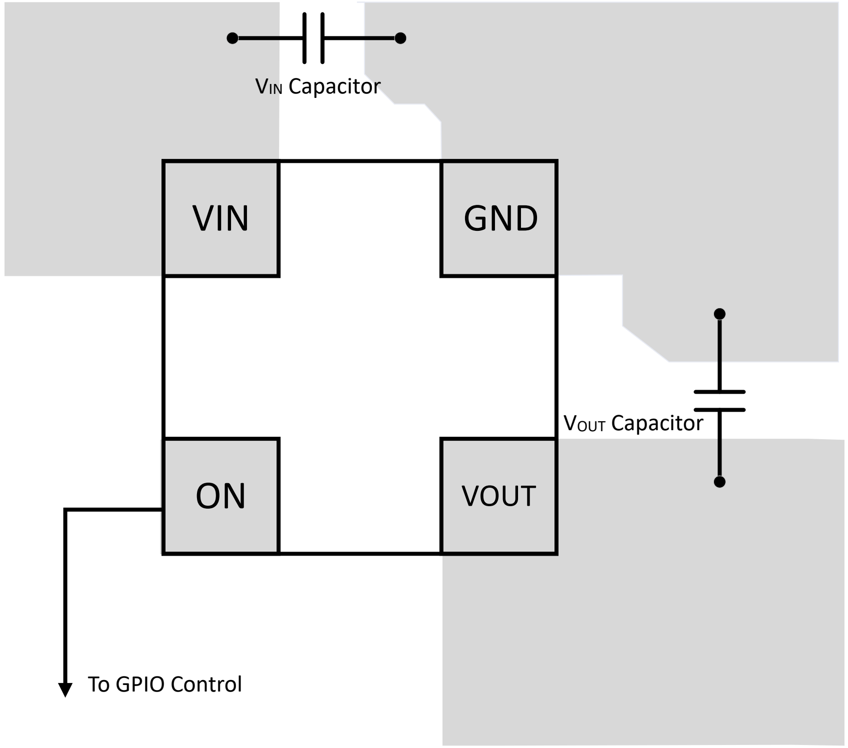


Figure 10-6. TPS22991 Layout

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (August 2024)	Page
• Changed the document status From: *Advance Information* To: *Production Data*	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22991BRAAR	ACTIVE	UQFN-HR	RAA	4	3000	TBD	Call TI	Call TI	-55 to 125		Samples
TPS22991BRAAR	ACTIVE	UQFN-HR	RAA	4	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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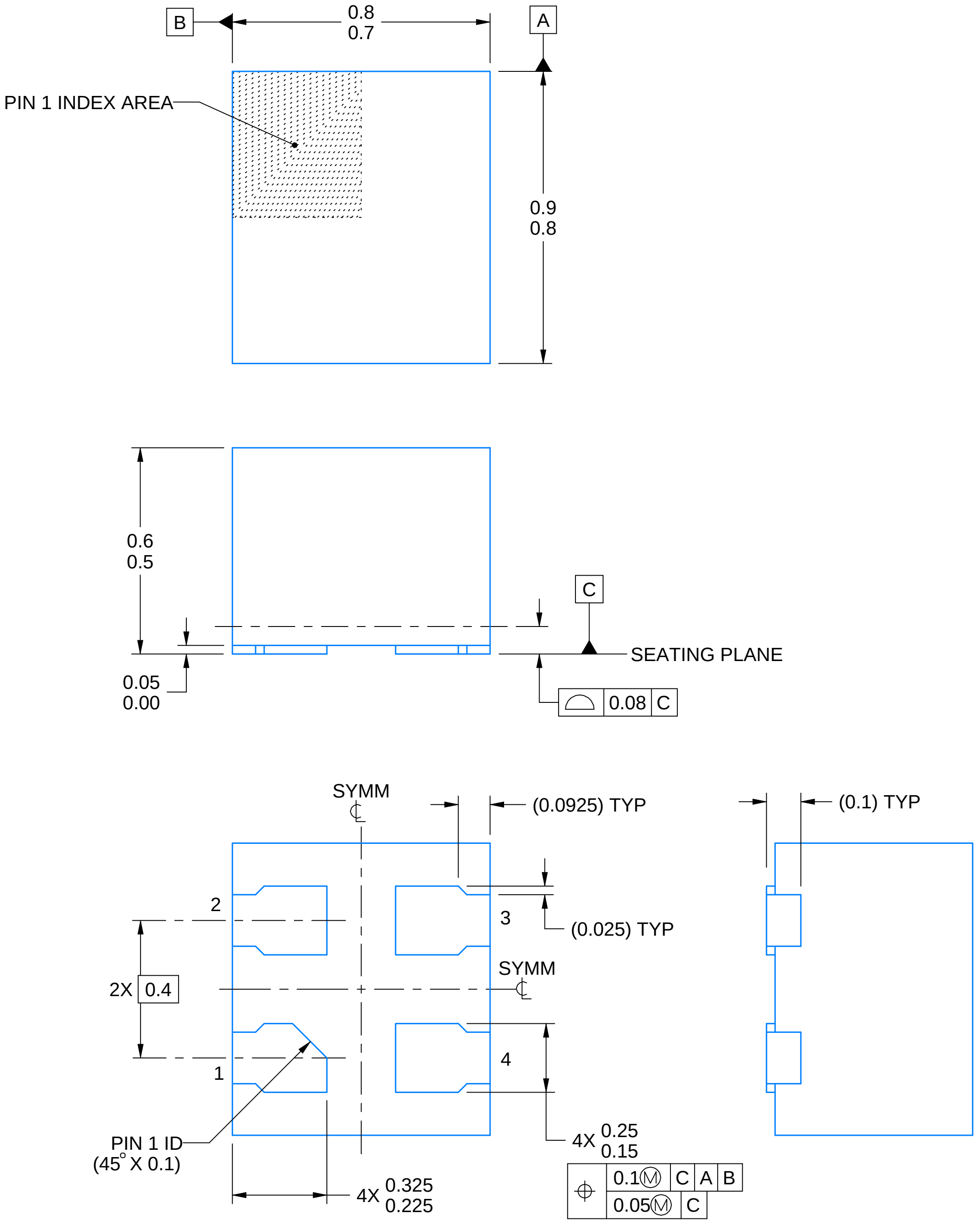
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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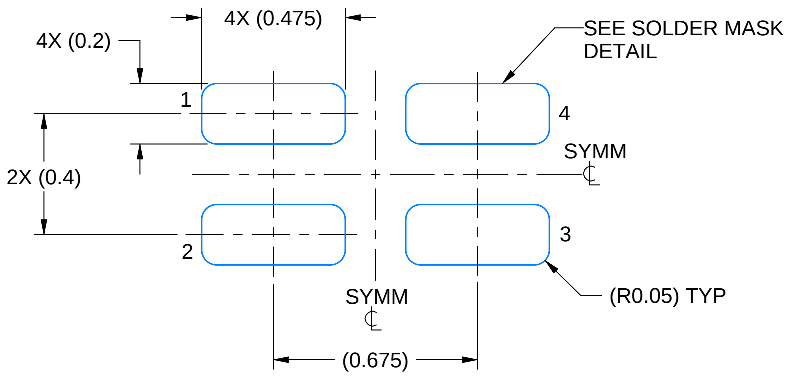
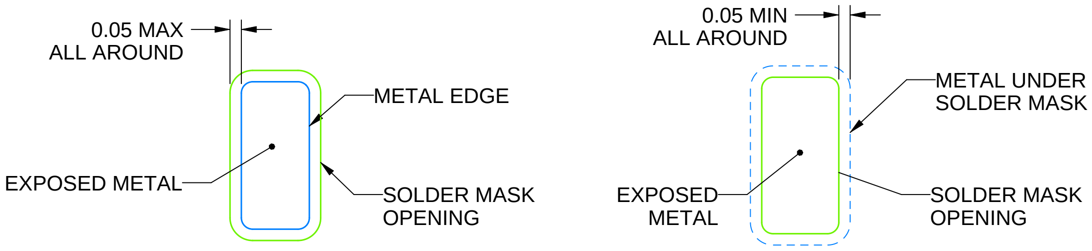
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



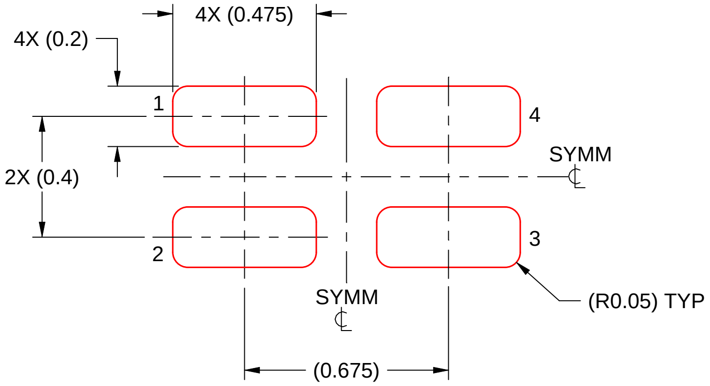
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 40X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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