# TPS22966-Q1 Dual-Channel, Ultralow Resistance Load Switch

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C6
- Integrated Dual-Channel Load Switch
- Input Voltage Range: 0 V to 5.5 V
- Ultralow ON-Resistance ($R_{ON}$)
  - $R_{ON}$ = 16 mΩ at $V_{IN}$ = 5 V ($V_{BIAS}$ = 5 V)
  - $R_{ON}$ = 16 mΩ at $V_{IN}$ = 3.3 V ($V_{BIAS}$ = 5 V)
  - $R_{ON}$ = 16 mΩ at $V_{IN}$ = 1.8 V ($V_{BIAS}$ = 5 V)
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 80 µA (Both Channels)
  - 80 µA (Single Channel)
- Low Control Input Threshold Enables Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD)
- SON 14-Pin Package With Thermal Pad

## 2 Applications

- Infotainment
- ADAS (Advanced Driver Assistance Systems)

## 3 Description

The TPS22966-Q1 device is a small, ultralow $R_{ON}$, dual-channel load switch with adjustable rise time. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0 V to 5.5 V and can support a maximum continuous current of up to 4 A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which can interface directly with low-voltage control signals. The TPS22966-Q1 includes a 230-Ω on-chip resistor for quick output discharge when the switch is turned off.

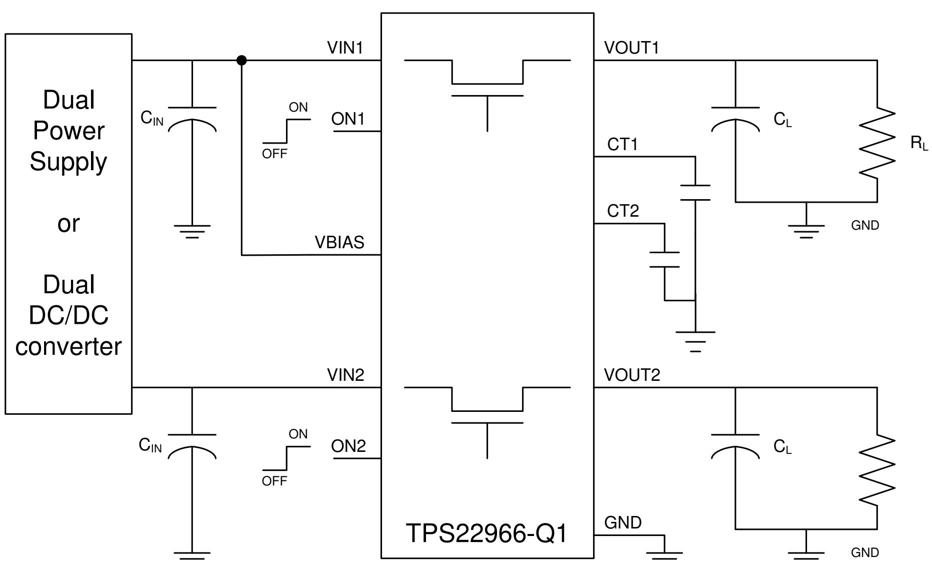
The TPS22966-Q1 is available in a small, space-saving 2-mm × 3-mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 105°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS22966-Q1 | WSON (14) | 3.00 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application Schematic**



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# 4 Revision History

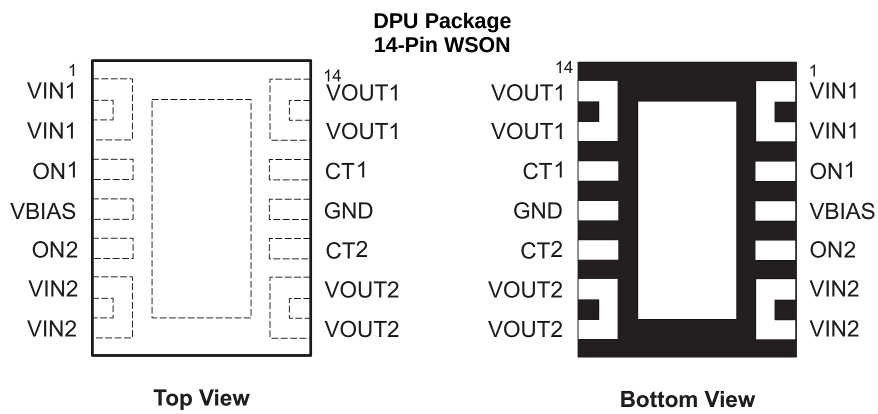
**Changes from Revision A (March 2015) to Revision B** — **Page**

- Changed Input voltage range from 0.8 V to 0 V in the *Recommended Operating Conditions* table .......... 4

**Changes from Original (December 2013) to Revision A** — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .......... 1

# 5 Pin Configuration and Functions




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | VIN1 | I | Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information section for more information. |
| 2 | VIN1 | I | Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information*for more information. |
| 3 | ON1 | I | Active high switch 1 control input. Do not leave floating. |
| 4 | VBIAS | I | Bias voltage. Power supply to the device. See *Application Information* for more information. |
| 5 | ON2 | I | Active high switch 2 control input. Do not leave floating. |
| 6 | VIN2 | I | Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information* for more information. |
| 7 | VIN2 | I | Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information* for more information. |
| 8 | VOUT2 | O | Switch 2 output. |
| 9 | VOUT2 | O | Switch 2 output. |
| 10 | CT2 | O | Switch 2 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance. |
| 11 | GND | – | Ground |
| 12 | CT1 | O | Switch 1 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance. |
| 13 | VOUT1 | O | Switch 1 output. |
| 14 | VOUT1 | O | Switch 1 output. |
| 15 | Thermal Pad | O | Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Guidelines* for layout guidelines. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN1,2}$ | Input voltage | –0.3 | 6 | V |
| $V_{OUT1,2}$ | Output voltage | –0.3 | 6 | V |
| $V_{ON1,2}$ | ON-pin voltage | –0.3 | 6 | V |
| $V_{BIAS}$ | VBIAS voltage | –0.3 | 6 | V |
| $I_{MAX}$ | Maximum continuous switch current per channel | | 4 | A |
| $I_{PLS}$ | Maximum pulsed switch current per channel, pulse <300 µs, 2% duty cycle | | 6 | A |
| $T_J$ | Maximum junction temperature | | 150 | °C |
| $T_{LEAD}$ | Maximum lead temperature (10-s soldering time) | | 300 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN1,2}$ | Input voltage range | | 0 | $V_{BIAS}$ | V |
| $V_{BIAS}$ | Bias voltage range | | 2.5 | 5.5 | V |
| $V_{ON1,2}$ | ON voltage range | | 0 | 5.5 | V |
| $V_{OUT1,2}$ | Output voltage range | | | $V_{IN}$ | V |
| $V_{IH}$ | High-level input voltage, ON | $V_{BIAS}$ = 2.5 V to 5.5 V | 1.2 | 5.5 | V |
| $V_{IL}$ | Low-level input voltage, ON | $V_{BIAS}$ = 2.5 V to 5.5 V | 0 | 0.5 | V |
| $C_{IN1,2}$ | Input capacitor | | 1(1) | | µF |
| $T_A$ | Operating free-air temperature(2) | | –40 | 105 | °C |

(1) Refer to *Application Information*.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS22966-Q1 DPU (WSON) 14 PINS | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 52.3 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 45.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 11.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 11.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 6.9 | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics: $V_{BIAS}$ = 5 V

Unless otherwise noted, the specifications apply over the operating ambient temperature, –40°C ≤ $T_A$ ≤ 105°C (full) and $V_{BIAS}$ = 5 V. Typical values are for $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES AND CURRENTS** | | | | | | | | |
| $I_{IN(VBIAS-ON)}$ | $V_{BIAS}$ quiescent current (both channels) | $I_{OUT1}$ = $I_{OUT2}$ = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = $V_{BIAS}$ = 5 V | | –40°C to 105°C | | 80 | 120 | µA |
| $I_{IN(VBIAS-ON)}$ | $V_{BIAS}$ quiescent current (single channel) | $I_{OUT1}$ = $I_{OUT2}$ = 0 mA, $V_{ON2}$ = 0 V $V_{IN1,2}$ = $V_{ON1}$ = $V_{BIAS}$ = 5 V | | –40°C to 105°C | | 80 | 120 | µA |
| $I_{IN(VBIAS-OFF)}$ | $V_{BIAS}$ shutdown current | $V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V | | –40°C to 105°C | | | 2 | µA |
| $I_{IN(VIN-OFF)}$ | $V_{IN1,2}$ off-state supply current (per channel) | $V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V | $V_{IN1,2}$ = 5 V | –40°C to 105°C | | 0.5 | 8 | µA |
| | | | $V_{IN1,2}$ = 3.3 V | | | 0.1 | 3 | |
| | | | $V_{IN1,2}$ = 1.8 V | | | 0.07 | 2 | |
| | | | $V_{IN1,2}$ = 0.8 V | | | 0.04 | 1 | |
| $I_{ON}$ | ON pin input leakage current | $V_{ON}$ = 5.5 V | | –40°C to 105°C | | | 1 | µA |
| **RESISTANCE CHARACTERISTICS** | | | | | | | | |
| $R_{ON}$ | ON-state resistance (per channel) | $I_{OUT}$ = –200 mA, $V_{BIAS}$ = 5 V | $V_{IN}$ = 5 V | 25°C | | 16 | 19 | mΩ |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| | | | $V_{IN}$ = 3.3 V | 25°C | | 16 | 19 | |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| | | | $V_{IN}$ = 1.8 V | 25°C | | 16 | 19 | |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| | | | $V_{IN}$ = 1.5 V | 25°C | | 16 | 19 | |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| | | | $V_{IN}$ = 1.2 V | 25°C | | 16 | 19 | |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| | | | $V_{IN}$ = 0.8 V | 25°C | | 16 | 19 | |
| | | | | –40°C to 85°C | | | 21 | |
| | | | | –40°C to 105°C | | | 23 | |
| $R_{PD}$ | Output pulldown resistance | $V_{IN}$ = 5.0 V, $V_{ON}$ = 0 V, $I_{OUT}$ = 15 mA | | –40°C to 105°C | | 230 | 330 | Ω |

## 6.6 Electrical Characteristics: $V_{BIAS}$ = 2.5 V

Unless otherwise noted, the specifications apply over the operating ambient temperature –40°C ≤ $T_A$ ≤ 105°C (full) and $V_{BIAS}$ = 2.5 V. Typical values are for $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES AND CURRENTS** | | | | | | | | |
| $I_{IN(VBIAS-ON)}$ | $V_{BIAS}$ quiescent current (both channels) | $I_{OUT1}$ = $I_{OUT2}$ = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = $V_{BIAS}$ = 2.5 V | | –40°C to 105°C | | 32 | 40 | µA |
| $I_{IN(VBIAS-ON)}$ | $V_{BIAS}$ quiescent current (single channel) | $I_{OUT1}$ = $I_{OUT2}$ = 0 mA, $V_{ON2}$ = 0 V $V_{IN1,2}$ = $V_{ON1}$ = $V_{BIAS}$ = 2.5 V | | –40°C to 105°C | | 32 | 40 | µA |
| $I_{IN(VBIAS-OFF)}$ | $V_{BIAS}$ shutdown current | $V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V | | –40°C to 105°C | | | 2 | µA |
| $I_{IN(VIN-OFF)}$ | $V_{IN1,2}$ off-state supply current (per channel) | $V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V | $V_{IN1,2}$ = 2.5 V | –40°C to 105°C | | 0.13 | 3 | µA |
| | | | $V_{IN1,2}$ = 1.8 V | | | 0.07 | 2 | |
| | | | $V_{IN1,2}$ = 1.2 V | | | 0.05 | 2 | |
| | | | $V_{IN1,2}$ = 0.8 V | | | 0.04 | 1 | |
| $I_{ON}$ | ON pin input leakage current | $V_{ON}$ = 5.5 V | | –40°C to 105°C | | | 1 | µA |
| **RESISTANCE CHARACTERISTICS** | | | | | | | | |
| $R_{ON}$ | ON-state resistance | $I_{OUT}$ = –200 mA, $V_{BIAS}$ = 2.5 V | $V_{IN}$ = 2.5 V | 25°C | | 21 | 24 | mΩ |
| | | | | –40°C to 85°C | | | 27 | |
| | | | | –40°C to 105°C | | | 29 | |
| | | | $V_{IN}$ = 1.8 V | 25°C | | 19 | 22 | |
| | | | | –40°C to 85°C | | | 25 | |
| | | | | –40°C to 105°C | | | 27 | |
| | | | $V_{IN}$ = 1.5 V | 25°C | | 18 | 21 | |
| | | | | –40°C to 85°C | | | 24 | |
| | | | | –40°C to 105°C | | | 26 | |
| | | | $V_{IN}$ = 1.2 V | 25°C | | 18 | 21 | |
| | | | | –40°C to 85°C | | | 24 | |
| | | | | –40°C to 105°C | | | 26 | |
| | | | $V_{IN}$ = 0.8 V | 25°C | | 17 | 20 | |
| | | | | –40°C to 85°C | | | 23 | |
| | | | | –40°C to 105°C | | | 25 | |
| $R_{PD}$ | Output pulldown resistance | $V_{IN}$ = 2.5 V, $V_{ON}$ = 0 V, $I_{OUT}$ = 1 mA | | Full | | 280 | 330 | Ω |

## 6.7 Switching Characteristics

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **$V_{IN}$ = $V_{ON}$ = $V_{BIAS}$ = 5 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | | | |
| $t_{ON}$ | Turnon time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 1559 | | µs |
| $t_{OFF}$ | Turnoff time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 6 | | µs |
| $t_R$ | $V_{OUT}$ rise time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 1991 | | µs |
| $t_F$ | $V_{OUT}$ fall time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 2 | | µs |
| $t_D$ | ON delay time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 665 | | µs |
| **$V_{IN}$ = 0.8 V, $V_{ON}$ = $V_{BIAS}$ = 5 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | | | |
| $t_{ON}$ | Turnon time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 732 | | µs |
| $t_{OFF}$ | Turnoff time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 161 | | µs |
| $t_R$ | $V_{OUT}$ rise time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 371 | | µs |
| $t_F$ | $V_{OUT}$ fall time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 14 | | µs |
| $t_D$ | ON delay time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 544 | | µs |
| **$V_{IN}$ = 2.5 V, $V_{ON}$ = 5 V, $V_{BIAS}$ = 2.5 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | | | |
| $t_{ON}$ | Turnon time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 2410 | | µs |
| $t_{OFF}$ | Turnoff time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 7 | | µs |
| $t_R$ | $V_{OUT}$ rise time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 2412 | | µs |
| $t_F$ | $V_{OUT}$ fall time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 2 | | µs |
| $t_D$ | ON delay time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 1181 | | µs |
| **$V_{IN}$ = 0.8 V, $V_{ON}$ = 5 V, $V_{BIAS}$ = 2.5 V, $T_A$ = 25ºC (unless otherwise noted)** | | | | | | |
| $t_{ON}$ | Turnon time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 1575 | | µs |
| $t_{OFF}$ | Turnoff time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 124 | | µs |
| $t_R$ | $V_{OUT}$ rise time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 927 | | µs |
| $t_F$ | $V_{OUT}$ fall time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 14 | | µs |
| $t_D$ | ON delay time | $R_L$ = 10 Ω, $C_L$ = 0.1 µF, CT = 1000 pF | | 1089 | | µs |

## 6.8 Typical Characteristics

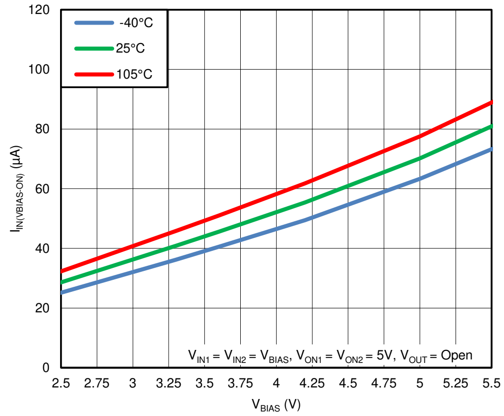



**Figure 1. Quiescent Current vs. $V_{BIAS}$ (Both Channels)**

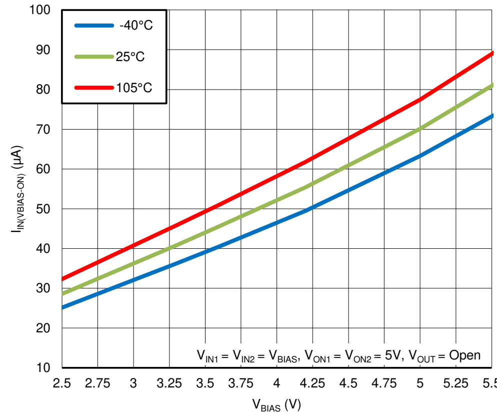



**Figure 2. Quiescent Current vs. $V_{BIAS}$ (Single Channel)**

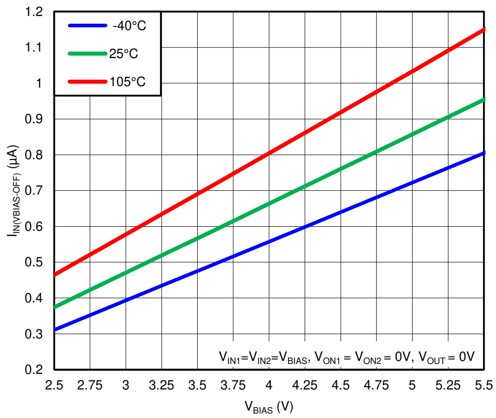



**Figure 3. Shutdown Current vs. $V_{BIAS}$ (Both Channels)**

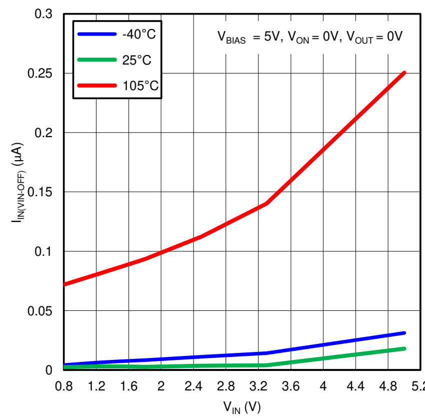



**Figure 4. Off-State VIN Current vs. $V_{IN}$ (Single Channel)**

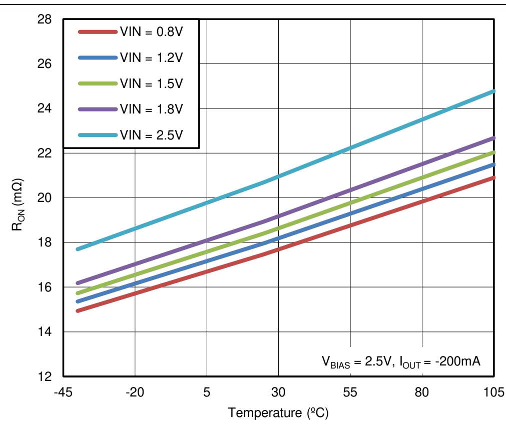



**Figure 5. $R_{ON}$ vs. Temperature ($V_{BIAS}$ = 2.5 V, Single Channel)**

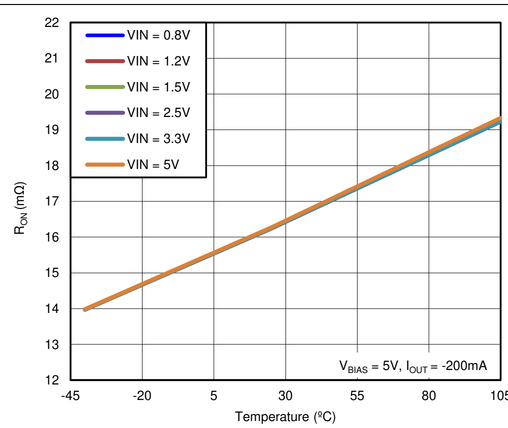



**Figure 6. $R_{ON}$ vs. Temperature ($V_{BIAS}$ = 5 V, Single Channel)**

## Typical Characteristics (continued)

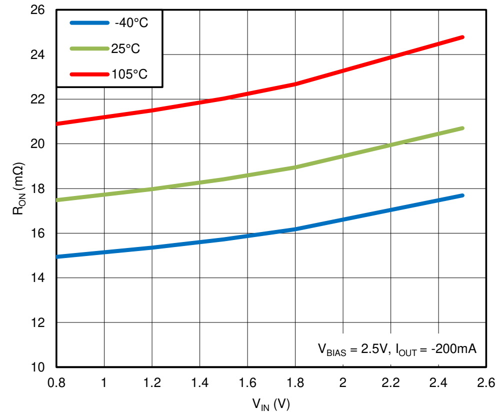



Figure 7. $R_{ON}$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, Single Channel)

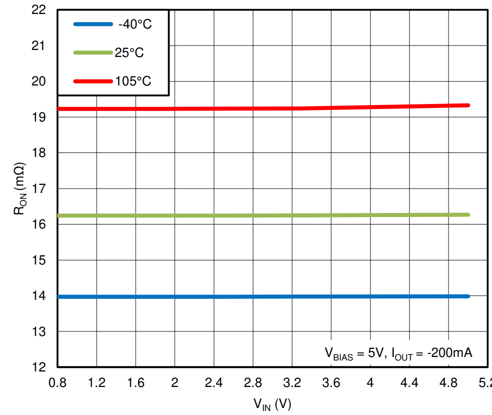



Figure 8. $R_{ON}$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, Single Channel)

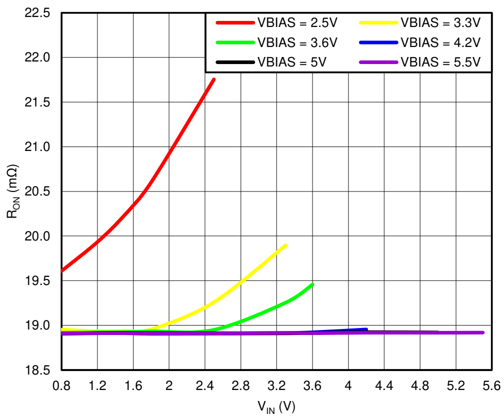



Figure 9. $R_{ON}$ vs. $V_{IN}$ ($T_A$ = 25°C, Single Channel)

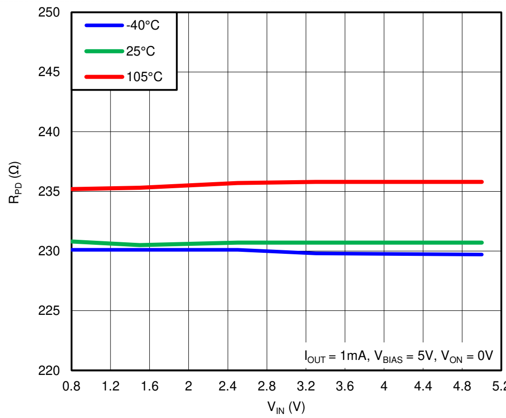



Figure 10. $R_{PD}$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, Single Channel)

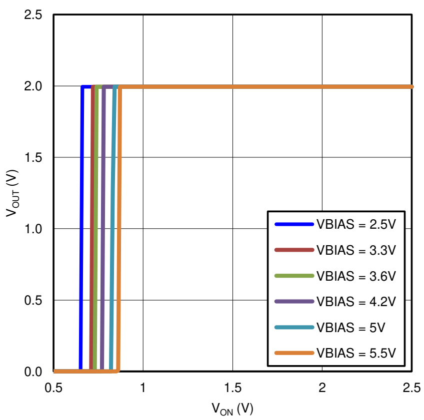



Figure 11. $V_{OUT}$ vs. $V_{ON}$ ($T_A$ = 25°C, Single Channel)

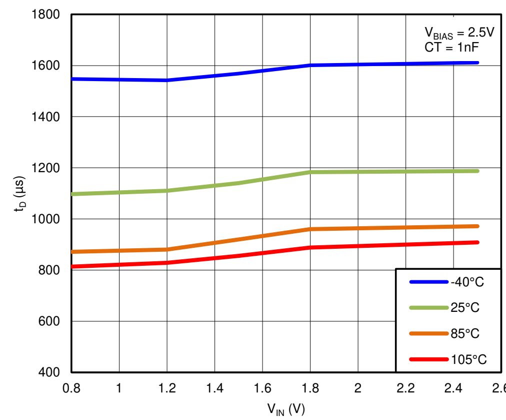



Figure 12. $t_D$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, CT = 1 nF)

## Typical Characteristics (continued)

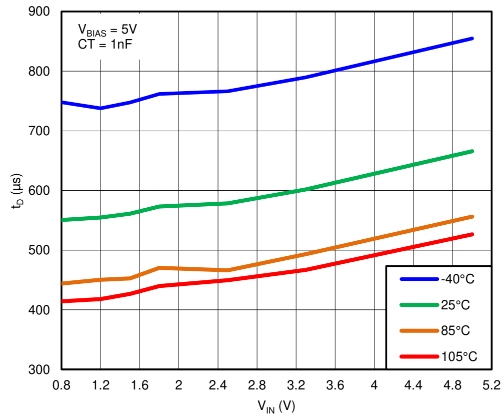



**Figure 13. $t_D$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, CT = 1 nF)**

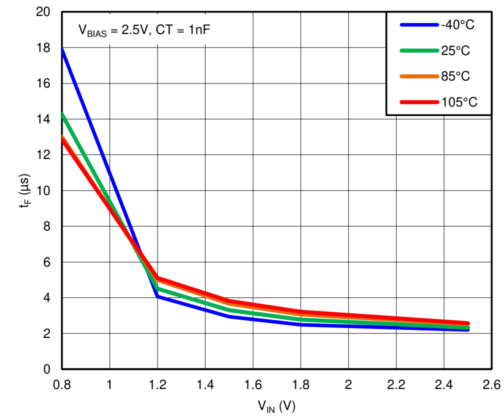



**Figure 14. $t_F$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, CT = 1 nF)**

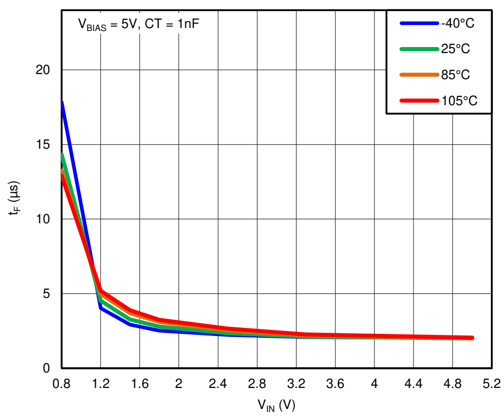



**Figure 15. $t_F$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, CT = 1 nF)**

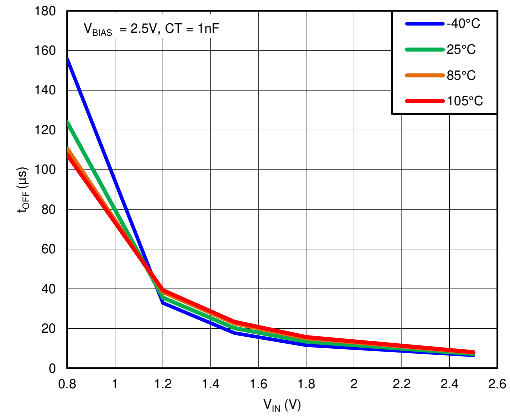



**Figure 16. $t_{OFF}$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, CT = 1 nF)**

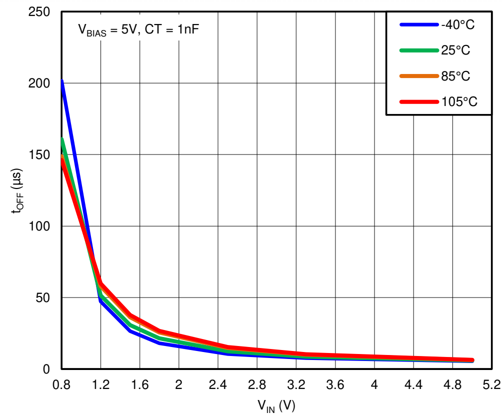



**Figure 17. $t_{OFF}$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, CT = 1 nF)**

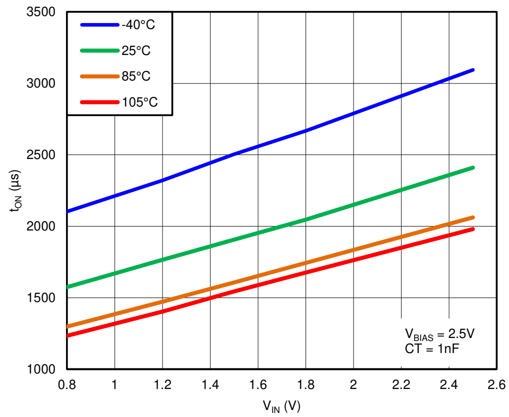



**Figure 18. $t_{ON}$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, CT = 1 nF)**

## Typical Characteristics (continued)

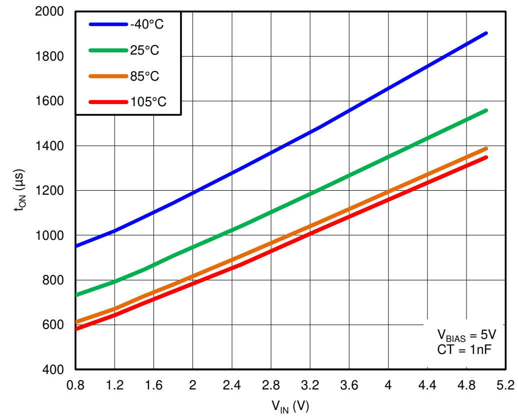



**Figure 19. $t_{ON}$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, CT = 1 nF)**

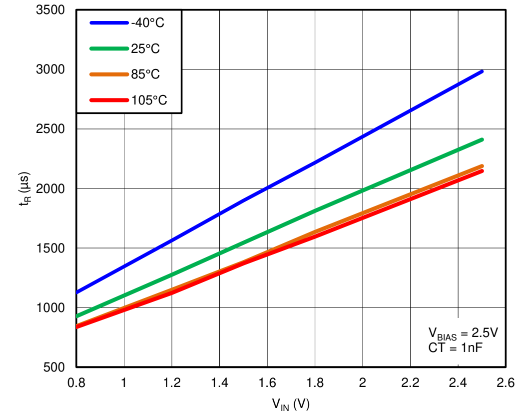



**Figure 20. $t_R$ vs. $V_{IN}$ ($V_{BIAS}$ = 2.5 V, CT = 1 nF)**

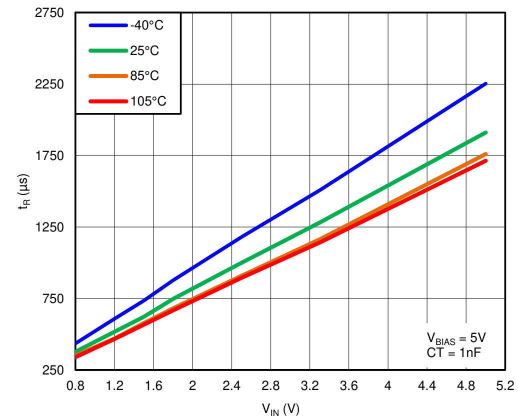



**Figure 21. $t_R$ vs. $V_{IN}$ ($V_{BIAS}$ = 5 V, CT = 1 nF)**

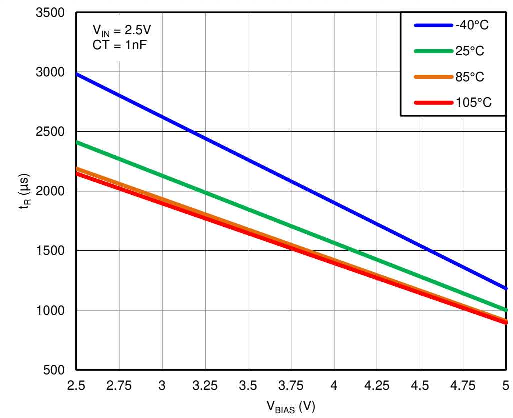



**Figure 22. $t_R$ vs. $V_{BIAS}$ ($V_{IN}$ = 2.5 V, CT = 1 nF)**

### 6.8.1 Typical AC Scope Captures at $T_A$ = 25ºC, CT = 1 nF

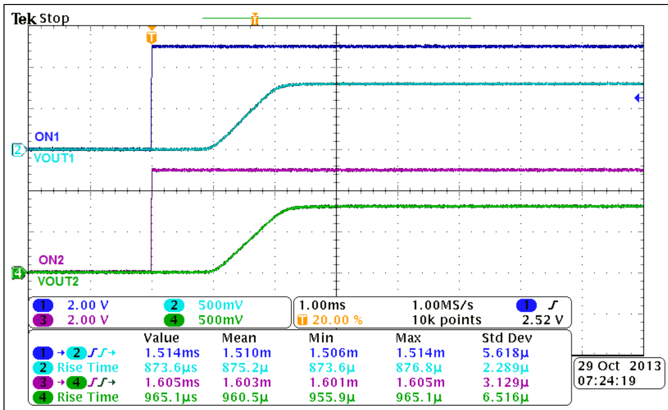



**Figure 23. Turnon Response Time ($V_{IN}$ = 0.8 V, $V_{BIAS}$ = 2.5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)**

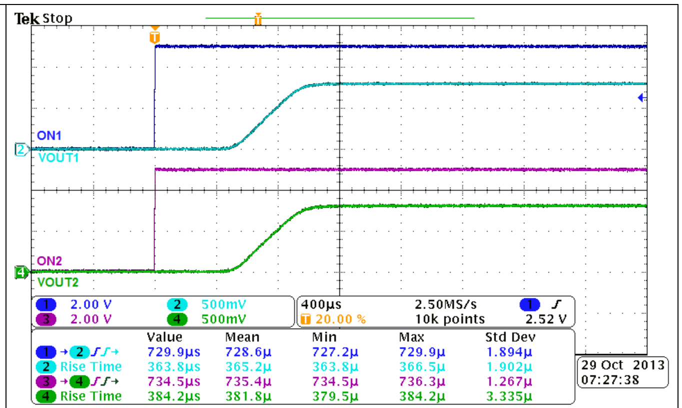



**Figure 24. Turnon Response Time ($V_{IN}$ = 0.8 V, $V_{BIAS}$ = 5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)**

## Typical AC Scope Captures at $T_A$ = 25ºC, CT = 1 nF (continued)

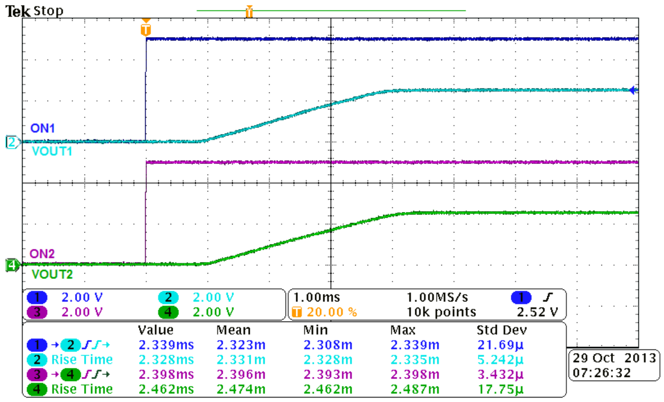



Figure 25. Turnon Response Time ($V_{IN}$ = 2.5 V, $V_{BIAS}$ = 2.5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

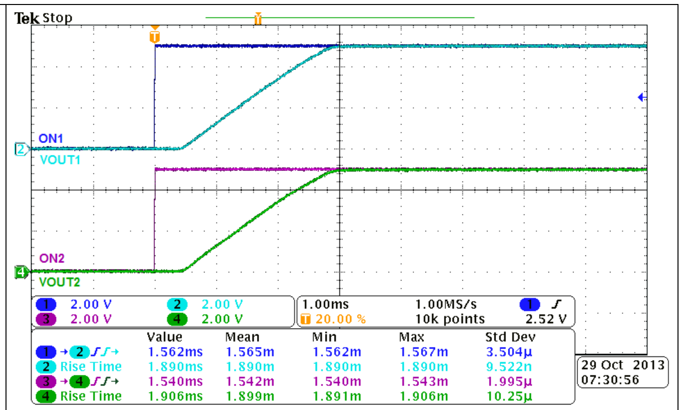



Figure 26. Turnon Response Time ($V_{IN}$ = 5 V, $V_{BIAS}$ = 5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

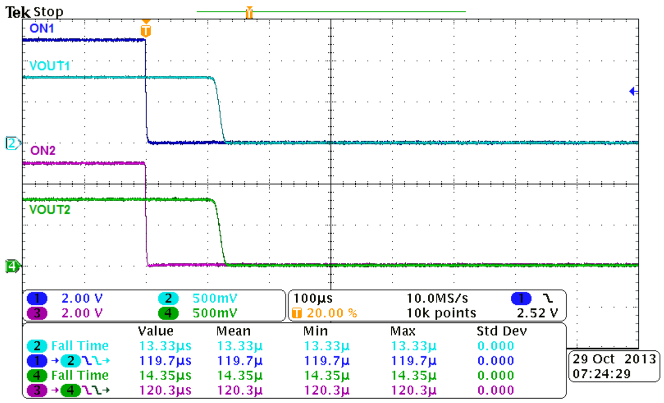



Figure 27. Turnoff Response Time ($V_{IN}$ = 0.8 V, $V_{BIAS}$ = 2.5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

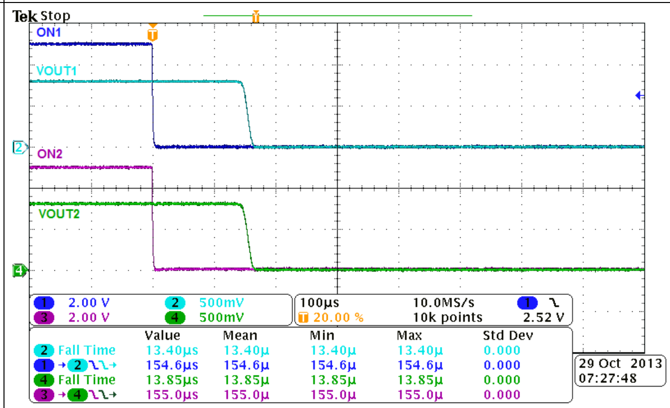



Figure 28. Turnoff Response Time ($V_{IN}$ = 0.8 V, $V_{BIAS}$ = 5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

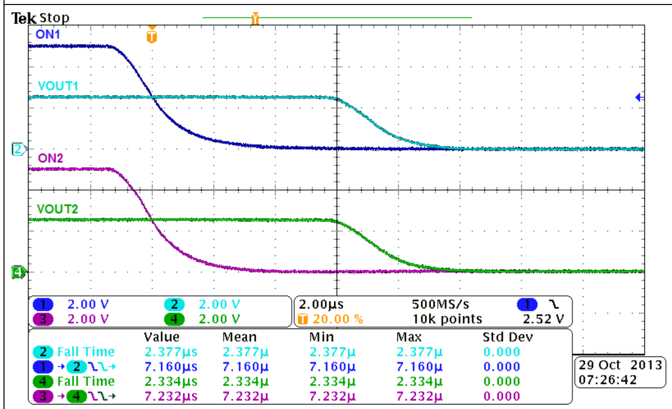



Figure 29. Turnoff Response Time ($V_{IN}$ = 2.5 V, $V_{BIAS}$ = 2.5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

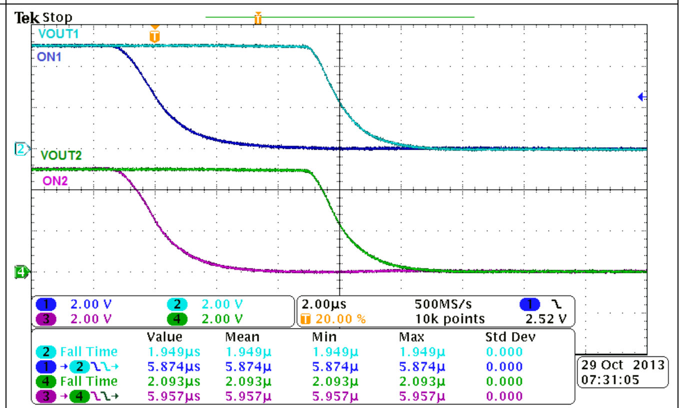
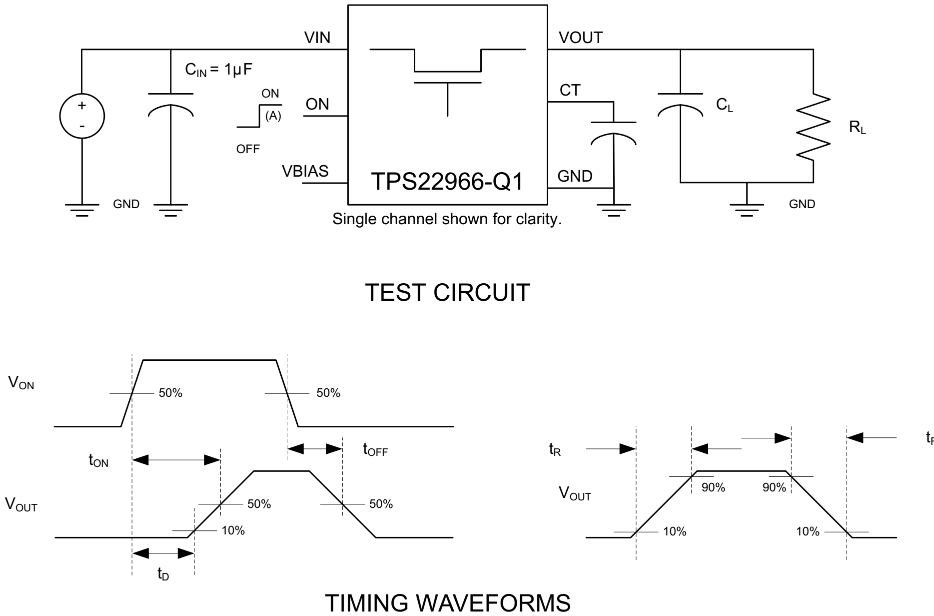



Figure 30. Turnoff Response Time ($V_{IN}$ = 5 V, $V_{BIAS}$ = 5 V, $C_{IN}$ = 1 µF, $C_L$ = 0.1 µF, $R_L$ = 10 Ω)

# 7 Parameter Measurement Information




(A) Control signal rise and fall times are 100 ns.

**Figure 31. Test Circuit and Timing Waveforms**

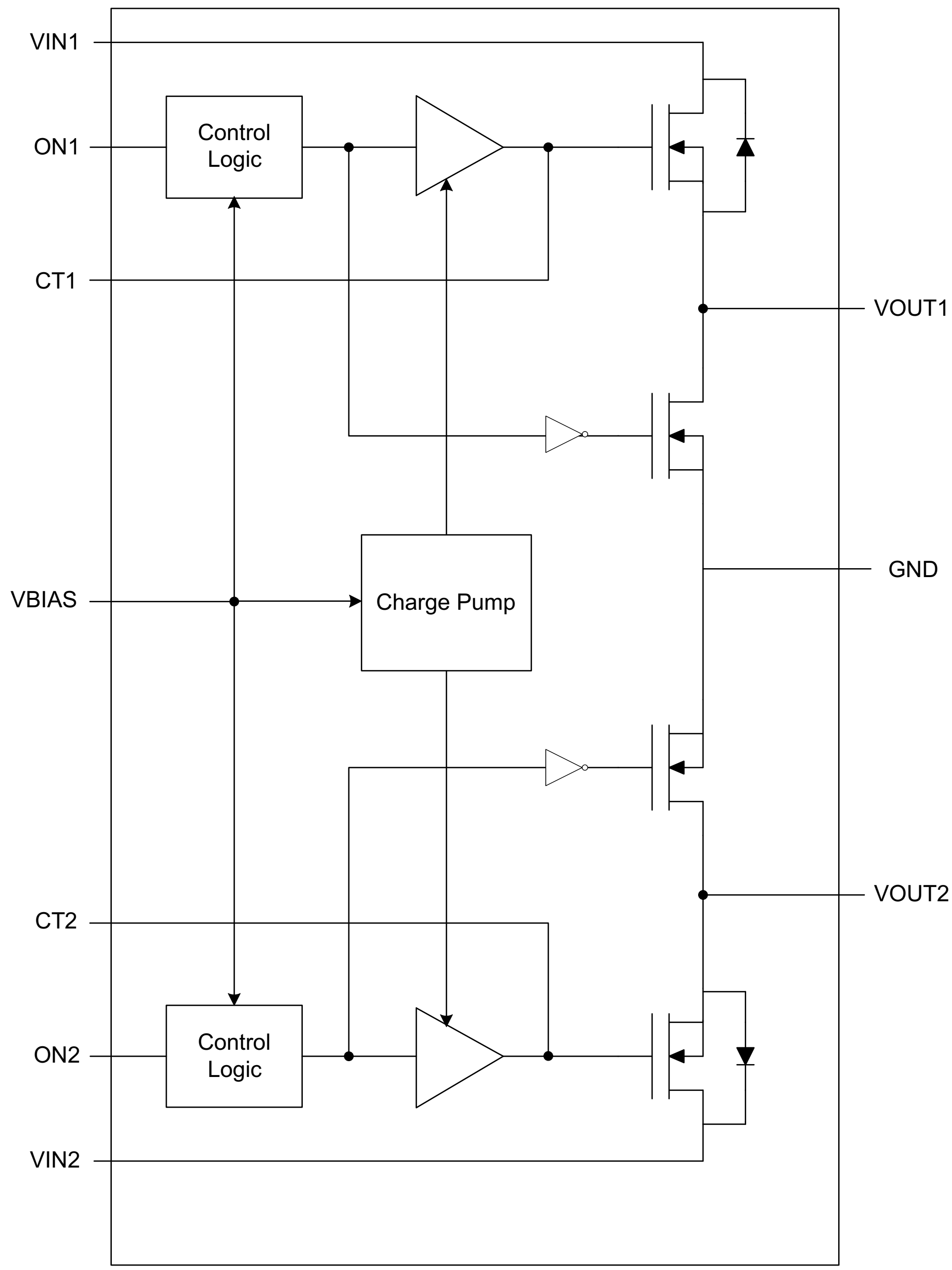
# 8 Detailed Description

## 8.1 Overview

The device is a dual-channel, 4-A automotive load switch in a 14-pin SON package. To reduce the voltage drop in high current rails, the device implements a low-resistance N-channel MOSFET.

The device has a programmable slew rate for applications that require specific rise-time. The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Quick Output Discharge

Each channel of the TPS22966-Q1 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 230-Ω and prevents the output from floating while the switch is disabled.

### 8.3.2 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

### 8.3.3 Adjustable Rise Time

A capacitor to GND on the CTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V should be used on the CTx pin. An approximate formula for the relationship between CTx and slew rate is (the equation below accounts for 10% to 90% measurement on $V_{OUT}$ and does **NOT** apply for CTx = 0 pF. Use Table 1 to determine rise times for when CTx = 0 pF):

$$SR = 0.32 \times CT + 13.7$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CTx pin (in pF)
- The units for the constant 13.7 is in µs/V. (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 shows rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where $V_{IN}$ and $V_{BIAS}$ are already in steady state condition, and the ON pin is asserted high.

**Table 1. Rise Time Values**

| CTx (pF) | RISE TIME (µs) 10% - 90%, $C_L$ = 0.1µF, $C_{IN}$ = 1µF, $R_L$ = 10Ω TYPICAL VALUES at 25°C, $V_{BIAS}$ = 5V, 25V X7R 10% CERAMIC CAP | | | | | | |
|---|---|---|---|---|---|---|---|
| | 5V | 3.3V | 1.8V | 1.5V | 1.2V | 1.05V | 0.8V |
| 0 | 124 | 88 | 63 | 60 | 53 | 49 | 42 |
| 220 | 481 | 323 | 193 | 166 | 143 | 133 | 109 |
| 470 | 855 | 603 | 348 | 299 | 251 | 228 | 175 |
| 1000 | 1724 | 1185 | 670 | 570 | 469 | 411 | 342 |
| 2200 | 3328 | 2240 | 1308 | 1088 | 893 | 808 | 650 |
| 4700 | 7459 | 4950 | 2820 | 2429 | 1920 | 1748 | 1411 |
| 10000 | 16059 | 10835 | 6040 | 5055 | 4230 | 3770 | 3033 |

## 8.4 Device Functional Modes

**Table 2. Functional Table**

| ONx | VINx to VOUTx | VOUTx to GND |
|---|---|---|
| L | Off | On |
| H | On | Off |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, $C_{IN}$, placed close to the pins, is usually sufficient. Higher values of $C_{IN}$ can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

### 9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a $C_{IN}$ greater than $C_L$ is highly recommended. A $C_L$ greater than $C_{IN}$ can cause $V_{OUT}$ to exceed $V_{IN}$ when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A $C_{IN}$ to $C_L$ ratio of 10 to 1 is recommended for minimizing $V_{IN}$ dip caused by inrush currents during start-up, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more $V_{IN}$ dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see *Adjustable Rise Time*).

### 9.1.3 $V_{IN}$ and $V_{BIAS}$ Voltage Range

For optimal $R_{ON}$ performance, make sure $V_{IN} \le V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit $R_{ON}$ greater than what is listed in *Electrical Characteristics*. See Figure 32 for an example of a typical device. Notice the increasing $R_{ON}$ as $V_{IN}$ exceeds $V_{BIAS}$ voltage.

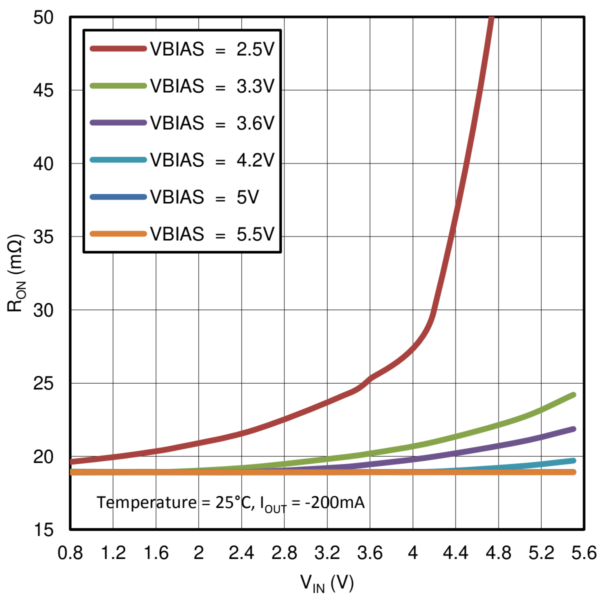



**Figure 32. $R_{ON}$ vs. $V_{IN}$ (Single Channel)**

## Application Information (continued)

### 9.1.4 Safe Operating Area (SOA)

The SOA curves in Figure 33 show the continuous current carrying capability of the device versus ambient temperature ($T_A$) to ensure reliable operation over 100,000 hours of device lifetime. Each curve represents a specific percent of time that the switch is on.

The 100% curve represents use for a full 24 hours in a day. The 75% curve indicates 18 hours of use in a day while the 12.5% curve shows 3 hours of use per day.

Examples on how to use this plot:

- The application has an ambient temperature of 60°C and the switch will be on 100% of the time. The maximum continuous current that can be applied is approximately 2.1 A.
- The application requires the switch to be on 12.5% of the time and the current while on will be 3 A. The maximum ambient temperature is approximately 100°C.
- The application requires 2 A and will be operated at 70°C. The switch can be on for a maximum of 75% of the time.
- It is expected that most applications will not have specific use cases as defined in the examples above. Different use cases can be combined to generate a more complete view of a specific application. This example shows use under various conditions simplified to an average use case. The application requires operation at 4 A for 25% of the time, 1 A for 25% of the time and is off the remaining 50% of the time. Ambient temperature will vary from 25°C to 50°C. Will there be any limitations? The average current can be calculated as (4 A × 25% + 1 A * 25% + 0 A * 50%). The average current calculates to be 1.25 A. Assuming worst case temperature of 50°C, the resulting application is within the safe operating area.

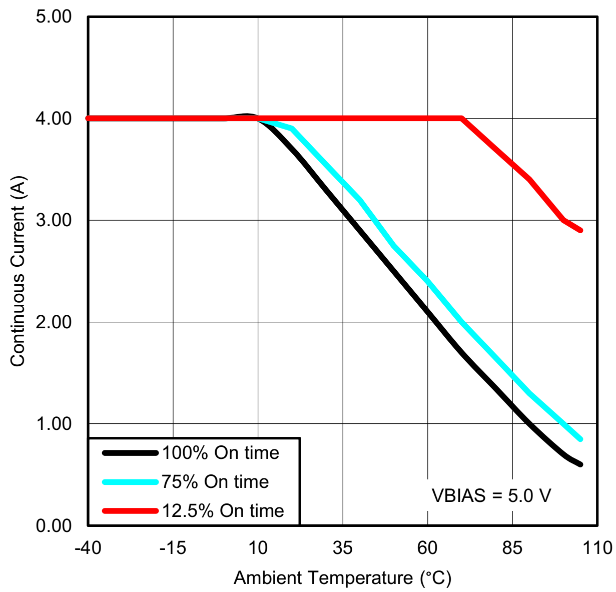



**Figure 33. Safe Operating Area**

## 9.2 Typical Application

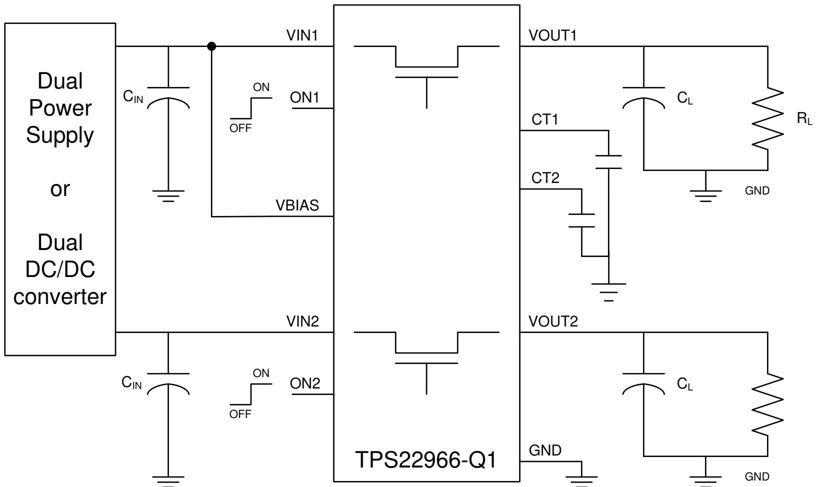



**Figure 34. Typical Application Schematic**

### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

**Table 3. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage | 3.3 V |
| Bias voltage | 5 V |
| Load capacitance ($C_L$) | 22 µF |
| Maximum acceptable inrush current | 400 mA |

### 9.2.2 Detailed Design Procedure

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2:

$$\text{Inrush Current} = C \times dV/dt$$

where

- C = output capacitance
- dV = output voltage
- dt = rise time (2)

The TPS22966-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using Table 3 and the inrush current equation.

$$400\text{ mA} = 22\ \mu\text{F} \times 3.3\text{ V}/dt \quad (3)$$

$$dt = 181.5\ \mu\text{s} \quad (4)$$

To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5 µs. See the oscilloscope captures in for an example of how the CT capacitor can be used to reduce inrush current.

### 9.2.3 Application Curves

$V_{BIAS}$ = 5 V ; $V_{IN}$ = 3.3 V ; $C_L$ = 22 µF

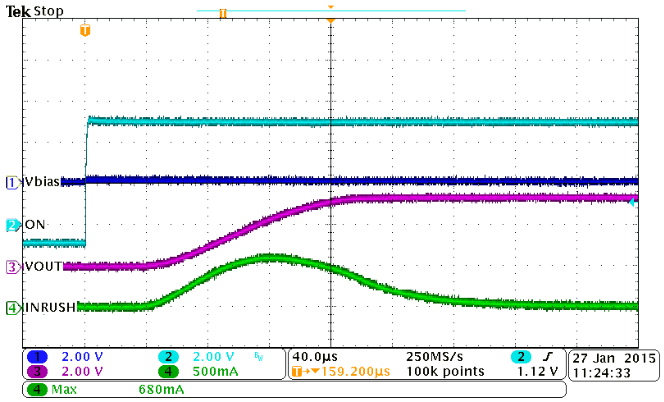



**Figure 35. Inrush Current With CT = 0 pF**

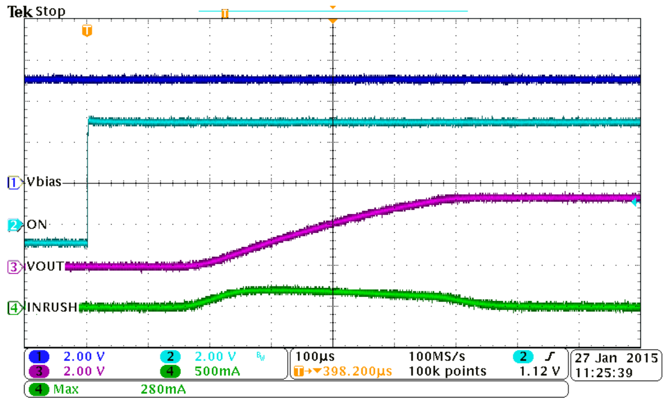



**Figure 36. Inrush Current With CT = 220 pF**

# 10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN voltage range of 0 V to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 uF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

# 11 Layout

## 11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22966-Q1)
- $T_A$ = ambient temperature
- $\Theta_{JA}$ = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

Figure 37 shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

## 11.2 Layout Example

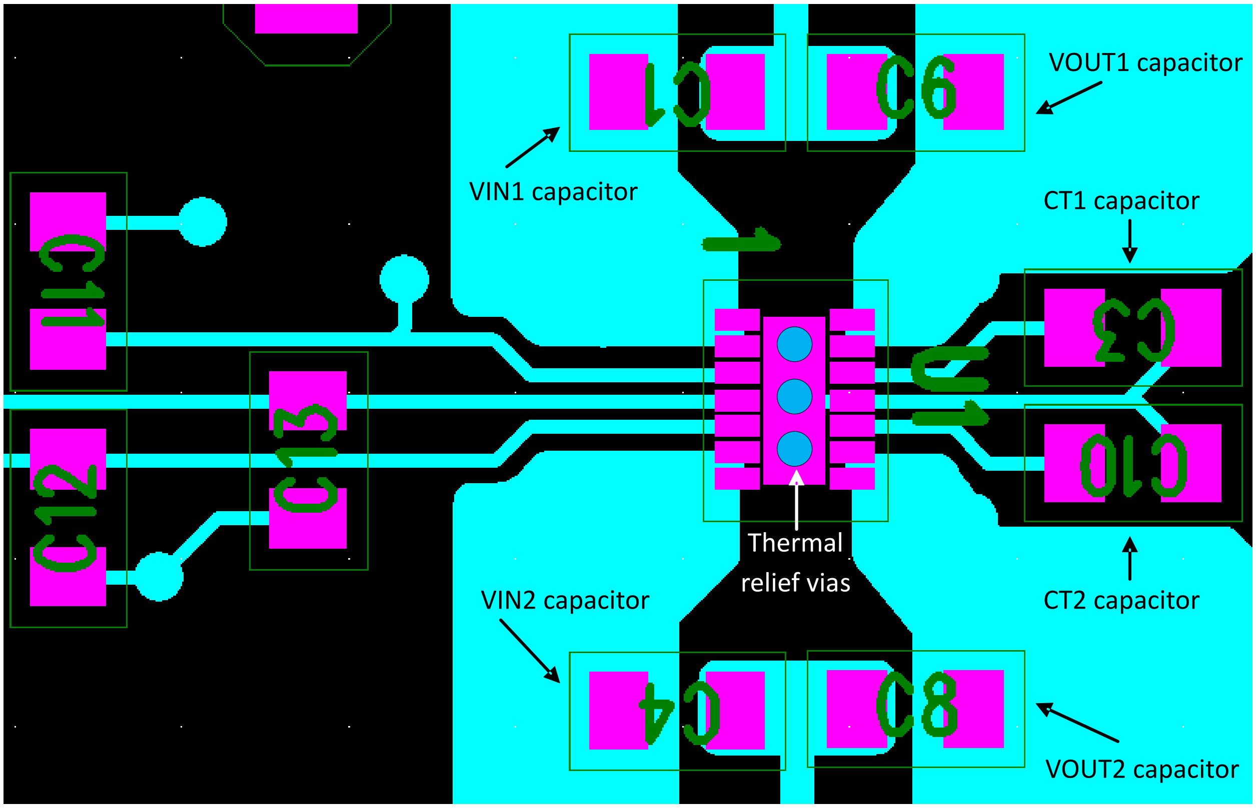



**Figure 37. Layout Example**

# 12 Device and Documentation Support

## 12.1 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22966TDPURQ1 | ACTIVE | WSON | DPU | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 966TQ1 | Samples |
| TPS22966TDPUTQ1 | ACTIVE | WSON | DPU | 14 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 966TQ1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS22966-Q1 :**

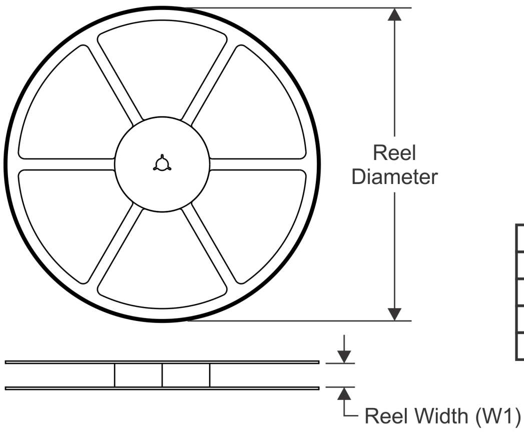
- Catalog: TPS22966

NOTE: Qualified Version Definitions:

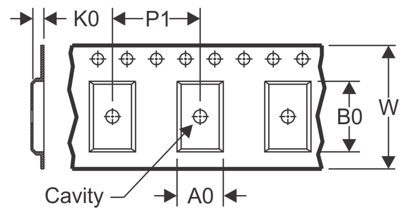
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

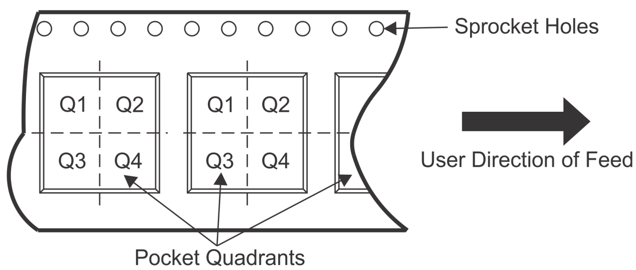



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

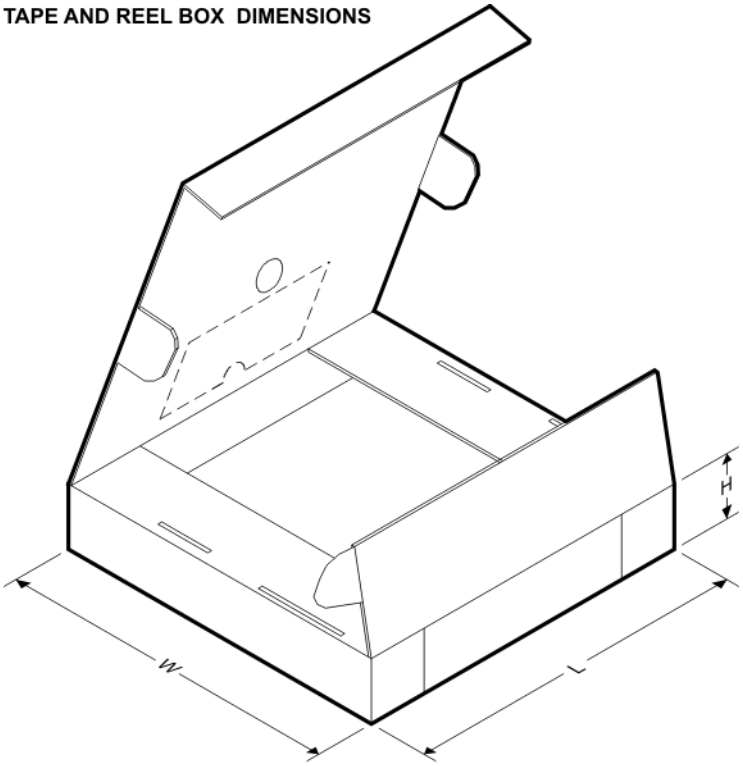
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22966TDPURQ1 | WSON | DPU | 14 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |
| TPS22966TDPUTQ1 | WSON | DPU | 14 | 250 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |

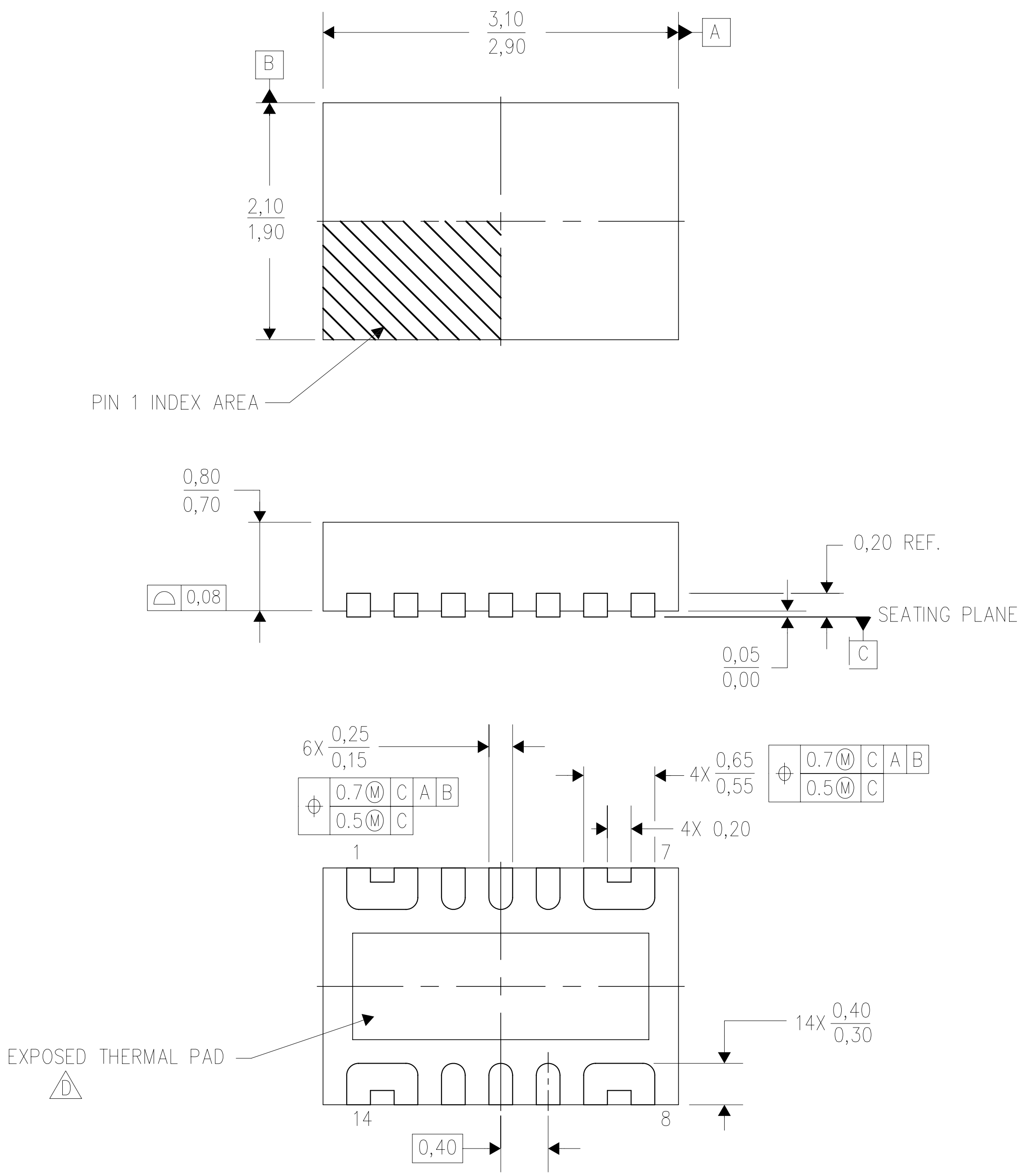
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS22966TDPURQ1 | WSON | DPU | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS22966TDPUTQ1 | WSON | DPU | 14 | 250 | 210.0 | 185.0 | 35.0 |

DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD

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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. This package is Pb–free.

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