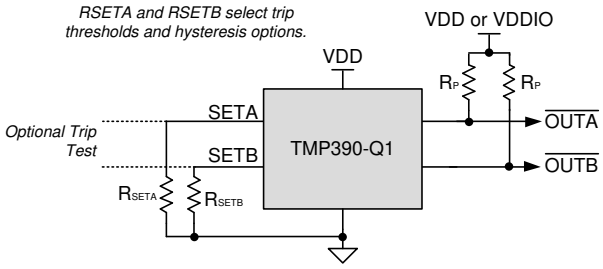
TMP390-Q1 Ultra-Small, Dual-Channel (Hot and Cold Trip), 0.5-µA, Resistor-Programmable Temperature Switch

1 Features

- AEC-Q100 qualified with the following results:
  - Temperature grade 1: –40°C to +125°C operating temperature range
  - Extended operating temperature range: −55°C to +130°C
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Resistor programmable temperature trip points and hysteresis options
  - Resistor tolerances contribute zero error
  - Hysteresis options: 5°C, 10°C and 20°C
- Separate outputs for overtemperature or undertemperature detection
  - Channel A (overtemperature): +30 to +124°C, 2°C steps
  - Channel B (undertemperature): –50 to +25°C, 5°C steps
- Accuracy without calibration
  - ±1.5°C (maximum) from 0°C to +70°C
  - ±3.0°C (maximum) from −55°C to +130°C
- Ultra-low power consumption: 0.5 µA typical at 25°C
- Supply voltage: 1.62 to 5.5 V
- Open-drain outputs
- Trip test function enables in-system testing
- Available in a SOT-563 (1.60-mm × 1.20-mm), 6-pin package

2 Applications

- Automotive infotainment systems
  - USB chargers
  - Instrument clusters
  - Media interface
- Cameras
- Radar/Lidar



Simplified Schematic

3 Description

The TMP390-Q1 device is part of a family of ultra-low power, dual channel, resistor programmable temperature switches that enable protection and detection of system thermal events from –55°C to 130°C. The TMP390-Q1 offers independent overtemperature (hot) and undertemperature (cold) detection . The trip temperatures (T_{TRIP}) and thermal hysteresis (T_{HYST}) options are programmed by two E96-series resistors (1% tolerance) on the SETA and SETB pins. Channel A resistors can range from 1.05 KΩ to 909 KΩ, representing one of 48 unique values. Channel B resistors can range from 10.5 KΩ to 909 KΩ

The value of the resistor to ground on SETA input sets the T_{TRIP} threshold of Channel A. The value of the resistor to ground on SETB input sets the T_{TRIP} threshold of Channel B, as well as the T_{HYST} options of 5°C, or 10°C for both channels, to prevent undesired digital output switching. When the SETB input is connected to ground, Channel A operates with 20°C hysteresis. Resistors accuracy has no impact to T_{TRIP} accuracy.

To enable customer board-level manufacturing, the TMP390-Q1 supports a trip test function where the digital outputs are activated by exercising the SETA or SETB pin.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP390-Q1	SOT-563 (6)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Comparison

PART NUMBER	FUNCTION	OUTPUT TYPE
TMP390-Q1	Hot / Cold	Open-Drain

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2020) to Revision B (August 2019)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Functional Safety bullets to the *Features* section	1

Changes from Revision * (September 2019) to Revision A (April 2020)	Page
• Changed data sheet status from: Advanced Information to: Production Data	1
• Added extended operating temperature range: −55°C to +130°C	1
• Changed accuracy without calibration range from +125°C to +130°C	1
• Added *Channel A Trip Point Accuracy vs Operating Temperature* graph	6
• Added *Channel B Trip Point Accuracy vs Operating Temperature* graph	6

5 Pin Configuration and Functions

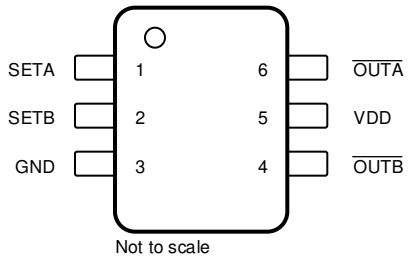


Figure 5-1. DRL Package 6-Pin SOT-563 Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SETA	Input	Channel A temperature set point. Connect a standard E96, 1% resistance between SETA and GND.
2	SETB	Input	Channel B temperature and Hysteresis set point. Connect a standard E96, 1% resistance between SETB and GND.
3	GND	Ground	Device ground.
4	$\overline{\text{OUTB}}$	Logic Output	Channel B logic open-drain active low output. If unused, the output can be left floating or connected to GND.
5	VDD	Supply	Power supply voltage (1.62 V – 5.5 V).
6	$\overline{\text{OUTA}}$	Logic Output	Channel A logic open-drain active low output. If unused, the output can be left floating or connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	6	V
Voltage at	$\overline{OUTA}$, $\overline{OUTB}$	-0.3	6	V
Voltage at	SETA, SETB	–0.3	VDD + 0.3	V
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Powering the device when the operating junction temperature is outside the *Recommended Operating Conditions*, may affect the functional operation of the device. The device must be power cycled after the system has returned to conditions as indicated under *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4A	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62	3.3	5.5	V
V_{OUTA}	Channel A output pull-up voltage (open-drain)			VDD + 0.3	V
V_{OUTB}	Channel B output pull-up voltage (open-drain)			VDD + 0.3	V
I_{SETA}	SETA pin circuit leakage current	-20		20	nA
I_{SETB}	SETB pin circuit leakage current	-20		20	nA
R_{PA}	Pullup resistor connected from $\overline{OUTA}$ to VDDIO(1)	1	10		kΩ
R_{PB}	Pullup resistor connected from $\overline{OUTB}$ to VDDIO(1)				
T_A	Operating free-air temperature (specified performance)	–40		125	°C
	Operating free-air temperature (extended performance)	–55		130	°C

(1) Where VDDIO is an independent power supply other than VDD, and shall not exceed (VDD + 0.3) V.

6.4 Thermal Information

THERMAL METRIC(1)		TMP390-Q1 DRL (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87	°C/W
M_T	Thermal Mass	1.83	mJ/°C

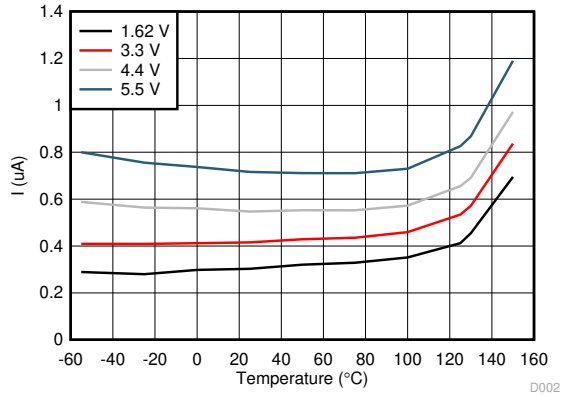
(1) For more information about traditional and new thermal metrics, see the *Semiconductor IC Package Thermal Metrics* application report, (SPRA953).

6.5 Electrical Characteristics

Minimum and maximum specifications are over -55°C to 130°C and VDD = 1.62V - 5.5V (unless otherwise noted); typical specifications are at T_A = 25°C and VDD = 3.3 V.

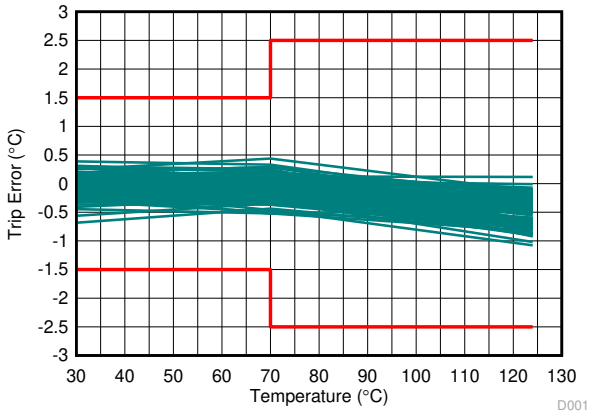
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE TO DIGITAL CONVERTER							
TEMPERATURE MEASUREMENT							
	Trip Point Accuracy (Channel A)	30°C to 70°C	VDD = 2.5V to 5.5V	–1.5	±0.5	1.5	°C
			VDD = 1.62V to 2.5V	–2.0	±0.5	2.0	
		30°C to 130°C	VDD = 2.5V to 5.5V	–2.5	±0.5	2.5	
			VDD = 1.62V to 2.5V	–3.0	±0.5	3.0	
	Trip Point Accuracy (Channel B)	0°C to 25°C	VDD = 2.5V to 5.5V	–1.75	±0.5	1.75	
			VDD = 1.62V to 2.5V	–2.0	±0.5	2.0	
		–55°C to 25°C	VDD = 2.5V to 5.5V	–2.5	±0.5	2.5	
			VDD = 1.62V to 2.5V	–3.0	±0.5	3.0	
T_{HYST}	Trip point hysteresis	Table 7-2 selection column 2			5		°C
		Table 7-2 selection column 3			10		°C
		Channel A only when SETB connected to GND			20		°C
TRIP POINT RESISTOR PROGRAMMING							
	SETA resistor range			1.05		909	kΩ
	SETB resistor range			10.5		909	kΩ
	SETA & SETB resistor tolerance	T_A=25°C		-1.0		1.0	%
	SETA & SETB resistor temperature coefficient			-100		100	ppm/°C
	SETA & SETB resistor lifetime drift			-0.2		0.2	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance for SETA & SETB (includes PCB)					50	pF
R_{PD}	Internal Pull down resistance	SETA & SETB			125		kΩ
V_{OL}	Output logic low level	I_{OL} = -3 mA		0		0.4	V
I_{LKG}	Leakage current on output high level			-0.1		0.1	µA
T_{Cov}	Conversion duration				0.65		ms
T_S	Sampling period				0.5		s
POWER SUPPLY							
I_Q	Average Quiescent current	VDD = 1.62V to 3.3V			0.5	1	µA
$I_{Standby}$	Standby current				0.25		
I_{Conv}	Conversion current				135		µA
I_{SU}	Startup (Reset) peak current	Reset Time interval only.			250		µA
V_{POR}	Power-on-reset threshold voltage	Supply going up			1.5		V
	Brownout detect	Supply going down			1.1		V
	Power Reset Time	Time required by device to reset after power up			10		ms

6.6 Typical Characteristics



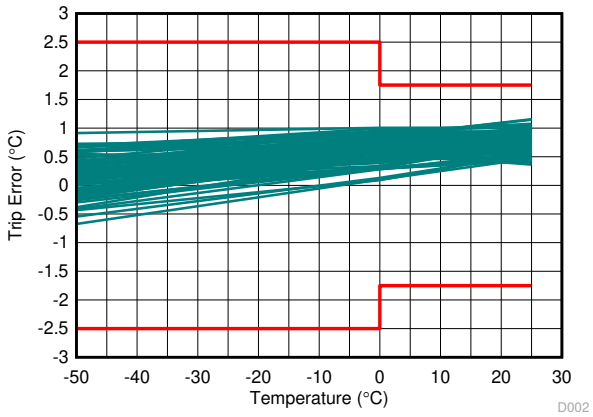
(V_S = 1.62 V, 3.3 V, 4.4 V, 5.5 V)

Figure 6-1. Average Supply Current vs Operating Temperature



(V_S = 3.3 V)

Figure 6-2. Channel A Trip Point Accuracy vs Operating Temperature



(V_S = 3.3 V)

Figure 6-3. Channel B Trip Point Accuracy vs Operating Temperature

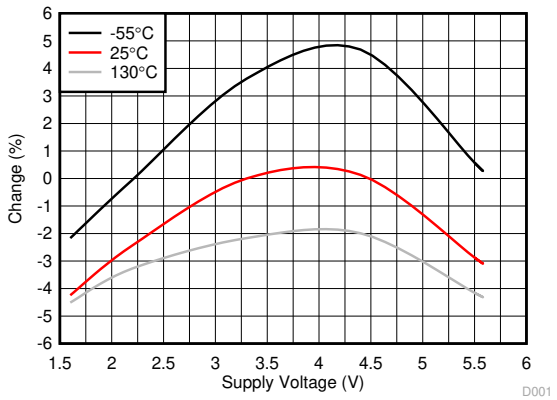


Figure 6-4. Sampling Period Variation vs Supply Voltage

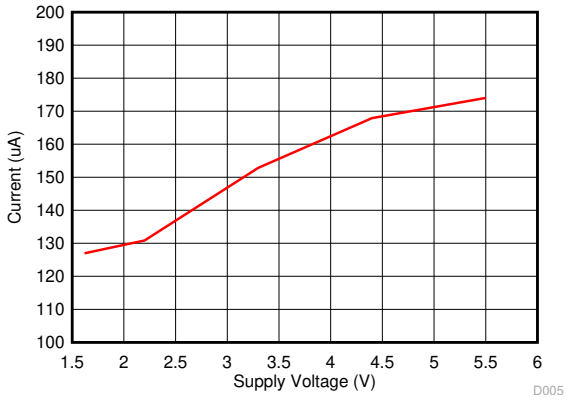
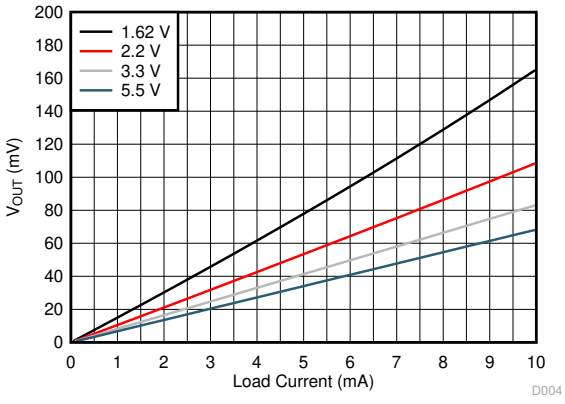


Figure 6-5. Conversion Current vs Supply Voltage



(T_{AMB} = 25°C)

Figure 6-6. Output Voltage vs Load Current

7 Detailed Description

7.1 Overview

The TMP390-Q1 ultra-low power, dual channel, resistor programmable temperature switches enable detection and protection of system thermal events over a wide temperature range. The TMP390-Q1 offers independent overtemperature (hot) and undertemperature (cold) detection. The trip temperatures and hysteresis options are programmed by two E96-series (1%) standard decade value resistors on the SETA and SETB pins. The TMP390-Q1 can enable a customer board-level manufacturing test through the trip test function that can force the SETA or SETB pins to logic high to activates the digital outputs.

7.2 Functional Block Diagram

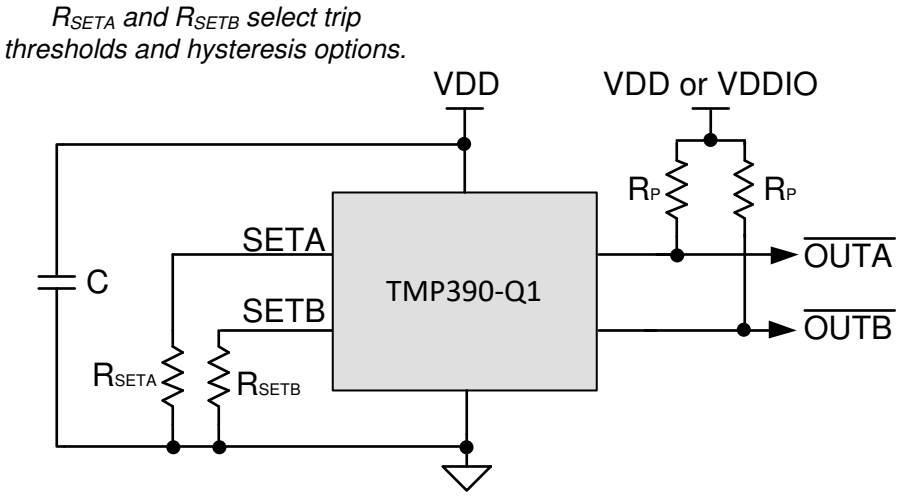


Figure 7-1. Simplified Schematic

7.3 Feature Description

The TMP390-Q1 requires two resistors to set the two trip points and hysteresis, according to Table 7-1 and Table 7-2, for the hot and cold channel device. The output of the TMP390-Q1 is open-drain and requires two pullup resistors. TI recommends to use a pullup voltage supply that does not exceed VDD + 0.3 V. The pullup resistors used in between the $\overline{OUTA}$ and $\overline{OUTB}$ pins and the pullup supply should be greater than 1 kΩ. The device powers on when the supply voltage goes beyond 1.5 V, and starts sampling the input resistors to set the two trip points and hysteresis value after power-on. These values will remain the same until the device goes through a power cycle. After the device sets the trip points and hysteresis level, the device will update the output every half a second. The conversion time is typically 0.65 ms when the temperature is checked against the trip points and the outputs are updated. The device remains in standby mode between conversions. If either channel is not used, the output can be grounded or left floating.

7.3.1 TMP390-Q1 Programming Tables

The temperature threshold and hysteresis options for the TMP390-Q1 device are programmed using two external 1% E96 standard resistors. The specific resistor value to ground on the SETA input sets the temperature threshold of channel A. The specific resistor value to ground on the SETB input sets the temperature threshold of channel B, as well as the hysteresis for both channel A and channel B.

Table 7-1. TMP390-Q1 Channel A Threshold Setting

CHANNEL A (HOT) TRIP TEMPERATURE (°C)	CHANNEL A NOMINAL 1% RESISTORS (KΩ)	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 5°C	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 10°C
30	1.05	25	20
32	1.21	27	22
34	1.40	29	24

Table 7-1. TMP390-Q1 Channel A Threshold Setting (continued)

CHANNEL A (HOT) TRIP TEMPERATURE (°C)	CHANNEL A NOMINAL 1% RESISTORS (KΩ)	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 5°C	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 10°C
36	1.62	31	26
38	1.87	33	28
40	2.15	35	30
42	2.49	37	32
44	2.87	39	34
46	3.32	41	36
48	3.83	43	38
50	4.42	45	40
52	5.11	47	42
54	5.90	49	44
56	6.81	51	46
58	7.87	53	48
60	9.09	55	50
62	10.5	57	52
64	12.1	59	54
66	14.0	61	56
68	16.2	63	58
70	18.7	65	60
72	21.5	67	62
74	24.9	69	64
76	28.7	71	66
78	33.2	73	68
80	38.3	75	70
82	44.2	77	72
84	51.1	79	74
86	59.0	81	76
88	68.1	83	78
90	78.7	85	80
92	90.9	87	82
94	105	89	84
96	121	91	86
98	140	93	88
100	162	95	90
102	187	97	92
104	215	99	94
106	249	101	96
108	287	103	98
110	332	105	100
112	383	107	102
114	442	109	104
116	511	111	106
118	590	113	108
120	681	115	110
122	787	117	112

Table 7-1. TMP390-Q1 Channel A Threshold Setting (continued)

CHANNEL A (HOT) TRIP TEMPERATURE (°C)	CHANNEL A NOMINAL 1% RESISTORS (KΩ)	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 5°C	CHANNEL A (HOT) TRIP RESET TEMPERATURE (°C) FOR HYSTERESIS = 10°C
124	909	119	114

Note

When the SETA pin is grounded or left floating during the device power up, the OUTA pin always stays low. The Channel B functionality is not affected by the SETA channel.

Table 7-2. TMP390-Q1 Channel B Threshold and Hysteresis Setting

CHANNEL B (COLD) TRIP TEMPERATURE (°C)	CHANNEL B NOMINAL 1% RESISTORS (KΩ)		CHANNEL B (COLD) TRIP RESET TEMPERATURE (°C)	
	HYSTERESIS = 5°C	HYSTERESIS = 10°C	HYSTERESIS = 5°C	HYSTERESIS = 10°C
–50	90.9	105	–45	–40
–45	78.7	121	–40	–35
–40	68.1	140	–35	–30
–35	59.0	162	–30	–25
–30	51.1	187	–25	–20
–25	44.2	215	–20	–15
–20	38.3	249	–15	–10
–15	33.2	287	–10	–5
–10	28.7	332	–5	0
–5	24.9	383	0	5
0	21.5	442	5	10
5	18.7	511	10	15
10	16.2	590	15	20
15	14.0	681	20	25
20	12.1	787	25	30
25	10.5	909	30	35

7.3.2 Trip Test

The purpose of the trip test is in system manufacturing test without putting the TMP390-Q1 through costly temperature verification of the assembly of TMP390-Q1 and pullup resistors. When the SETA or SETB pin is set to a high logic level, the associated output goes low. When the input pin level goes low, the output goes to its previous condition before the trip test. The trip test does not affect the current condition of the device. The trip test signals should stay above 0.8 × VDD for logic high and below 0.2 × VDD for logic low.

The trip test operation is shown in Figure 7-2. The trip test must be performed with a single toggle when the device is operating at a temperature that will not cause the corresponding output to trip. The trip test is intended for production testing after assembly, and must not be used as a functional feature.

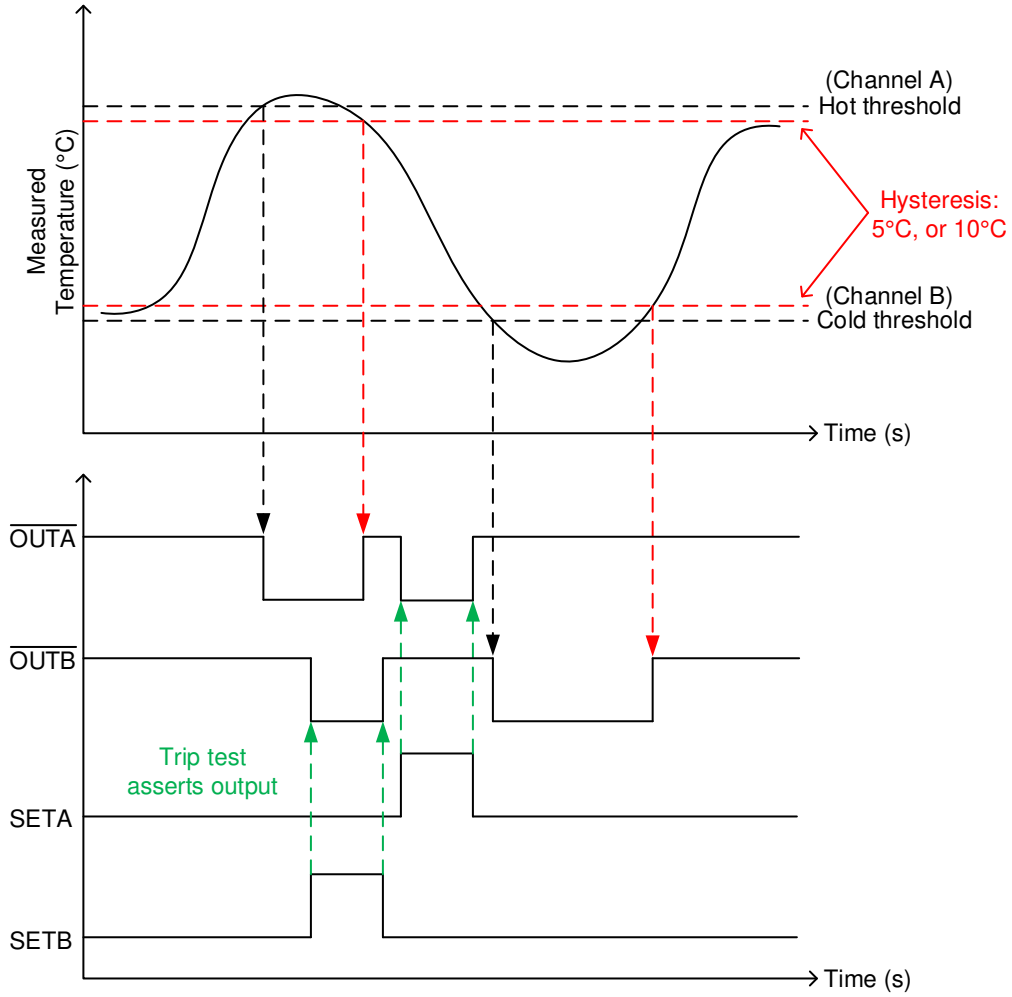


Figure 7-2. TMP390-Q1 Trip Test Operation

7.3.3 20°C Hysteresis

The 20°C hysteresis feature is only available on Channel A. To activate the feature, the SETB pin must be connected to ground and SETA pin connected to the resistor to set the appropriate trip point on Channel A.

7.4 Device Functional Modes

The device has one mode of operation, as described above, that applies when operated within the *Recommended Operating Conditions*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Applications Information

The TMP390-Q1 device is part of a family of ultra-low power, dual channel, resistor programmable temperature switches that can enable detection and protection of system thermal events over a wide temperature range. The trip temperatures (T_{TRIP}) and hysteresis options are programmed by two E96-series (1%) standard decade value resistors on the SETA and SETB pins. The thermal hysteresis (T_{HYST}) function is to prevent undesired digital output switching due to small temperature changes.

8.2 Typical Applications

8.2.1 Simplified Application Schematic

Figure 8-1 shows the simplified schematic where R_{SETA} and R_{SETB} are used to set channel A trip point (SETA) and channel B trip point and hysteresis for both channels (SETB). SETA and SETB can be programmed at a variety of temperatures based on the device, as described in Table 7-1 for channel A trip point, and Table 7-2 for channel B trip point and hysteresis for both channels. $\overline{OUTA}$ and $\overline{OUTB}$ outputs correspond to the temperature threshold detection at SETA and SETB, respectively.

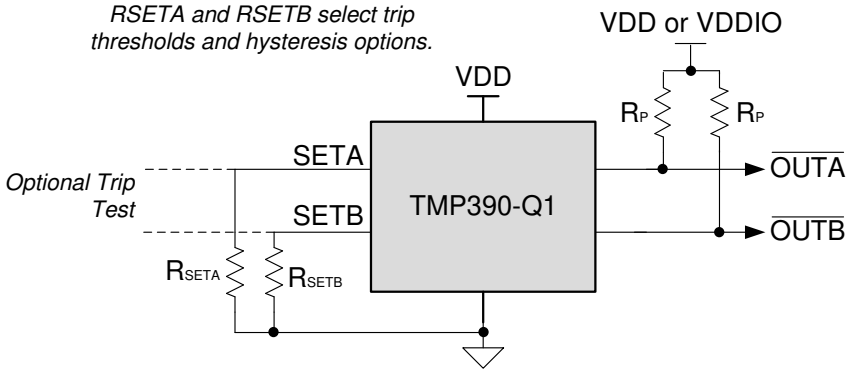


Figure 8-1. Simplified Schematic

8.2.1.1 Design Requirements

The TMP390-Q1 requires two resistors to set the high and low trip points and hysteresis, and two pullup resistors for the open-drain device. TI also highly recommends to place a 0.1-µF, power-supply bypassing capacitor close to the VDD supply pin. To minimize the internal power dissipation, use two pullup resistors greater than 1 kΩ from the $\overline{OUTA}$ and $\overline{OUTB}$ pins to the VDD pin. A separate supply, VDDIO, may be used for the pullup voltage to set the output voltage level to the level required by the MCU, as shown in Figure 8-1. The open-drain output gives flexibility of pulling up to any voltage independent of VDD (VDDIO must be less than or equal to VDD + 0.3 V). This allows for use of longer cables or different power supply options. If a separate voltage level is not required, TI recommends to tie the pullup to the TMP390-Q1 VDD.

If the SETA or SETB connected resistor value is outside the legal range, the associated output goes to permanent output zero stage and the channel cannot be used. The other channel still will be in operating condition, and device can be used in one channel mode. If the SETB input is grounded or left floating, the Channel B cannot be used and the hysteresis for Channel A will be 20°C. The SETA and SETB connected resistors are measured during POR. If two consecutive measurements are not matching each other, then the device sets the associated channel output to zero and repeats the resistor measurements until the

measurements match. When the measurements match, the channel output is released. Note that it is possible to connect some device outputs together by shorting the $\overline{OUTA}$ or $\overline{OUTB}$ line.

8.2.1.2 Detailed Design Procedure

The resistor to ground values on the SETA input sets the T_{TRIP} threshold of Channel A. The resistor to ground value on the SETB input sets the T_{TRIP} threshold of Channel B as well as the T_{HYST} 5°C and 10°C options. TI recommends that the resistors at SETA and SETB have a 1% tolerance at room temperature. Each resistor can range from 1.05 KΩ to 909 KΩ, representing one of 48 unique values. The exact temperature thresholds and trip points are shown in Table 7-1 and Table 7-2. The pullup resistors should be at least 1 kΩ to minimize internal power dissipation. To get the correct threshold for resistor values, take care to minimize the board level capacitance and leakage at the SETA and SETB pins.

The waveform for the TMP390-Q1 output under the hot/cold thresholds is shown in Figure 8-2. The hysteresis can be set to 5°C, 10°C or 20°C. When the temperature exceeds the hot trip point threshold, $\overline{OUTA}$ goes low until the temperature drops below the hysteresis threshold. When the temperature drops below the cold trip threshold, $\overline{OUTB}$ goes low and returns high after the temperature rises above the hysteresis threshold. If the switch has already tripped and the temperature is in the hysteresis band, a POR event will cause the output to go high after the power is restored.

8.2.1.3 Application Curves

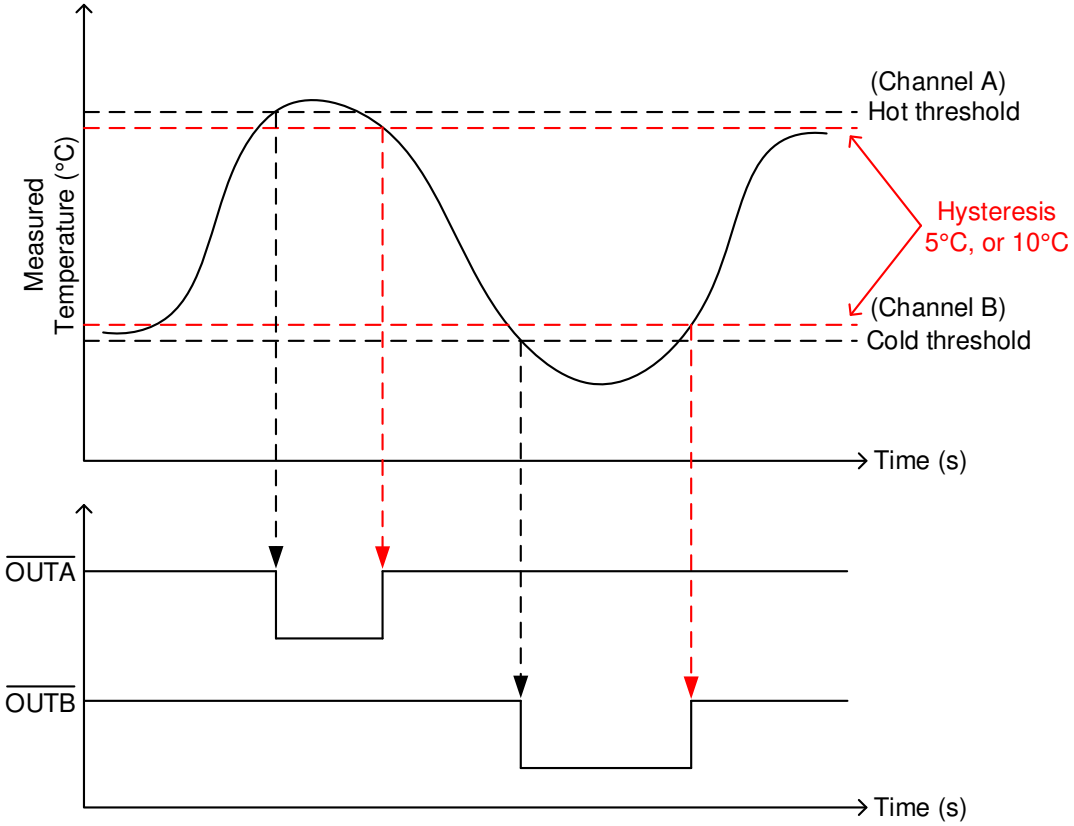


Figure 8-2. TMP390-Q1 Output With Hot/Cold Thresholds With Hysteresis

8.2.2 TMP390-Q1 With 10°C Hysteresis

Figure 8-3 shows an example circuit for overtemperature and undertemperature protection using the TMP390-Q1. In this example, the trip points are set at –25°C and +90°C with 10°C hysteresis.

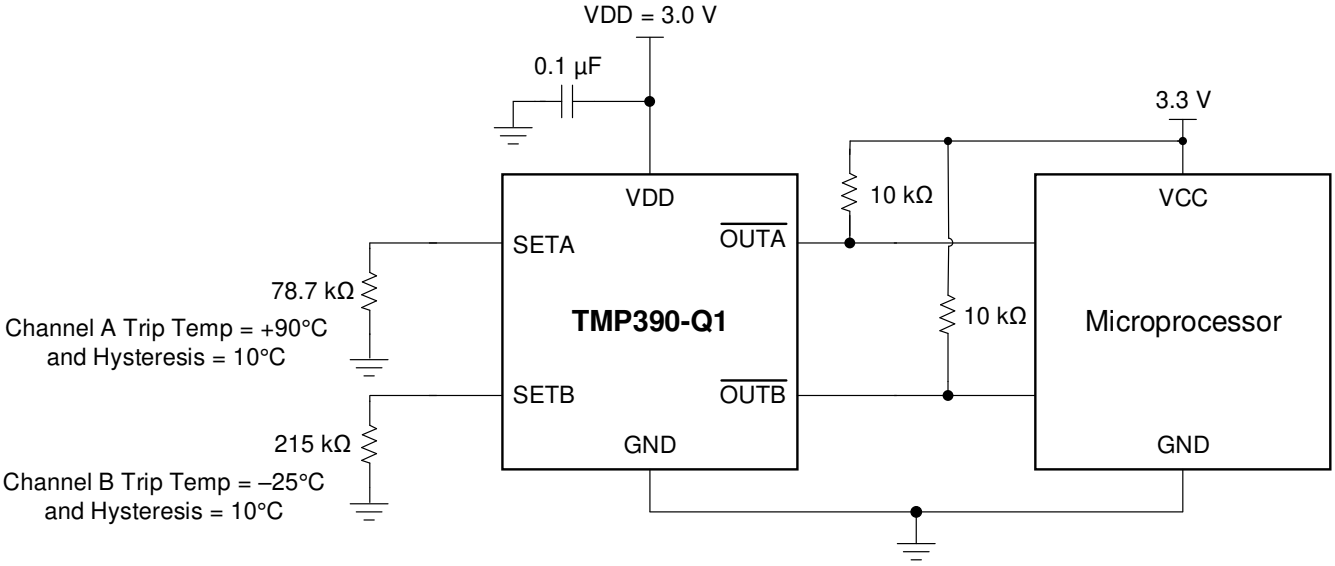


Figure 8-3. TMP390-Q1 Example Circuit at +90°C and –25°C Thresholds With 10°C Hysteresis

8.2.2.1 Design Requirements

In this example, VDD can be ≥ 3 V. The output pins may be tied to a switch to control a fan or other analog circuitry. This example uses 10-kΩ pullup resistors at the $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ outputs. Place a 0.1-µF bypass capacitor close to the TMP390-Q1 device to reduce noise coupled from the power supply. If needed, the output of multiple parts can be connected together.

8.2.2.2 Detailed Design Procedure

SETA sets the +90°C threshold using 78.7 kΩ. SETB sets the –25°C trip point and 10°C hysteresis using 215 kΩ. These values were determined using Table 7-1 and Table 7-2. These resistors should have maximum of 1% tolerance and 100 ppm/°C or less over the desired temperature range. A summary of the resistor settings used in this example is shown in Table 8-1. See Table 7-1 and Table 7-2 for additional trip points and hysteresis configurations.

The switching output of the TMP390-Q1 can be visualized with the output diagram shown in Figure 8-4. It is key to notice that hysteresis is subtracted from the Channel A threshold and added to the Channel B threshold values. $\overline{\text{OUTA}}$ remains high until the sensor reaches +90°C where the output goes low, and returns high after the temperature drops back down to +80°C. $\overline{\text{OUTB}}$ trips when the temperature stays below –25°C and goes low until the temperature rises above –15°C.

Table 8-1. Example Resistor Settings and Trip Points

CHANNEL	RESISTOR SETTING (kΩ)	HYSTERESIS (°C)	TRIP TEMPERATURE (°C)
SETA	78.7	10	+90
SETB	215		–25

8.2.2.3 Application Curve

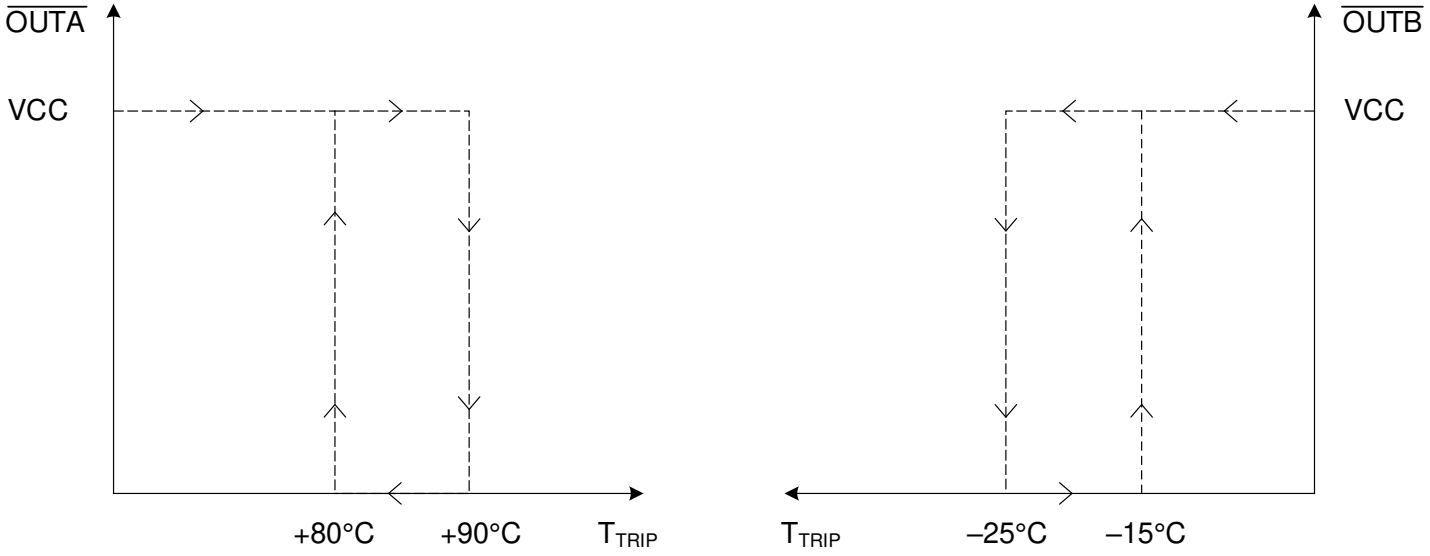


Figure 8-4. TMP390-Q1 Output Response With Hysteresis

8.2.3 One Channel Operation for Hot Trip Point up to 124°C

Figure 8-5 shows the TMP390-Q1 configured for one channel operation, with a single resistor to set the hot trip point and hysteresis. Table 8-2 shows the possible resistor values and hysteresis values that may be used for one channel applications.

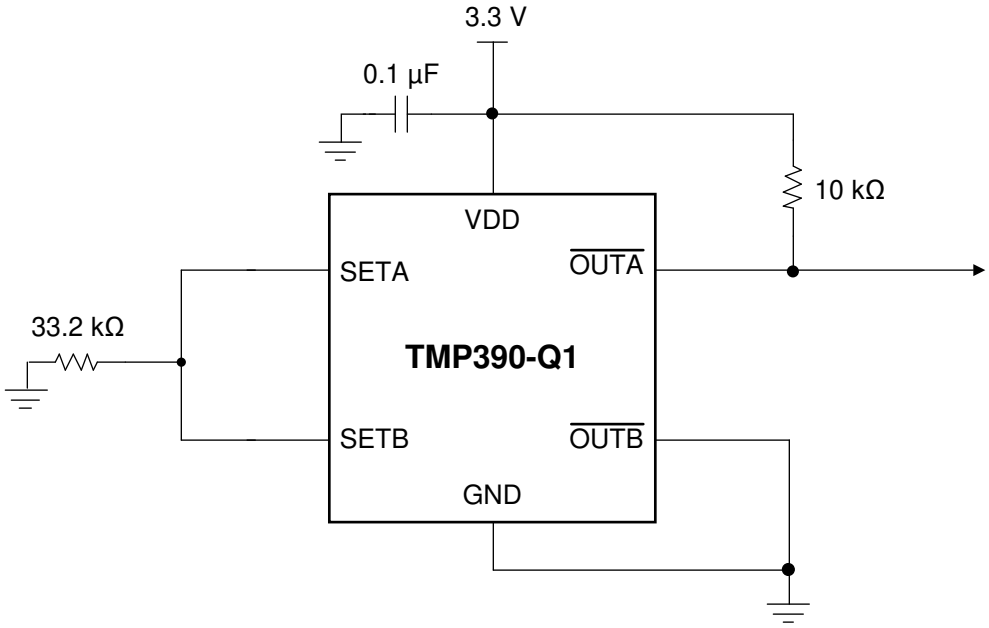


Figure 8-5. TMP390-Q1 One Channel (Hot) Operation Example Circuit With 78°C Trip Point and 5°C Hysteresis

Table 8-2. Single Resistor One Channel Setting

NOMINAL 1% RESISTOR (KΩ)	CHANNEL A TRIP TEMPERATURE (°C)	HYSTERESIS (°C)
10.5	62	5
12.1	64	5
14.0	66	5
16.2	68	5
18.7	70	5
21.5	72	5
24.9	74	5
28.7	76	5
33.2	78	5
38.3	80	5
44.2	82	5
51.1	84	5
59.0	86	5
68.1	88	5
78.7	90	5
90.0	92	5
105	94	10
121	96	10
140	98	10
162	100	10
187	102	10

Table 8-2. Single Resistor One Channel Setting (continued)

NOMINAL 1% RESISTOR (KΩ)	CHANNEL A TRIP TEMPERATURE (°C)	HYSTERESIS (°C)
215	104	10
249	106	10
287	108	10
332	110	10
383	112	10
442	114	10
511	116	10
590	118	10
681	120	10
787	122	10
909	124	10

8.2.3.1 Application Curve

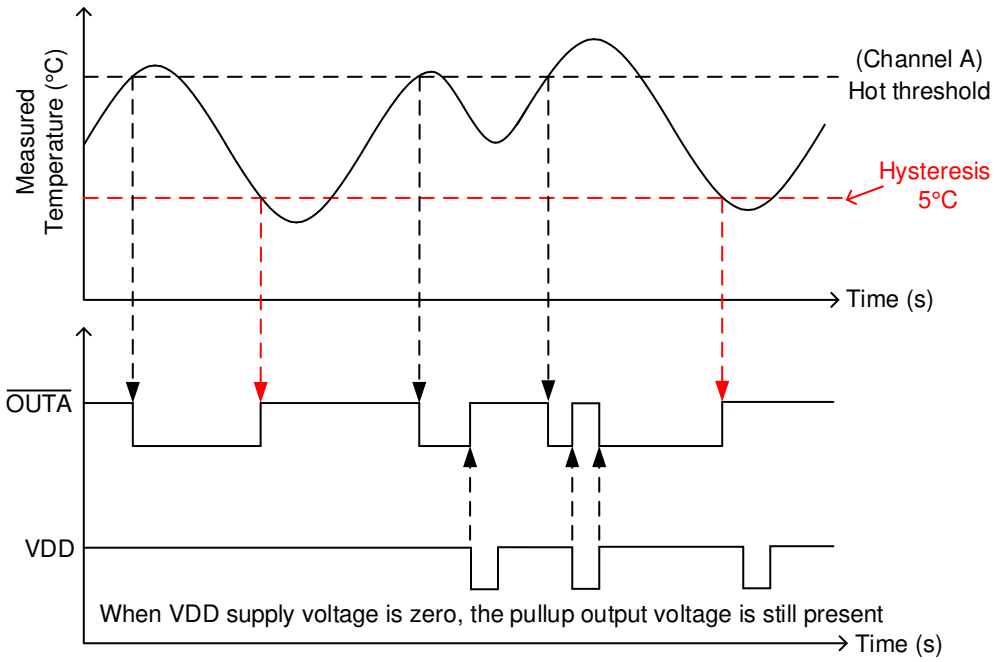


Figure 8-6. TMP390-Q1 One Channel (Hot) Operation Thresholds and Hysteresis

8.2.4 One Channel Operation for Cold Trip Point

Figure 8-7 shows the TMP390-Q1 configured for one channel operation, with a single resistor to set the warm trip point and hysteresis. The resistor values for one channel warm trip point is same as described in Table 7-2.

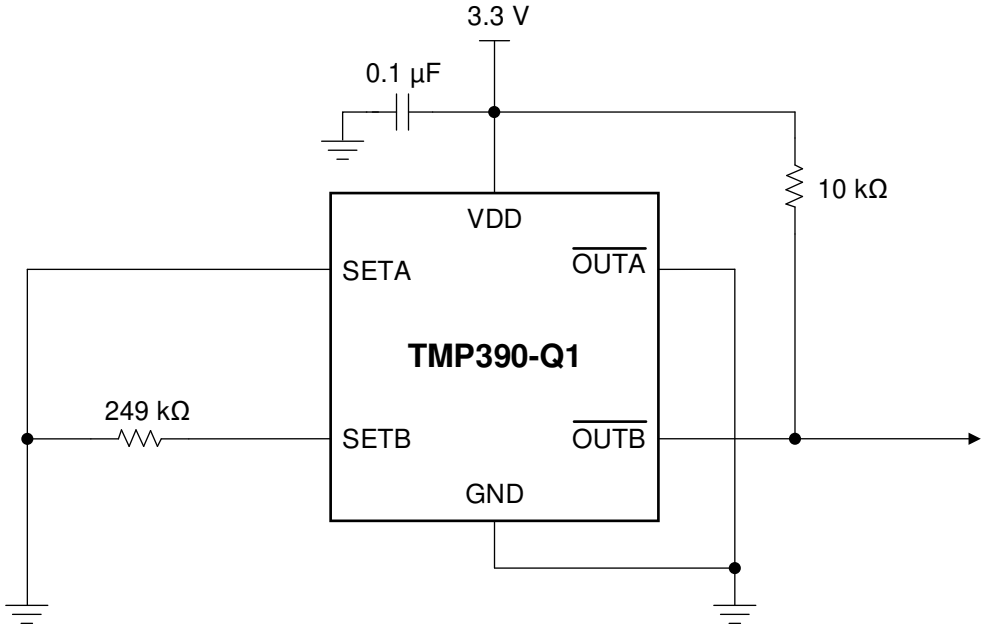


Figure 8-7. TMP390-Q1 One Channel (Cold) Operation Example Circuit With –20°C Trip Point and 10°C Hysteresis

8.2.4.1 Application Curve

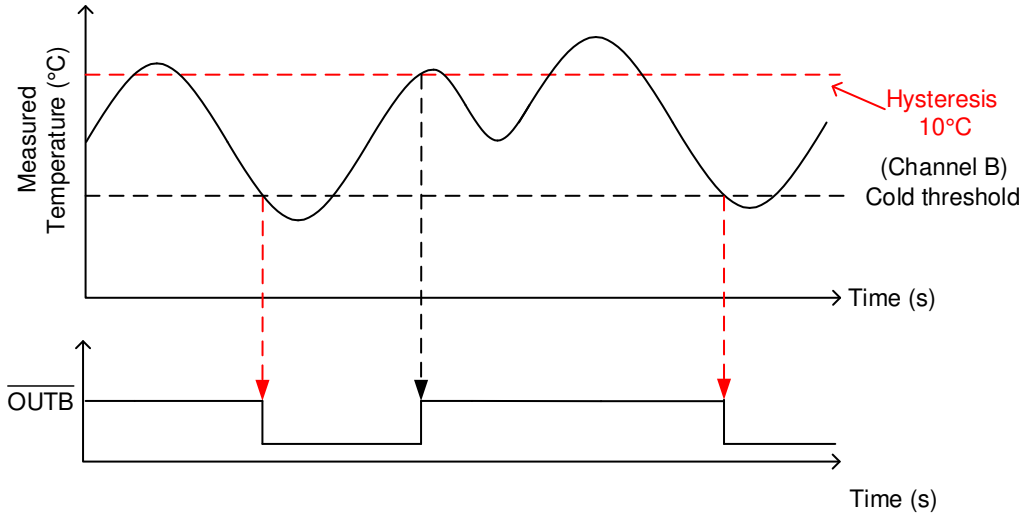


Figure 8-8. TMP390-Q1 One Channel (Cold) Operation Thresholds and Hysteresis

9 Power Supply Recommendations

The low supply current and wide supply range of the TMP390-Q1 allow the device to be powered from many sources. VDDIO must always be lower than or equal to VDD + 0.3 V.

Power supply bypassing is strongly recommended by adding a 0.1-µF capacitor from VDD to GND. In noisy environments, TI recommends to add a filter with 0.1-µF capacitor and 100-Ω resistor between external supply and VDD to limit the power supply noise.

10 Layout

10.1 Layout Guidelines

The TMP390-Q1 is extremely simple to layout. Place the power supply bypass capacitor as close to the device as possible, and connect the capacitor as shown in Figure 10-1. Place the R_{SETA} and R_{SETB} resistors as close to the device as possible. Carefully consider the resistor placement to avoid additional leakage or parasitic capacitance, as this may affect the actual resistor sense value for the trip thresholds and hysteresis. If there is a possibility of moisture condensation on the SETA and SETB circuits, which may lead to additional leakage current, consider adding a conformal coating to the circuits.

10.2 Layout Example

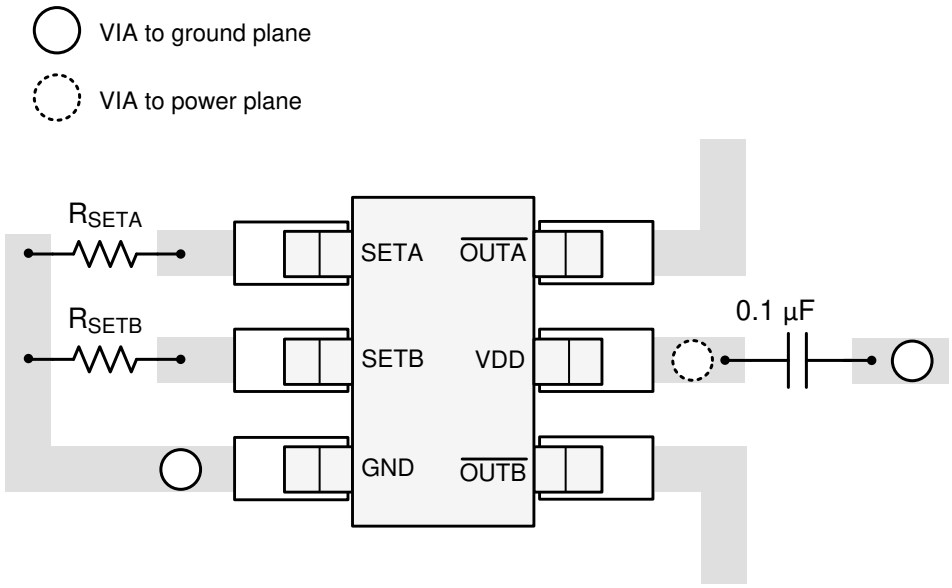


Figure 10-1. TMP390-Q1 Recommended Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP390AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 130	1G1	Samples
TMP390AQDRLTQ1	OBSOLETE	SOT-5X3	DRL	6		TBD	Call TI	Call TI	-55 to 130	1G1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TMP390-Q1 :

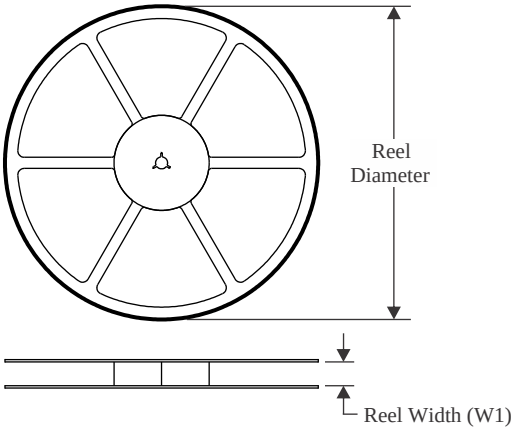
- Catalog : TMP390

NOTE: Qualified Version Definitions:

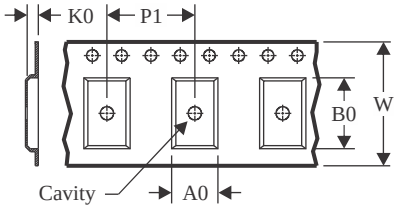
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

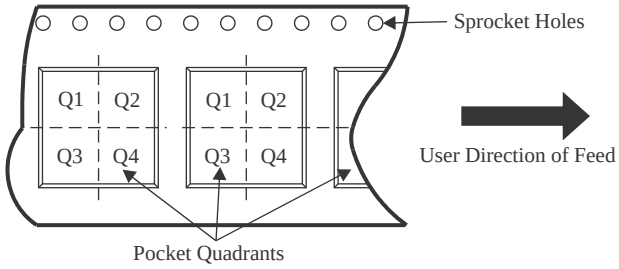


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

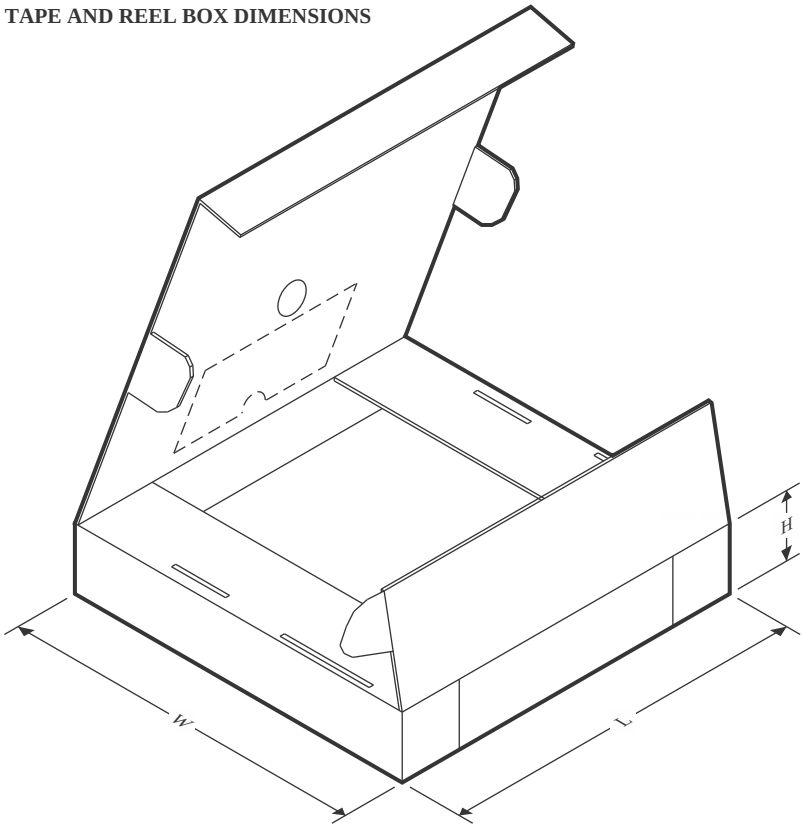
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP390AQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

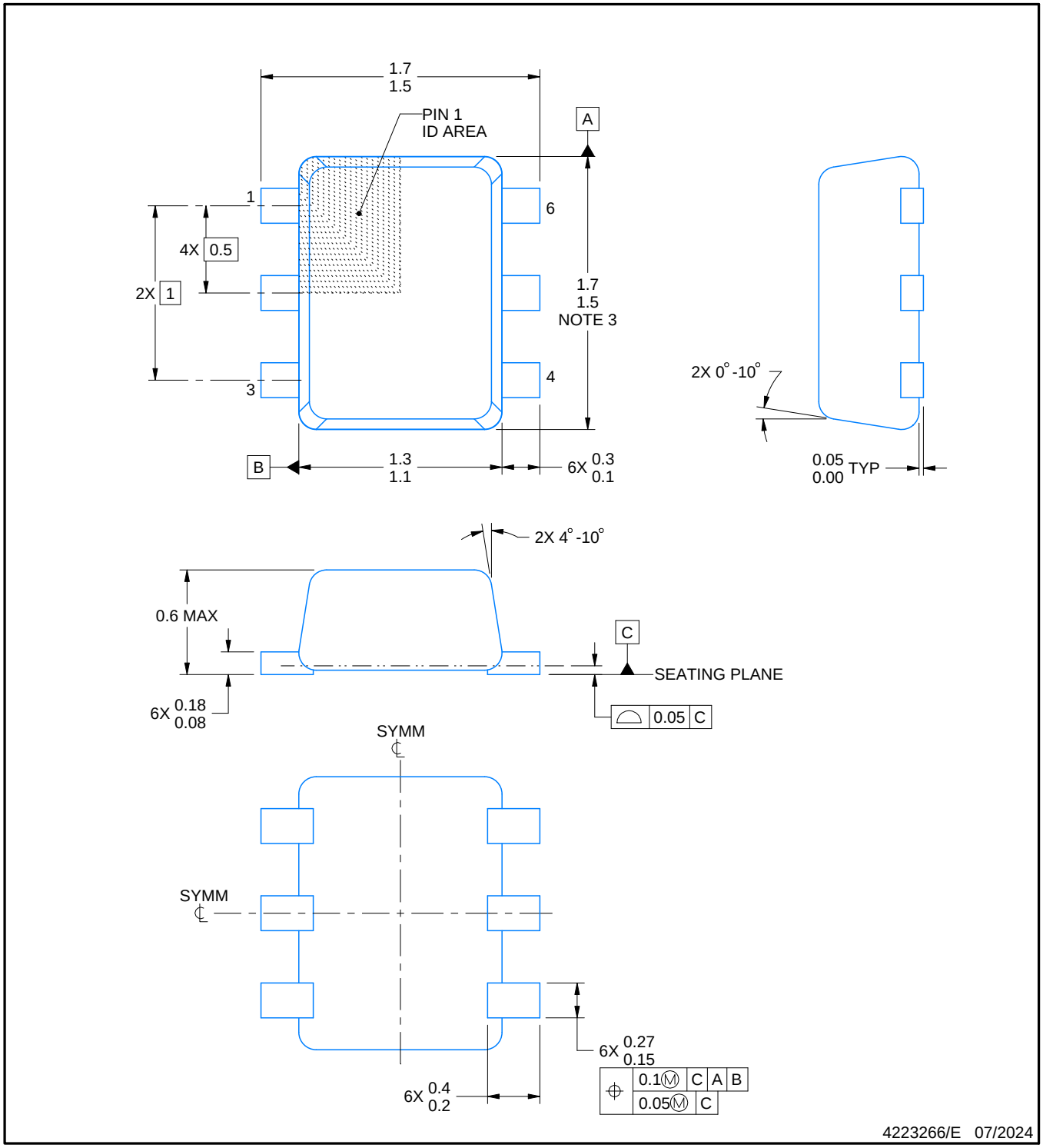
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP390AQDRLRQ1	SOT-5X3	DRL	6	4000	183.0	183.0	20.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

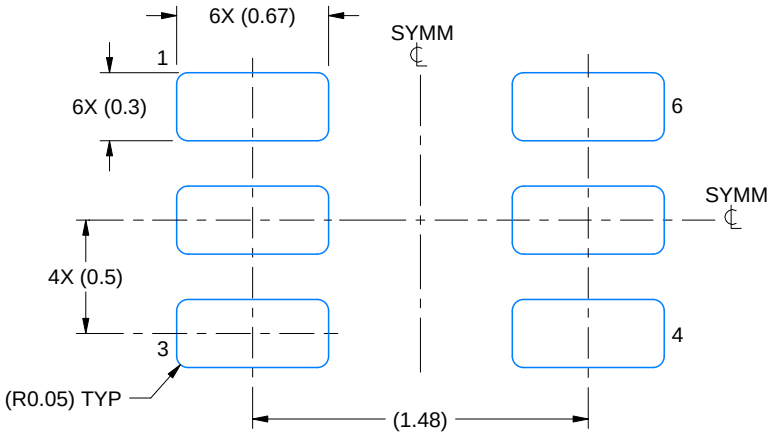
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

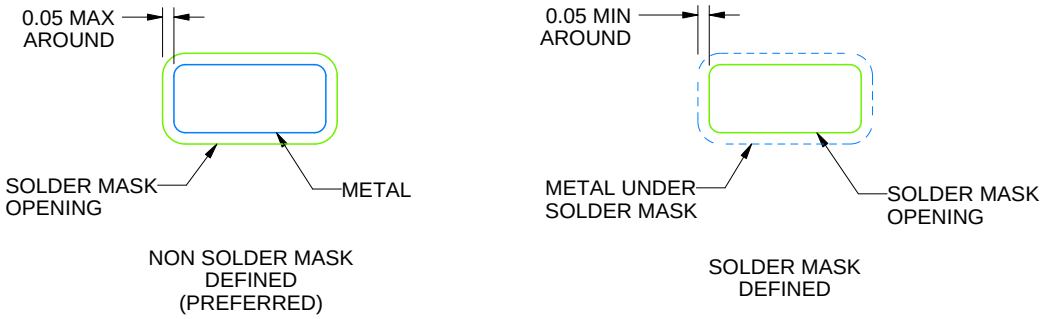
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X

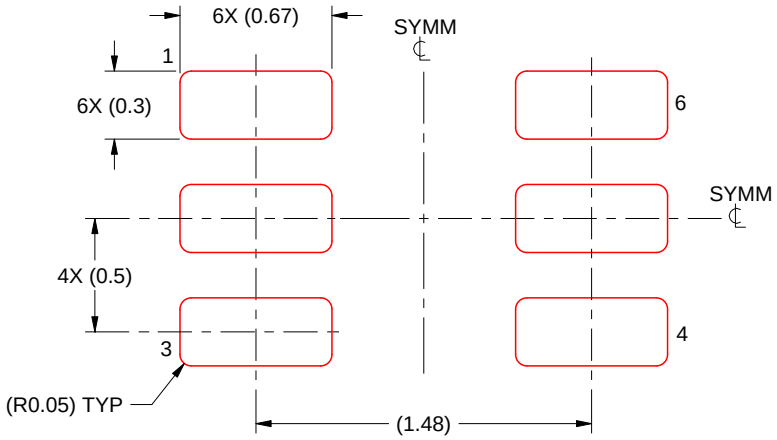


SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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