TMP113 Ultra-Small, 1.4V to 5.5V Supply, ±0.3°C Accurate, I²C Digital Temperature Sensor

1 Features

- Available in WCSP package:
  - Body size (DSBGA-6): 1.5 × 1.0 × 0.525mm
- Wide operating ranges
  - V+ operating range: 1.4V to 5.5V
  - Temperature range: -40°C to 125°C
- Accuracy holds across temperature
  - ±0.1°C (typical) at 25°C
  - ±0.3°C (maximum) from -25°C to 85°C
  - ±0.5°C (maximum) from -40°C to 125°C
- 12-bit resolution: 0.0625°C (LSB)
- Flexible digital interface
  - I²C and SMBus compatible
  - I3C Mixed Bus co-existence capable
- Low supply current
  - 3.4µA Average current (typical) at 4Hz
  - 1.4µA Average current (typical) at 1Hz
  - 70nA Shutdown current (typical)
- Only 2m°C/V DC power supply rejection over wide supply range of 1.4V to 5.5V
- Safety and compliance
  - NIST Traceable
- Software compatible with normal mode of Industry-Standard
  - TMP102, TMP110, TMP112
- Available compatible dual source device in the market

2 Applications

- Building automation
  - Occupancy detection
  - Video doorbell
  - HVAC: Wireless environmental sensor
- Factory automation & control
  - Machine vision camera
  - Power Delivery Units
  - Industrial PC: Single board computer
  - CPU (PLC controller)
- Medical Equipment
  - Continuous glucose monitor
- Data center & enterprise computing
  - Solid state drive (SSD)
  - Rack Server Motherboard
- Personal electronics
  - PC & notebooks, tablets, Gaming
  - Digital still & video camera
  - Augmented reality glasses
  - Smart speakers

3 Description

The TMP113 is a I²C-compatible digital temperature sensor in a 6-pin WCSP-package. The TMP113 offers an accuracy of ±0.3°C across the -25°C to 85°C temperature range with an on-chip 12-bit analog-to-digital converter (ADC) that provides a temperature resolution of 0.0625°C.

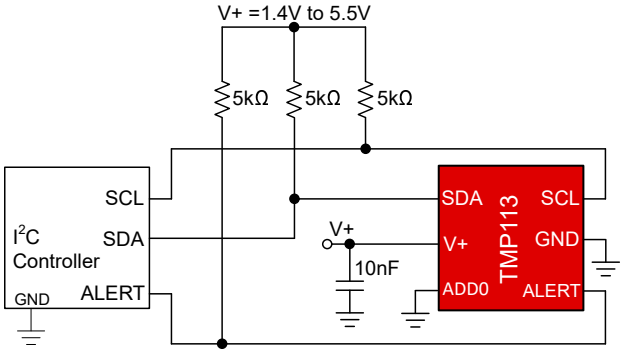
The TMP113 is designed to operate from a supply range as low as 1.4V, with a low average and shutdown current of 1.4µA (at 1Hz) and 70nA, allowing for an on-demand temperature conversion and maximizing of battery life. At the same time the supply can be raised to as high as 5.5V for a range of industrial applications with only 2m°C/V DC power supply rejection. This device has a very fast thermal step response equal to 0.2s with flexible PCB.

The TMP113 production units are 100% tested against sensors that are NIST-traceable and are verified with equipment that are NIST-traceable through ISO/IEC 17025 accredited calibrations.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP113	DSBGA (6)	1.5mm × 1.0mm × 0.525mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Note: Pull-up resistors are recommended to be higher than 5kΩ.

Simplified Schematic

Table of Contents

4 Related Products

Similar devices in terms of software are available.

Table 4-1. Related Temperature Sensors

DEVICE	BEST ACCURACY (MAXIMUM ERROR)	SOFTWARE COMPATIBLE	ADDRESS/ALERT PIN FUNCTIONALITY	PACKAGE OPTIONS
TMP102	2.0°C	Yes (in Normal Mode)	Address + Alert	DRL (6-pin SOT563) (1.6mm × 1.6mm)
TMP110	1.0°C	Yes (in Normal Mode)	Separate (Address & Alert)	DPW (5-pin X2SON) (0.8mm × 0.8mm)
TMP112	0.5°C	Yes (in Normal Mode)	Address + Alert (DRL)	DRL (6-pin SOT563) (1.6mm × 1.6mm)
			Separate (Address & Alert) (DPW)	DPW (5-pin X2SON) (0.8mm × 0.8mm)
TMP113	0.3°C	Yes	Address + Alert	YBG (6-pin DSBGA) (1.5mm × 1.0mm

5 Pin Configuration and Functions

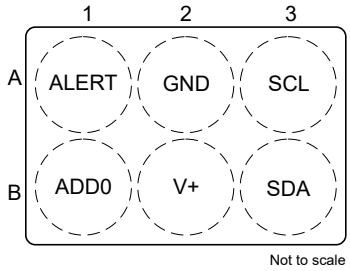


Figure 5-1. YBG Package, 6-Pin DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	A2	—	Ground
SCL	A3	I	Serial clock
ADD0	B1	I	Address select. Connect to GND, SCL, SDA or V+
ALERT	A1	O	Overtemperature alert. Open-drain output; requires a pullup resistor. **Note**: if Alert pin is not used, connecting this pin to GND is preferred.
SDA	B3	I/O	Serial data input. Open-drain output; requires a pullup resistor.
V+	B2	I	Supply voltage

1. I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V+	–0.3	6	V
Input/Output voltage	SCL, SDA, ADD0, ALERT	–0.3	6	V
Output current, I_{OL}			±3	mA
Operating temperature, T_A		–40	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.4	3.3	5.5	V
$V_{I/O}$	SCL, SDA, ADD0, ALERT			V+	V
I_{OL}	SDA, ALERT	0		3	mA
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP113 YBG (DSBGA-6) 6-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W
M_T	Thermal Mass	0.7	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application note.*

6.5 Electrical Characteristics

Over free-air temperature range and V+ = 1.4V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR					

Over free-air temperature range and V+ = 1.4V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{ERR}	Accuracy (temperature error)	25°C			± 0.1		°C
		-25°C to 85°C		-0.3		0.3	
		-40°C to 125°C		-0.5		0.5	
PSR	DC power supply rejection				2		m°C/V
T_{RES}	Temperature resolution				12		Bits
					62.5		m°C
T_{REPEAT}	Repeatability(1)	1Hz conversion cycle			±1		LSB
T_{LTD}	Long-term stability and drift	1000 hours at 125°C(2)			±1		LSB
t_{RESP_L}	Response time (Stirred Liquid)	2-layer FR4 PCB 1.5748mm thickness	τ = 63% for step response from 25°C to 75°C		1.1		s
		Flexible PCB 0.2mm thickness			0.2		
T_{HYST}	Temperature cycling and hysteresis(3)				±1		LSB
t_{ACT}	Active conversion time				11.4	12.8	ms
t_{CONV}	Conversion Period (Set by user)	CR1 = 0, CR0 = 0 (0.25Hz)			4	4.4	s
		CR1 = 0, CR0 = 1 (1Hz)			1	1.1	
		CR1 = 1, CR0 = 0 (default, 4Hz)			0.25	0.28	
		CR1 = 1, CR0 = 1 (8Hz)			0.125	0.14	
t_{VAR}	Timing variation of all device settings			-10		10	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance				4.5		pF
V_{IH}	Input logic high			0.7 × V+			V
V_{IL}	Input logic low			-0.3		0.3 × V+	V
V_{HYST}	Hysteresis				0.11		V
I_{IN}	Input current					±0.1	µA
V_{OL}	Output logic	I_{OL} = –3mA		0		0.4	V
POWER SUPPLY							
I_{DD_AVG}	Average current consumption	Continuous conversion mode 1Hz conversion period	Serial bus idle		1.4	4	µA
		Continuous conversion mode 4Hz conversion period			3.4	7	
		One shot conversion mode 1Hz conversion period	SCL = 400kHz		6.7		
			SCL = 1MHz		14		
I_{DD_SB}	Standby current(4)	Continuous conversion mode Serial bus idle and connected to V+			0.85	3.3	µA
I_{DD_SD}	Shutdown current (Serial bus level = GND or V+)	T_A = +25°C, Serial bus inactive and connected to V+			0.07	0.2	µA
		T_A = -40°C to 125°C				2	
		Serial bus active, SCL frequency = 400kHz			5.5		
		Serial bus active, SCL frequency = 1MHz			13		
I_{DD_ACTIVE}	Supply current during active conversion	Active Conversion, serial bus idle			55	95	µA
V_{POR}	Power-on reset threshold voltage	Supply rising			1.02		V
	Brownout detect	Supply falling			0.97		V

Over free-air temperature range and V+ = 1.4V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{INIT}	Initialization time after power-on reset			10		ms
t_{RESET}	Reset Time	General Call Reset		0.1		ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150°C.
(3) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot →room→cold→room. The temperatures used for this test are -40°C, 25°C, and 125°C.
(4) Quiescent current between conversion periods in continuous conversion mode

6.6 I²C Interface Timing

Minimum and maximum specifications are over –40°C to 125°C and V+ = 1.4V to 5.5V (unless otherwise noted)(1)

		FAST MODE		FAST MODE PLUS		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	1	0.001	3.4	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	600	–	500		160	–	ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	100	–	100		100	–	ns
$t_{(SUSTA)}$	Repeated START condition setup time	100	–	100		100	–	ns
$t_{(SUSTO)}$	STOP condition setup time	600	–	260		160	–	ns
$t_{(HDDAT)}$	Data hold time(2)	10	900	10	150	10	105	ns
$t_{(SUDAT)}$	Data setup time	100	–	10		10	–	ns
$t_{(LOW)}$	SCL clock low period	1300	–	500		160	–	ns
$t_{(HIGH)}$	SCL clock high period	600	–	260		60	–	ns
$t_{(VDAT)}$	Data valid time (data response time)(3)		900		450			ns
t_F	SDA, SCL fall time	–	300		120	–	80	ns
t_R	SDA, SCL rise time	–	300	–	120	–	80	ns
$t_{timeout}$	Timeout (SCL = Low or SDA = Low)	30		30		–	40	ms
t_{LPF}	Glitch suppression filter	50		50		–	40	ns

(1) The controller and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

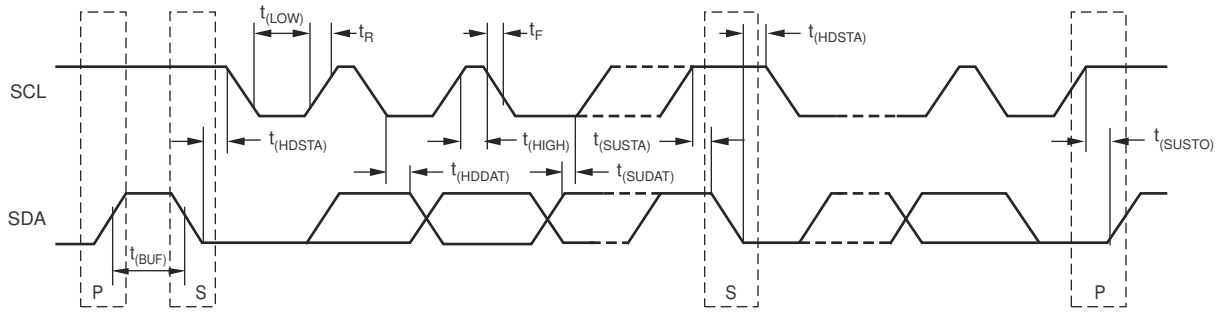


Figure 6-1. I²C Timing Diagram

6.8 Typical Characteristics

at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

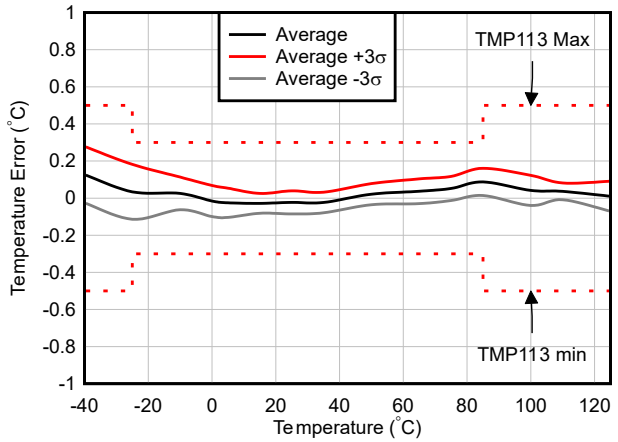


Figure 6-2. Temperature Error vs Temperature

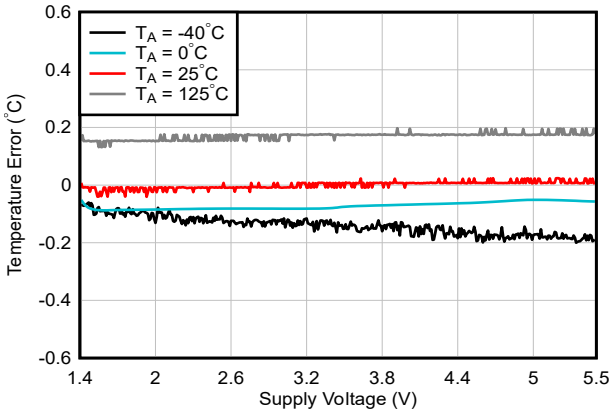


Figure 6-3. Temperature Error vs Supply Voltage

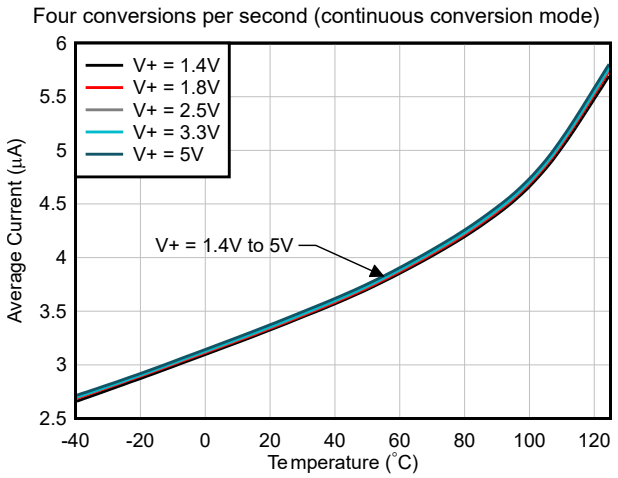


Figure 6-4. Average Quiescent Current vs Temperature

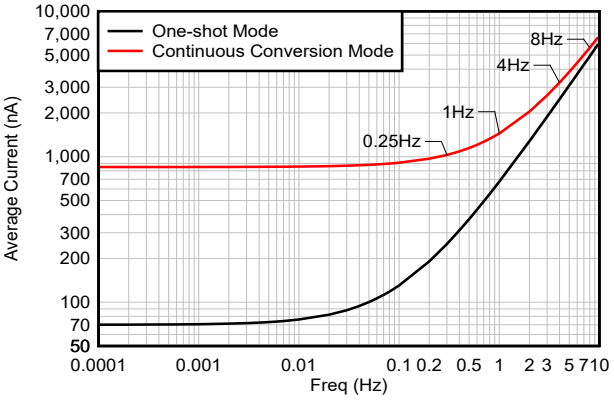


Figure 6-5. Average Quiescent Current vs Frequency (V+ = 1.4V to 5.5V)

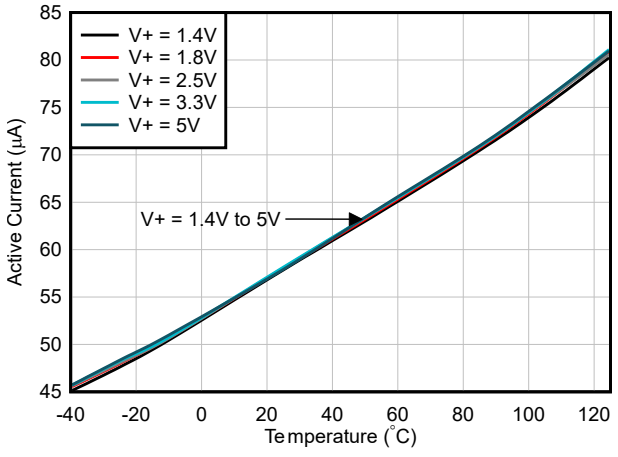


Figure 6-6. Active Conversion Current vs Temperature

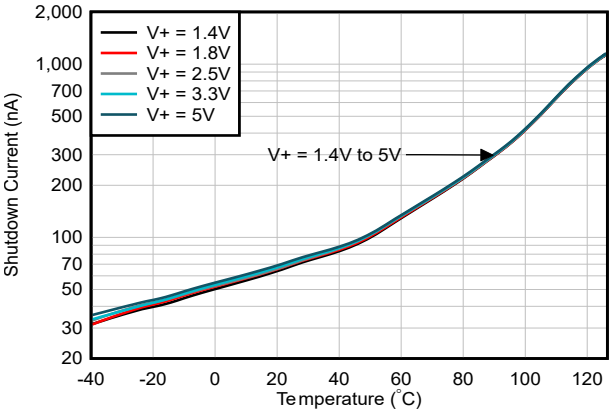


Figure 6-7. Shutdown Current vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

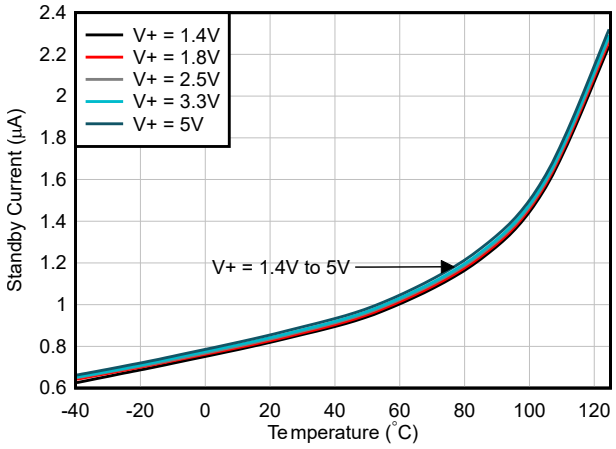


Figure 6-8. Standby Current vs Temperature

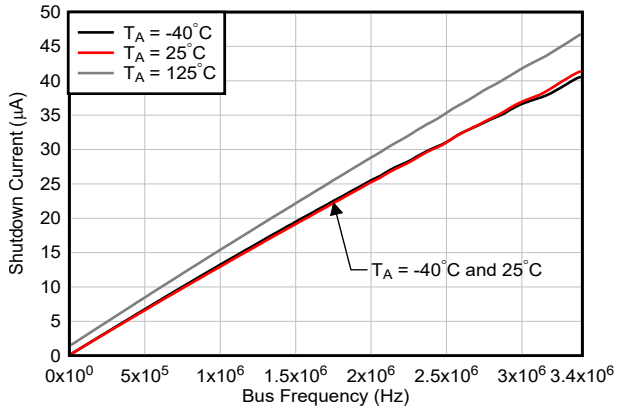


Figure 6-9. Shutdown Current vs Bus Frequency (Temperature at 3.3V Supply)

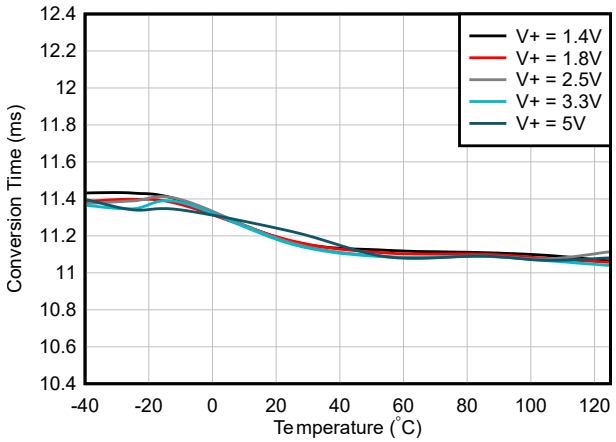


Figure 6-10. Conversion Time vs Temperature

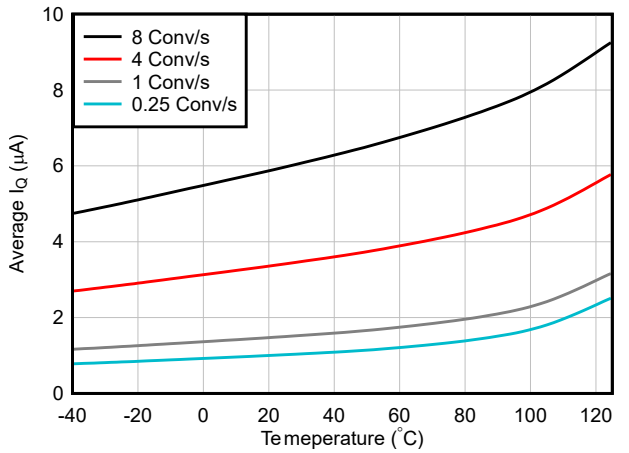


Figure 6-11. Average Supply Current (continous conversion mode) vs Conversion Rate

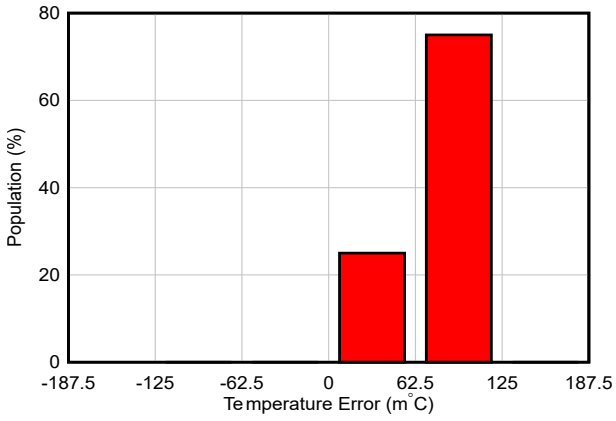


Figure 6-12. Temperature Error at 25 °C (V+ = 1.4V to 5.5V)

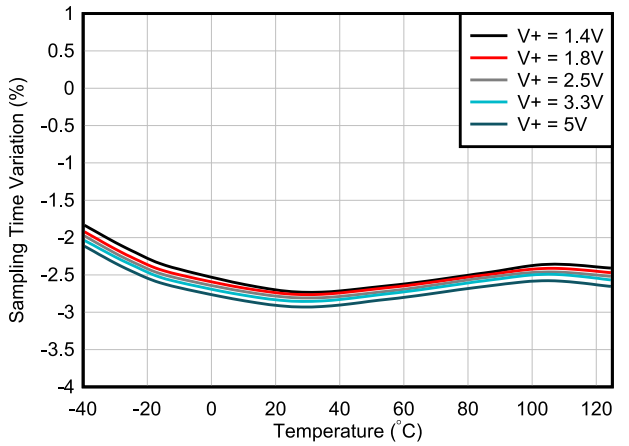


Figure 6-13. Sampling Time vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

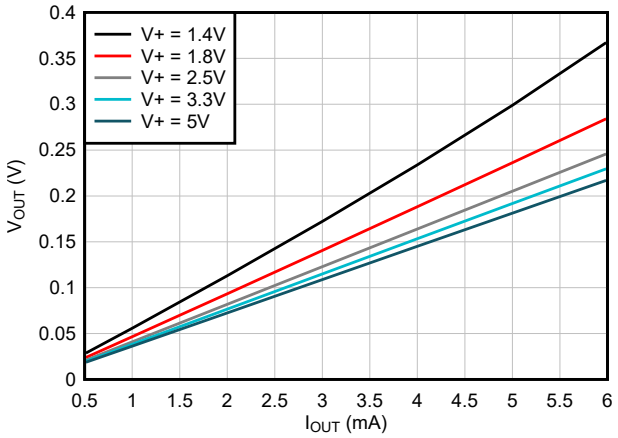


Figure 6-14. ALERT Pin Output Voltage vs Pin Sink Current

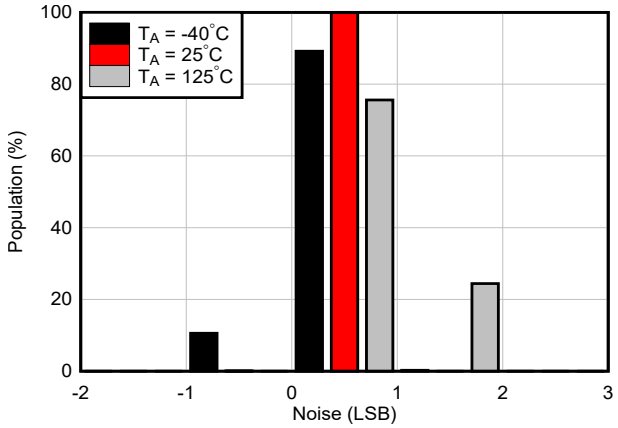


Figure 6-15. Noise Histogram (Oil bath measurement and V+ = 1.4V to 5.5V)

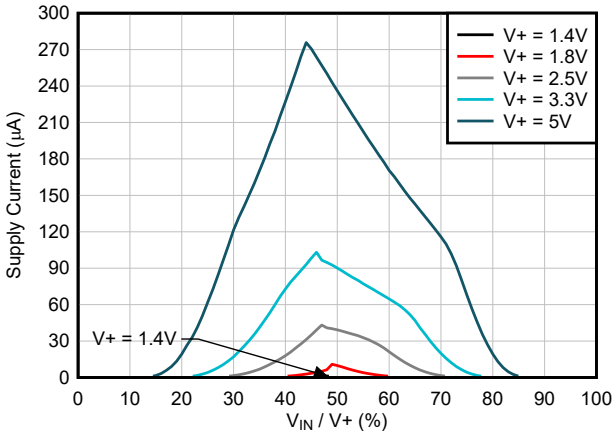


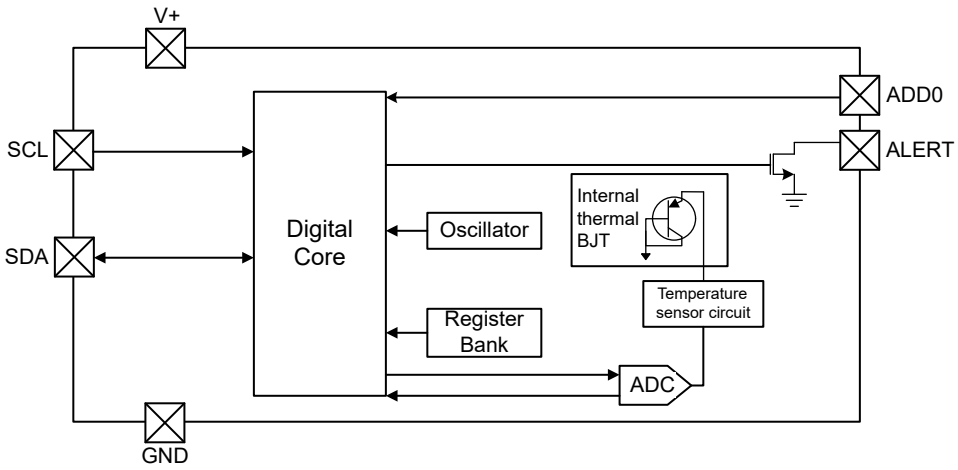
Figure 6-16. Supply Current vs one Input Cell Input Voltage

7 Detailed Description

7.1 Overview

The TMP113 is a digital output temperature sensor that comes factory calibrated for accuracy. The device features a two-wire, SMBus and I^{2}C compatible interface with two modes of operation: continuous conversion mode and one-shot conversion mode, designed for thermal management and thermal protection applications. The TMP113 also includes an alert status register with individual high and low thresholds.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement is stored in the read-only temperature register. The temperature register of the TMP113 device is configured as a 12-bit, read-only register that stores the output of the most recent conversion. The device output is as shown in Table 7-1.

Table 7-1. 12-Bit Temperature Data Guidelines

Temperature Bit Length	Q Notation	LSB (°C)	Range (+)	Range (-)
12	4	0.0625	127.93475	-128

Two bytes have to be read to obtain data. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 7-2. One LSB equals 0.0625°C. Negative numbers are represented in binary two's complement format. Following power-up or reset, the temperature register has 0°C until the first conversion is complete. The unused bits in the temperature register always read 0.

Table 7-2. 12-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX (four LSBs are not used)
>127.9375	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0.0625	0000 0000 0001	001

Table 7-2. 12-Bit Temperature Data Format (continued)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX (four LSBs are not used)
0	0000 0000 0000	000
-0.0625	1111 1111 1111	FFF
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

Table 7-2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

   Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

   Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the two's complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

   Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

   Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

1. Generate the two's complement of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

   Example: 1110 0111 0000 has two's complement of 0001 1001 0000 = 0001 1000 1111 + 1

   Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

7.3.2 Decoding Temperature Data

The TMP113 temperature registers use a 12-bit format. The 12 bits are aligned to the left side, or most significant side, of the 16-bit word. The four unused bits are on the right side, or least significant side. For this reason, a shift is needed to discard the extra bits. Two's complement is employed to describe negative temperatures. C code can easily convert the two's complement data when the data is typecast into the correct signed data type. Q notation describes the number of bits which represent a fractional result. 4 bits of fractional data, known as Q4, offer 0.0625°C resolution.

Table 7-3. 12-Bit Q4 Encoding Parameters

PARAMETER	VALUE
Bits	12

Table 7-3. 12-Bit Q4 Encoding Parameters (continued)

PARAMETER	VALUE
Q	4
Resolution	0.0625
Range (+)	127.9375
Range (–)	-128
25˚C	0x0190

Table 7-4. 12-Bit Q4 Bit Values in °C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	-	-	-	-
-128	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	-	-	-	-
-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	-	-	-	-

```
/* 12-bit format will have 4 bits discarded by right shift
 q4 is 0.062500 resolution
 the following bytes represent 24.5C */
uint8_t byte1 = 0x18;
uint8_t byte2 = 0x80;
float f = (((int8_t) byte1 << 8 | byte2) >> 4) * 0.0625f;
int mC = (((int8_t) byte1 << 8 | byte2) >> 4) * 1000 >> 4;
int C = (int8_t) byte1;
```

7.3.3 Temperature Limits and Alert

The TMP113 has an alert feature and uses the TLow_Limit register for low threshold comparison and THigh_Limit register for high threshold comparison. The alert limit is programmed in the TMP113 in a 12-bit two's complement format based in the Configuration register, with a resolution of 62.5m°C. At the end of each temperature conversion, the temperature result is compared with the high limit and low limit registers, and the alert status flag and ALERT pin are updated.

The alert status flag in the configuration register and the ALERT pin are updated after every temperature conversion based on the Alert_Mode and Polarity bit settings in the configuration register.

As shown in Figure 7-1, in comparator mode (Alert_Mode = 0b), the ALERT pin and status flag become active when the temperature equals or exceeds the value in THigh_Limit for Fault number of consecutive conversions. The ALERT pin and status flag remain active until the temperature falls below the TLow_Limit for the same number of consecutive conversions.

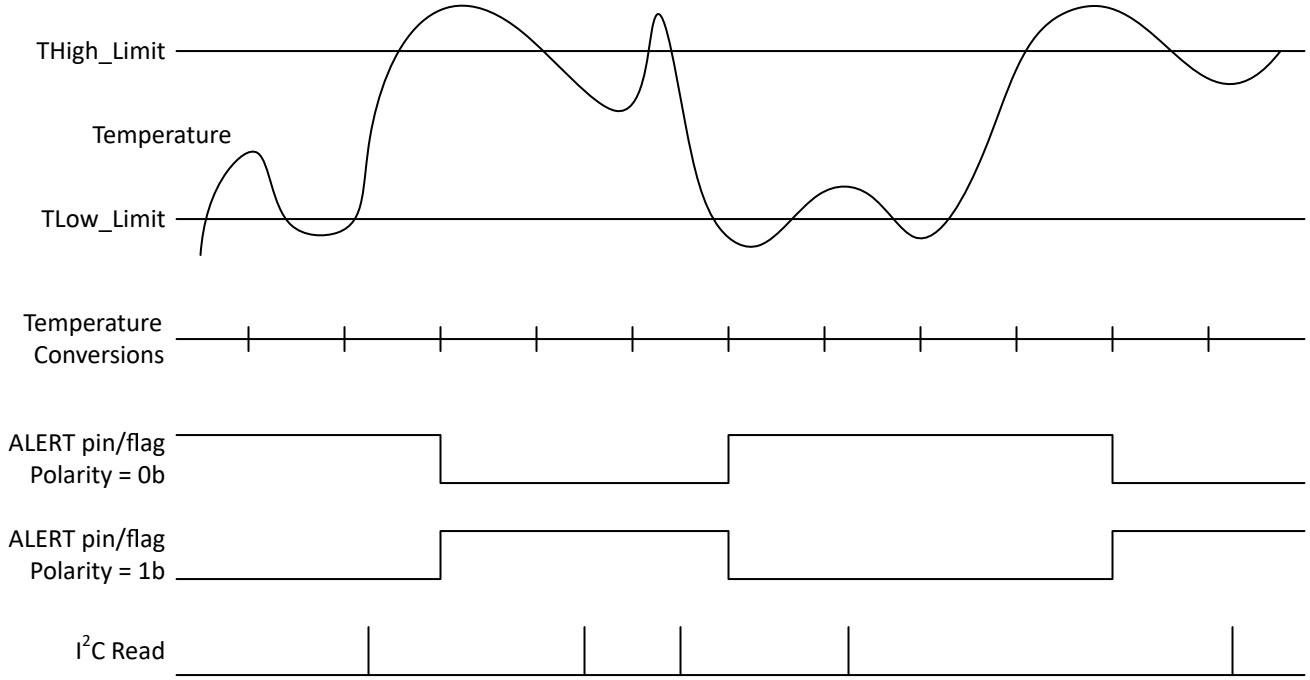


Figure 7-1. Comparator Mode

As shown in Figure 7-2, in Alert mode (Alert_Mode = 1b), the ALERT pin and status flag become active when the temperature equals or exceeds the THigh_Limit for Fault number of consecutive conversion. The ALERT pin/flag remains active until a read operation of any register occurs or the device responds to the SMBus Alert Response. When the ALERT pin and status flag are cleared, the pin/flag becomes active only when the temperature is less than the TLow_Limit for Fault number of consecutive conversion, and remains active until a read operation of any register occurs or the device responds to the SMBus Alert Response. When the ALERT pin/flag is cleared after a TLow_Limit crossing, the above cycle repeats. The ALERT pin and status flag can also be cleared by issuing the General Call Reset command.

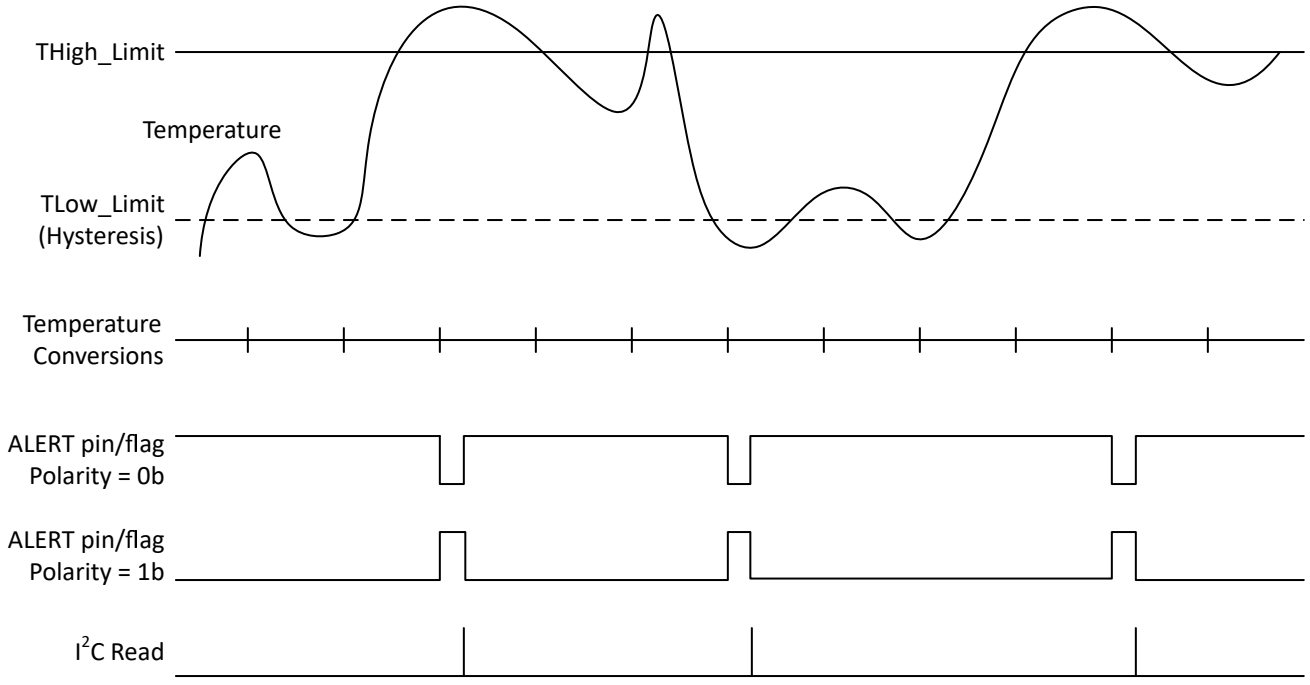


Figure 7-2. Alert Mode

7.3.4 NIST Traceability

The TMP113 offers 3 Unique ID registers (48-bit) to support NIST traceability. These unique IDs can be used to provide an audit trail to standards provided by the National Institute of Standards and Technology (NIST), a US Commerce Department agency.

Reading the Unique ID registers requires a specific procedure to retrieve the content from the memory. The procedure is as follows:

1. Place the device in Shutdown Mode by setting bit 8 of Register 01h (Configuration register) to 1b.
2. Write 0x0000 to desired Unique ID pointer address (0Ch, 0Dh, 0Eh, or 0Fh).
3. Read Unique ID from the same pointer address.
4. Repeat step #2 above for each pointer address as desired.

Note address 0Fh is expected to be read 0x0000 for this device and is reserved for future use. In addition, for high speed mode, the user must wait 25µs after step-3 and before communicating.

7.4 Device Functional Modes

The TMP113 can be configured to operate in continuous or one-shot (shutdown) mode. This flexibility enables designers to balance the requirements of power efficiency and performance.

7.4.1 Continuous-Conversion Mode

When the Shutdown bit is set to 0b in the configuration register, the device operates in continuous conversion mode. Figure 7-3 shows the device in a continuous conversion cycle. In this mode, the device performs conversion at fixed periods and updates the temperature result register at the end of every conversion, The typical active conversion time is 11ms.

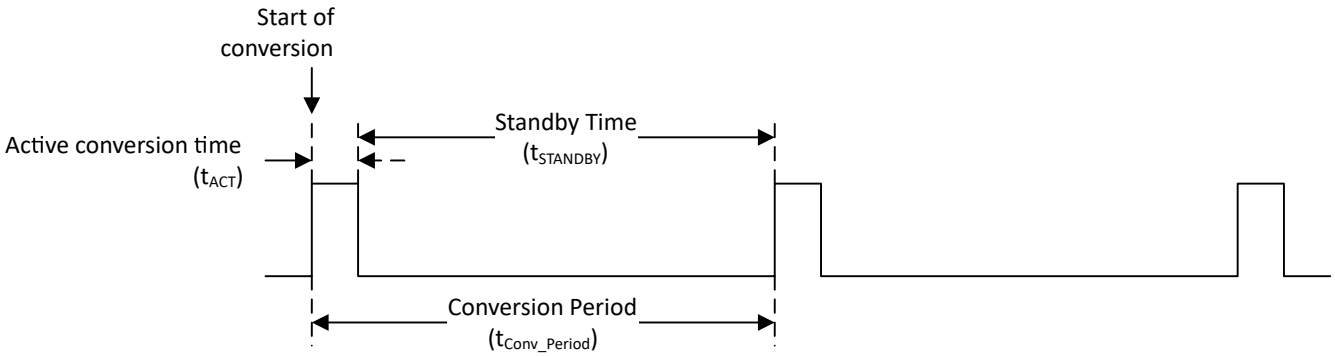


Figure 7-3. Continuous Conversion Cycle Timing Diagram

The Conversion_Rate[1:0] bits in the configuration register control the rate at which the conversions are performed. The device typically consumes 55µA during conversion and 0.85µA during the low power standby time. By decreasing the rate at which conversions are performed, the application can benefit from reduced average current consumption in continuous mode.

Use Equation 1 to calculate the average current in continuous mode.

$$\text{Average Current} = ((I_{DD\_ACTIVE} \times t_{ACT}) + (I_{DD\_SB} \times t_{STANDBY})) / t_{Conv\_Period} \quad (1)$$

Where

- t_{ACT} = Active conversion time
- t_{Conv_Period} = Conversion Period
- $t_{STANDBY}$ = Standby time between conversions calculated as t_{Conv_Period} - t_{ACT}

7.4.2 One-Shot Mode

When a 1 is written to the One_Shot bit in the configuration register, the TMP113 immediately starts a one-shot temperature conversion as shown in Figure 7-4. Requesting another conversion when the TMP113 is performing a temperature conversion, the device does not stop the active conversion. After completing the one-shot conversion, the TMP113 enters shutdown mode and the One_Shot bit is set to 1b.

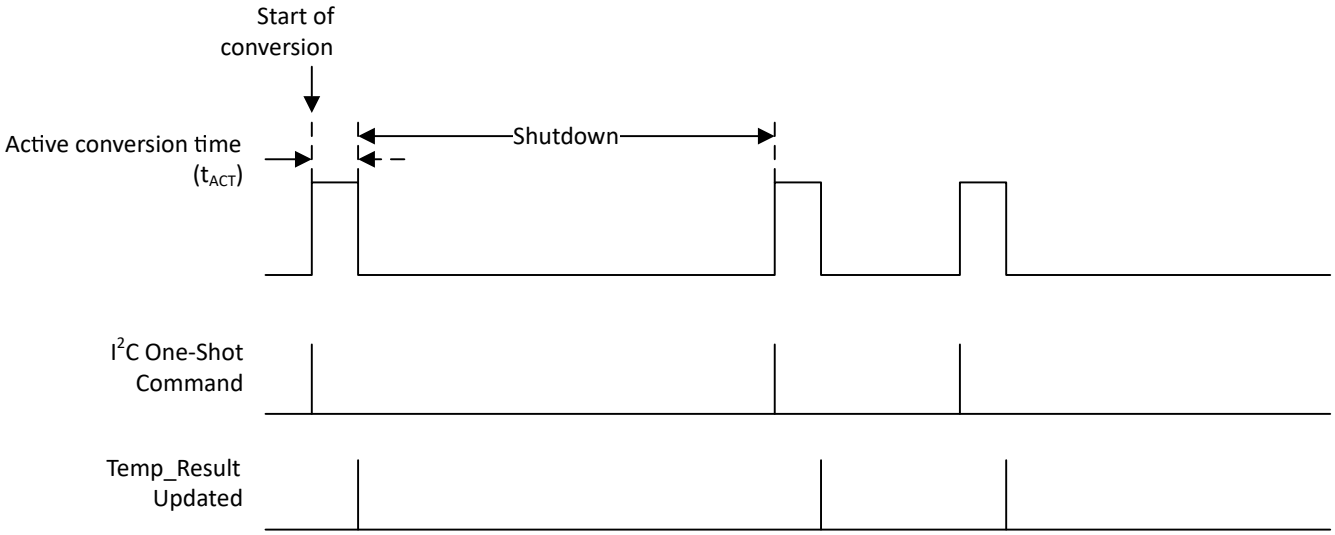


Figure 7-4. One-Shot Timing Diagram

The one-shot conversion is only supported when the Shutdown bit is set to 1b. Due to the short conversion time, the TMP113 device achieves a higher conversion rate. A single conversion typically takes 11ms and a read can take place in less than 80µs. When using the one-shot mode, 50 or more conversions per second are possible.

7.5 Programming

7.5.1 Serial Interface

The TMP113 has a standard bidirectional I^2C interface that is controlled by a controller device to be configured or read the data from TMP113 device. Each target on the I^2C bus has a specific device address to differentiate between other target devices that are on the same I^2C bus. Many target devices require configuration upon start-up to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. The TMP113 includes 50ns glitch suppression filters, allowing the device to coexist on an I3C mixed bus. The TMP113 supports transmission data rates up to 3.4MHz.

7.5.2 Bus Overview

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. The SDA line must be connected to a supply through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I^2C lines, the communication frequency and I^2C bus voltage. For further details, see the I^2C Pullup Resistor Calculation application note. Data transfer can be initiated by a controller only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition or time out events (see Figure 7-5 and Figure 7-6).

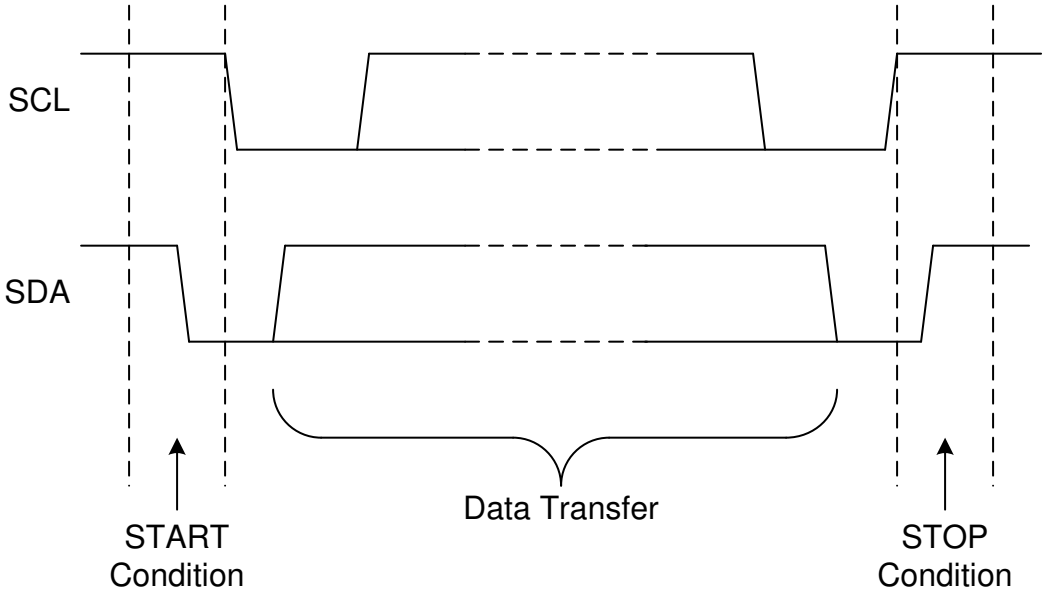


Figure 7-5. Definition of Start and Stop Conditions

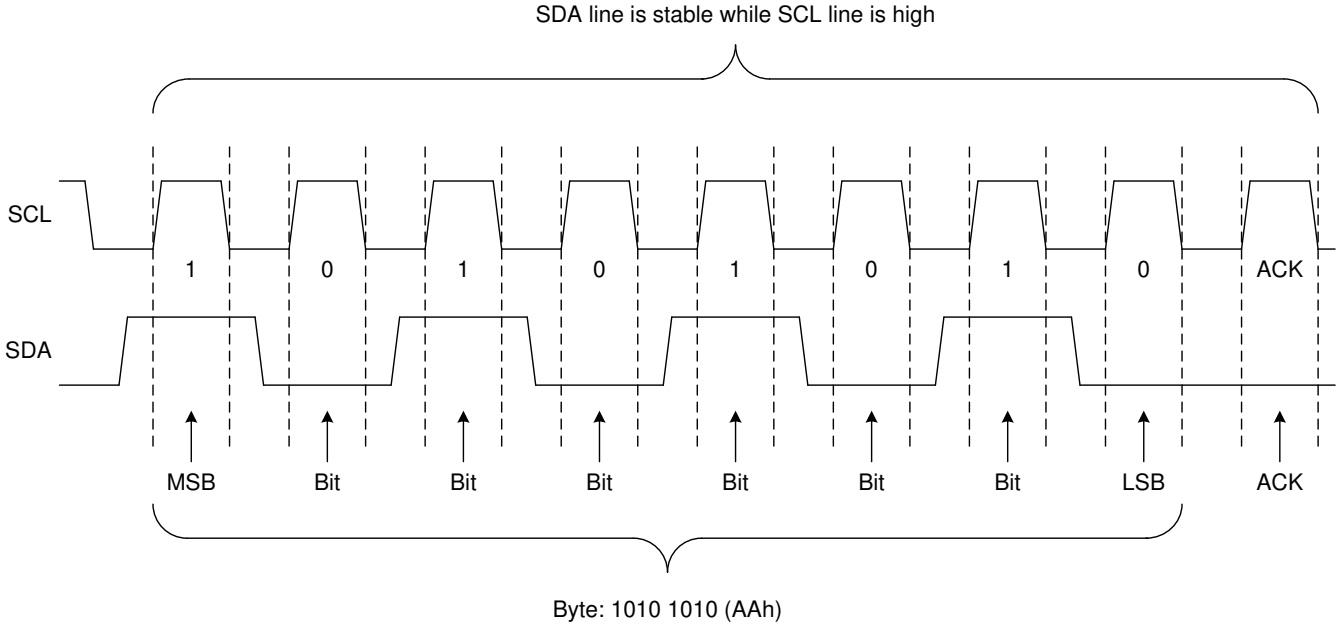


Figure 7-6. Bit Transfer

7.5.3 Device Address

To communicate with the TMP113, the controller must first address target devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation. The TMP113 features an address pin to allow up to four TMP113 devices to be addressed on a single bus simultaneously. Table 7-5 describes the pin logic levels used to properly connect up to four devices on the same I^2C bus.

Table 7-5. Address Pin and Device Target Address

DEVICE TARGET ADDRESS[1]	ADD0 PIN CONNECTION	DEVICE ORDERABLE
1001000	GND	TMP113
1001001	V_{DD}	
1001010	SDA	
1001011	SCL	

7.5.4 Bus Transactions

7.5.4.1 Writes

To write on the I^{2}C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/W bit) set to 0b, which signifies a write. The target acknowledges, letting the controller know the target is ready. After this operation, the controller starts sending the register pointer and data to the target, and the controller terminates the transmission with a STOP condition.

Writes to read-only registers or register locations outside of the register map are ignored. The TMP113 still performs and acknowledges when writing outside of the register map. Figure 7-7 shows an example of writing a single word write communication.

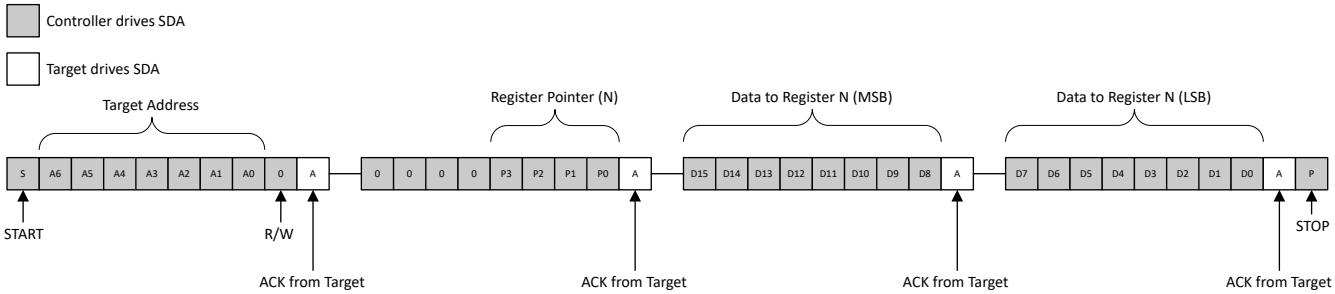


Figure 7-7. Write to Single Register

7.5.4.2 Reads

For a read operation the controller sends a START condition, followed by the target address with the R/W bit set to 0b (signifying a write). The target acknowledges the write request, and the controller sends the Register Pointer. The controller initiates a restart followed by the target address with the R/W bit set to 1b (signifying a read). The controller continues to send out clock pulses but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that the controller is ready for more data. For repeated read operations from the same register (like temperature register), resending the register pointer is not necessary. The read operation from the same register can be repeated as many time as the controller needs when the pointer is set. Once the controller has received the expected number of bytes, the controller sends a NACK, signaling to the target to halt communications and release the SDA line. The controller follows this up with a STOP condition. Reading from a non-indexed register location returns 00h. Figure 7-8 shows an example of reading a single word from a target register. Note that after resetting, the pointer is set to zero and the temperature register must be addressed.

[1] Additional address options can be available on request

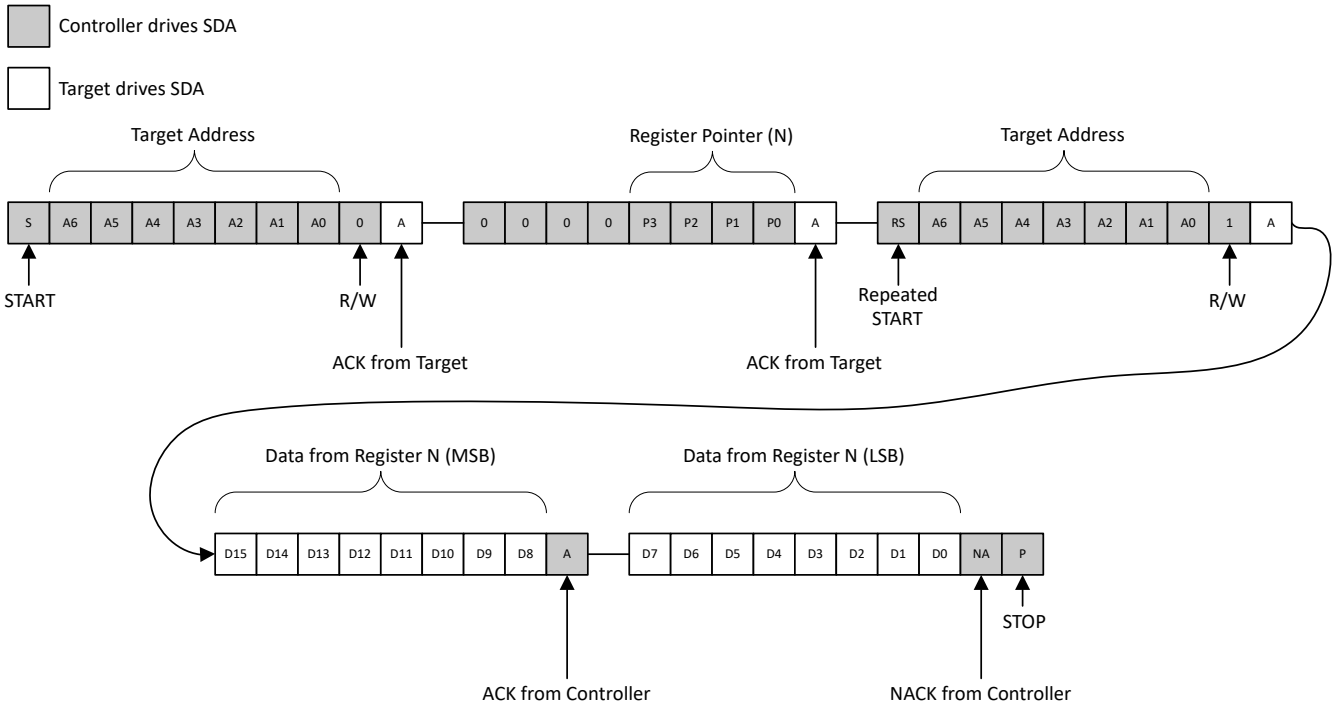


Figure 7-8. Read from Single Register

7.5.4.3 General Call Reset Function

The TMP113 responds to a general-call address (0000 000) if the eighth bit (R/W bit) is 0b. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000b 0110b, the TMP113 internal registers are reset to power-up values as shown in SMBus General Call Reset Timing Diagram. The serial address is unaffected by the general call reset.

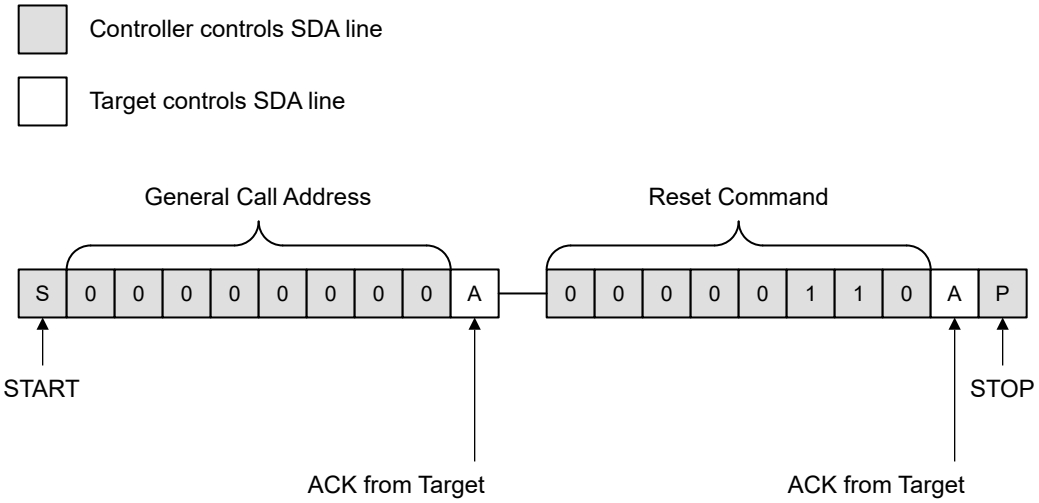


Figure 7-9. SMBus General Call Reset Timing Diagram

7.5.4.4 SMBus Alert Response

The TMP113 device supports the SMBus alert response. When the TMP113 operates in Alert Mode, and the ALERT pin is available, the controller can sense that an alert condition is present. Irrespective of the availability of the ALERT pin, the alert status is set. As shown in Figure 7-10, if the controller sends an SMBus alert command (19h or 00011001b) on the bus, and the alert is set, the device acknowledges the SMBus alert command and responds by returning the device address on the SDA line. The eighth bit (LSB) of the device

address byte indicates if the alert condition is caused by the temperature exceeding THigh_Limit or falling below the TLow_Limit. The value of the eight bit follows the Polarity bit setting.

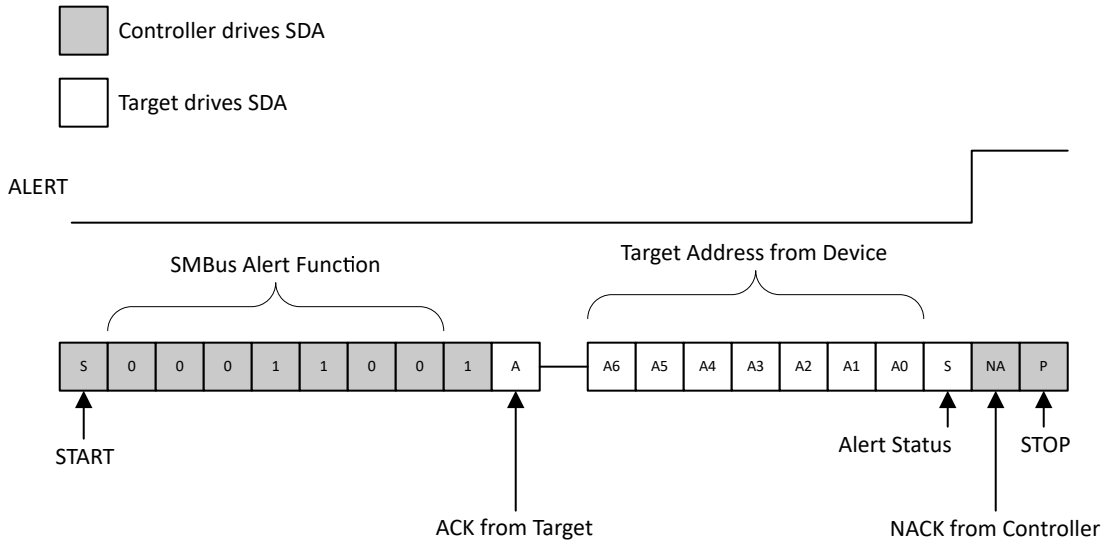


Figure 7-10. SMBus Alert Response

If multiple devices on the bus respond to the SMBus alert command, arbitration during the device address portion of the SMBus alert command determines which devices the ALERT pin is activated. The device with the lowest address wins the arbitration. On winning the arbitration, the TMP113 inactivates the ALERT pin and/or clears the status bit. To prevent the device with lowest I^2C address in continuous conversion mode sees the alert line and halt others with higher I^2C address to report the alert, the controller has to temporarily disable the Alert mode in device with smallest I^2C address until all alerts in the system are cleared.

7.5.4.5 Time-Out Function

The TMP113 resets the serial interface if the SCL line is held low by the controller or the SDA line is held low by the TMP113 for 30ms (typical) between a START and STOP condition. The TMP113 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the controller. To avoid activating the timeout function, maintain a communication speed of at least 1kHz for the SCL operating frequency. If another device on the bus is holding the SDA pin low, the TMP113 does not reset.

7.5.4.6 Coexist on I3C Mixed Bus

A bus with both I3C and I^2C interfaces is referred to as a mixed bus with clock speeds up to 12.5MHz. The TMP113 is an I^2C device that can be on the same bus that has an I3C device attached, as the TMP113 incorporates a spike suppression filter of 50ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I3C devices.

8 Register Map

Table 8-1. TMP113 Register Map

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	0000h	Temp_Result	Temperature result register	Go
01h	R/W	40A0h	Configuration	Configuration register	Go
02h	R/W	4B00h	TLow_Limit	Temperature low limit register	Go
03h	R/W	5000h	THigh_Limit	Temperature high limit register	Go
04h - 0Ah	R	xxxxh	Reserved	Reserved	-
0Bh	R	1130h	Device_ID	Device ID	Section 8.5
0Ch	R	xxxxh	Unique_ID0	NIST Data 0 Register	Section 8.6
0Dh	R	xxxxh	Unique_ID1	NIST Data 1 Register	Section 8.7
0Eh	R	xxxxh	Unique_ID2	NIST Data 2 Register	Section 8.8
0Fh	R	xxxxh	Reserved	Reserved	-

Table 8-2. TMP113 Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

8.1 Temp_Result Register (address = 00h) [reset = 0000h]

This register stores the latest temperature conversion result in a 12-bit two's complement format with a LSB equal to 0.0625°C.

Return to Register Map.

Table 8-3. Temp_Result Register

15	14	13	12	11	10	9	8
Temp_Result[11:4]							
R-xxh							
7	6	5	4	3	2	1	0
Temp_Result[3:0]				Reserved			
R-xh				R-0000b			

Table 8-4. Temp_Result Register Field Description

Bit	Field	Type	Reset	Description
15:4	Temp_Result[11:0]	R	xxxh	12-bit temperature conversion result Temperature data is represented by a 12-bit, two's complement word with an LSB equal to 0.0625°C.
3:0	Reserved	R	0000b	Reserved

8.2 Configuration Register (address = 01h) [reset = 40A0h]

This register is used to configure the operation of the TMP113 and also provides the alert status.

Return to Register Map.

Table 8-5. Configuration Register

15	14	13	12	11	10	9	8
One_Shot	Reserved		Fault[1:0]		Polarity	Alert_Mode	Shutdown
R/W-0b	R-11b		R/W-00b		R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
Conversion_Rate[1:0]		Alert Flag	Reserved				
R/W-10b		R-1b	R-00000b				

Table 8-6. Configuration Register Field Description

Bit	Field	Type	Reset	Description
15	One_Shot	R/W	0b	One-shot conversion trigger applicable in shutdown mode only. In continuous conversion mode the bit reads 0b. In shutdown mode the bit reads 1b, then after the conversion is finished the bit reads 0b. Triggering a one-shot conversion happens only when the device is in shutdown mode. 0b = Active conversion ongoing 1b = Trigger a one-shot conversion or active conversion complete
14:13	Reserved	R	10b	Reserved
12:11	Fault[1:0]	R/W	00b	Fault bits are used to set the number of consecutive conversions for which the alert condition exists before the ALERT pin is asserted and status bit is set. 00b = 1 fault 01b = 2 faults 10b = 4 faults 11b = 6 faults
10	Polarity	R/W	0b	The polarity bit allows the host to adjust the polarity of the ALERT pin/flag output. 0b = ALERT pin/flag output is active low 1b = ALERT pin/flag output is active high
9	Alert_Mode	R/W	0b	The alert mode bit indicates the how the temperature limits operate. 0b = Comparator mode 1b = Alert mode
8	Shutdown	R/W	0b	The shutdown bit is used to change the device conversion mode. 0b = Continuous conversion mode 1b = Shutdown mode
7:6	Conversion_Rate[1:0]	R/W	10b	The conversion rate bits configure the device conversion period. The default is conversion every 250ms. 00b = 4s / 0.25Hz 01b = 1s / 1Hz 10b = 0.25s / 4Hz 11b = 0.125s / 8Hz
5	Alert flag	R	1b	The alert bit is a read-only bit which provides the information about the alert status in comparator mode and is affected by Alert_Mode setting. The polarity bit affects the alert flag.
4:0	Reserved	R	00000b	Reserved

8.3 TLow_Limit Register (address = 02h) [reset = 4B00h]

This register is used to configure the low temperature alert limit of the device. The limit is formatted in a 12-bit two's complement format with a LSB equal to 62.5m°C. The default value on start-up is 4B00h or 75°C.

Return to Register Map.

Table 8-7. TLow_Limit Register

15	14	13	12	11	10	9	8
TLow_Limit[11:4]							
R/W-4Bh							
7	6	5	4	3	2	1	0
TLow_Limit[3:0]				Reserved			
R/W-0h				R-0000b			

Table 8-8. TLow_Limit Register Field Description

Bit	Field	Type	Reset	Description
15:4	TLow_Limit[11:0]	R/W	4B0h	12-bit temperature low limit setting. Temperature low limit is represented by a 12-bit, two's complement word with an LSB equal to 62.5m°C. The default setting for this is 75°C.
3:0	Reserved	R	0000b	Reserved

8.4 THigh_Limit Register (address = 03h) [reset = 5000h]

This register is used to configure the high temperature alert limit of the device. The limit is formatted in a 12-bit two's complement format with a LSB equal to 62.5m°C. The default value on start-up is 5000h or 80°C.

Return to Register Map.

Table 8-9. THigh_Limit Register

15	14	13	12	11	10	9	8
THigh_Limit[11:4]							
R/W-50h							
7	6	5	4	3	2	1	0
THigh_Limit[3:0]				Reserved			
R/W-0h				R-0000b			

Table 8-10. THigh_Limit Register Field Description

Bit	Field	Type	Reset	Description
15:4	THigh_Limit[11:0]	R/W	500h	12-bit temperature high limit setting. Temperature high limit is represented by a 12-bit, two's complement word with an LSB equal to 62.5m°C. The default setting for this is 80°C.
3:0	Reserved	R	0000b	Reserved

8.5 Device ID Register (Address = 0Bh) [reset = 113xh]

This read-only register indicates the device ID and revision number.

Return to Register Map.

Table 8-11. Device_ID Register

15	14	13	12	11	10	9	8
DID[11:4]							
R-11h							
7	6	5	4	3	2	1	0
DID[3:0]				Rev[3:0]			
R-3h				R-0h			

Table 8-12. Device_ID Register Field Description

Bit	Field	Type	Reset	Description
15:4	DID[11:0]	R	113h	Indicates the device ID.
3:0	Rev[3:0]	R	0h	Indicates the revision number.

8.6 Unique_ID0 Register (Address = 0Ch) [reset = xxxxh]

This register contains bits 0:15 of the Unique ID for the device. The Unique ID of the device is used for NIST traceability purposes. For the procedure how to read the Unique IDs, please go to Section 7.3.4.

Return to Register Map.

Table 8-13. Unique_ID0 Register

15	14	13	12	11	10	9	8
Unique_ID0[15:8]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID0[7:0]							
R-xxh							

Table 8-14. Unique_ID0 Register Field Description

Bit	Field	Type	Reset	Description
15:0	Unique_ID0[15:0]	R	xxxxh	Bits 15:0 of the device Unique ID

8.7 Unique_ID1 Register (Address = 0Dh) [reset = xxxxh]

This register contains bits 31:16 of the Unique ID for the device. The Unique ID of the device is used for NIST traceability purposes. For the procedure how to read the Unique IDs, please go to Section 7.3.4.

Return to Register Map.

Table 8-15. Unique_ID1 Register

15	14	13	12	11	10	9	8
Unique_ID1[31:24]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID1[23:16]							
R-xxh							

Table 8-16. Unique_ID1 Register Field Description

Bit	Field	Type	Reset	Description
15:0	Unique_ID0[31:16]	R	xxxxh	Bits 31:16 of the device Unique ID

8.8 Unique_ID2 Register (Address = 0Eh) [reset = xxxxh]

This register contains bits 47:32 of the Unique ID for the device. The Unique ID of the device is used for NIST traceability purposes. For the procedure how to read the Unique IDs, please go to Section 7.3.4.

Return to Register Map.

Table 8-17. Unique_ID2 Register

15	14	13	12	11	10	9	8
Unique_ID2[47:40]							
R-xxh							
7	6	5	4	3	2	1	0
Unique_ID2[39:32]							
R-xxh							

Table 8-18. Unique_ID2 Register Field Description

Bit	Field	Type	Reset	Description
15:0	Unique_ID2[47:32]	R	xxxxh	Bits 47:32 of the device Unique ID

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP113 can be operated with a two-wire I²C or SMBus compatible interface and features the ability to operate with a 1.4V to 5.5V bus voltage. The TMP113 features a uniquely small size of 1.5mm × 1mm with a 0.525mm z-height.

9.2 Equal I²C Pullup and Supply Application

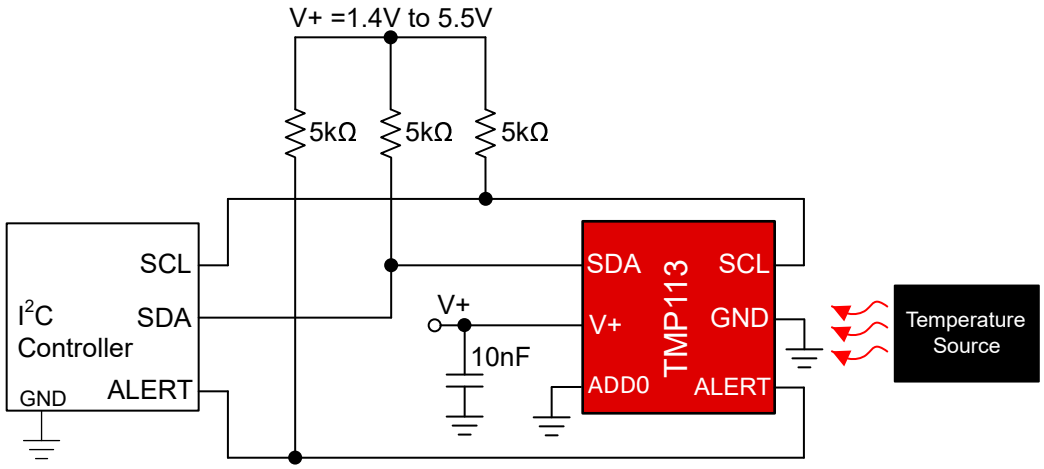


Figure 9-1. Equal I²C Pullup and Supply Voltage Application

9.2.1 Design Requirements

For this design example, use the parameters listed below.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply (V+)	1.4V to 5.5V
SDA, SCL V_{PULLUP}	≥ V+
SDA, SCL R_{PULLUP}	≥ 5kΩ
ALERT R_{PULLUP}	≥ 5kΩ (20kΩ is preferred)

9.2.2 Detailed Design Procedure

The SDA and SCL pin voltage of the TMP113 can be the same as the supply voltage V+. The accuracy of the TMP113 is not affected by the pullup voltage. However, using a minimal SDA and ALERT pins pull-up current is recommended to prevent self-heating and temperature accuracy reduction. In addition, to minimize measurement noise, having communication on the I2C bus during temperature conversion is not recommended.

9.2.3 Application Curve

Figure 9-2 shows the step response of the TMP113 to a submersion in an oil bath of 75ºC from room temperature (25ºC). The time-constant, or the time for the output to reach 63% of the input step, is 0.2s (for flexible PCB) and 1.1s (for rigid PCB). The time-constant result depends on the printed-circuit board (PCB) size

and thickness that the TMP113 is mounted on. For the rigid PCB, the TMP113 is soldered to a two-layer PCB that measured 0.5 inches × 0.5 inches.

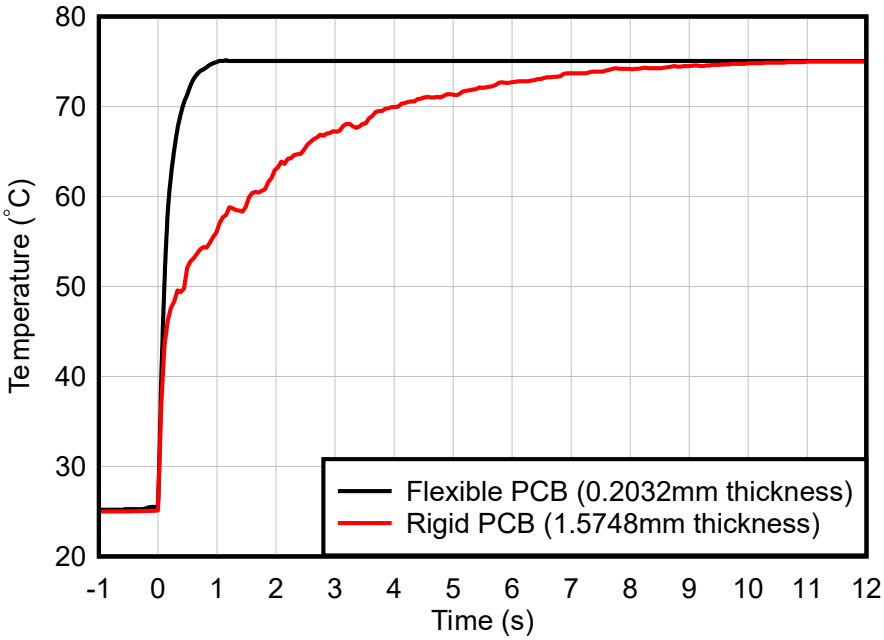


Figure 9-2. Temperature Step Response (TMP113 mounted on flexible and rigid PCBs)

9.3 Power Supply Recommendations

The TMP113 operates with power supply in the range of 1.4V to 5.5V and slew rate as low as 10mV/ms. The device can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

9.4 Layout

9.4.1 Layout Guidelines

The TMP113 is a simple device to layout. Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA, SCL and ALERT) through 5kΩ or 20kΩ pullup resistors.

9.4.2 Layout Example

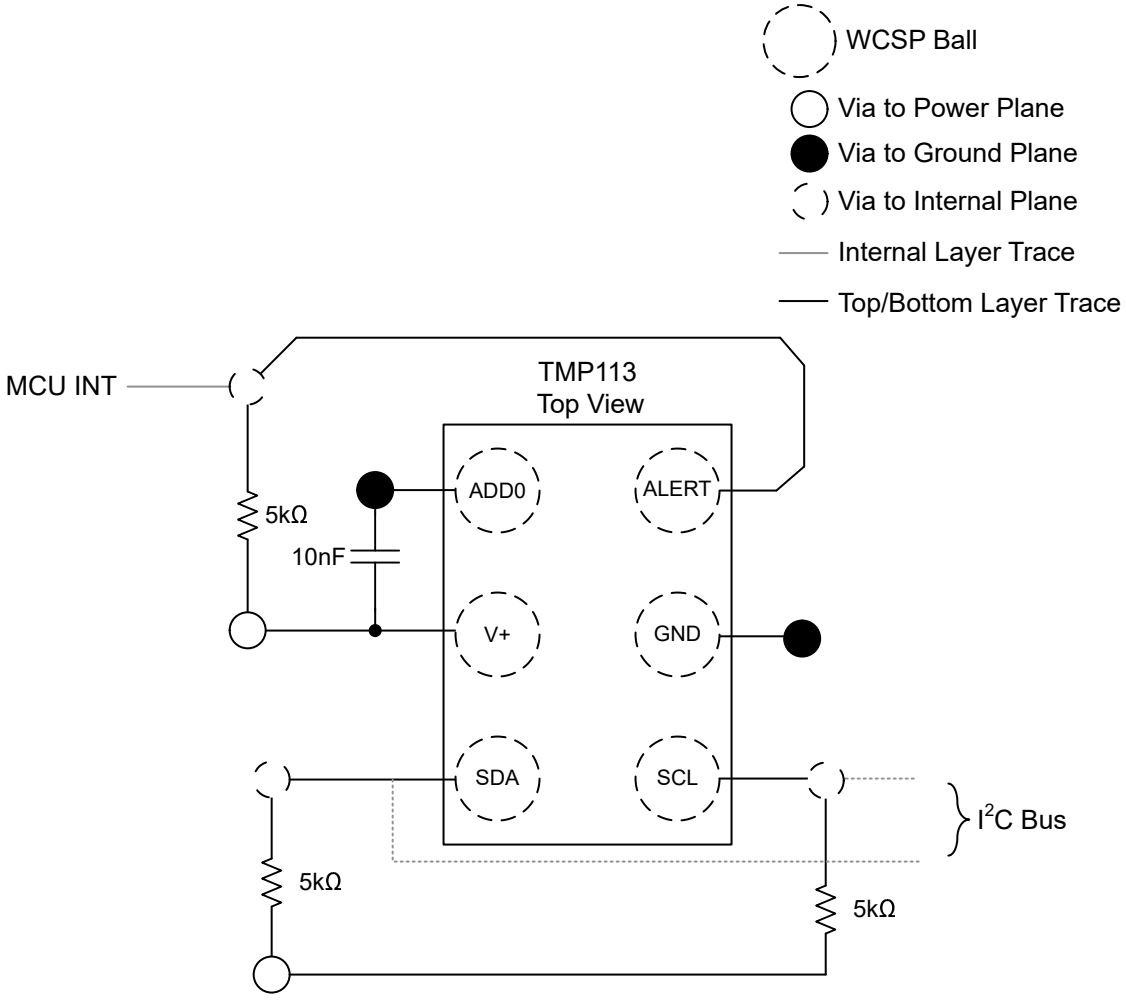


Figure 9-3. Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP102 Low-Power Digital Temperature Sensor With SMBus and Two-Wire Serial Interface in SOT563*, data sheet
- Texas Instruments, *TMP110 Ultra-Small, ±1.0°C Accurate, I2C Digital Temperature Sensor for CostSensitive System*, data sheet
- Texas Instruments, *TMP112x High-Accuracy, Low-Power, Digital Temperature Sensors With SMBus and TwoWire Serial Interface in SOT563*, data sheet
- Texas Instruments, *TMP113 Evaluation Module*, EVM

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

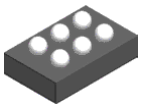
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

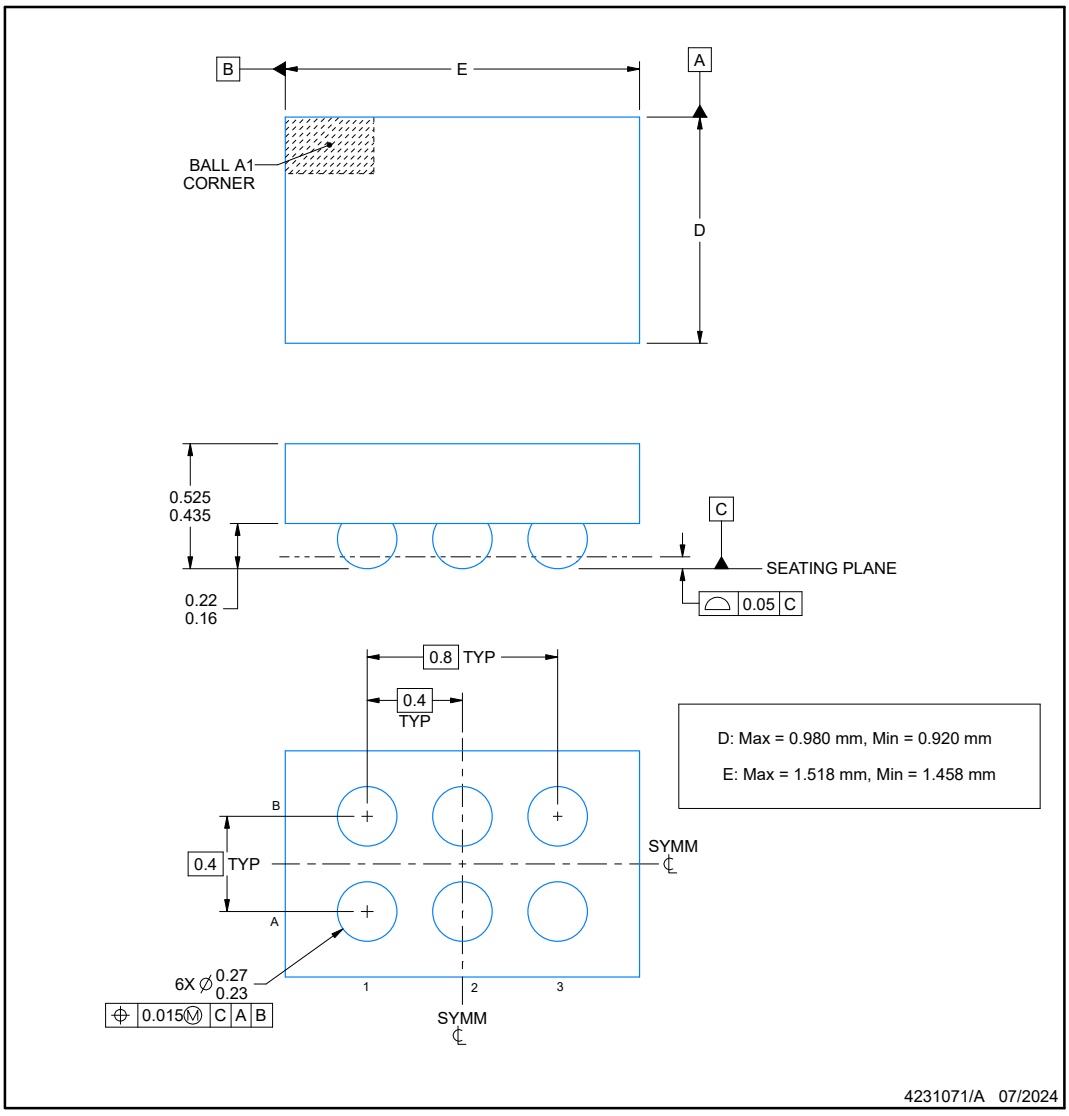
YBG0006-C04



PACKAGE OUTLINE

DSBGA - 0.525 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

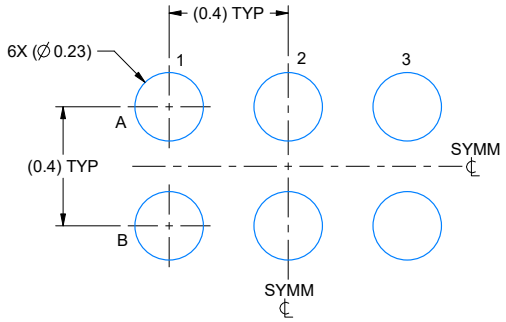
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

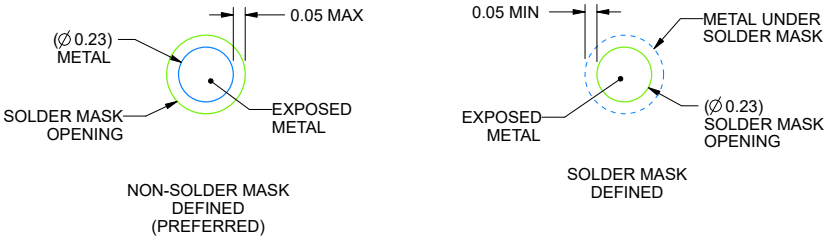
YBG0006-C04

DSBGA - 0.525 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4231071/A 07/2024

NOTES: (continued)

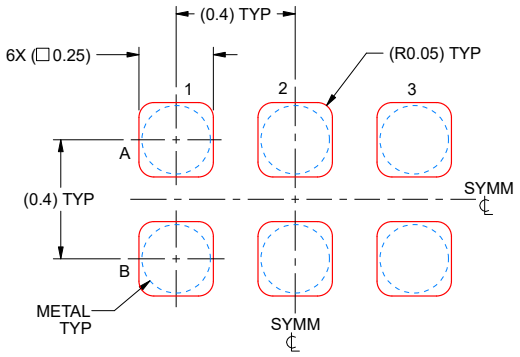
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0006-C04

DSBGA - 0.525 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4231071/A 07/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TMP113AIYBGR	PRE_PROD	DSBGA	YBG	6	3000	RoHS & Green	SnAgCu	Level-1-260C-UNLIM	-40 to 125	QU

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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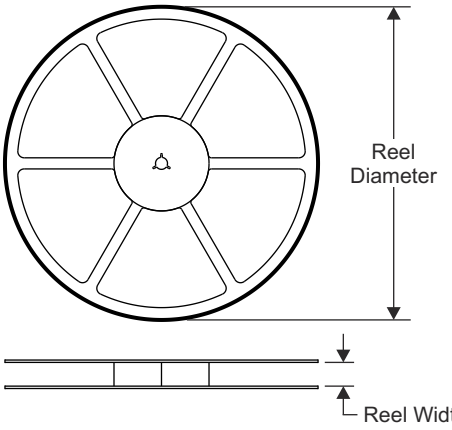
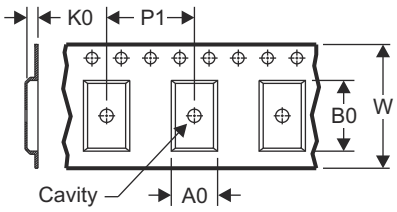
12.2 Tape and Reel Information

REEL DIMENSIONS

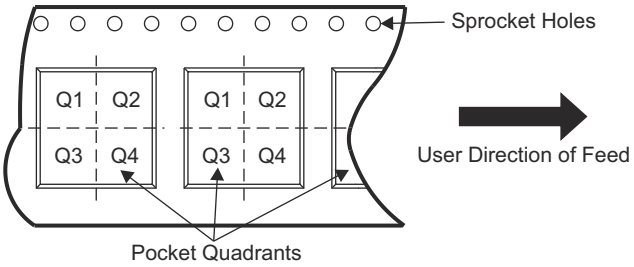


TAPE DIMENSIONS



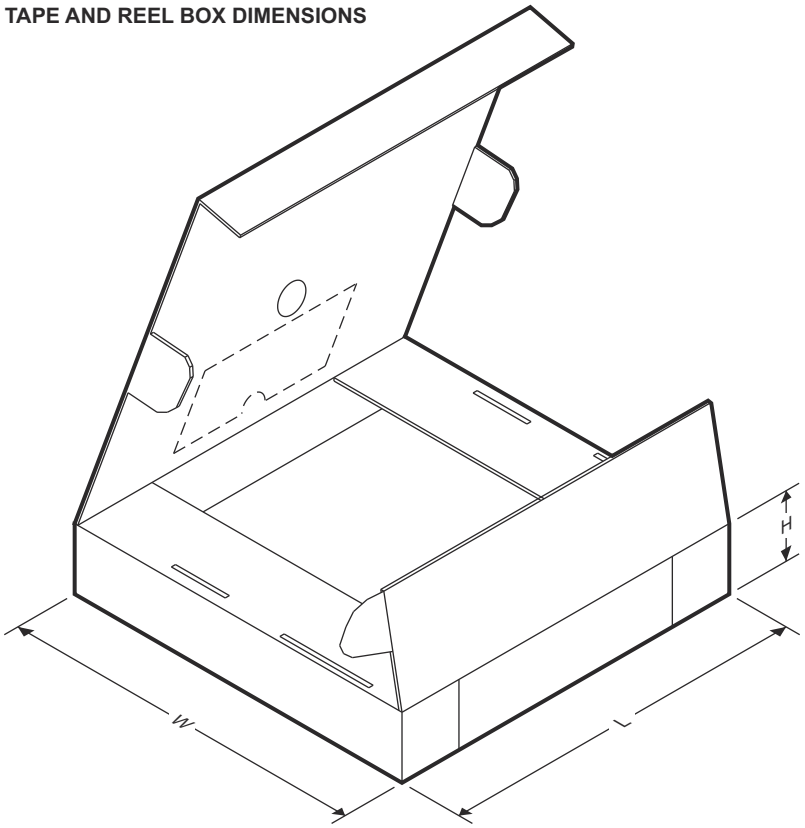
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP113AIYBGR	DSBGA	YBG	6		180	8.4	1.14	1.64	.59	4	8	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP113AIYBGR	DSBGA	YBG	6		182	182	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP113AIYBGR	ACTIVE	DSBGA	YBG	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	QU	Samples

(1) The marketing status values are defined as follows:
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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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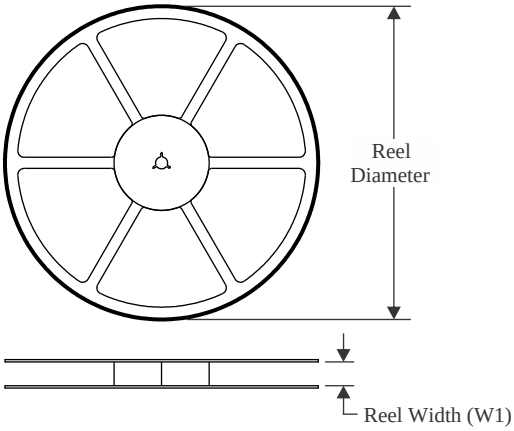
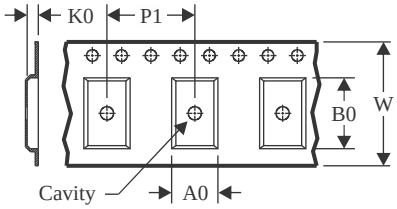
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
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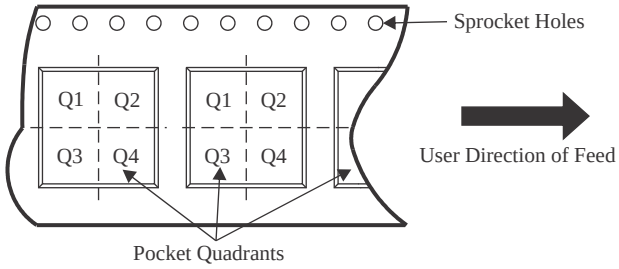
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

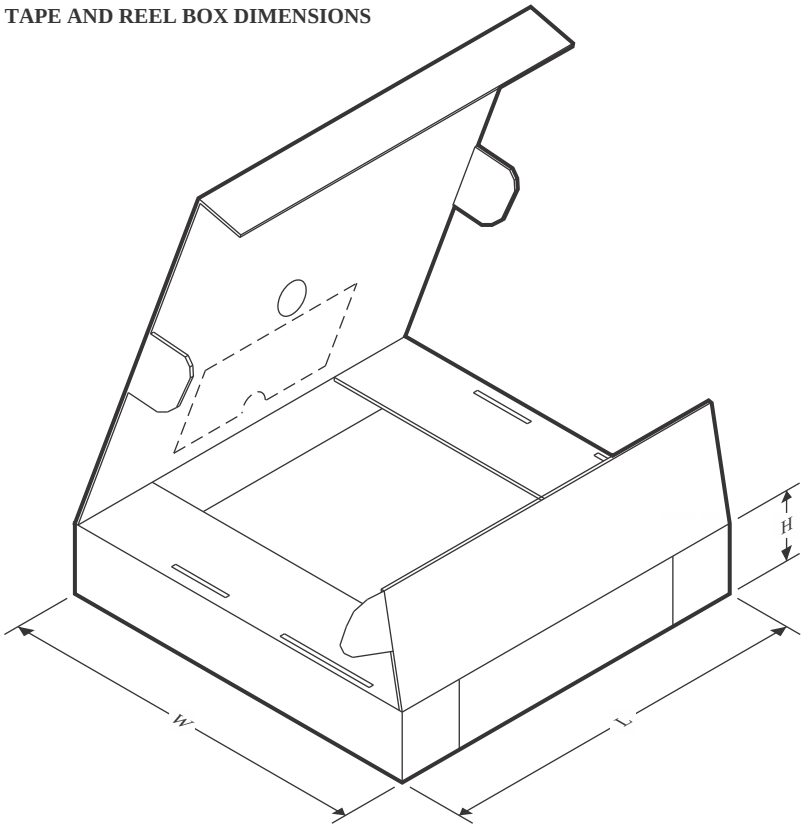
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP113AIYBGR	DSBGA	YBG	6	3000	180.0	8.4	1.14	1.64	0.59	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP113AIYBGR	DSBGA	YBG	6	3000	182.0	182.0	20.0

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