

TLV770 50mA, Small-Size, High-PSRR, Low-Dropout Regulator

1 Features

- High PSRR: 55dB (1MHz)
- V_{IN} range: 1.4V to 5.5V
- Fixed output voltage range: 0.6V to 3.3V
- Output voltage accuracy: 2%
- Low dropout voltage:
 - 45mV at 50mA ($3.3V_{OUT}$)
- Active output pulldown resistor
- Packages:
 - 1mm × 1mm, 4-pin X2SON (DQN)
 - 5-pin SOT-23 (DBV)

2 Applications

- [Smartphones](#)
- [Tablets](#)
- [Gaming consoles](#)
- [Notebooks](#)
- [Streaming media players](#)
- [Set-top boxes](#)
- [Camera modules](#)

3 Description

The TLV770 is a small, low-dropout (LDO) linear regulator that sources 50mA of output current. This LDO is designed to provide a voltage source with high PSRR. The device also provides load and line transient performance that meets the requirements of a variety of circuits. With a 1.4V to 5.5V input voltage range and a 0.6V to 3.3V output voltage range, the TLV770 is flexible enough to support multiple applications.

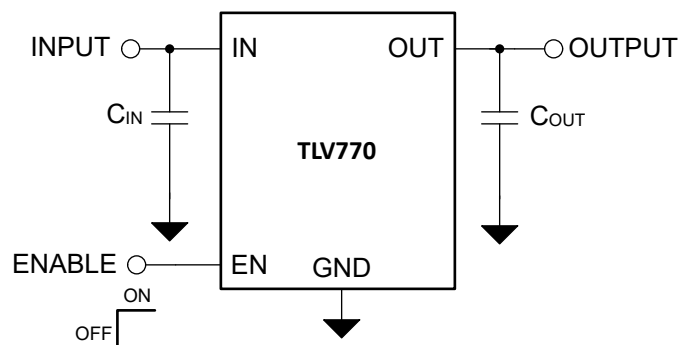
The TLV770 features an internal soft-start circuit to avoid excessive inrush current, thus minimizing the input voltage drop during start-up. An active pulldown circuit quickly discharges the output when the LDO is disabled and provides a known start-up state. The EN input allows an external logic signal to enable or disable the regulated output. The LDO is stable with small ceramic capacitors, allowing for a small overall package size. The operating junction temperature range is from -40°C to $+125^{\circ}\text{C}$. This LDO is available in standard SOT-23 (DBV) and 1mm × 1mm X2SON (DQN) packages.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TLV770	DQN (X2SON, 4)	1mm × 1mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



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4 Pin Configuration and Functions

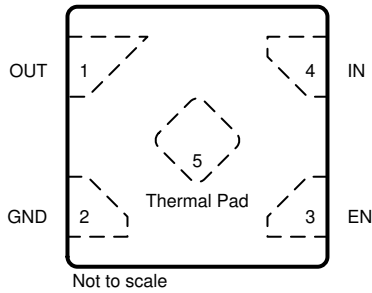


Figure 4-1. DQN Package, 1mm × 1mm, 4-Pin X2SON (Top View)

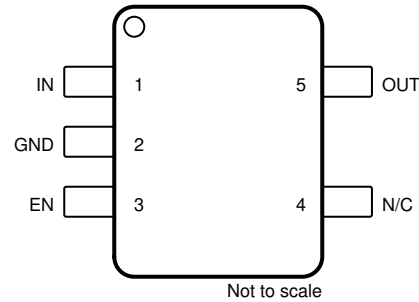


Figure 4-2. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	X2SON	SOT-23		
EN	3	3	I	Enable input. A low voltage ($< V_{EN(Low)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(Hi)}$) on this pin enables the regulator output.
GND	2	2	G	Common ground.
IN	4	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground; see Section 5.3 . Place the input capacitor as close to the IN and GND pins of the device as possible.
N/C	—	4	—	No internal electrical connection. Connect to GND for improved thermal performance.
OUT	1	5	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor, as listed in Section 5.3 . Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{EN(Low)}$).
Thermal Pad	5	—	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

(1) I = input, O = output, I/O = input or output, and G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	-0.3	6.5	V
	Output, V_{OUT}	-0.3	6.0 or $V_{IN} + 0.3$ ⁽²⁾	
	Enable, V_{EN}	-0.3	6.5	
Current	Maximum output, I_{OUT} ⁽⁴⁾	Internally limited		A
Temperature	Operating junction, T_J	-55	150	°C
	Storage, T_{stg}	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The maximum value of V_{OUT} is the lesser of 6.0V or $(V_{IN} + 0.3V)$.
- (3) All voltages are with respect to the GND pin.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.4		5.5	V
V_{EN}	Enable input voltage	0		5.5	V
V_{OUT}	Nominal output voltage range	0.6		3.3	V
I_{OUT}	Output current	0		50	mA
C_{IN}	Input capacitor ⁽²⁾		1		μF
C_{OUT}	Output capacitance ⁽³⁾	0.47		40	μF
ESR	Output capacitor effective series resistance			100	mΩ
T_J	Operating junction temperature	-40		125	°C

- (1) All voltages are with respect to GND.
- (2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47μF minimum is recommended to counteract the effect of source resistance and inductance, which in some cases causes symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients. If needed use a larger input capacitance, depending on the characteristics of the input voltage source.
- (3) Effective output capacitance of 0.47μF minimum and 40μF maximum is required for stability. The effective output capacitance accounts for tolerance, temperature, voltage, and any other factors that affect the value, and is often 50% smaller than the capacitors specified value.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV770		UNIT
		DBV (SOT-23)	DQN (X2SON)	
		5 PINS	4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	242.5	236.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	140.9	218.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	109.4	180.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	76.1	16.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	108.8	179.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	157.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [yes](#) application note.

5.5 Electrical Characteristics

specifications apply for T_J = 25°C, V_{IN} = V_{OUT(NOM)} + 0.5V or 1.4V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 1μF, and C_{OUT} = 1μF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV _{OUT}	Output voltage tolerance	T _J = -40°C to 85°C	1.2V ≤ V _{OUT} < 1.8V	-2.5		2.5	%
			1.8V ≤ V _{OUT} ≤ 3.3V	-2		2	
			1.2V ≤ V _{OUT} < 1.8V	-3		3	
			1.8V ≤ V _{OUT} < 2.5V	-2.75		2.75	
			2.5V ≤ V _{OUT} ≤ 3.3V	-2.5		2.5	
ΔV _{OUT}	Line regulation	V _{IN} = (V _{OUT(NOM)} + 0.5V) to 5.5V		0.01		0.1	%/V
ΔV _{OUT}	Load regulation	I _{OUT} = 1mA to 50mA		85		110	μV/mA
I _{GND}	Quiescent ground current	V _{EN} = V _{IN} = 5.5V, I _{OUT} = 0mA, T _J = -40°C to 85°C		80		120	μA
I _{SHDN}	Shutdown ground current	V _{EN} < V _{EN(LOW)} , V _{IN} = 5.5V, T _J = -40°C to 85°C		0.01		2	μA
V _{DO}	Dropout voltage	I _{OUT} = 50mA, V _{IN} = 95% × V _{OUT(NOM)}	1.2V ≤ V _{OUT} < 1.8V ^{(1) (2)}			220	mV
			1.8V ≤ V _{OUT} < 2.5V			60	
			2.5V ≤ V _{OUT} ≤ 3.3V			45	
		I _{OUT} = 50mA, V _{IN} = 95% × V _{OUT(NOM)} , T _J = -40°C to 85°C	1.2V ≤ V _{OUT} < 1.8V ^{(1) (2)}			230	
			1.8V ≤ V _{OUT} < 2.5V			65	
			2.5V ≤ V _{OUT} ≤ 3.3V			50	
I _{CL}	Output current limit	V _{OUT} = 0.9 × V _{OUT(NOM)} , T _J = -40°C to 85°C		80		210	mA
PSRR	Power-supply rejection ratio	I _{OUT} = 50mA, V _{IN} = V _{OUT} + 1.0V	f = 100kHz		56		dB
			f = 1MHz		55		
V _N	Output noise voltage	BW = 10Hz to 100kHz, V _{OUT} = 1.2V, I _{OUT} = 50mA			90		μV _{RMS}
R _{PULLDOWN}	Output automatic discharge pulldown resistance	V _{EN} < V _{EN(LOW)} (output disabled), V _{IN} = 3.3V			135		Ω
T _{SD}	Thermal shutdown	T _J rising			160		°C
		T _J falling			140		
V _{EN(LOW)}	Low input threshold	V _{EN} falling until the output is disabled, T _J = -40°C to 85°C				0.3	V
V _{EN(HI)}	High input threshold	V _{EN} rising until the output is enabled, T _J = -40°C to 85°C		0.9			V
I _{EN}	EN input leakage current	V _{EN} = 5.5V and V _{IN} = 5.5V			0.01		1 μA

(1) For V_{OUT} < 1.5V, dropout is tested with V_{IN} = 1.4V.

(2) For V_{OUT} = 0.6V, Dropout voltage < Headroom voltage. At V_{IN} = 1.4V, a 0.6V output device will not be in dropout. Headroom voltage = V_{IN} - V_{OUT}.

5.6 Switching Characteristics

specifications apply for $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$ or 1.4V , whichever is greater, $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 1\mu\text{F}$, and $C_{OUT} = 1\mu\text{F}$ (unless otherwise noted); all typical values are at $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time (V_{EN})	From $V_{EN} > V_{EN(HI)}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$; V_{IN} rise time = $1\text{V}/\mu\text{s}$		320		μs

5.7 Typical Characteristics

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$, $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\mu\text{F}$ (unless otherwise noted)

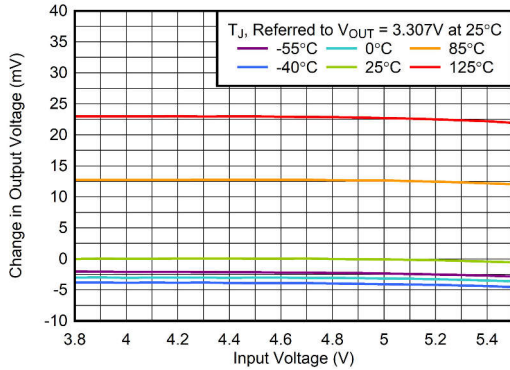


Figure 5-1. Line Regulation vs V_{IN}

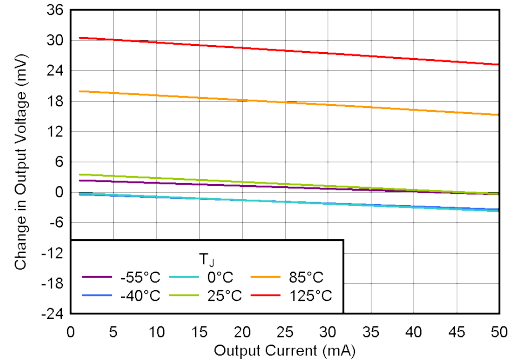


Figure 5-2. Load Regulation vs I_{OUT}

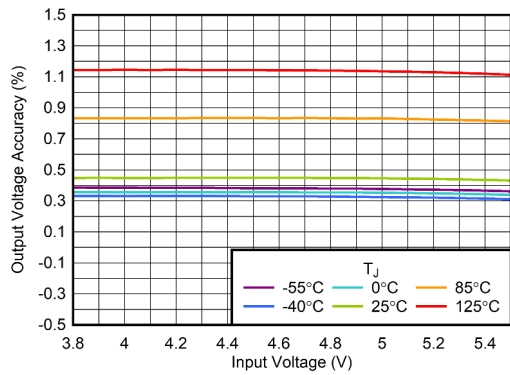


Figure 5-3. Output Voltage Accuracy vs V_{IN}

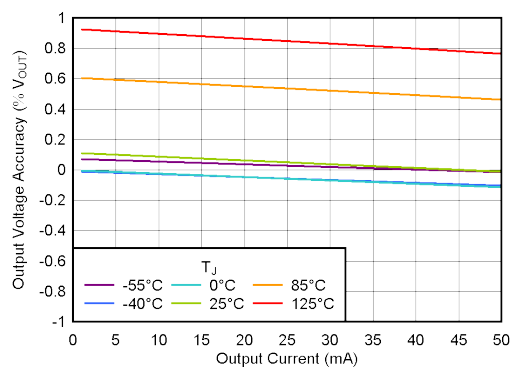


Figure 5-4. Output Voltage Accuracy vs I_{OUT}

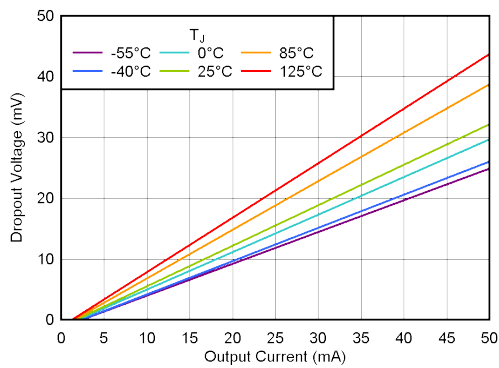


Figure 5-5. Dropout Voltage vs I_{OUT}

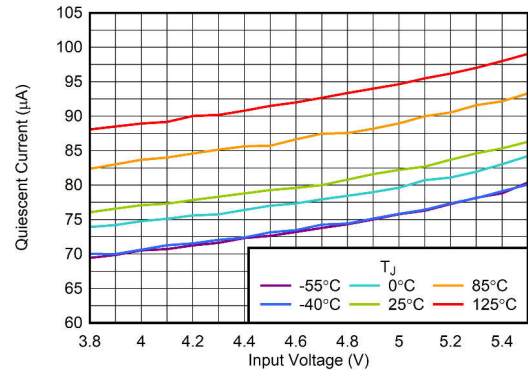


Figure 5-6. Quiescent Current vs V_{IN}

5.7 Typical Characteristics (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$, $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\mu\text{F}$ (unless otherwise noted)

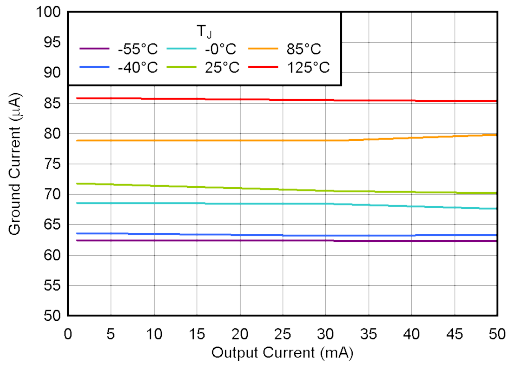


Figure 5-7. Ground Current vs I_{OUT}

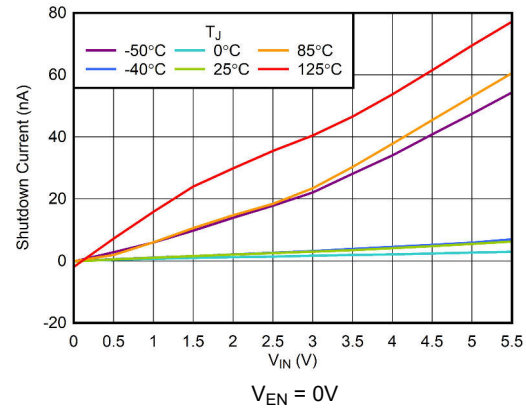


Figure 5-8. Shutdown Current vs V_{IN}
 $V_{EN} = 0\text{V}$

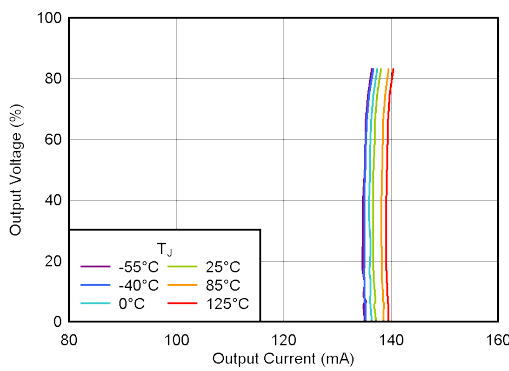


Figure 5-9. Current Limit

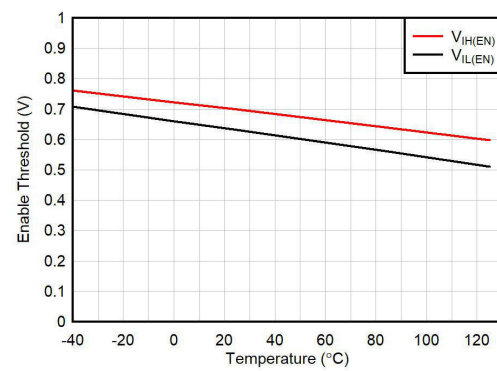
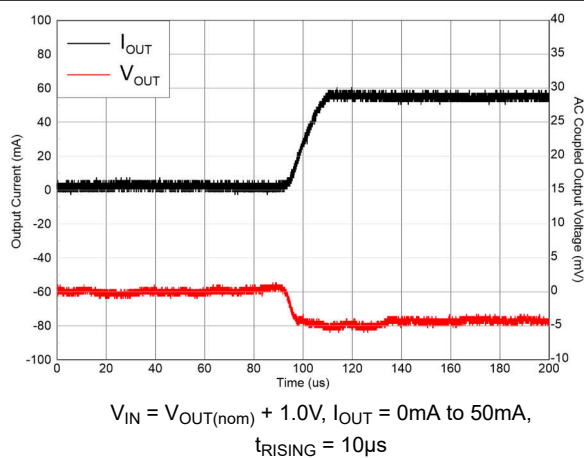
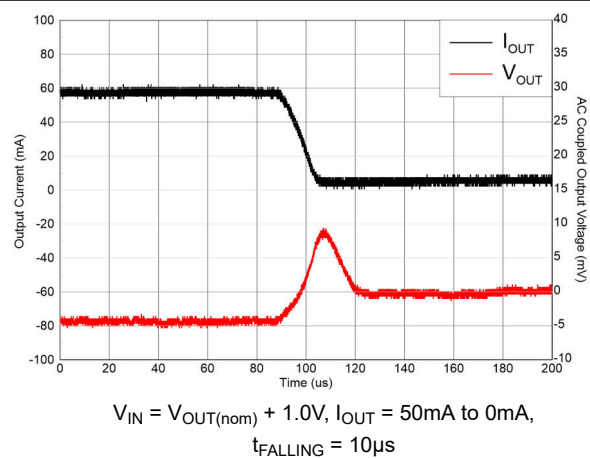


Figure 5-10. Enable Logic Threshold vs Temperature



$V_{IN} = V_{OUT(nom)} + 1.0\text{V}$, $I_{OUT} = 0\text{mA to } 50\text{mA}$,
 $t_{RISING} = 10\mu\text{s}$

Figure 5-11. Load Transient

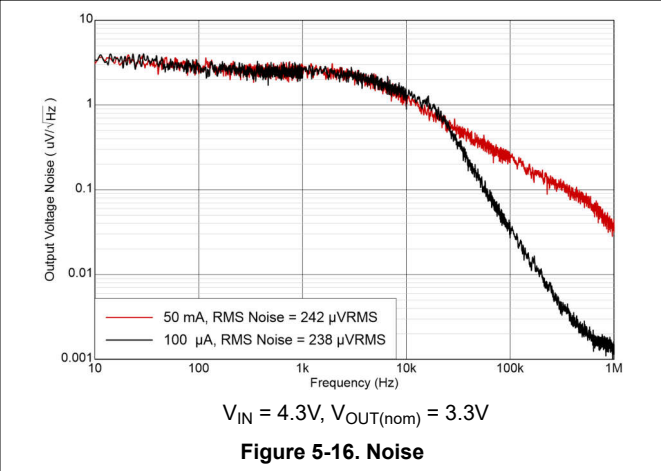
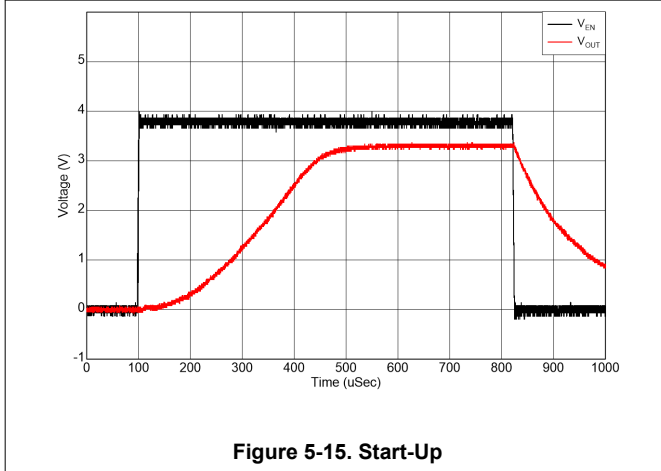
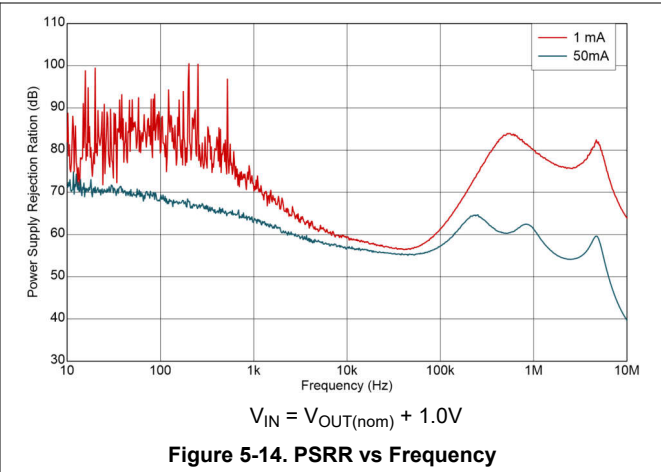
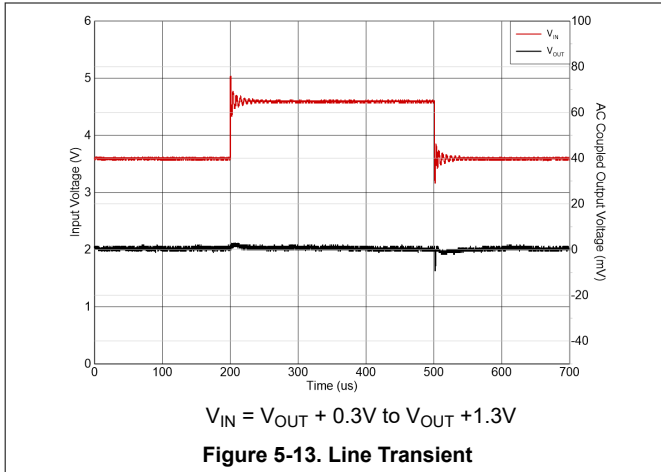


$V_{IN} = V_{OUT(nom)} + 1.0\text{V}$, $I_{OUT} = 50\text{mA to } 0\text{mA}$,
 $t_{FALLING} = 10\mu\text{s}$

Figure 5-12. Load Transient

5.7 Typical Characteristics (continued)

at operating temperature $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{NOM})} + 0.5\text{V}$, $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1\mu\text{F}$ (unless otherwise noted)



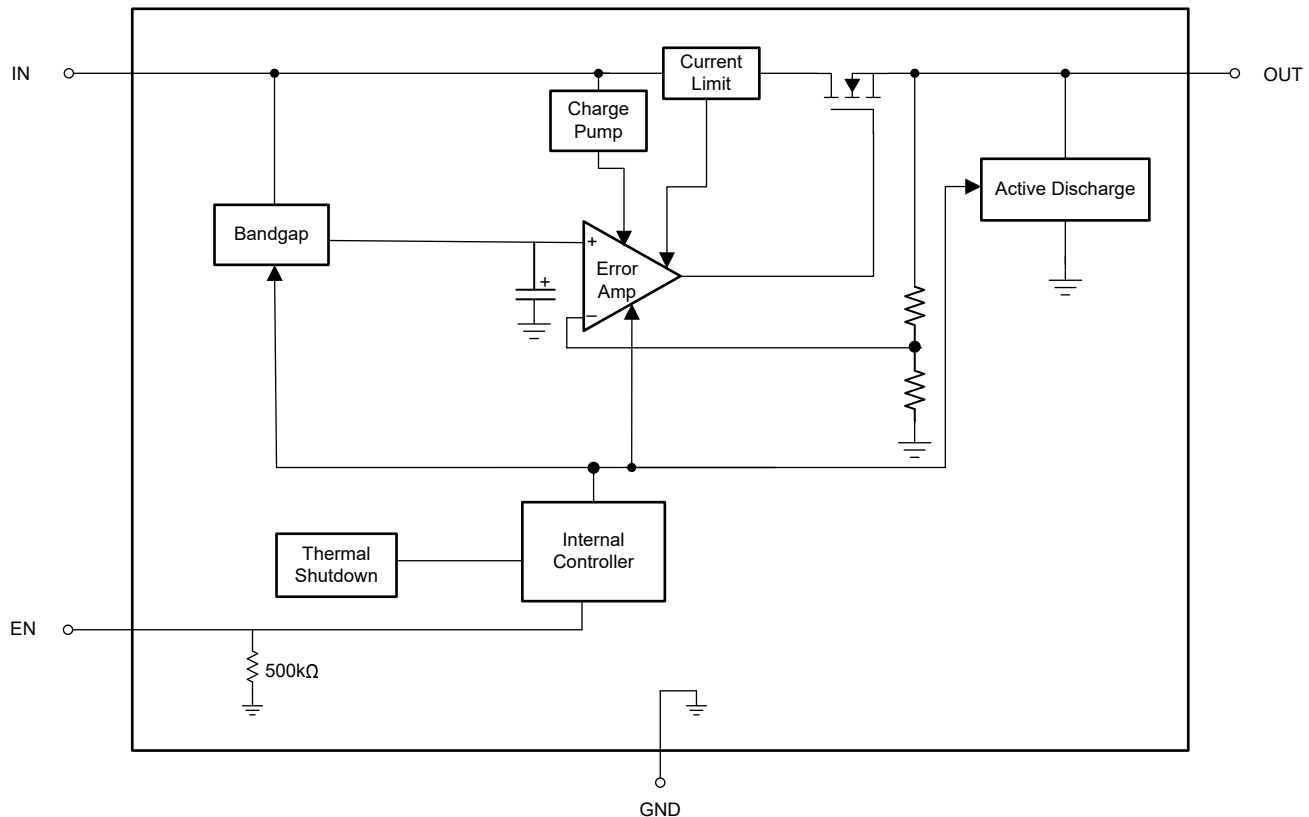
6 Detailed Description

6.1 Overview

The TLV770 provides high PSRR and good transient response in a small, 50mA LDO.

This LDO is designed to operate with a single 1µF input capacitor and a single 1µF ceramic output capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} - V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the [Recommended Operating Conditions](#) table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.2 Active Discharge

The regulator has an internal MOSFET that connects a pulldown resistor between the output and ground when the device is disabled. This connection actively discharges the output voltage. The active discharge circuit is activated by the enable pin or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses. Reverse current flow from the output to the input potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.3 Brick-Wall Current Limit

The device has an internal current limit circuit that protects the device during overcurrent or shorting conditions. The current-limit circuit, as shown in Figure 6-1, is a brick-wall scheme. When the device is in current limit, the device sources the output current limit (I_{CL}) and the output voltage is unregulated. In this scenario, the output voltage depends on the load impedance.

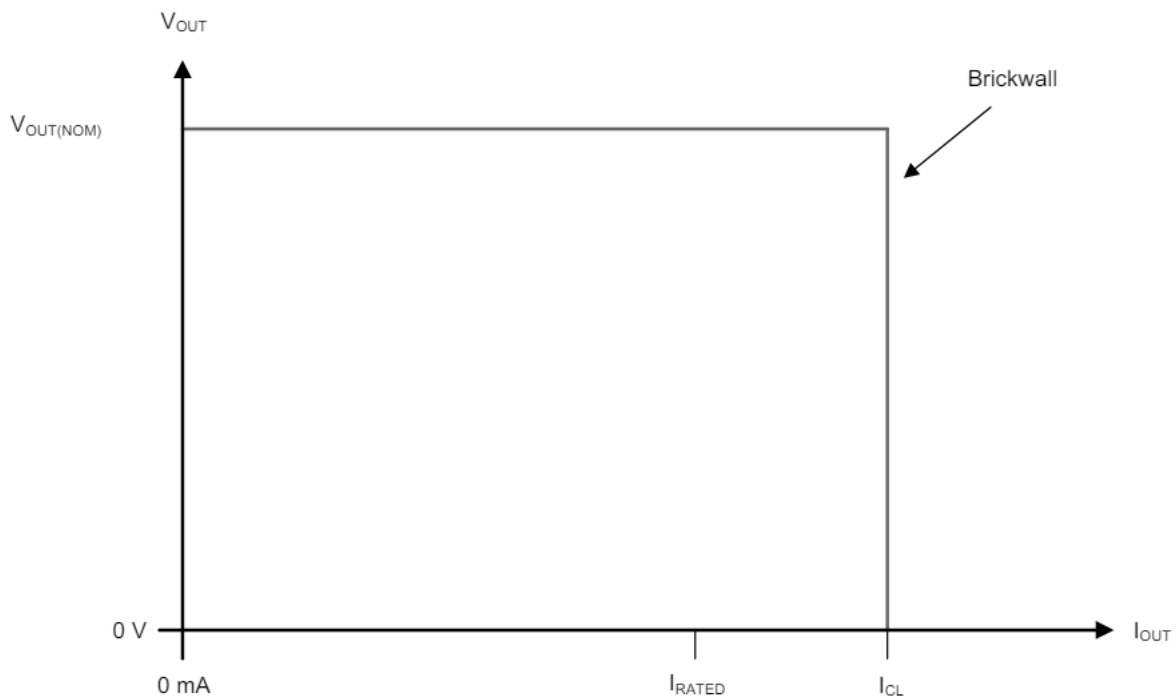


Figure 6-1. Brick-Wall Current Limit Scheme

During a current-limit event, the potential for high power dissipation exists because of the elevated current level and increased input-to-output differential voltage ($V_{IN} - V_{OUT}$). If the device heats enough, the device enters thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device reenters thermal shutdown. This cycle continues until the current-limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the [Recommended Operating Conditions](#) table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

6.4.3 Disabled

Shutdown the device output by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the [Electrical Characteristics](#) table). When disabled, the pass transistor turns off and internal circuits shut down. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the [Recommended Operating Conditions](#) table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. For typical operation of the TLV770, connect a 1μF capacitor to the input. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the [Recommended Operating Conditions](#) table for stability. Make sure that the minimum derated output capacitance is equal to or greater than 0.47μF. When the output voltage is ramping up, the inrush current depends on the size of the output capacitance. During start-up, the output current is potentially as high as the current limit value for larger output capacitors.

7.2 Typical Application

7.2.1 Application

Figure 7-1 shows a typical application circuit for the TLV770.

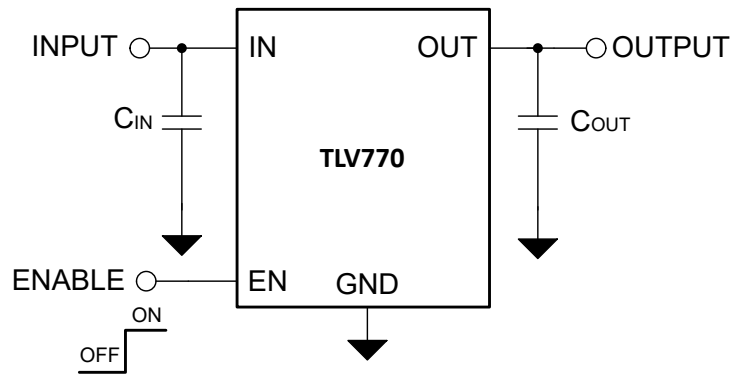


Figure 7-1. TLV770 Typical Application

7.2.2 Design Requirements

Table 7-1 summarizes the design requirements for Figure 7-1.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.0V \pm 5%
Output voltage	3.3V
Output current	50mA
Maximum ambient temperature	125°C

7.2.3 Detailed Design Procedure

For this design example, the 3.3V output version (TLV77033) is selected. A nominal 4.0V input supply is assumed. Use a minimum 1 μ F input capacitor to minimize the effect of resistance and inductance between the 4.0V source and LDO input. Use a minimum 0.47 μ F output capacitance for stability and good load transient response. The dropout voltage (V_{DO}) is less than 50mV maximum at a 3.3V output voltage and 50mA output current. There are no dropout issues with a minimum 3.8V input voltage (4.0V – 5%) and a maximum 50mA output current.

7.2.4 Application Curves

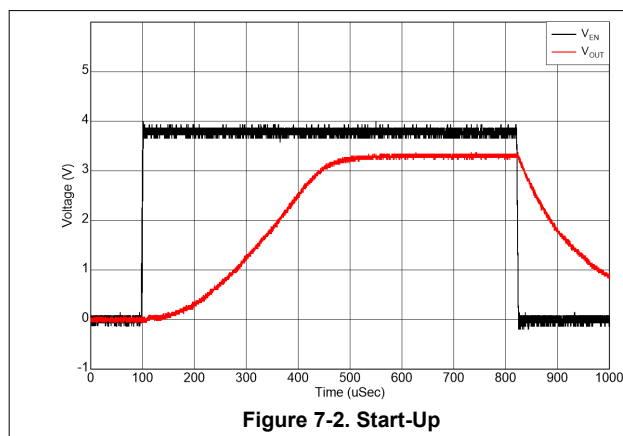


Figure 7-2. Start-Up

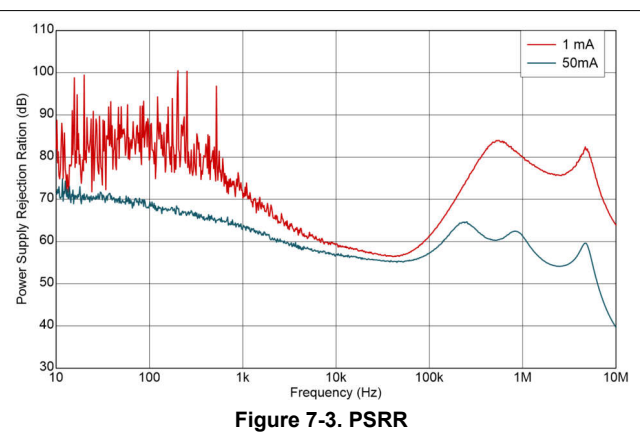


Figure 7-3. PSRR

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4V to 5.5V. Make sure input supply is well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is optimum, set the input supply to at least $V_{OUT(nom)} + 0.5V$ or 1.4V, whichever is greater.

Use a 1 μ F or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via wicks solder or solder paste away from the thermal pad joint during the soldering process. Thus, leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Examples

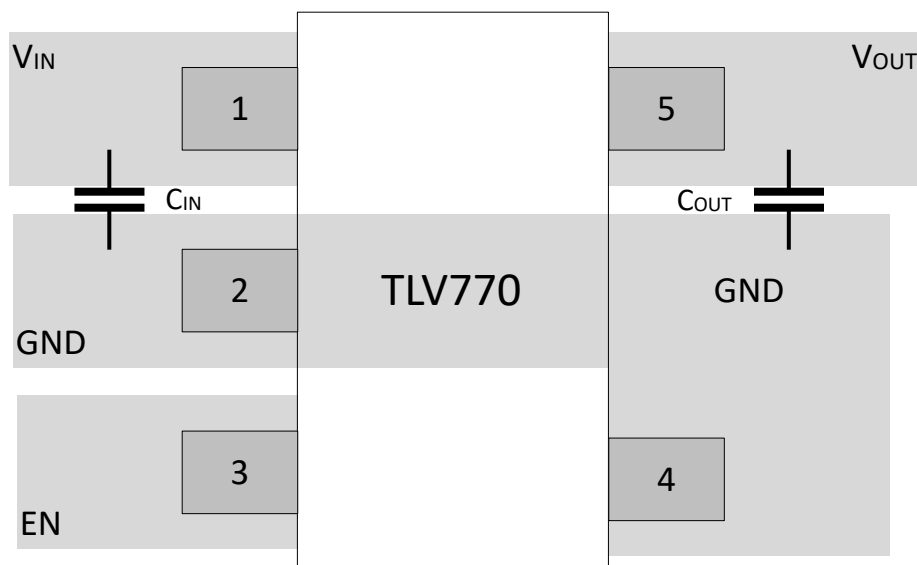


Figure 7-4. DBV Package (SOT-23) Typical Layout

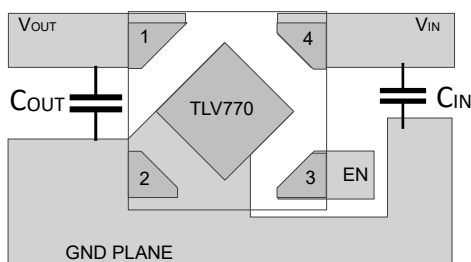


Figure 7-5. DQN Package (X2SON) Typical Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT ⁽¹⁾	DESCRIPTION
TLV770xx(x)Pyyyz	<p>xx(x) is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number. Otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V).</p> <p>P indicates an active output discharge feature.</p> <p>yyy is the package designator.</p> <p>z is the package quantity. R is for reel (3000 pieces).</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Know Your Limits application note](#)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.5 Trademarks

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV77012PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3F5F	Samples
TLV77012PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PG	Samples
TLV77018PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3F6F	Samples
TLV77018PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PH	Samples
TLV77025PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3F7F	Samples
TLV77025PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PI	Samples
TLV77028PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3F8F	Samples
TLV77028PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJ	Samples
TLV77033PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3F9F	Samples
TLV77033PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PK	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV77012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV77012PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV77018PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV77025PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77028PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV77028PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV77033PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV77033PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV77012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV77012PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV77018PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV77025PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77028PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV77028PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV77033PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV77033PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

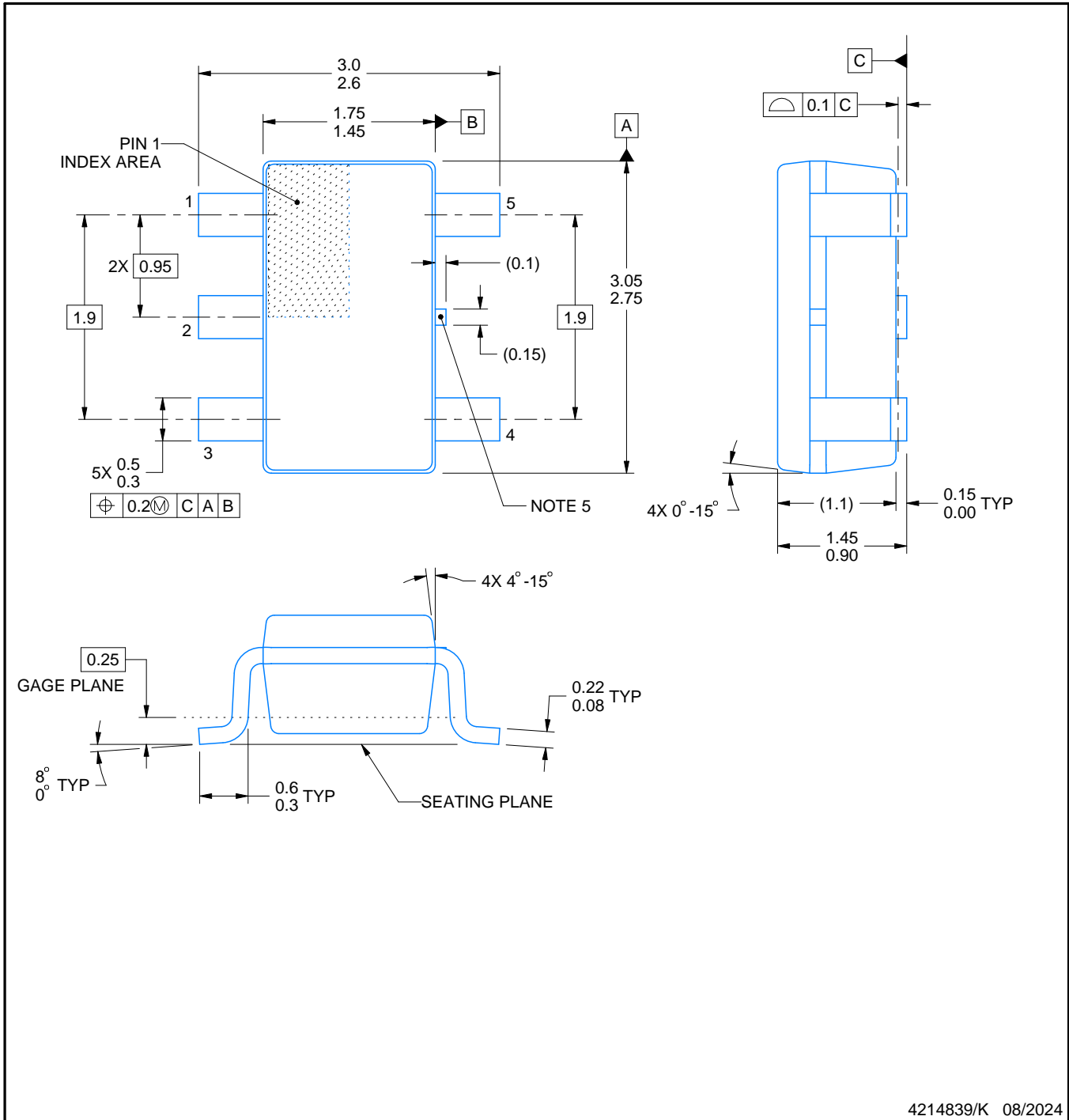
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4

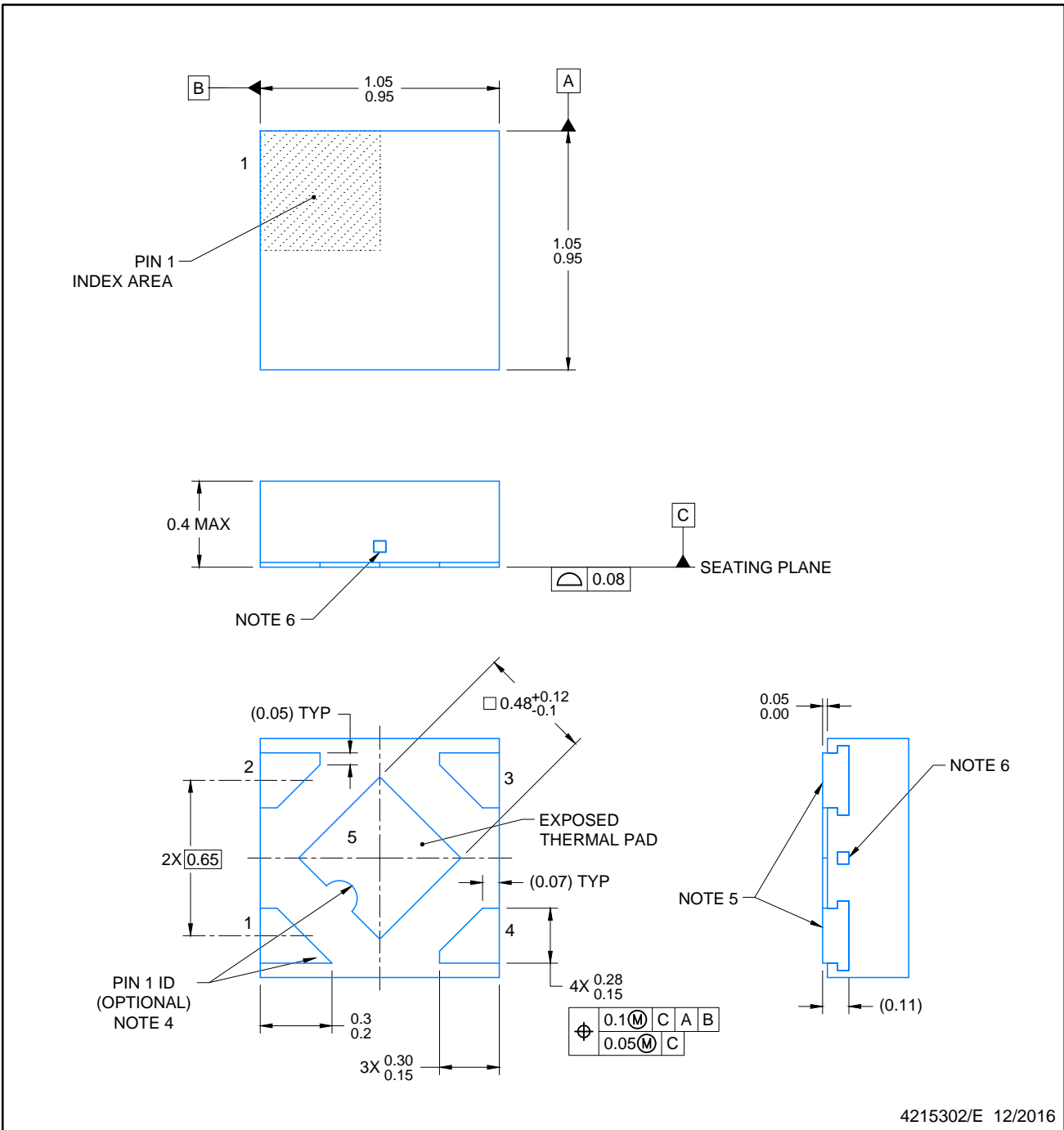
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



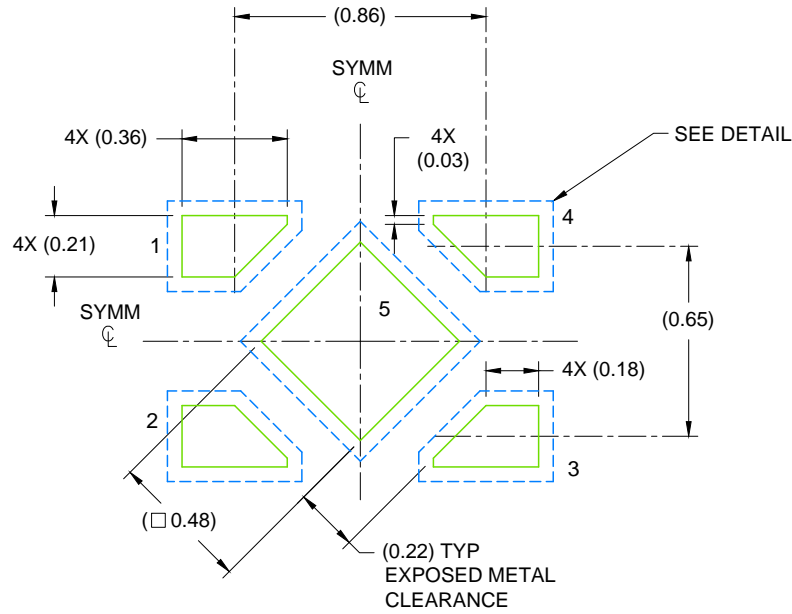
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4210367/F

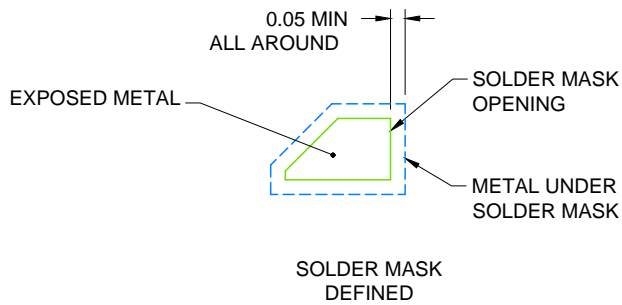


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

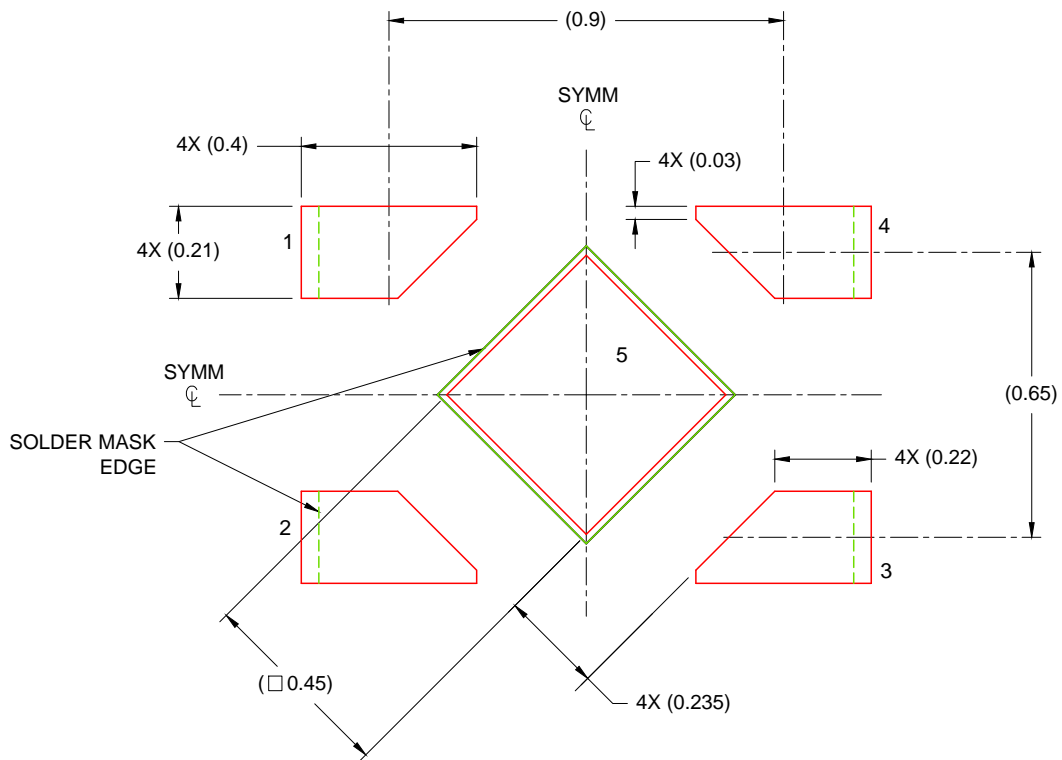


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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