TLV61220A Low-Input Voltage Step-Up Converter in Thin SOT-23 Package

1 Features

- Up to 95% Efficiency at Typical Operating Conditions
- 5.5µA Quiescent Current
- Startup Into Load at 0.7-V Input Voltage
- Operating Input Voltage from 0.7V to 5.5V
- Pass-Through Function during Shutdown
- Minimum Switching Current 200mA
- Protections:
  - Output Overvoltage
  - Overtemperature
  - Input Undervoltage Lockout
- Adjustable Output Voltage from 1.8V to 5.5V
- Small 6-pin Thin SOT-23 Package

2 Applications

- Battery Powered Applications
  - 1 to 3 Cell Alkaline, NiCd or NiMH
  - 1 Cell Li-Ion or Li-Primary
- Solar or Fuel Cell Powered Applications
- Consumer and Portable Medical Products
- Personal Care Products
- White or Status LEDs
- Smartphones

3 Description

The TLV61220A device provides a power-supply solution for products powered by either a single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. Possible output currents depend on the input-to-output voltage ratio. The boost converter is based on a hysteretic controller topology using synchronous rectification to obtain maximum efficiency at minimal quiescent currents. The output voltage of the adjustable version can be programmed by an external resistor divider, or is set internally to a fixed output voltage. The converter can be switched off by a featured enable pin. While being switched off, battery drain is minimized. The device is packaged in a 6-pin thin SOT-23 package (DBV).

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV61220A	SOT (6)	2.90mm x 1.60mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

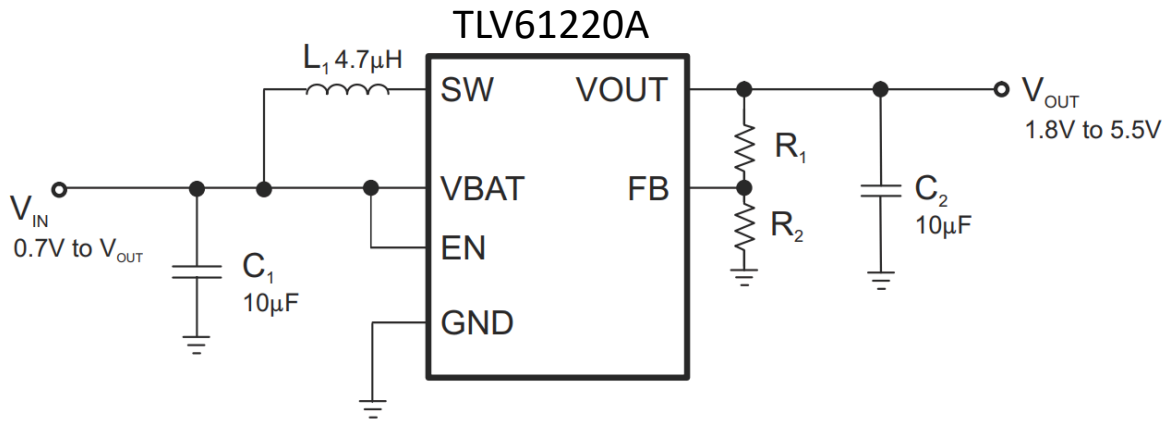


Figure 3-1. Typical application

Table of Contents

4 Device Comparison

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE	PART NUMBER
–40°C to 85°C	Adjustable	6-Pin SOT-23	TLV61220ADBV

5 Pin Configuration and Functions

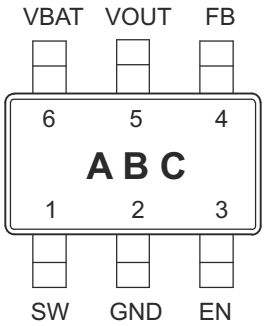


Figure 5-1. DBV Package 6 Pins Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable input (VBAT enabled, GND disabled)
FB	4	I	Voltage feedback for programming the output voltage
GND	2	—	IC ground connection for logic and power
SW	1	I	Boost and rectifying switch input
VBAT	6	I	Supply voltage
VOUT	5	O	Boost converter output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage on VBAT, SW, VOUT, EN, FB	–0.3	7.5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage at VIN	0.7		5.5	V
T_A	Operating free air temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV61220A DBV 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.3	
ψ_{JT}	Junction-to-top characterization parameter	22.9	
ψ_{JB}	Junction-to-board characterization parameter	30.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

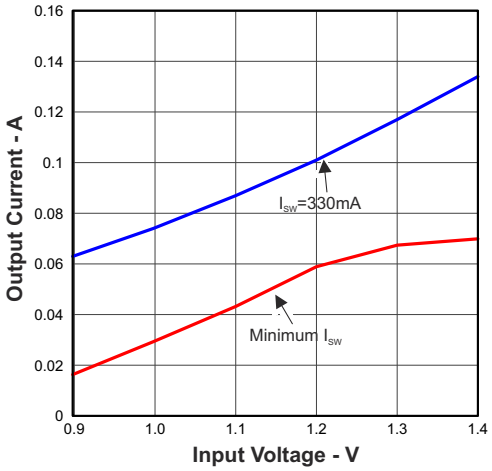
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

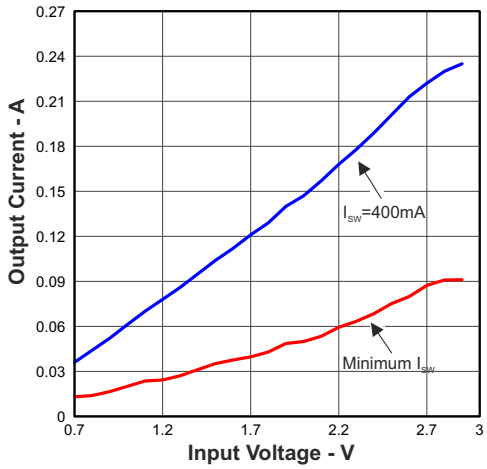
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			0.7		5.5	V
V_{IN}	Minimum input voltage at startup		R_{Load} ≥ 150Ω			0.7	V
V_{OUT}	TLV61220A output voltage range		V_{IN} < V_{OUT}	1.8		5.5	V
V_{FB}	TLV61220A feedback voltage			483	500	513	mV
I_{LH}	Inductor current ripple				200		mA
I_{SW}	switch current limit		V_{OUT} = 3.3V, V_{IN} = 1.2V, T_A = 25 °C	220	400		mA
			V_{OUT} = 3.3 V, T_A = -40°C to 85 °C	180	400		mA
			V_{OUT} = 3.3 V, T_A = 0°C to 85 °C	200	400		mA
$R_{DS(on)}$	Rectifying switch on resistance, HSD		V_{OUT} = 3.3V		1000		mΩ
			V_{OUT} = 5 V		700		mΩ
	Main switch on resistance, LSD		V_{OUT} = 3.3V		600		mΩ
			V_{OUT} = 5V		550		mΩ
	Line regulation		V_{IN} < V_{OUT}		0.5%		
	Load regulation		V_{IN} < V_{OUT}		0.5%		
I_Q	Quiescent current	V_{IN}	I_O = 0mA, V_{EN} = V_{IN} = 1.2V, V_{OUT} = 3.3V		0.5	0.9	µA
		V_{OUT}			5	7.5	µA
I_{SD}	Shutdown current	V_{OUT}	V_{EN} = 0V, V_{IN} =SW= 1.5V, T_A = 25°C		0.2	7.5	µA
I_{SD}	Shutdown current	V_{OUT}	V_{EN} = 0 V, V_{IN} =SW= 3V, T_A = 25°C		0.2	7.5	µA
I_{LKG}	Leakage current into VOUT		V_{EN} = 0V, V_{IN} = 1.2V, V_{OUT} = 3.3V		1		µA
	Leakage current into SW		V_{EN} = 0V, V_{IN} = 1.2V, V_{SW} = 1.2V, V_{OUT} ≥ V_{IN}		0.01	0.2	µA
I_{FB}	TLV61220A Feedback input current		V_{FB} = 0.5V		0.01		µA
I_{EN}	EN input current		Clamped on GND or V_{IN} (V_{IN} < 1.5V)		0.005	0.1	µA
CONTROL STAGE							
V_{IL}	EN input low voltage		V_{IN} ≤ 1.5V			0.2 × V_{IN}	V
V_{IH}	EN input high voltage		V_{IN} ≤ 1.5V	0.8 × V_{IN}			V
V_{IL}	EN input low voltage		5V > V_{IN} > 1.5V			0.4	V
V_{IH}	EN input high voltage		5V > V_{IN} > 1.5V	1.2			V
V_{UVLO}	Undervoltage lockout threshold for turn off		V_{IN} decreasing		0.5	0.7	V
	Overvoltage protection threshold			5.5		7.5	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

6.6 Typical Characteristics



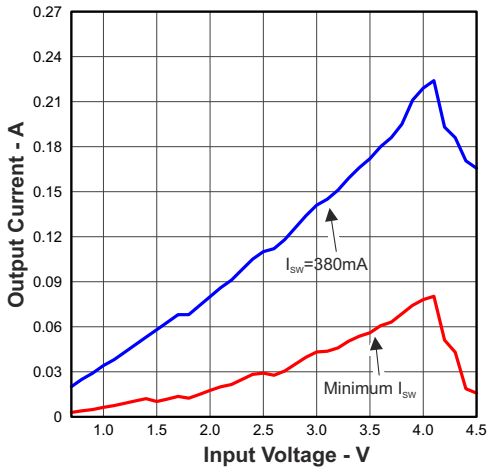
V_O = 1.8 V

Figure 6-1. Maximum Output Current vs Input Voltage



V_O = 3.3 V

Figure 6-2. Maximum Output Current vs Input Voltage



V_O = 5 V

Figure 6-3. Maximum Output Current vs Input Voltage

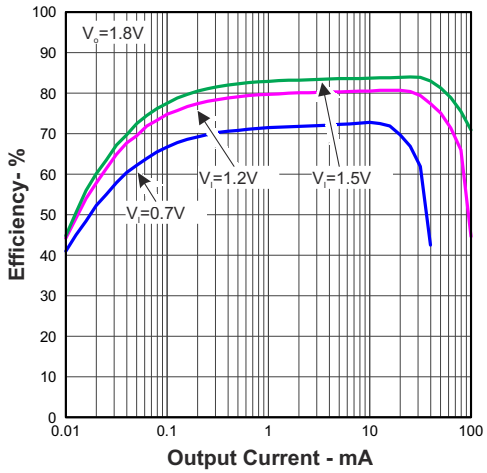


Figure 6-4. Efficiency vs Output Current and Input Voltage

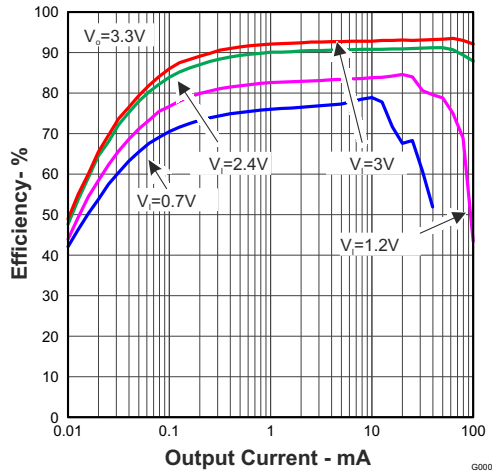


Figure 6-5. Efficiency vs Output Current and Input Voltage

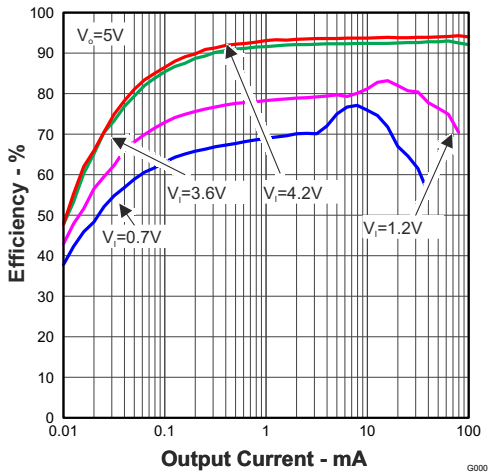


Figure 6-6. Efficiency vs Input Voltage and Output Current

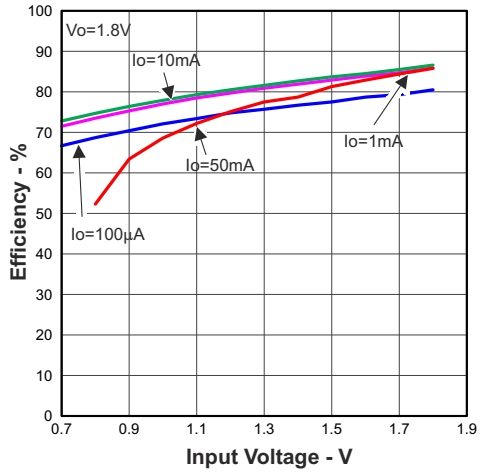


Figure 6-7. Efficiency vs Input Voltage and Output Current

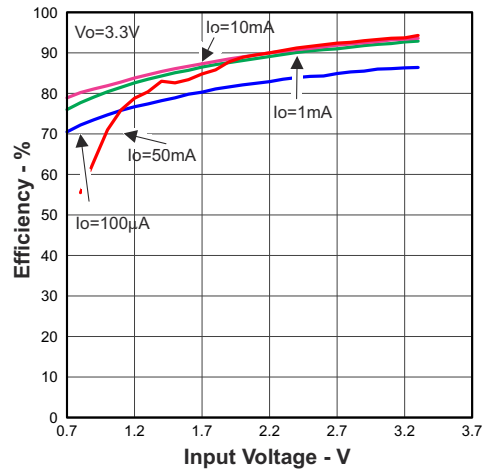


Figure 6-8. Efficiency vs Input Voltage and Output Current

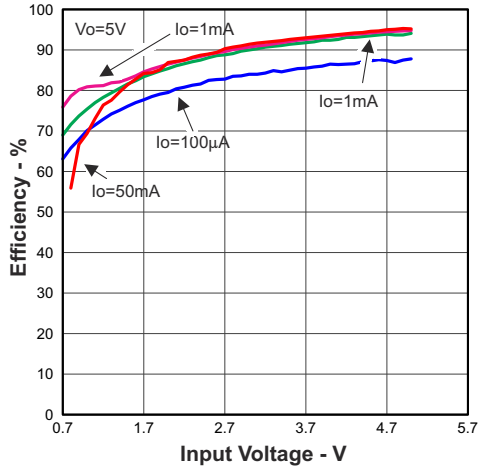


Figure 6-9. Efficiency vs Input Voltage and Output Current

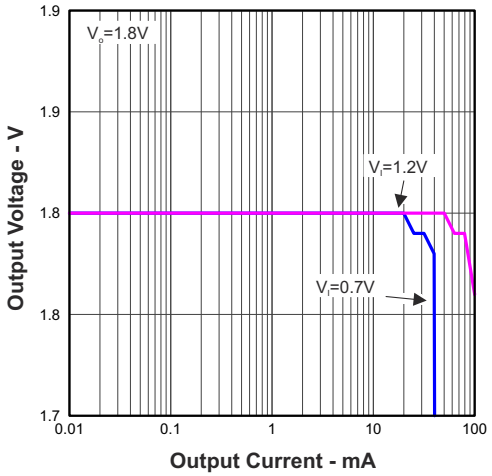


Figure 6-10. Output Voltage vs Output Current and Input Voltage

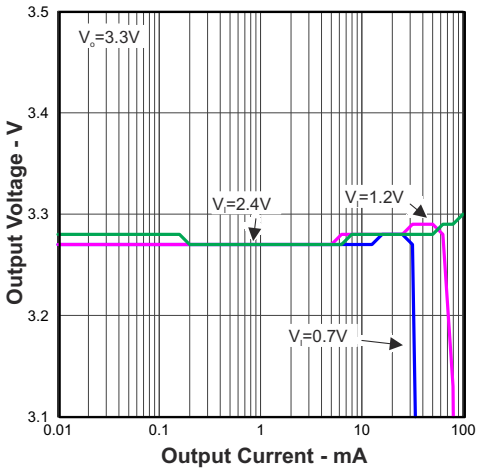


Figure 6-11. Output Voltage vs Output Current and Input Voltage

7 Parameter Measurement Information

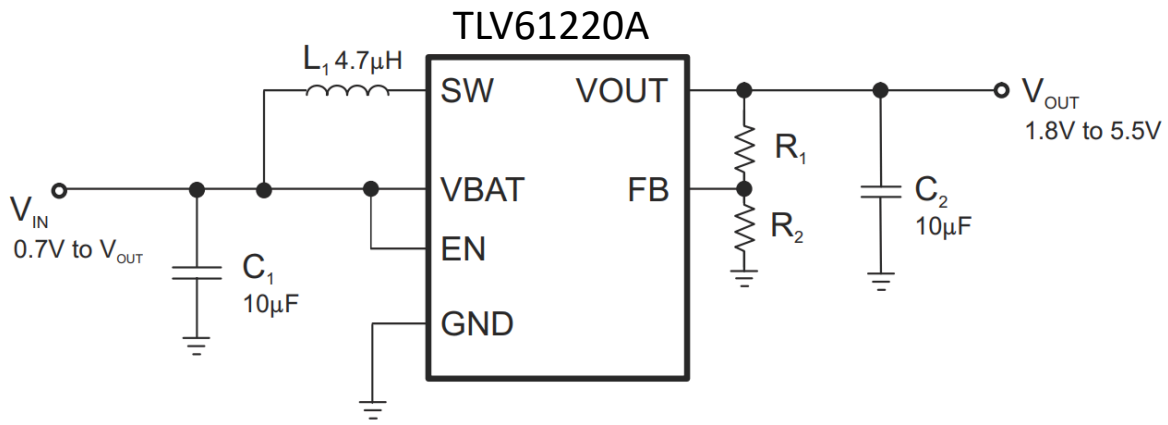


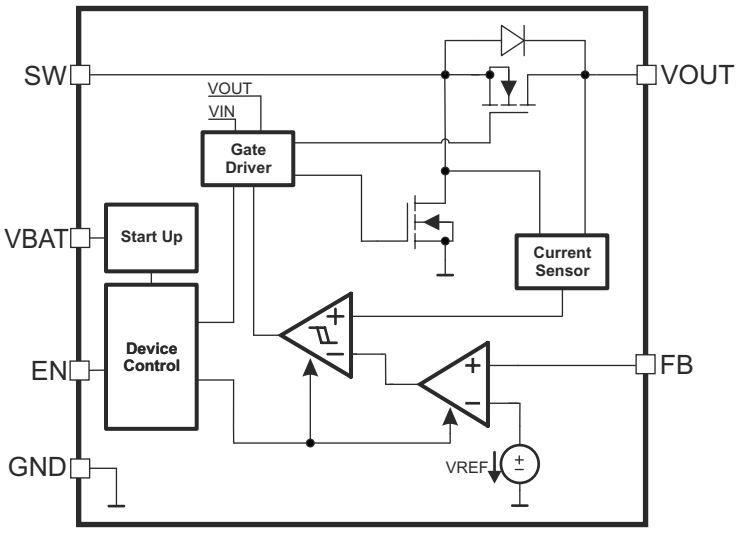
Figure 7-1. Parameter Measurement Schematic

8 Detailed Description

8.1 Overview

The TLV61220A is a high performance, highly efficient boost converter. To achieve high efficiency the power stage is realized as a synchronous boost topology. For the power switching two actively controlled low $R_{DS(on)}$ power MOSFETs are implemented.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Controller Circuit

The device is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. In case the required average input current is lower than the average inductor current defined by this constant ripple the inductor current gets discontinuous to keep the efficiency high at low load conditions.

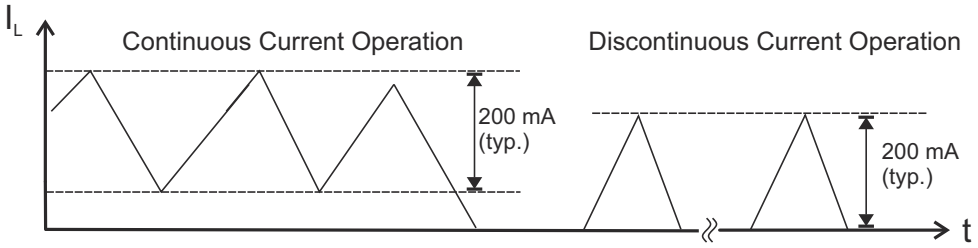


Figure 8-1. Hysteretic Current Operation

The output voltage V_{OUT} is monitored via the feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly. An external resistor divider needs to be connected.

The self oscillating hysteretic current mode architecture is inherently stable and allows fast response to load variations. It also allows using inductors and capacitors over a wide value range.

8.3.1.1 Startup

After the EN pin is tied high, the device starts to operate. In case the input voltage is not high enough to supply the control circuit properly a startup oscillator starts to operate the switches. During this phase the switching

frequency is controlled by the oscillator and the maximum switch current is limited. As soon as the device has built up the output voltage to about 1.8 V, high enough for supplying the control circuit, the device switches to its normal hysteretic current mode operation. The startup time depends on input voltage and load current.

8.3.1.2 Operation at Output Overload

If in normal boost operation the inductor current reaches the internal switch current limit threshold the main switch is turned off to stop further increase of the input current.

In this case the output voltage will decrease since the device can not provide sufficient power to maintain the set output voltage.

If the output voltage drops below the input voltage the backgate diode of the rectifying switch gets forward biased and current starts flow through it. This diode cannot be turned off, so the current finally is only limited by the remaining DC resistances. As soon as the overload condition is removed, the converter resumes providing the set output voltage.

8.3.1.3 Undervoltage Lockout

An implemented undervoltage lockout function stops the operation of the converter if the input voltage drops below the typical undervoltage lockout threshold. This function is implemented in order to prevent malfunctioning of the converter.

8.3.1.4 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore an overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TLV61220A output voltage is also monitored internally. In case it reaches the internally programmed threshold of 6.5 V typically the voltage amplifier regulates the output voltage to this value.

If the TLV61220A is used to drive LEDs, this feature protects the circuit if the LED fails.

8.3.1.5 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC junction temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. To prevent unstable operation close to the region of overtemperature threshold, a built-in hysteresis is implemented.

8.4 Device Functional Modes

8.4.1 Device Enable and Shutdown Mode

The device is enabled when EN is set high and shut down when EN is low. During shutdown, the converter stops switching and all internal control circuitry is turned off. In this case the input voltage is connected to the output through the back-gate diode of the rectifying MOSFET. This means that there always will be voltage at the output which can be as high as the input voltage or lower depending on the load.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV61220A is intended for systems powered by a single cell battery to up to three Alkaline, NiCd or NiMH cells with a typical terminal voltage between 0.7 V and 5.5 V. It can also be used in systems powered by one-cell Li-Ion or Li-Polymer batteries with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source with a typical output voltage between 0.7 V and 5.5 V can be used with the TLV61220A.

9.2 Typical Application

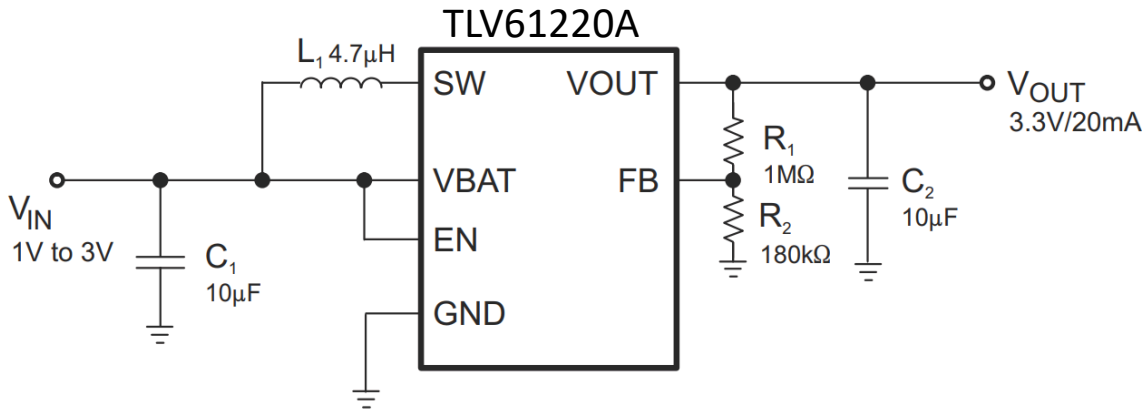


Figure 9-1. Typical Application Circuit for Adjustable Output Voltage Option

9.2.1 Design Requirements

In this example, TLV61220A is used to design a 3.3V power supply with up to 50mA output current capability. The TLV61220A can be powered by a single-cell battery to up to three Alkaline, NiCd or NiMH cells with a typical terminal voltage between 0.7V and 5.5V. It can also be used in systems powered by one-cell Li-Ion or Li-Polymer batteries with a typical voltage between 2.5V and 4.2V. In this example, the input voltage range is from 2V to 3V for one-cell coin cell battery input design.

Table 9-1. TLV61220A 3.3 V Output Design Requirements

PARAMETERS	VALUES
Input Voltage	2V to 3V
Output Voltage	3.3V
Output Current	50mA

9.2.2 Detailed Design Procedure

Table 9-2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_1	GRM188R60J106ME84D	Murata	10µF, 6.3V. X5R Ceramic
C_2	GRM188R60J106ME84D	Murata	10µF, 6.3V. X5R Ceramic
L_1	1269AS-H-4ZR7N	Toko	4.7µH
R_1, R_2			R_1= 1MΩ, R_2= Values depending on the programmed output voltage

9.2.2.1 Adjustable Output Voltage Version

An external resistor divider is used to adjust the output voltage. The resistor divider needs to be connected between VOUT, FB and GND as shown in Figure 9-1. When the output voltage is regulated properly, the typical voltage value at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on those two values, the recommended value for R_2 should be lower than 500 kΩ, in order to set the divider current to 1 µA or higher. The value of the resistor connected between VOUT and FB, R_1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{1}$$

As an example, if an output voltage of 3.3 V is needed, a 1-MΩ resistor is calculated for R_1 when for R_2 a 180-kΩ has been selected.

9.2.2.2 Inductor Selection

To make sure that the TLV61220A can operate, a suitable inductor must be connected between pin VBAT and pin SW. Inductor values of 4.7 µH show good performance over the whole input and output voltage range .

Choosing other inductance values affects the switching frequency *f* proportional to 1/L as shown in Equation 2.

$$L = \frac{1}{f \times 200\ mA} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \tag{2}$$

Choosing inductor values higher than 4.7 µH can improve efficiency due to reduced switching frequency and, therefore, with reduced switching losses. Using inductor values below 2.2 µH is not recommended.

Having selected an inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 3 gives the peak current estimate.

$$I_{L,MAX} = \begin{cases} \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN}} + 100\ mA; & \text{continous current operation} \\ 200\ mA; & \text{discontinuous current operation} \end{cases} \tag{3}$$

For selecting the inductor this would be the suitable value for the current rating. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents.

Equation 4 helps to estimate whether the device will work in continuous or discontinuous operation depending on the operating points. As long as the inequation is true, continuous operation is typically established. If the inequation becomes false, discontinous operation is typically established.

$$\frac{V_{OUT} \times I_{OUT}}{V_{IN}} > 0.8 \times 100\ mA \quad (4)$$

The following inductor series from different suppliers have been used with TLV61220A converters:

Table 9-3. List of Inductors

VENDOR	INDUCTOR SERIES
Toko	DFE252010C
Coilcraft	EPL3015
	EPL2010
Murata	LQH3NP
Taiyo Yuden	NR3015
Wurth Elektronik	WE-TPC Typ S

9.2.2.3 Capacitor Selection

9.2.2.3.1 Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VBAT and GND pins of the IC is recommended.

9.2.2.3.2 Output Capacitor

For the output capacitor C_2, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, the use of a small ceramic capacitor with an capacitance value of around 2.2µF in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

A minimum capacitance value of 4.7µF should be used, 10 µF are recommended. If the inductor value exceeds 4.7µH, the value of the output capacitance value needs to be half the inductance value or higher for stability reasons, see Equation 5.

$$C_2 \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \quad (5)$$

The TLV61220A is not sensitive to the ESR in terms of stability. Using low ESR capacitors, such as ceramic capacitors, is recommended anyway to minimize output voltage ripple. If heavy load changes are expected, the output capacitor value should be increased to avoid output voltage drops during fast load transients.

9.2.3 Application Curves

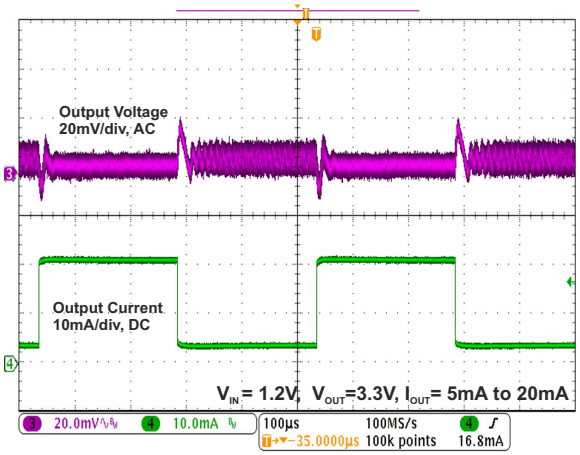


Figure 9-2. Load Transient Response

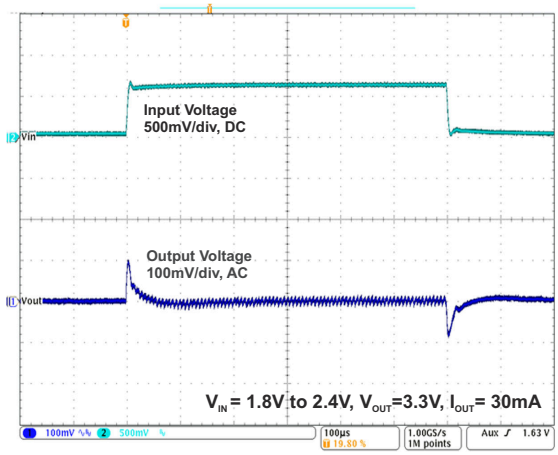


Figure 9-3. Line Transient Response

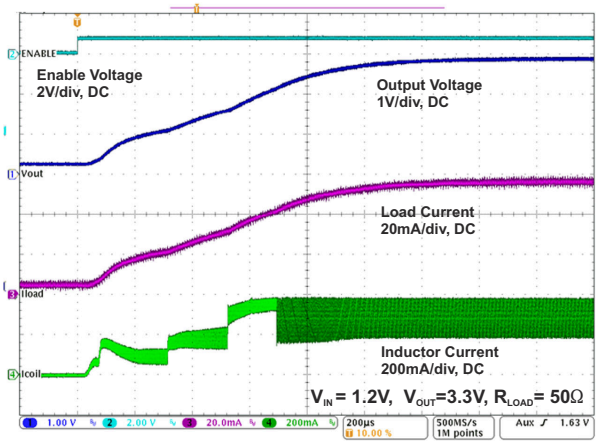


Figure 9-4. Start Up After Enable

10 Power Supply Recommendations

The power supply can be single-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery.

The input supply should be well regulated with the rating of TLV61220A. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

11.2 Layout Example

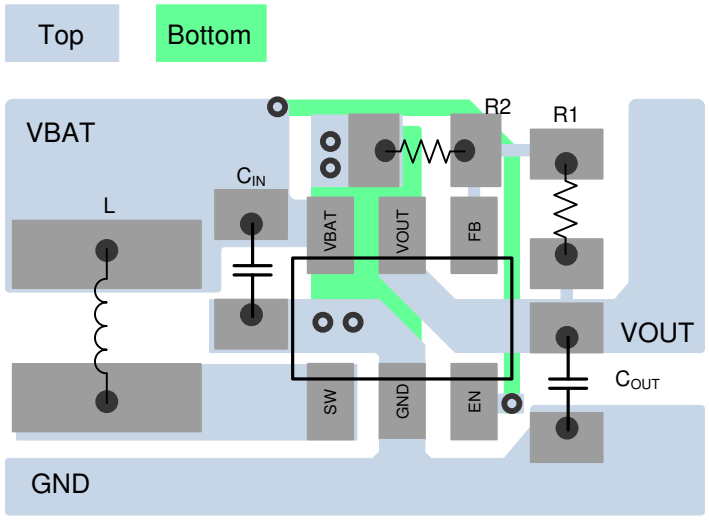


Figure 11-1. PCB Layout Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power-dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

For more details on how to use the thermal parameters in the dissipation ratings table please check the *Thermal Characteristics Application Note* and the *IC Package Thermal Metrics Application Note*.

12 Device and Documentation Support

12.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

- Texas Instruments, *Thermal Characteristics Application Note*
- Texas Instruments, *IC Package Thermal Metrics Application Note*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV61220ADBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUAI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

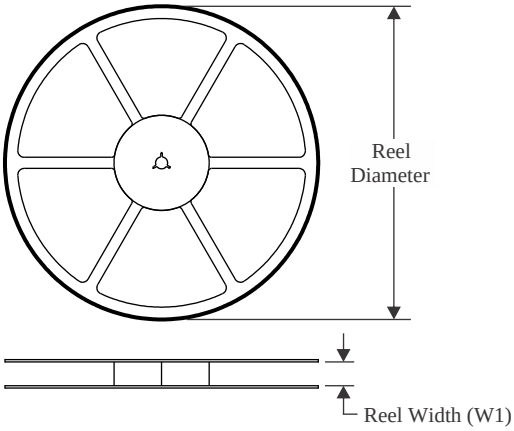
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

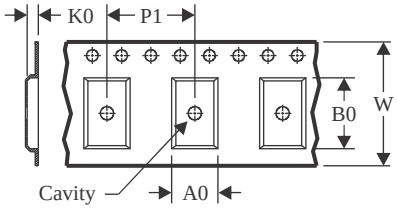
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

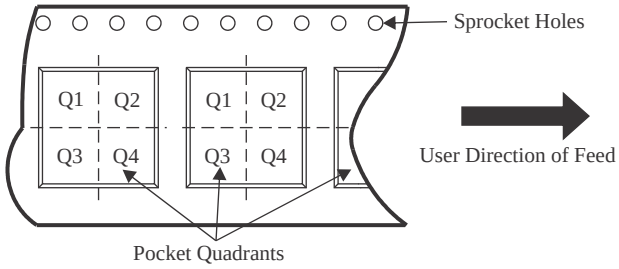


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

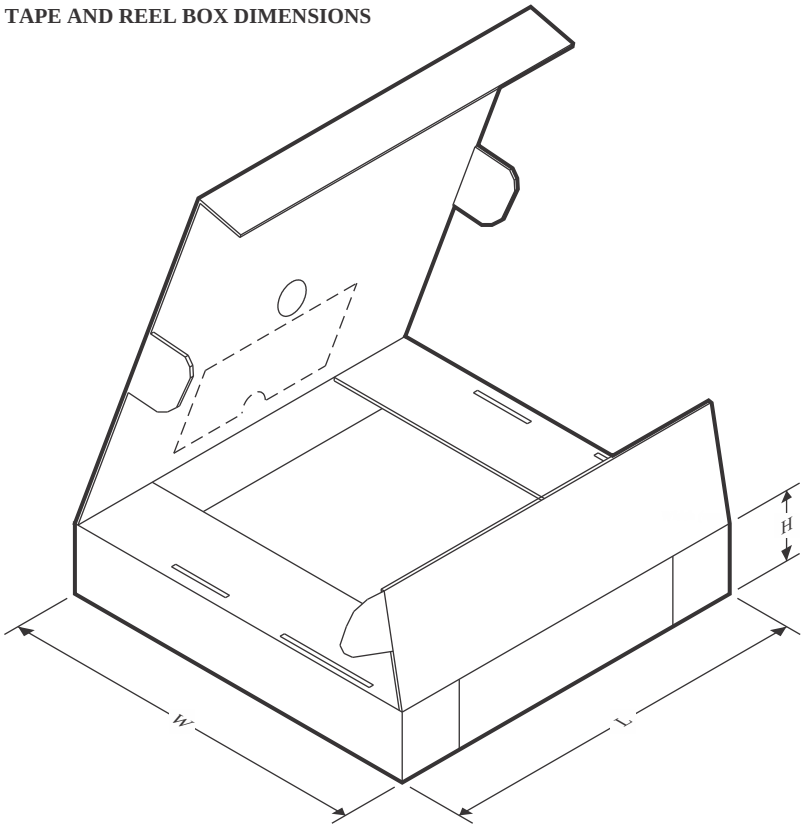
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV61220ADBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

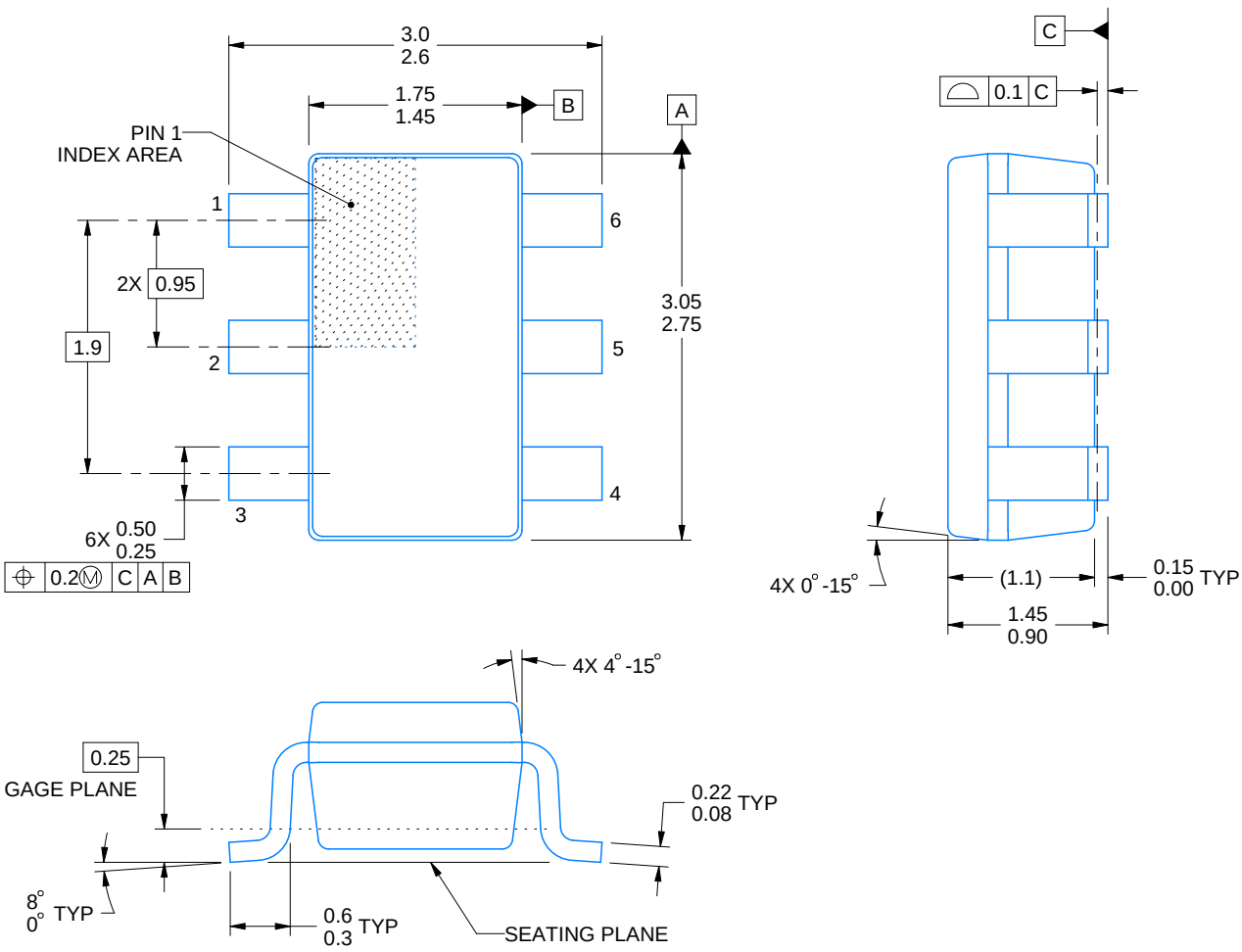
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV61220ADBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

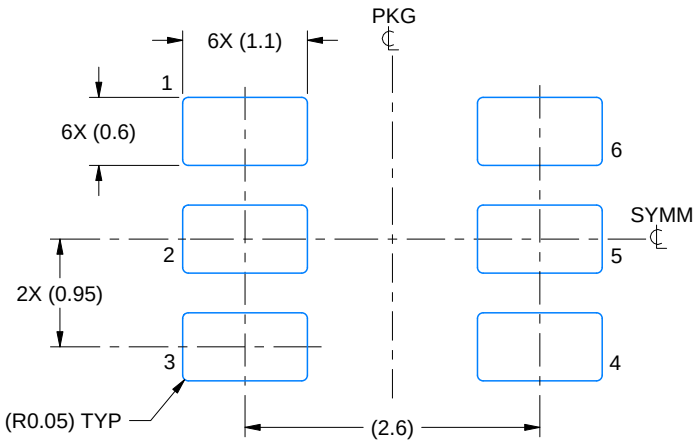
SMALL OUTLINE TRANSISTOR



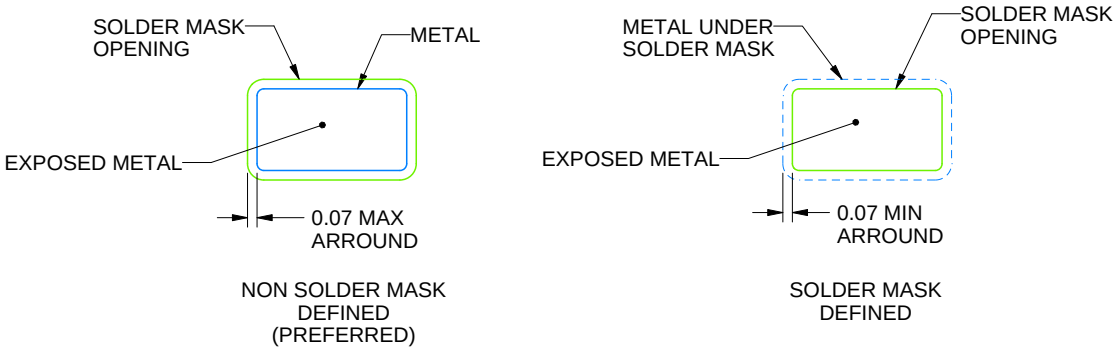
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

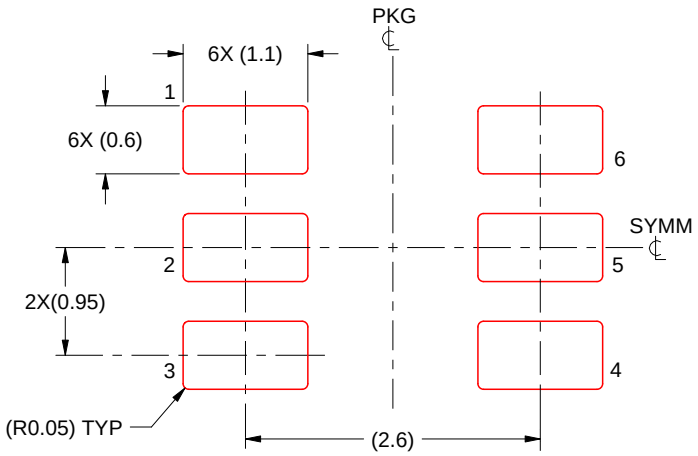


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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