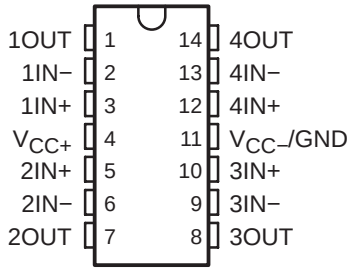
SLVS461B − JANUARY 2003 − REVISED JULY 2003

- **Low Offset . . . 3 mV (Max) for A-Grade**
- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**
- **Alternative to MC33074/A and MC34074/A**

D, N, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

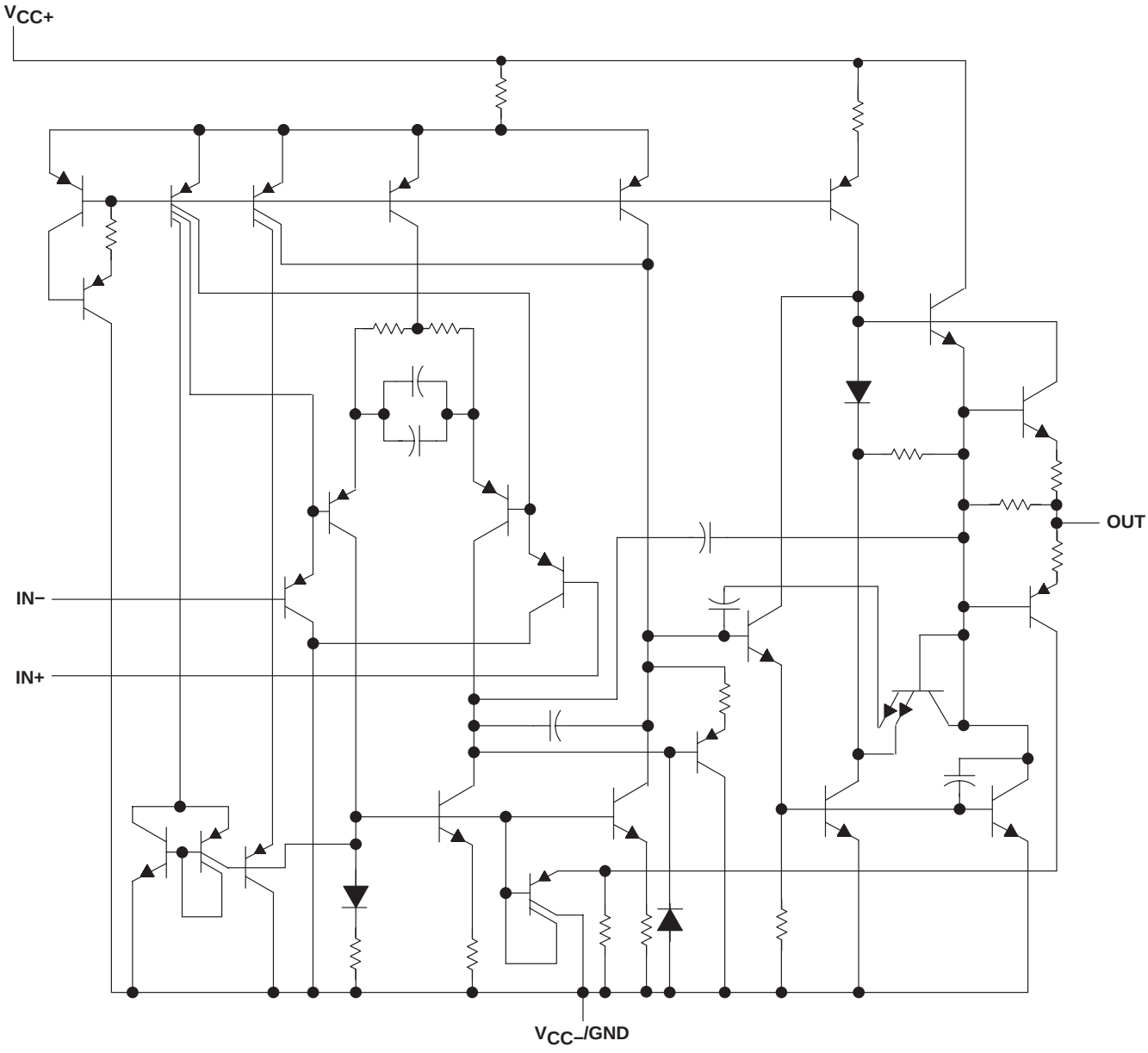
T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474ACN	TL3474ACN
		SOIC (D)	Tube of 50	TL3474ACD	TL3474A
			Reel of 2500	TL3474ACDR	
		TSSOP (PW)	Tube of 90	TL3474ACPW	T3474A
			Reel of 2000	TL3474ACPWR	
	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474CN	TL3474CN
		SOIC (D)	Tube of 50	TL3474CD	TL3474C
			Reel of 2500	TL3474CDR	
		TSSOP (PW)	Tube of 90	TL3474CPW	TL3474
			Reel of 2000	TL3474CPWR	
−40°C to 105°C	A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474AIN	Z3474A
		SOIC (D)	Tube of 50	TL3474AID	TL3474AI
			Reel of 2500	TL3474AIDR	
		TSSOP (PW)	Tube of 90	TL3474AIPW	Z3474A
			Reel of 2000	TL3474AIPWR	
	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474IN	TL3474IN
		SOIC (D)	Tube of 50	TL3474ID	TL3474I
			Reel of 2500	TL3474IDR	
		TSSOP (PW)	Tube of 90	TL3474IPW	Z3474
			Reel of 2000	TL3474IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3474, TL3474A operational amplifiers. These devices offer 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time without the use of JFET device technology. Although the TL3474 and TL3474A can be operated from split supplies, they are particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, these devices exhibit high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. These low-cost amplifiers are an alternative to the MC34074/A and MC33074/A operational amplifiers.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 18 V
V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±36 V
Input voltage, V_I (any input) . . . . . $V_{CC±}$
Input current, I_I (each input) . . . . . ±1 mA
Output current, I_O . . . . . ±80 mA
Total current into V_{CC+} . . . . . 80 mA
Total current out of V_{CC-} . . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package . . . . . 86°C/W
N package . . . . . 80°C/W
PW package . . . . . 113°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}/GND.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-} − 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.8	V
		$V_{CC±}$ = ±15 V	−15	12.8	
T_A	Operating free-air temperature	TL3474C, TL3474AC	0	70	°C
		TL3474I, TL3474AI	−40	105	

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TL3474			TL3474A			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = 5 V	25°C		1.5	10		1.5	3	mV
			V_{CC} = ±15 V	25°C		1.0	10		1.0	3	
				Full range‡			12			5	
αV_{IO}	Temperature coefficient of input offset voltage		V_{CC} = ±15 V	Full range‡		10			10		µV/°C
I_{IO}	Input offset current		V_{CC} = ±15 V	25°C		6	75		6	75	nA
				Full range‡			300			300	
I_{IB}	Input bias current		V_{CC} = ±15 V	25°C		100	500		100	500	nA
				Full range‡			700			700	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C		−15 to 12.8			−15 to 12.8		V
				Full range‡		−15 to 12.8			−15 to 12.8		
V_{OH}	High-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C	3.7	4		3.7	4		V
		R_L = 10 kΩ		25°C	13.6	14		13.6	14		
		R_L = 2 kΩ		Full range‡	13.4			13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C		0.1	0.3		0.1	0.3	V
		R_L = 10 kΩ		25°C		−14.7	−14.3		−14.7	−14.3	
		R_L = 2 kΩ		Full range‡			−13.5			−13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	25	100		25	100		V/mV
				Full range‡	20			20			
I_{OS}	Short-circuit output current	Source: V_{ID} = 1 V,	V_O = 0	25°C	−10	−34		−10	−34		mA
		Sink: V_{ID} = −1 V,	V_O = 0		20	27		20	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min),	R_S = 50 Ω	25°C	65	97		80	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±13.5 V to ±16.5 V, R_S = 100 Ω		25°C	70	97		70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0,	No load	25°C		3.5	4.5		3.5	4.5	mA
				Full range‡		4.5	5.5		4.5	5.5	
		V_{CC+} = 5 V, V_O = 2.5 V, V_{CC-} = 0, No load		25°C		3.5	4.5		3.5	4.5	

† All typical values are at T_A = 25°C.
‡ Full range is 0°C to 70°C for the TL3474C, TL3474AC devices and −40°C to 105°C for the TL3474I, TL3474AI devices.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL3474			TL3474A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	V_I = −10 V to 10 V, R_L = 2 kΩ, C_L = 300 pF	A_V = 1	8	10		8	10		V/μs
SR−	Negative slew rate		A_V = −1		13			13		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		1.1			1.1		μs
			To 0.01%		2.2			2.2		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 100 Ω		49			49		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.22			0.22		pA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V to 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.02			0.02		%
GBW	Gain-bandwidth product	f =100 kHz		3	4		3	4		MHz
BW	Power bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, THD = 5.0%			160			160		kHz
ϕ_m	Phase margin	R_L = 2 kΩ,	C_L = 0		70			70		deg
		R_L = 2 kΩ,	C_L = 300 pF		50			50		
	Gain margin	R_L = 2 kΩ,	C_L = 0		12			12		dB
		R_L = 2 kΩ,	C_L = 300 pF		4			4		
r_i	Differential input resistance	V_{IC} = 0			150			150		MΩ
C_i	Input capacitance	V_{IC} = 0			2.5			2.5		pF
	Channel separation	f = 10 kHz			101			101		dB
z_o	Open-loop output impedance	f = 1 MHz,	A_V = 1		20			20		Ω

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

OUTPUT IMPEDANCE vs FREQUENCY

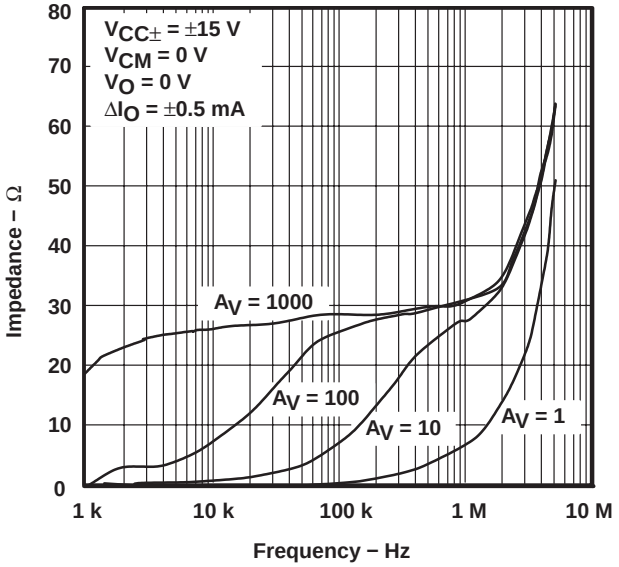


Figure 1

TOTAL HARMONIC DISTORTION vs FREQUENCY

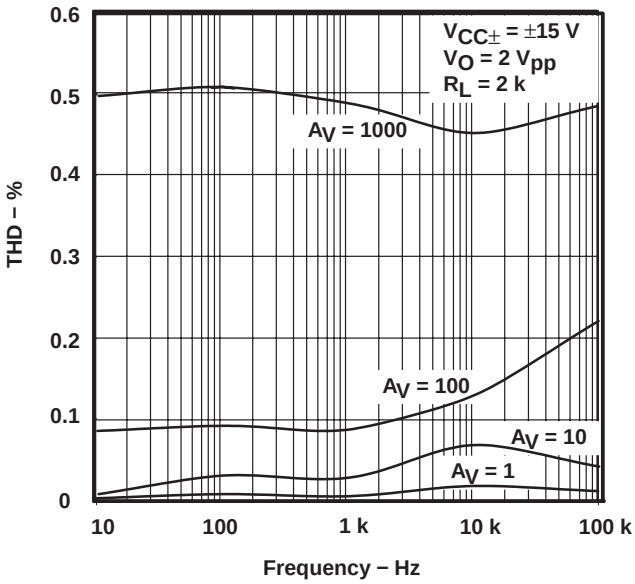


Figure 2

GAIN AND PHASE vs FREQUENCY

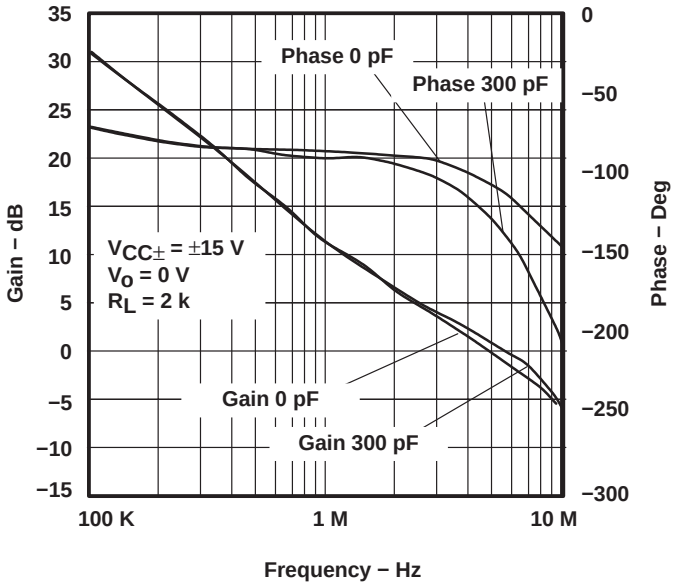


Figure 3

NORMALIZED INPUT BIAS CURRENT vs TEMPERATURE

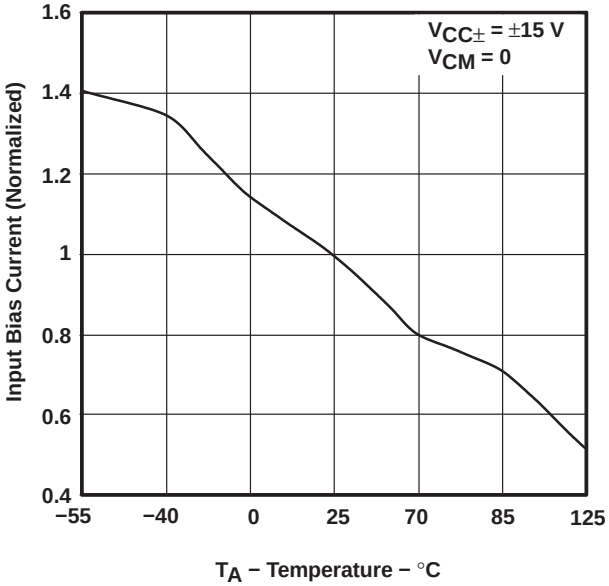


Figure 4

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

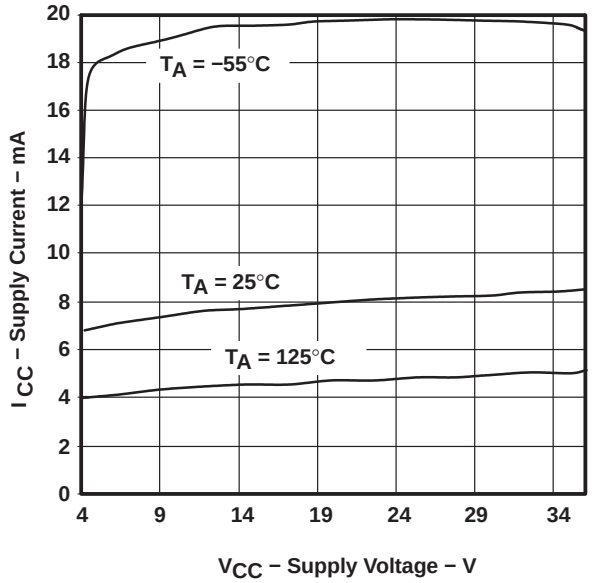


Figure 5

OFFSET VOLTAGE DRIFT
vs
TEMPERATURE

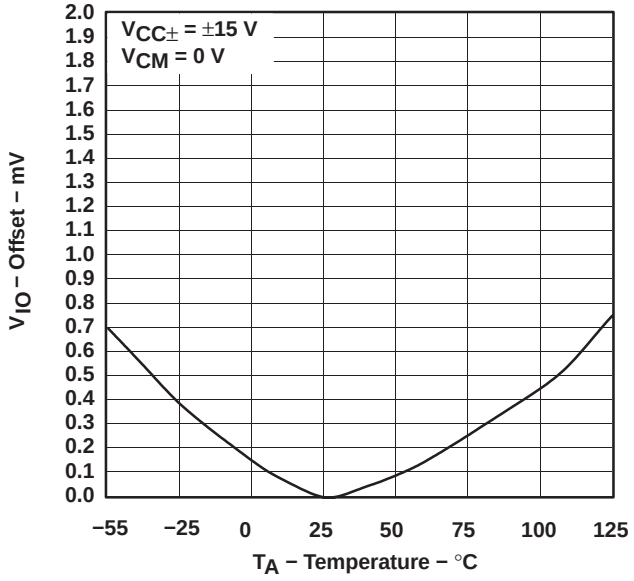


Figure 6

NORMALIZED INPUT BIAS CURRENT
vs
INPUT COMMON-MODE VOLTAGE

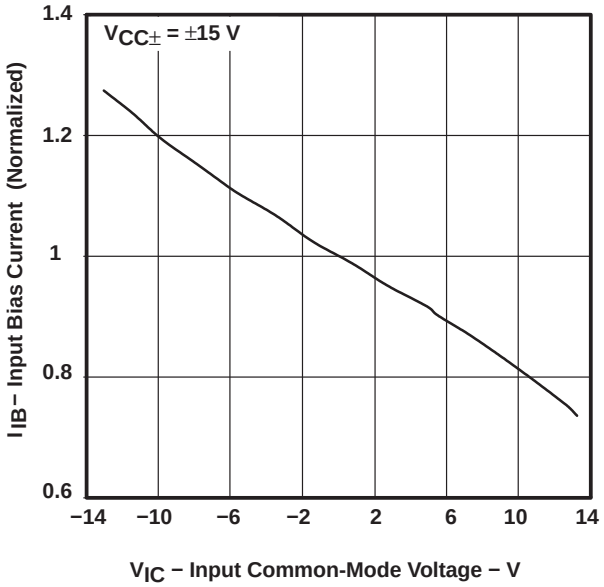


Figure 7

NORMALIZED SLEW RATE
vs
TEMPERATURE

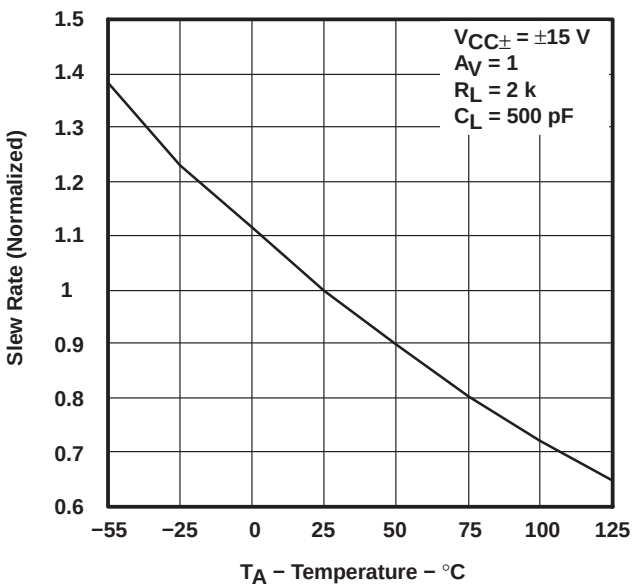


Figure 8

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

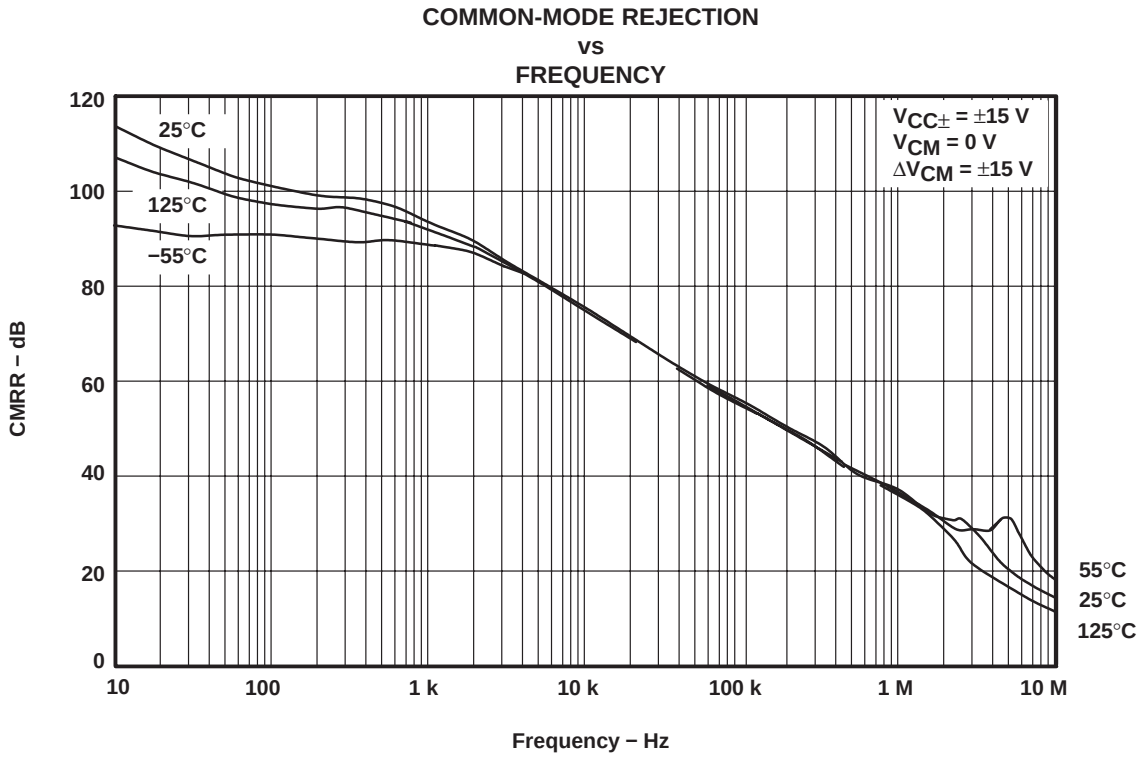


Figure 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3474ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A	Samples
TL3474ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3474ACN	Samples
TL3474ACPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A	Samples
TL3474AID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 105	TL3474AI	
TL3474AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI	Samples
TL3474AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	TL3474AIN	Samples
TL3474AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A	Samples
TL3474CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL3474C	
TL3474CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C	Samples
TL3474CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3474CN	Samples
TL3474CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474	Samples
TL3474ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 105	TL3474I	
TL3474IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I	Samples
TL3474IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	TL3474IN	Samples
TL3474IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

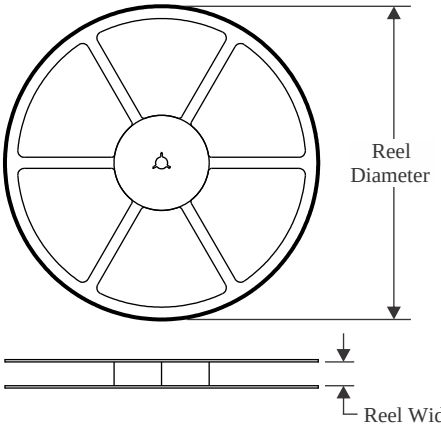
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

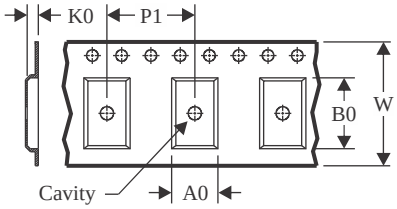
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

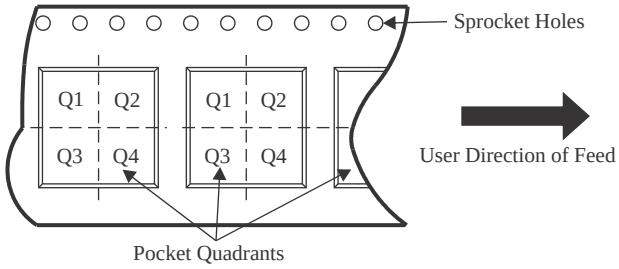


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

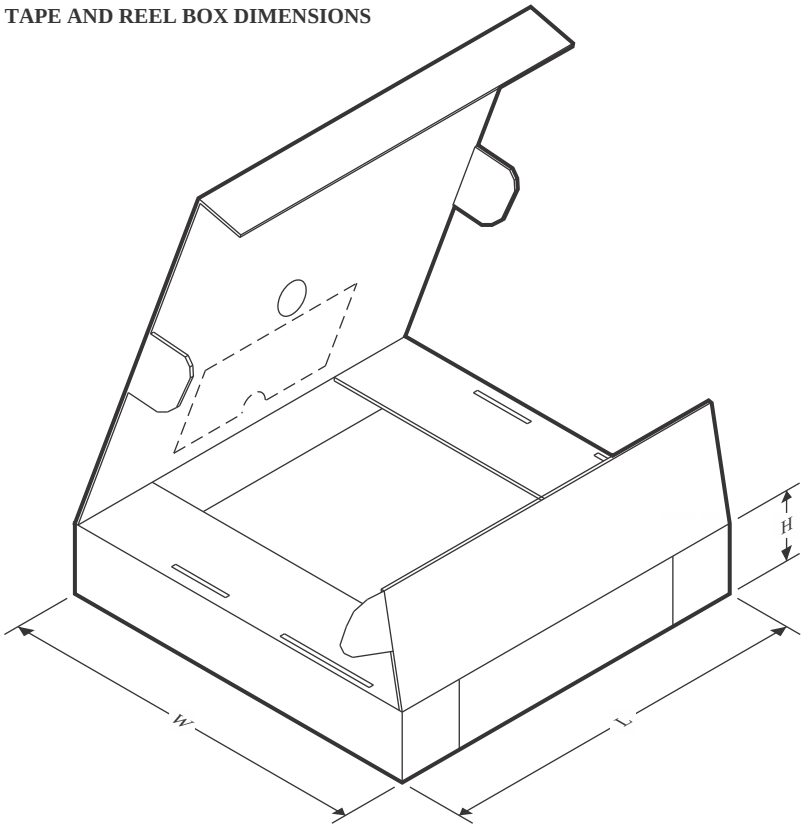
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3474ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

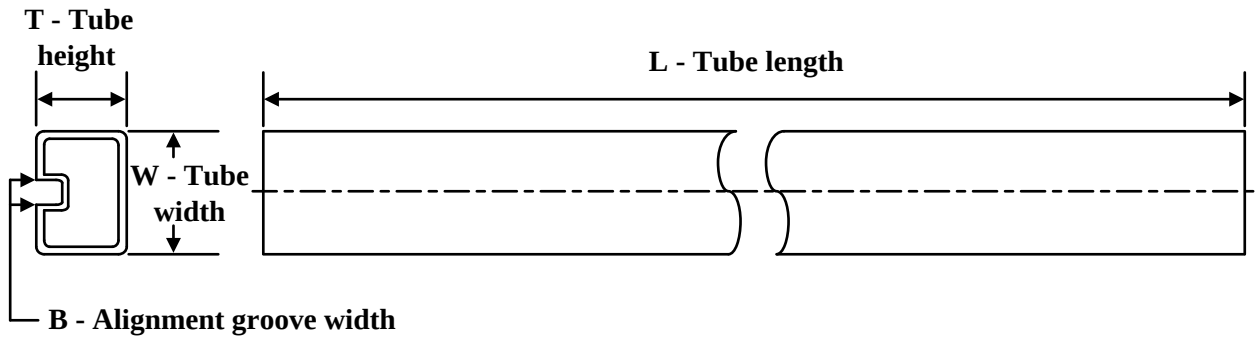
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

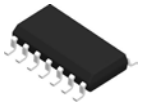
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3474ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474ACPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL3474ACPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474AIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3474ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN	N	PDIP	14	25	506	13.97	11230	4.32

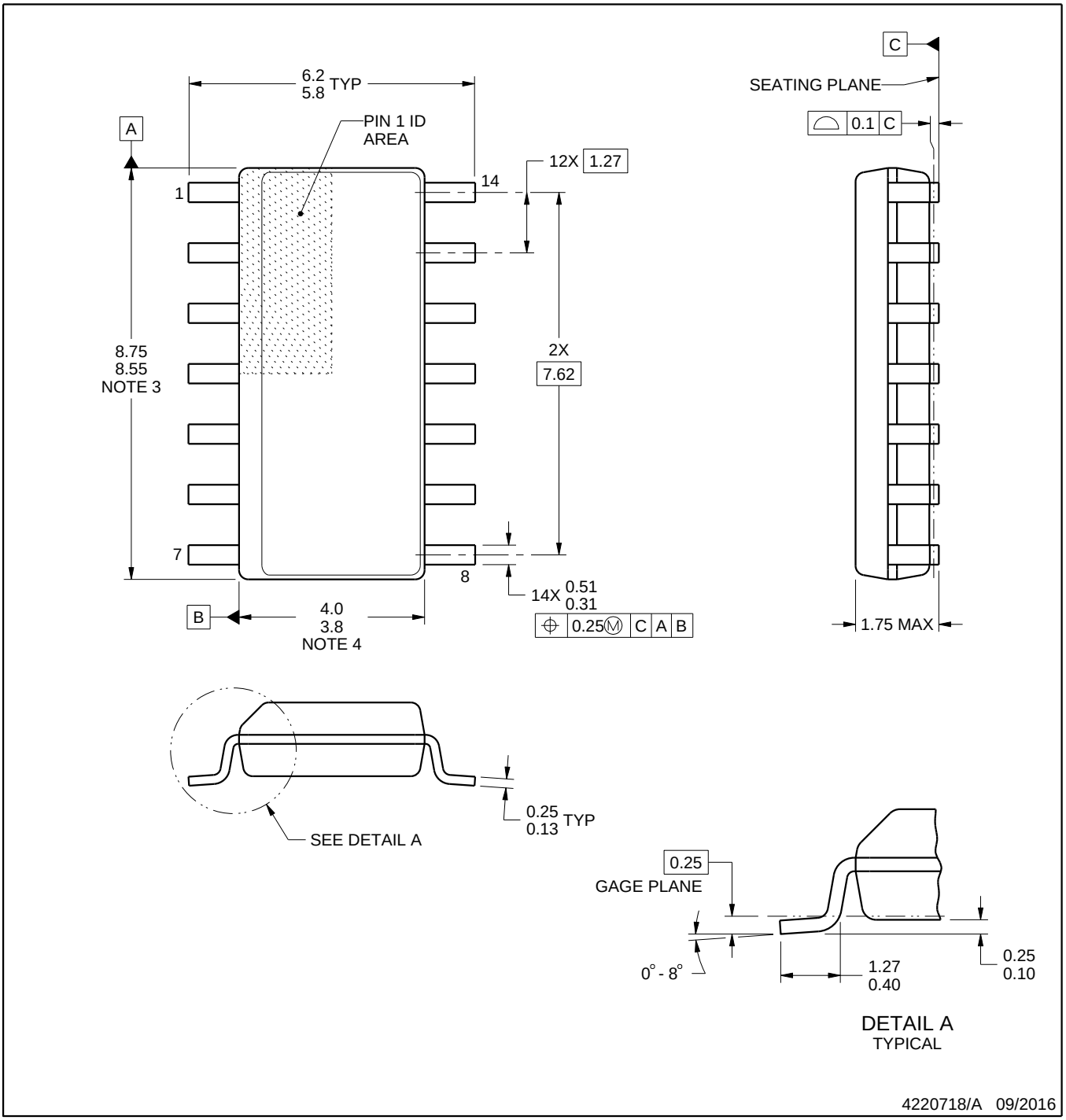


PACKAGE OUTLINE

D0014A

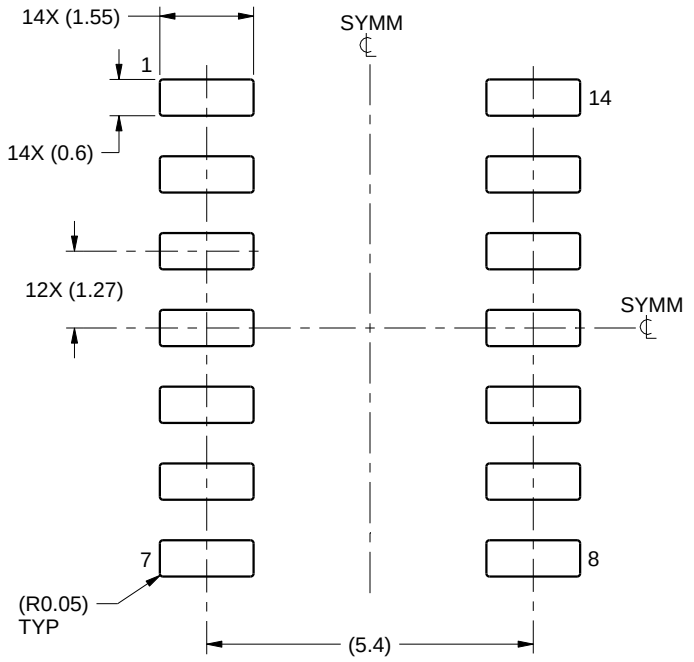
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

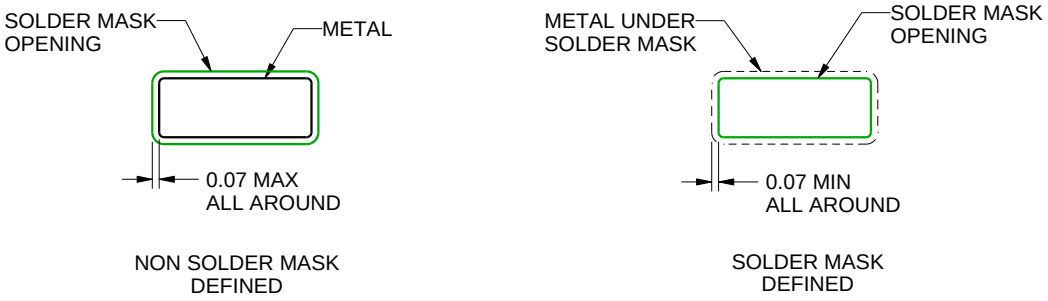


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

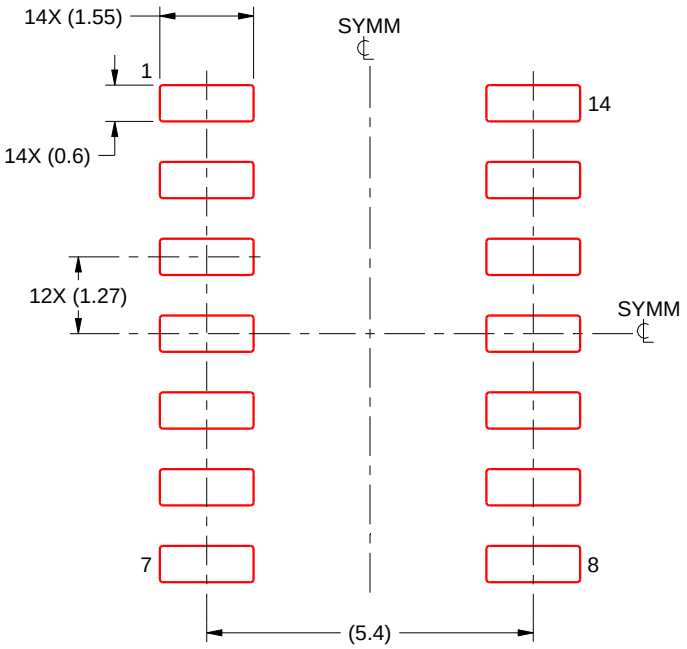
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

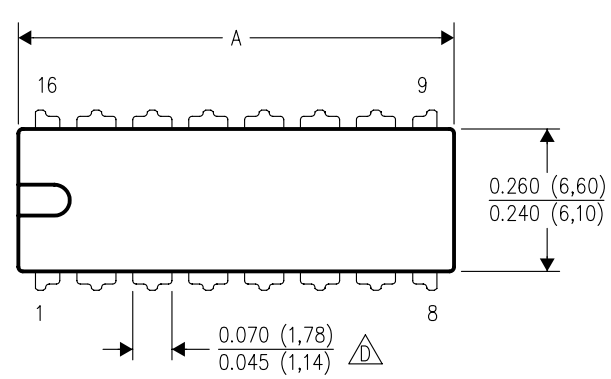
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

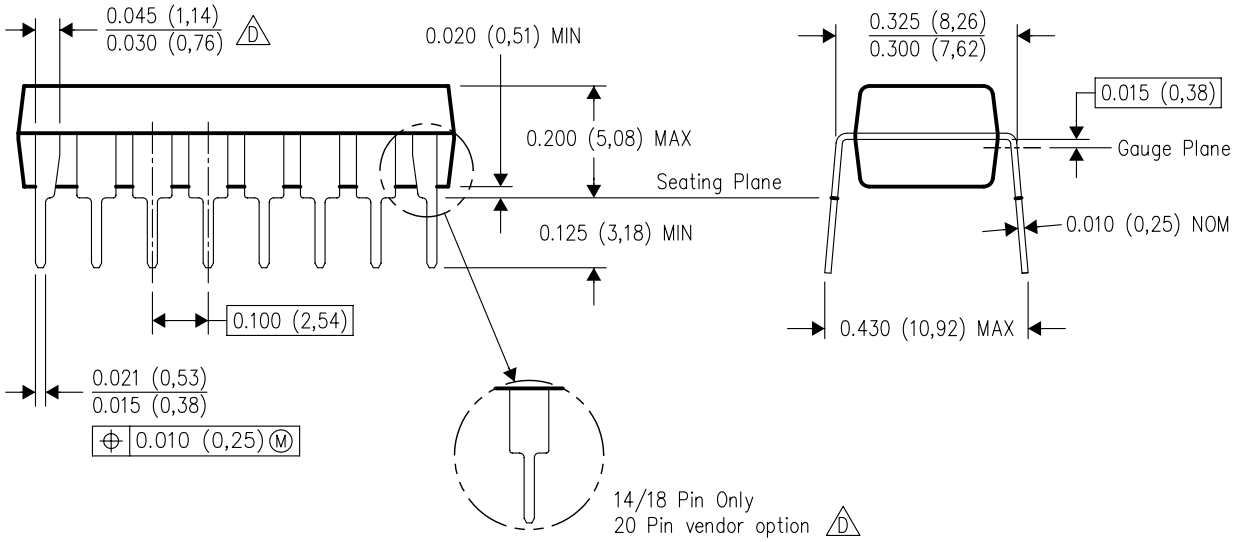
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

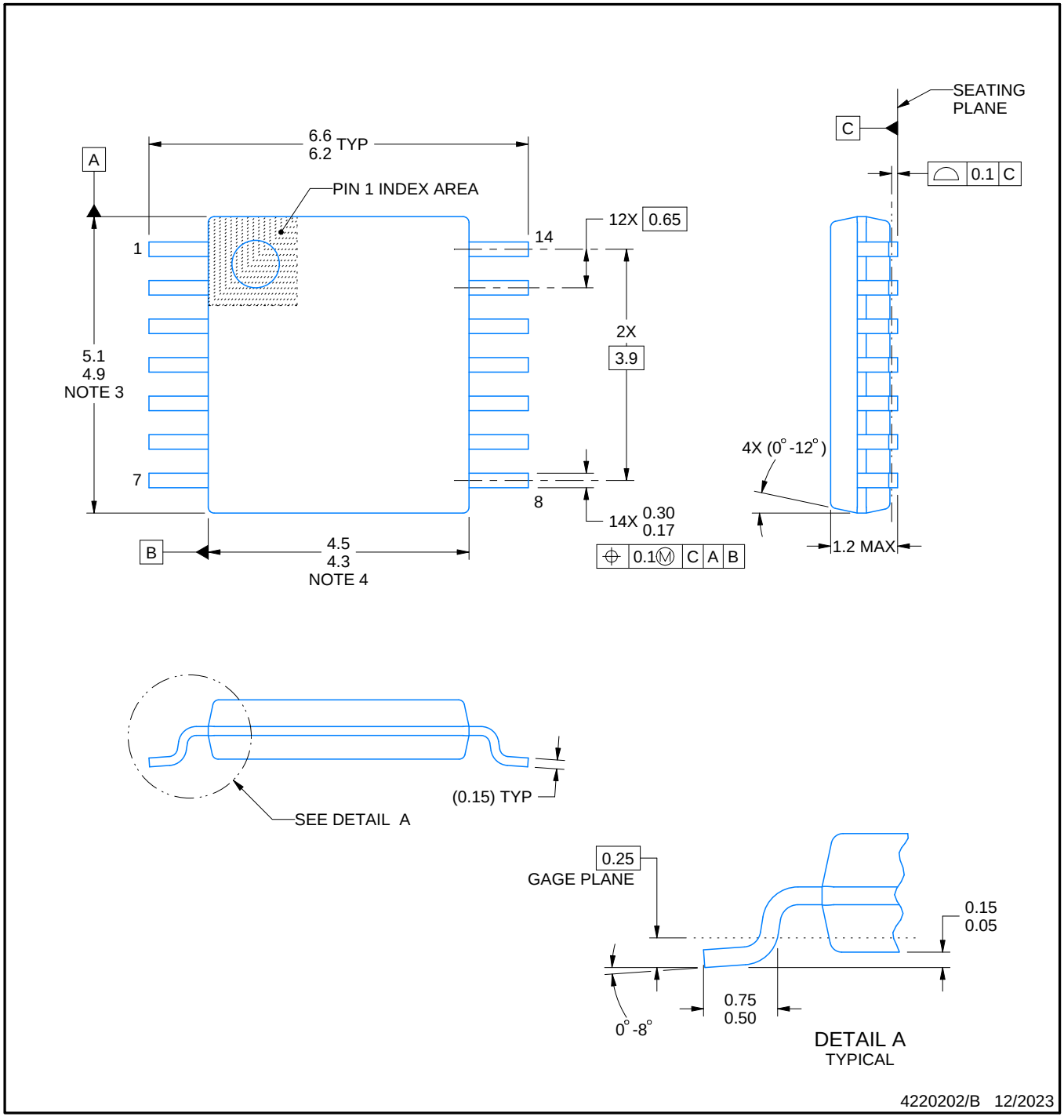
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

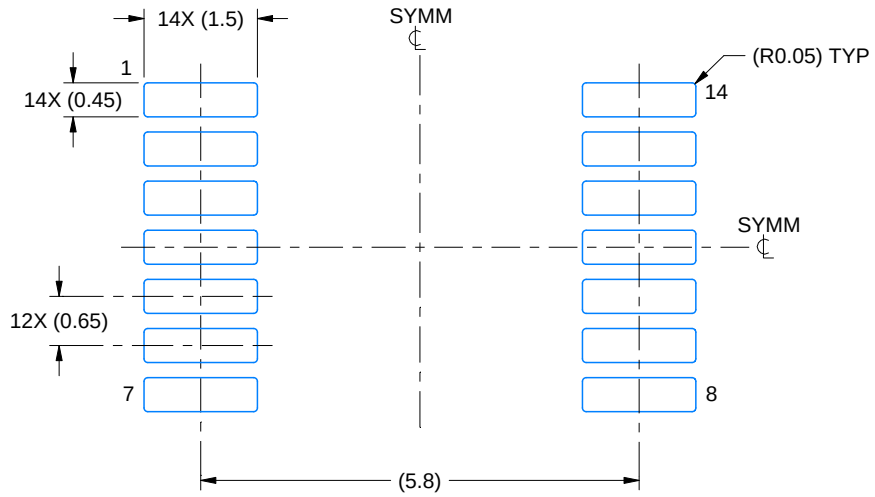
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

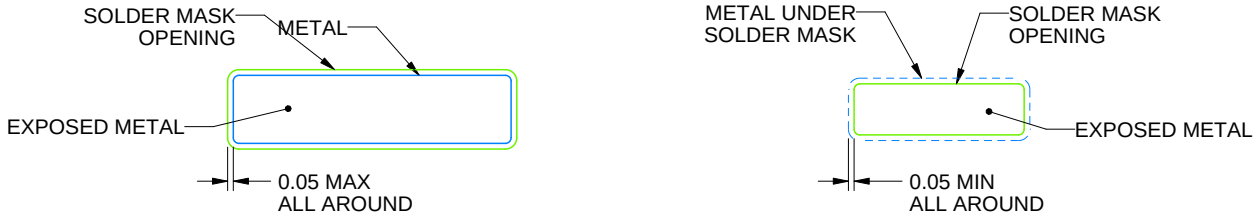


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

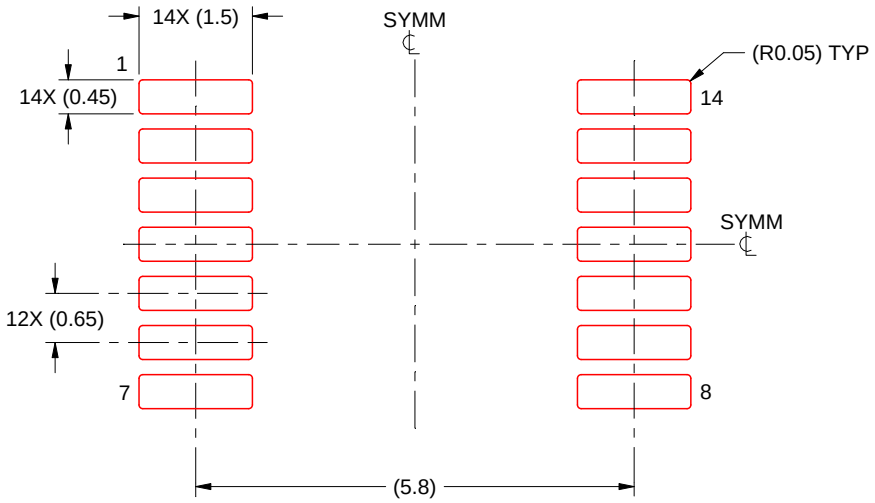


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265