THS4541-DIE Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier

1 Features

- Bandwidth: 500 MHz (G = 2 V/V)
- Gain bandwidth product: 850 MHz
- Slew rate: 1500 V/µs
- HD_2: –95 dBc at 10 MHz (2 V_{PP}, R_L = 500 Ω)
- HD_3: –90 dBc at 10 MHz (2 V_{PP}, R_L = 500 Ω)
- Input voltage noise: 2.2 nV/ $\sqrt{Hz}$ (f > 100 kHz)
- Low offset drift: ±0.5 µV/°C (typical)
- Negative rail input (NRI)
- Rail-to-rail output (RRO)
- Power supply:
  - Single-supply voltage range: 2.7 V to 5.4 V
  - Split-supply voltage range: ±1.35 V to ±2.7 V
  - Quiescent current: 10.1 mA (5-V supply)
- Power-down capability: 2 µA (typical)

2 Applications

- Low-power, high-performance ADC driver:
  - SAR, ΔΣ, and pipeline
- Low power, high performance (DC or AC coupled):
  - Single-ended to differential amplifier
  - Differential to differential amplifier
- Differential active filters
- Differential transimpedance for DAC outputs
- DC- or AC-coupled interface to the ADC3xxx Family of low-power, high-performance ADCs

3 Description

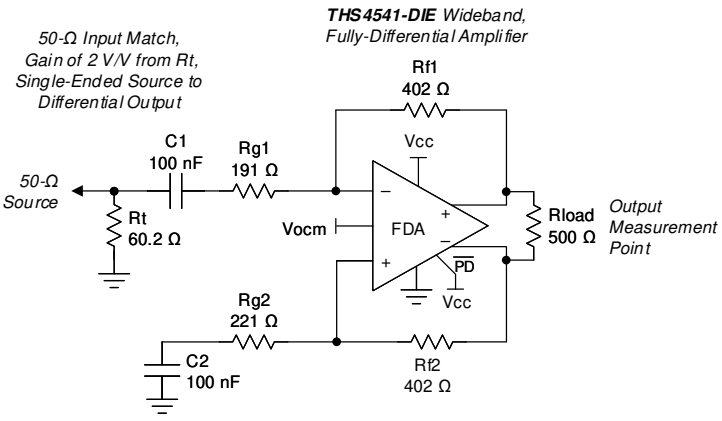
The THS4541-DIE is a low-power, voltage-feedback, fully differential amplifier (FDA) with an input common-mode range below the negative rail, and rail-to-rail output. This is a bare die product that can be used in multi-chip modules (MCM), system-in-package (SiP), chip-on-board (COB), hybrids, and systems that require an extremely small size. The THS4541-DIE is designed for low-power data acquisition systems where high density is critical in a high-performance analog-to-digital converter (ADC) or digital-to-analog converter (DAC) interface design.

The THS4541-DIE features the negative-rail input required when interfacing a DC-coupled, ground-centered, source signal. This negative-rail input, with rail-to-rail output, allows for easy interface between single-ended, ground-referenced, bipolar signal sources and a wide variety of successive approximation register (SAR), delta-sigma (ΔΣ), or pipeline ADCs using only a single 2.7 V to 5.4 V power supply.

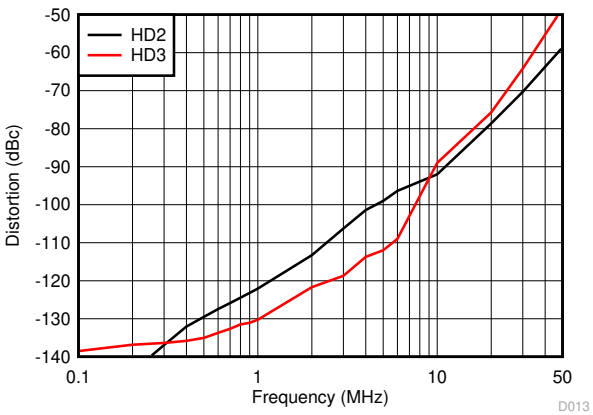
Device Information(1)

PART NUMBER	PACKAGE	DIE SIZE
THS4541-DIE	Bare die in tape and reel	1198 µm × 1006 µm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic



Single to Differential Gain of 2, 2-V Output

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (March 2022)	Page
• Updated the die size units from mm to µm	1

5 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS (X x Y)
15 mils (381 µm)	Silicon with backgrind	Wafer backside is electrically isolated from active circuitry	AlCu	85.0 µm × 85.0 µm

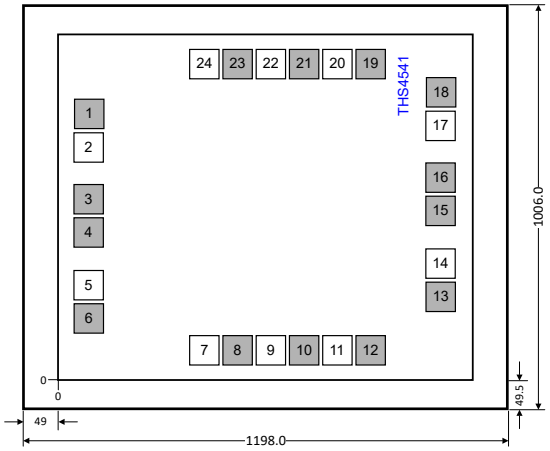


Figure 5-1. THS4541-DIE 24 Pad Die Diagram

Table 5-1. Bond Pad Coordinates in Microns

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
1	DNC(1)	4.50	686.50	89.50	771.50
2	IN+	4.50	590.50	89.50	675.50
3	DNC(1)	4.50	458.50	89.50	543.50
4	DNC(1)	4.50	363.50	89.50	448.50
5	IN-	4.50	231.50	89.50	316.50
6	DNC(1)	4.50	135.50	89.50	220.50
7	VOCM	283.85	4.50	368.85	89.50
8	DNC(1)	378.85	4.50	463.85	89.50
9	VS+	473.85	4.50	558.85	89.50
10	DNC(1)	568.85	4.50	653.85	89.50
11	VS+	663.85	4.50	748.85	89.50
12	DNC(1)	758.85	4.50	843.85	89.50
13	DNC(1)	1010.50	92.65	1095.50	177.65
14	OUT+	1010.50	188.65	1095.50	273.65
15	DNC(1)	1010.50	363.50	1095.50	448.50
16	DNC(1)	1010.50	458.50	1095.50	543.50
17	OUT-	1010.50	633.35	1095.50	718.35
18	DNC(1)	1010.50	729.35	1095.50	814.35
19	DNC(1)	758.85	817.50	843.85	902.50
20	VS-	663.85	817.50	748.85	902.50
21	DNC(1)	568.85	817.50	653.85	902.50
22	VS-	473.85	817.50	558.85	902.50
23	DNC(1)	378.85	817.50	463.85	902.50
24	PD	283.85	817.50	368.85	902.50

(1) DNC pads are covered with passivation and cannot be used.

6 Pin Configuration and Functions

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	PAD NO.		
IN+	2	I	Noninverting (positive) amplifier input
IN–	5	I	Inverting (negative) amplifier input
OUT+	14	O	Noninverted (positive) amplifier output
OUT–	17	O	Inverted (negative) amplifier output
$\overline{PD}$	24	I	Power down. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
Vocm	7	I	Common-mode voltage input
Vs+	9	I	Positive power-supply input
	11		
Vs–	20	I	Negative power-supply input
	22		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, (Vs+) – Vs–		5.5	V
	Input/output voltage range	(Vs–) – 0.5	(Vs+) + 0.5	
	Differential input voltage		±1	
Current	Continuous input current		±20	mA
	Continuous output current		±80	
	Continuous power dissipation			
Temperature	Maximum junction		150	°C
	Operating free-air	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs+	Single-supply voltage	2.7	5	5.4	V
T_J	Junction temperature	–40	25	125	°C

7.3 Electrical Characteristics: (Vs+) - Vs- = 5 V

At T_A ≈ 25°C, Vocm = open (defaults midsupply), V_{OUT}= 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1		620		MHz
		Vout = 100 mV_{PP}, G = 2		500		MHz
		Vout = 100 mV_{PP}, G = 5		210		MHz
		Vout = 100 mV_{PP}, G = 10		125		MHz
	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20		850		MHz
	Large-signal bandwidth	Vout = 2 V_{PP}, G = 2		340		MHz
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}, G = 2		100		MHz
	Slew rate(1)	Vout = 2-V_{PP}, FPBW		1500		V/µs
	Rise/fall time	Vout = 2-V step, G = 2 input ≤ 0.3 ns t_r		1.4		ns
	Settling time	To 1%, Vout = 2-V step, t_r = 2 ns, G = 2		4		ns
		To 0.1%,Vout = 2-V step, t_r = 2 ns, G = 2		8		ns
	Overshoot and undershoot	Vout = 2-V step G = 2, input ≤ 0.3 ns t_r		10%		
	100-kHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2		–140		dBc
		Vout = 2 V_{PP}, G = 2, HD3		–140		dBc
	10-MHz harmonic distortion	Vout = 2 V_{PP}, G = 2, HD2		–95		dBc
		Vout = 2 V_{PP}, G = 2, HD3		–90		dBc

7.3 Electrical Characteristics: (Vs+) - Vs- = 5 V (continued)

At T_A ≈ 25°C, Vocm = open (defaults midsupply), V_{OUT}= 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone			–90		dBc
	3rd-order intermodulation distortion				–85		dBc
	Input voltage noise	f > 100 kHz			2.2		nV/√Hz
	Input current noise	f > 1 MHz			1.9		pA/√Hz
	Overdrive recovery time	2x output overdrive, either polarity			20		ns
	Closed-loop output impedance	f = 10 MHz (differential)			0.1		Ω
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain			100	119		dB
	Input-referred offset voltage			–900	±100	900	µV
	Input offset voltage drift(2)	T_A = –40°C to +125°C			±0.5		µV/°C
	Input bias current (positive out of node)				10	15	µA
	Input bias current drift(2)	T_A = –40°C to +125°C			6		nA/°C
	Input offset current			–650	±150	650	nA
	Input offset current drift(2)	T_A = –40°C to +125°C			±0.3		nA/°C
INPUT							
	Common-mode input low	< 3-dB degradation in CMRR from midsupply			(Vs–) – 0.2	(Vs–) – 0.1	V
	Common-mode input high			(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at ((Vs+) – Vs–) / 2		85	100		dB
	Input impedance differential mode				110 || 0.85		kΩ || pF
OUTPUT							
	Output voltage low				(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high			(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive			±75	±100		mA
POWER SUPPLY							
	Specified operating voltage			2.7	5	5.4	V
	Quiescent operating current	Vs+ = 5 V	Vs+ = 5 V	9.7	10.1	10.5	mA
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout		85	100		dB
POWER DOWN							
	Enable voltage threshold			(Vs–) + 1.7			V
	Disable voltage threshold					(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+			20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V			6	30	µA
		$\overline{PD}$ = Vs–			2	8	µA
	Turnon-time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value			100		ns
	Turnoff time delay				60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(3)							
	Small-signal bandwidth	Vocm = 100 mV_{PP}			150		MHz
	Slew rate(1)	Vocm = 2-V step			400		V/µs
	Gain			0.975	0.982	0.995	V/V

7.3 Electrical Characteristics: (Vs+) - Vs- = 5 V (continued)

At T_A ≈ 25°C, Vocm = open (defaults midsupply), V_{OUT}= 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = +Vs, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input bias current	Considered positive out of node	–0.8	0.1	0.8	µA
	Input impedance	Vocm input driven to ((Vs+) – Vs–) / 2		47 || 1.2		kΩ || pF
	Default voltage offset from ((Vs+) – Vs–) / 2	Vocm pin open	–40	±8	40	mV
CM Vos	Common-mode offset voltage	Vocm input driven to ((Vs+) – Vs–) / 2	–5	±2	5	mV
	Common-mode offset voltage drift(2)			±4		mV/°C
	Common-mode loop supply headroom to negative supply	< ±12-mV shift from midsupply CM Vos	0.88			V
	Common-mode loop supply headroom to positive supply		1.1			V

(1) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_P / \sqrt{2}) \cdot 2\pi \cdot f_{-3dB}$.
(2) Input offset voltage drift, input bias current drift, input offset current drift, and Vocm drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range.
(3) Specifications are from the input Vocm pin to the differential output average voltage.

7.4 Typical Characteristics 5-V Single Supply

at Vs+ = 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, R_F = 402 Ω, Gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

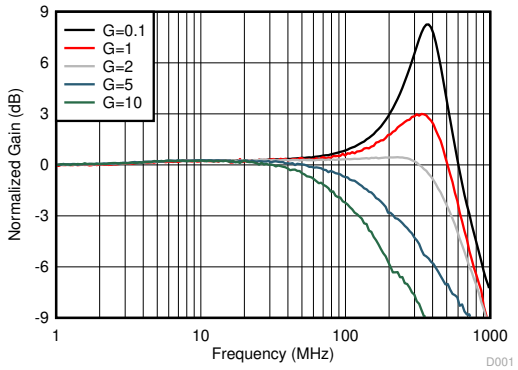


Figure 7-1. Small-Signal Frequency Response vs Gain

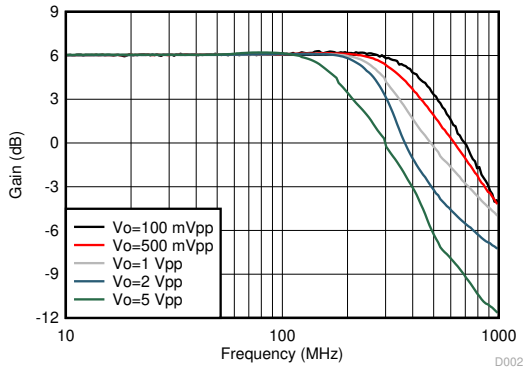
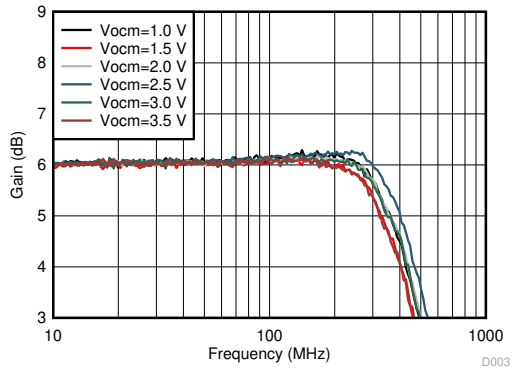
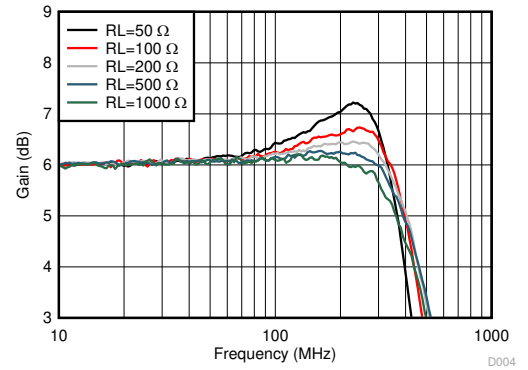


Figure 7-2. Frequency Response vs Vopp



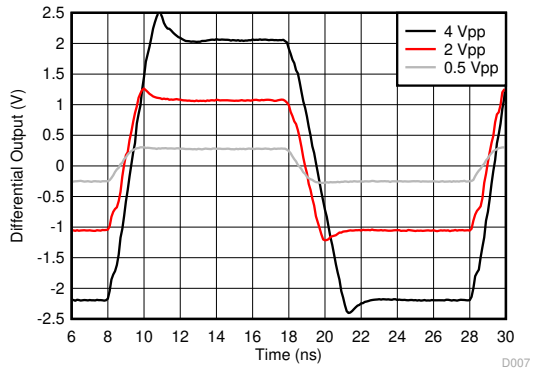
Vout = 100 mV_{PP}

Figure 7-3. Small-Signal Frequency Response vs Vocm



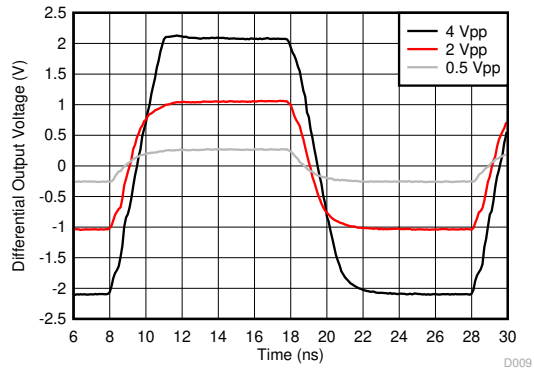
Vout = 100 mV_{PP}

Figure 7-4. Small-Signal Frequency Response vs Rload (RL)



50-MHz input, 0.3-ns input edge rate, single-ended to differential output, DC coupled

Figure 7-5. Small- and Large-Signal Step Response

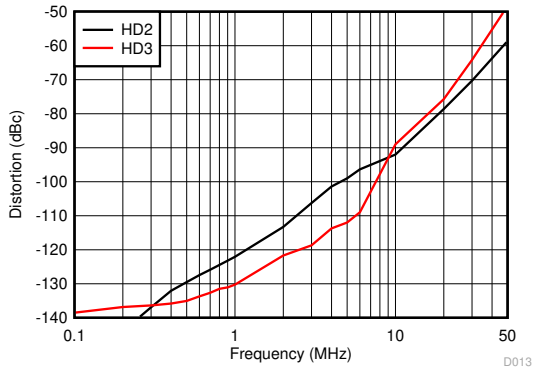


G = 5 V/V, 50-MHz input, 0.3-ns input edge rate, single-ended input to differential output

Figure 7-6. Small- and Large-Signal Step Response

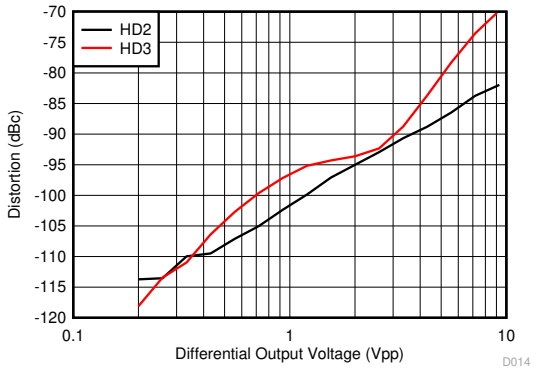
7.4 Typical Characteristics 5-V Single Supply (continued)

at Vs+ = 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, R_F = 402 Ω, Gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



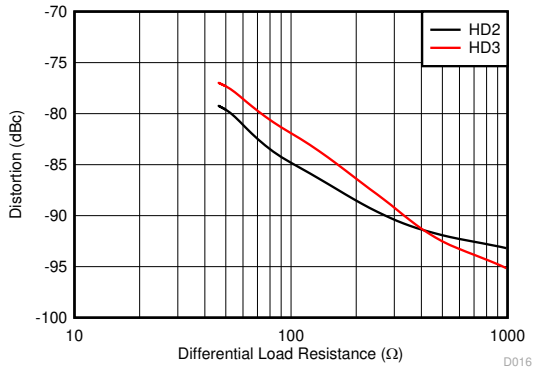
Vo = 2-V_{PP}

Figure 7-7. Harmonic Distortion Over Frequency



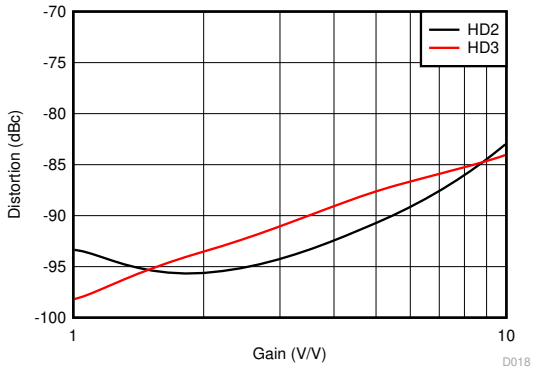
f = 10 MHz

Figure 7-8. Harmonic Distortion vs Output Swing



f = 10 MHz

Figure 7-9. Harmonic Distortion vs Rload



f = 10 MHz, Vo = 2-V_{PP}

Figure 7-10. Harmonic Distortion vs Gain

7.5 Typical Characteristics: 3-V to 5-V Supply Range

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, R_F = 402 Ω,Gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

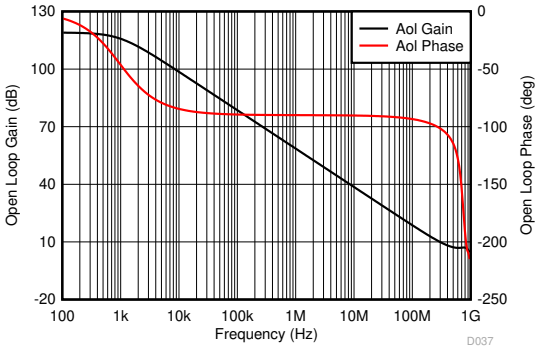
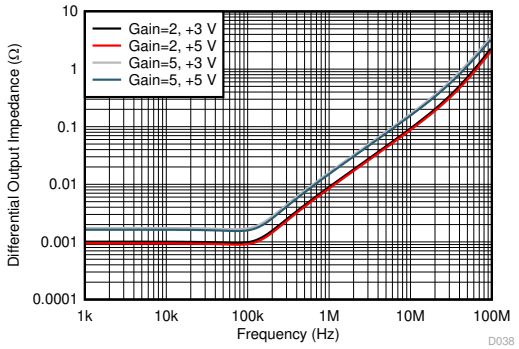


Figure 7-11. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Single-ended input to differential output, simulated differential output impedance, (closed-loop) gain of 2 and 5

Figure 7-12. Closed-Loop Output Impedance

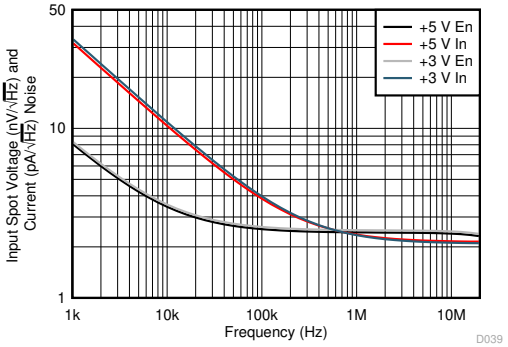
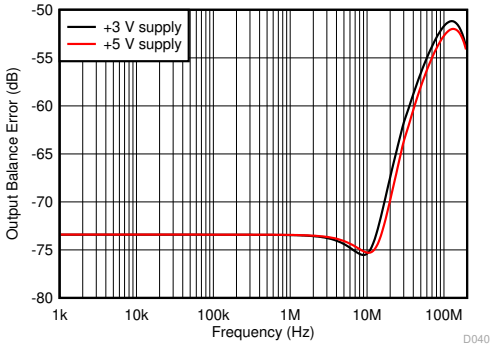
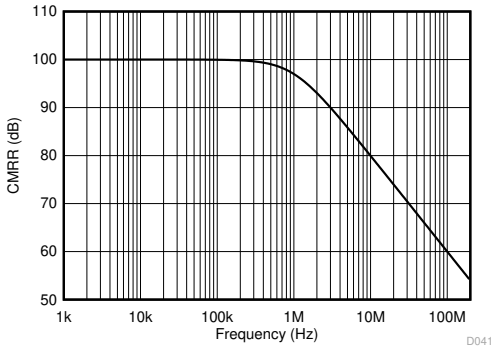


Figure 7-13. Input Spot Noise Over Frequency



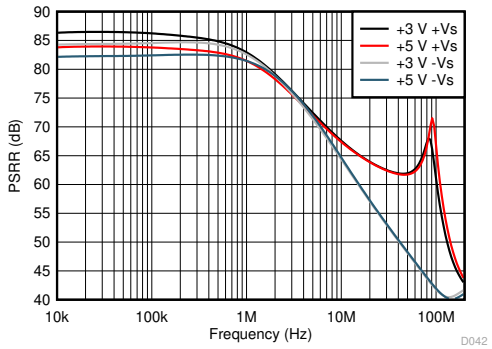
Single-ended input to differential output, gain of 2, simulated with 1% resistor, worst-case mismatch

Figure 7-14. Output Balance Error Over Frequency



Common-mode in to differential out, gain of 2 simulation

Figure 7-15. CMRR Over Frequency



Single-ended to differential, gain of 2
PSRR simulated to differential output

Figure 7-16. PSRR Over Frequency

7.5 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, R_F = 402 Ω,Gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)

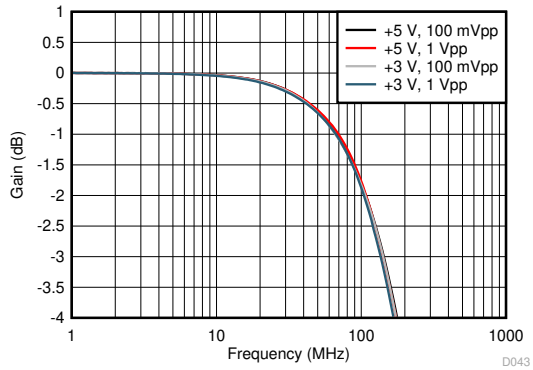
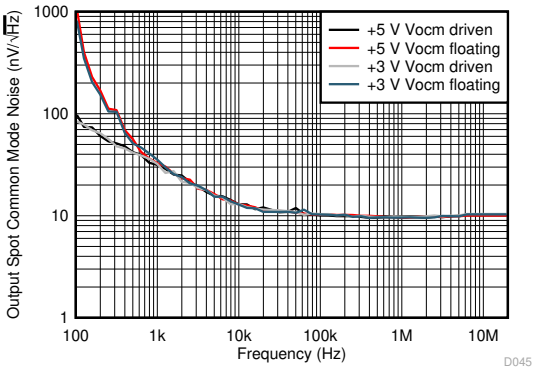
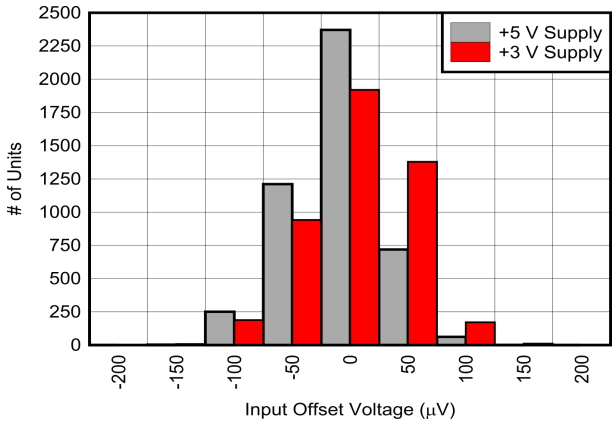


Figure 7-17. Common-Mode, Small- and Large-Signal Response (Vocm pin driven)



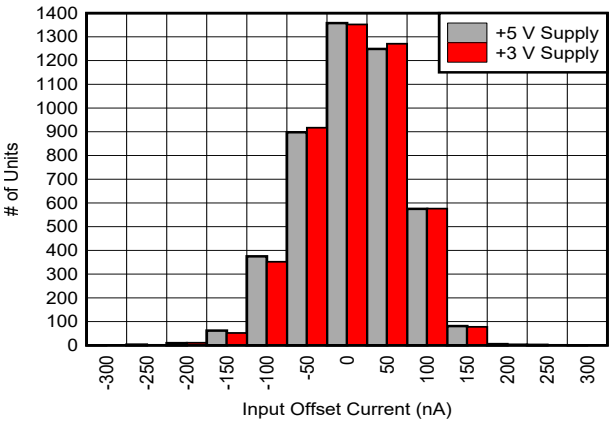
Vocm input either driven to mid-supply by low impedance source, or allowed to float and default to mid-supply

Figure 7-18. Output Common-Mode Noise



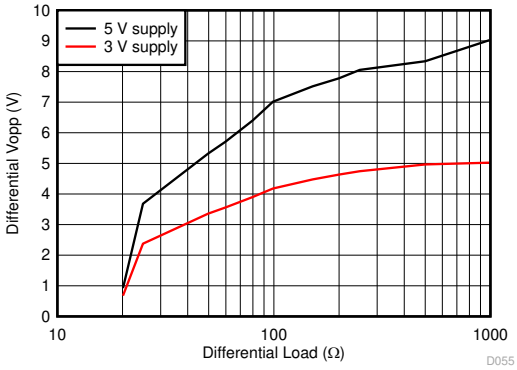
Total of 4618 units, At Vs = 5V: µ = -35.1µV, σ = 38.9µV

Figure 7-19. Input Offset Voltage



Total of 4618 units, At Vs = 5V: µ = 16.7nA, σ = 62.3nA

Figure 7-20. Input Offset Current



Maximum differential output swing, Vocm at midsupply

Figure 7-21. Maximum Vopp vs Rload

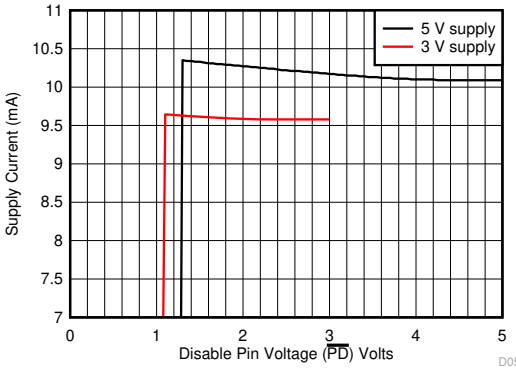
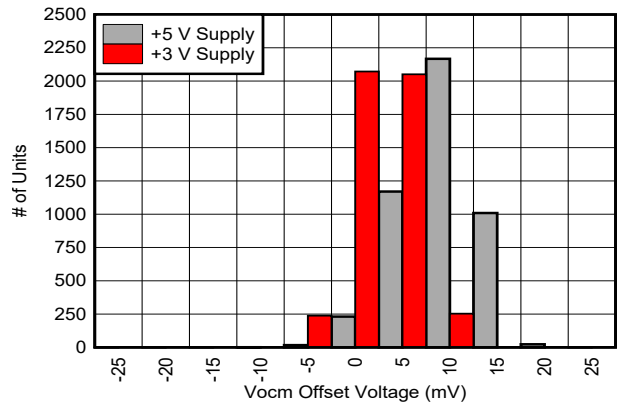


Figure 7-22. Supply Current vs $\overline{PD}$ Voltage

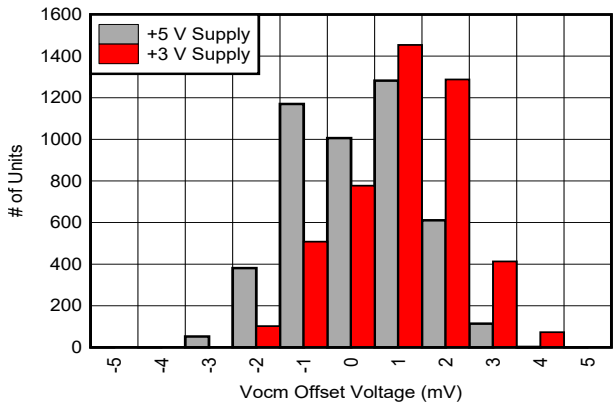
7.5 Typical Characteristics: 3-V to 5-V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, Vocm is open, 50-Ω single-ended input to differential output, R_F = 402 Ω,Gain = 2 V/V, Rload = 500 Ω, and T_A ≈ 25°C (unless otherwise noted)



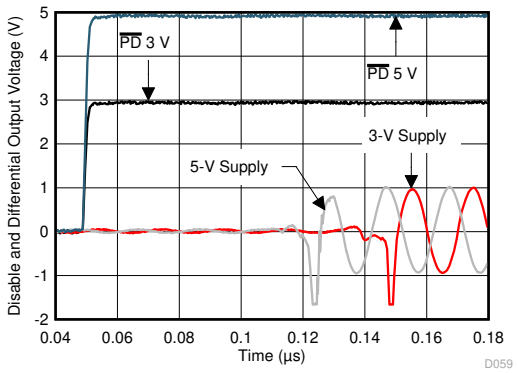
Vocm input floating, Total of 4618 units,
At Vs = 5V: μ = 6.8mV, σ = 3.9mV

Figure 7-23. Common-Mode Output Offset from Vs+ / 2 Default Value



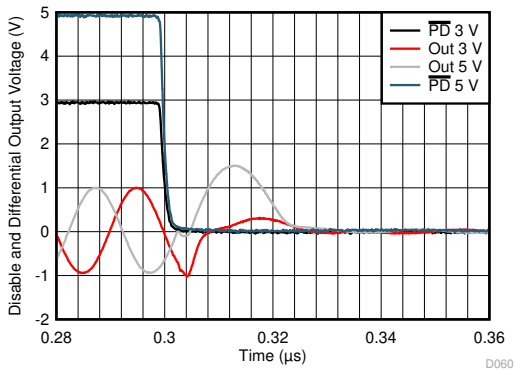
Total of 4618 units, At Vs = 5V: μ = -0.3mV, σ = 1.3mV

Figure 7-24. Common-Mode Output Offset from Driven Vocm



10 MHz, 1-Vpp input single to differential gain of 2

Figure 7-25. $\overline{PD}$ Turn On Waveform



10 MHz, 1-V_{PP} input single to differential gain of 2

Figure 7-26. $\overline{PD}$ Turn Off Waveform

8 Detailed Description

8.1 Overview

The THS4541-DIE is a voltage-feedback (VFA) based, fully-differential amplifier (FDA) offering greater than 500-MHz, small-signal bandwidth at a gain of 2 V/V with trimmed supply current and input offset voltage. The core differential amplifier is a slightly decompensated voltage-feedback design with a high slew-rate, precision input stage. This design gives the 500-MHz gain of 2-V/V small-signal bandwidth shown in the characterization curves, with a 1500-V/µs slew rate, yielding approximately a 340-MHz, 2-V_{PP}, large-signal bandwidth in the same circuit configuration.

The outputs offer near rail-to-rail output swing (0.2-V headroom to either supply), while the device inputs are negative rail inputs with approximately 1.2 V of headroom required to the positive supply. This negative rail input directly supports a bipolar input around ground in a dc-coupled, single-supply design. Similar to all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the Vocm input pin that can be either floated to default near midsupply or driven to a desired output common-mode voltage. The Vocm range extends from a very low 0.91 V above the negative supply to 1.1 V below the positive supply, supporting a wide range of modern analog-to-digital converter (ADC) input common-mode requirements using a single 2.7-V to 5.4-V supply range for the THS4541-DIE.

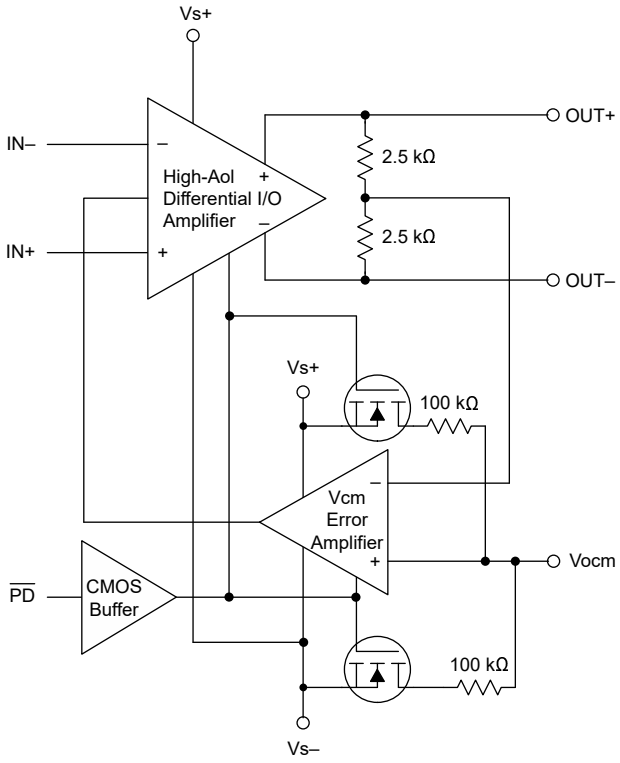
A power-down pin ($\overline{PD}$) is included. Pull the $\overline{PD}$ pin voltage to the negative supply to turn the device off, putting the THS4541-DIE into a very-low quiescent current state. For normal operation, the $\overline{PD}$ pin must be asserted high. When the device is disabled, remember that the signal path is still present through the passive external resistors. Input signals applied to a disabled THS4541-DIE still appear at the outputs at some level through this passive resistor path as they would for any disabled FDA device.

8.1.1 Terminology and Application Assumptions

Like all widely-used devices, numerous common terms have developed that are unique to this type of device. These terms include:

- Fully differential amplifier (FDA)—In this document, this term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not high-impedance input) and includes a second internal control-loop setting the output average voltage (Vocm) to a default or set point. This second loop interacts with the differential loop in some configurations.
- The desired output signal at the two output pins is a *differential* signal swinging symmetrically around a *common-mode* voltage where that is the average voltage for the two outputs.
- Single-ended to differential—always use the outputs differentially in an FDA; however, the source signal can be either a single-ended source or differential, with a variety of implementation details for either. When the FDA operation is single-ended to differential, only one of the two input resistors receives the source signal with the other input resistor connected to a DC reference (often ground) or through a capacitor to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Differential I/O

The THS4541-DIE combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage with a dominant pole at approximately 900 Hz. This voltage feedback structure projects a single-pole, unity-gain Aol at 850 MHz (gain bandwidth product). The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the Vocm pin. If floated, this reference is at half the total supply voltage across the device using two 100-kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the Vocm pin. The bandwidth of this error amplifier is approximately the same bandwidth as the main differential I/O amplifier.

The differential outputs are collector outputs to obtain the rail-to-rail output swing. These outputs are relatively high-impedance, open-loop sources; however, closing the loop provides a very low output impedance for load driving. No output current limit or thermal shutdown features are provided in this lower-power device. The differential inputs are PNP inputs to provide a negative-rail input range.

To operate the THS4541-DIE connect the OUT– pin to the IN+ pin through an Rf, and the OUT+ pin to the IN– pin through the same value of Rf.Bring in the inputs through additional resistors to the IN+ and IN– pins. The differential I/O op amp operates similarly to an inverting op amp structure where the source must drive the input resistor and the gain is the ratio of the feedback to the input resistor.

8.3.2 Power-Down Control Pin ($\overline{PD}$)

The THS4541-DIE includes a power-down control pin, $\overline{PD}$. This pin must be asserted high for correct amplifier operation. The $\overline{PD}$ pin cannot be floated because there is no internal pullup or pulldown resistor on this pin to reduce disabled power consumption. Asserting this pin low (within 0.7 V of the negative supply) puts the THS4541-DIE into a very low quiescent state (approximately 2 µA). Switches in the default Vocm resistor string open to eliminate the fixed bias current (25 µA) across the supply in this 200-kΩ voltage divider to mid-supply.

8.3.2.1 Operating the Power Shutdown Feature

Assert this CMOS input pin to the desired voltage for operation. For applications that require the device to only be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

When the $\overline{PD}$ pin is somewhat below the positive supply pin, slightly more quiescent current is drawn; see Figure 7-22. For the minimum-on power, assert this pin to the positive supply.

The disable operation is referenced from the negative supply; normally, ground. For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the THS4541-DIE off when the negative supply exceeds –0.7 V.

For single-supply operation, a minimum of 1.7 V above the negative supply (ground, in this case) is required to assure operation. This minimum logic-high level allows for direct operation from 1.8-V supply logic.

8.3.3 Input Overdrive Operation

The THS4541-DIE input stage architecture is intrinsically robust to input overdrives with the series input resistor required by all applications. High input overdrives cause the outputs to limit into their maximum swings with the remaining input current through the Rg resistors absorbed by internal, back-to-back protection diodes across the two inputs. These diodes are normally off in application, and only turn on to absorb the currents that a large input overdrive might produce through the source impedance and or the series Rg elements required by all designs.

The internal input diodes can safely absorb up to ±15 mA in an overdrive condition. For designs that require more current to be absorbed, consider adding an external protection diode such as the BAV99 device used in the example ADC interface design of Figure 9-1.

8.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than (Vs–) + 1.7 V, or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The Vocm control pin sets the output average voltage. Left open, Vocm defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal Vcm error amplifier.

8.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the Rg value. This input active impedance issue applies to both AC- and DC-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in the following subsections.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The THS4541-DIE offers an effective solution over a broad range of applications. The example shown here is a gain of 2 V/V, matched input of 50 Ω to an output set to 0.95 V common-mode followed by a third-order Bessel filter with approximately 20 MHz of bandwidth feeding into the ADC34J22, a low-power, 12-bit, quad 50-MSPS JESD 204B ADC.

9.2 Typical Applications

9.2.1 Interfacing to High-Performance ADCs

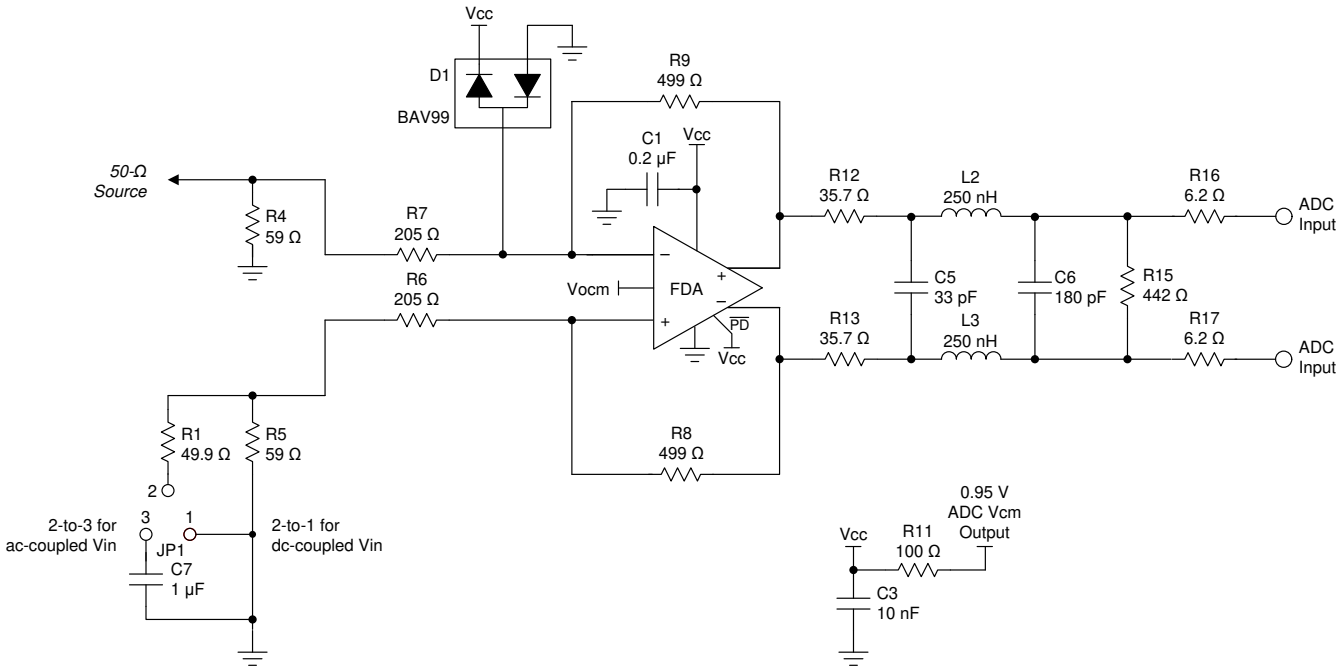


Figure 9-1. DC-Coupled, Bipolar Input Gain of 2 V/V Single-Ended to Differential Interface to ADC

9.2.1.1 Design Requirements

In this example design, an impedance matched input assuming a 50-Ω source is implemented with a DC-coupled gain of 2 V/V to the ADC. This configuration effectively reduces the required full-scale input to ±0.5 V for a 2-V_{PP} full-scale input ADC. Add a low insertion-loss interstage filter to the ADC to control the broadband noise where the goal is to show minimal SNR reduction in the FFT, as well as minimal degradation in SFDR performance.

9.2.1.2 Detailed Design Procedure

The THS4541-DIE provides a very flexible element for interfacing from a variety of sources to a wide range of ADCs. Because all precision and high-speed ADCs require a differential input on a common-mode voltage, this design is the primary application for the THS4541-DIE.

The THS4541-DIE provides a simple interface to a wide variety of precision SAR, ΔΣ, or higher-speed pipeline ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than typically required in the signal path to the ADC inputs is provided by the THS4541-DIE. For instance, the gain of 2 single-ended to differential design example provides approximately a 500-MHz, small-signal bandwidth. Even if the source signal is Nyquist bandlimited, this broad bandwidth can possibly integrate enough THS4541-DIE noise to degrade the SNR through the ADC if the broadband noise is not bandlimited between the amplifier and ADC.

Figure 9-1 shows an example DC-coupled, gain of 2 interface with a controlled, interstage-bandwidth filter implemented on the demonstration board for the JESD digital-output interface, ADC34J22 (a 50-MSPS, quad, 12-bit ADC). This board uses the packaged THS4541 and is called the DEV-ADC34J22 ADC HSMC MODULE with complete documentation at dallaslogic.com.

Designed for a DC-coupled 50Ω input match, this design starts with a 499-Ω feedback resistor, and provides a gain of 2.35V/V to the THS4541 output pins. The third-order interstage, low-pass filter provides a 20-MHz Bessel response with a 0.85 V/V insertion loss to the ADC, providing a net gain of 2 V/V from board edge to the ADC inputs. Although the THS4541 can absorb overdrives, an external protection element is added using the BAV99 low-capacitance device, shown in Figure 9-1. For DC-coupled testing, pins 1 and 2 are jumpered together. When the source is an AC-coupled, 50-Ω source, pins 2 and 3 are jumpered to maintain differential balance. FFT testing normally uses a bandpass filter into the board; an AC-coupled source. A typical 5-MHz, full-scale, single-tone FFT is shown in Figure 9-2, where the jumper is placed from pins 2 to 3. The reported SNR of 70.09 dBFs is only a slight reduction from the tested ADC-only performance of 70.42 dBFs, showing the value of the interstage noise bandwidth limiting filter. The exceptionally low harmonic distortion for the THS4541 also shows up in the very low SFDR and THD shown in Figure 9-2. This 96-dB SFDR and 92.83-dB THD are comparable to the ADC-only test results.

9.2.1.3 Application Curve

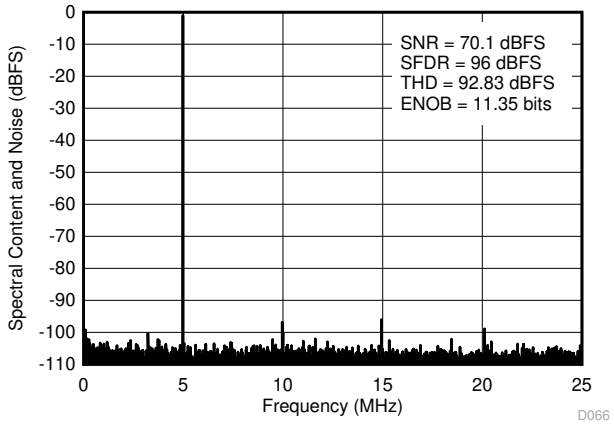


Figure 9-2. 5-MHz FFT, 50-MSPS Test for the Gain of 2 Interface in Figure 9-1

10 Power Supply Recommendations

The THS4541-DIE is principally intended to operate with a nominal single-supply voltage of +3 V to +5 V. Supply-voltage tolerances are supported with the specified operating range of 2.7 V (10% low on a 3-V nominal supply) and 5.4 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in Section 8.1.1. Split (or bipolar) supplies can be used with the THS4541-DIE, as long as the total value across the device remains less than 5.5 V (absolute maximum).

Using a negative supply to deliver a true swing to ground output in driving SAR ADCs may be desired. While the THS4541-DIE quotes a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3-V to 5-V positive supply input used by the THS4541-DIE and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective solution, as described in *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts*.

11 Layout

11.1 Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with a close attention to board layout. For the THS4541-DIE, general high-speed signal-path layout suggestions include:

- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. A supply decoupling capacitor across the two power supplies (for bipolar operation) should also be added. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- For each THS4541-DIE, attach a separate 0.1-µF capacitor to a nearby ground plane. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor is often useful to the local high-frequency decoupling capacitor.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Connect any Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the Rg elements can have more trace length if needed to the source or to ground.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA Simulation Model Features

The device model is available as part of the TINA model library. The model includes numerous features intended to speed designer progress over a wide range of application requirements. The following list shows the performance parameters included in the model:

- For the small-signal response shape with any external circuit:
  - Differential open loop gain and phase
  - Parasitic input capacitance
  - Open-loop differential output impedance
- For noise simulations:
  - Input differential spot voltage noise and a 100-kHz 1/f corner
  - Input current noise on each input with a 1-MHz 1/f corner
- For time-domain, step-response simulations:
  - Differential slew rate
  - I/O headroom models to predict clipping
  - Fine-scale, DC precision terms:
    - PSRR
    - CMRR

The typical characterization curves show more detail than the macromodels can provide; some of those unmodeled features include:

- Harmonic distortion
- Temperature drift in DC error terms (V_{IO} and I_{OS})

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ADC34J2x Quad-Channel, 12-Bit, 50-MSPS to 160-MSPS, Analog-to-Digital Converter with JESD204B Interface* data sheet
- Texas Instruments, *Design for a Wideband, Differential Transimpedance DAC Output* application report
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide
- Texas Instruments, *LM7705 Low-Noise Negative Bias Generator* data sheet
- Texas Instruments, *LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier* data sheet
- Texas Instruments, *THS451RGT EVM* user guide
- Texas Instruments, *Maximizing the dynamic range of analog front ends having a transimpedance amplifier* technical brief

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4541YR	ACTIVE	DIESALE	Y	0	3000	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF THS4541-DIE :

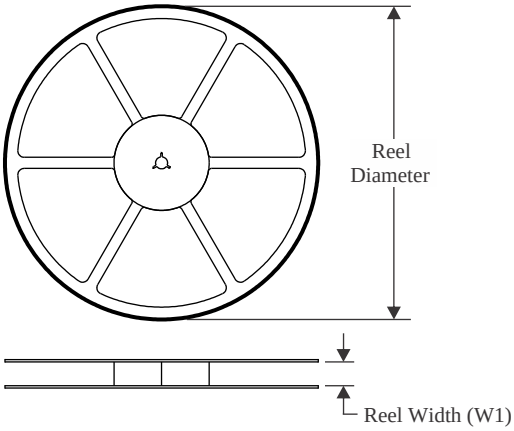
- Automotive : THS4541-Q1

NOTE: Qualified Version Definitions:

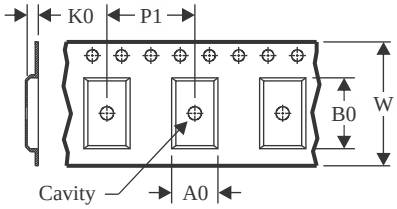
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

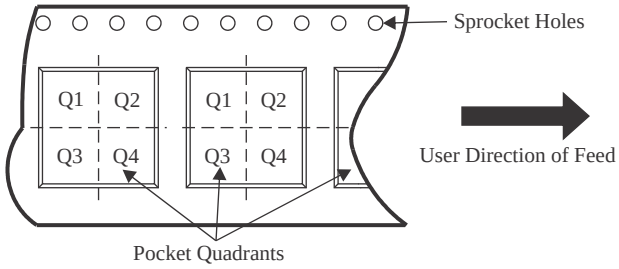


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

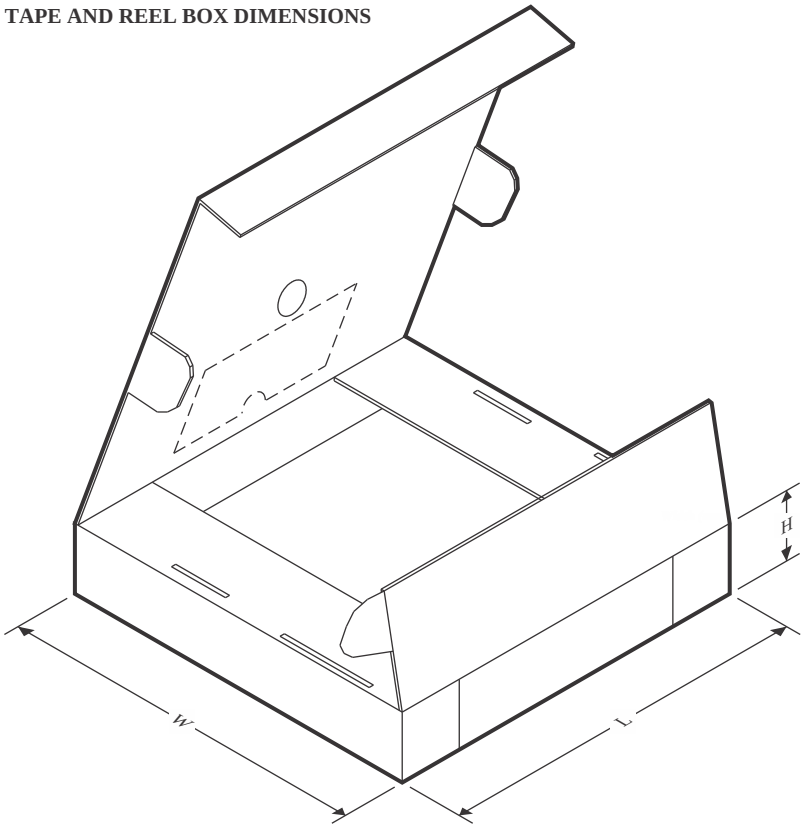
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4541YR	DIESALE	Y	0	3000	180.0	8.4	1.07	1.26	0.54	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4541YR	DIESALE	Y	0	3000	210.0	185.0	35.0

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