

SN74LV164A 8-Bit Parallel-Out Serial Shift Registers

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Maximum t_{pd} of 10.5 ns at 5 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Ioff supports live insertion, partial power-down mode, and back-drive protection
- Support mixed-mode voltage operation on all ports
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- IP routers
- Enterprise switches
- Access control and security: access keypads and biometrics
- Smart meters: power line communication

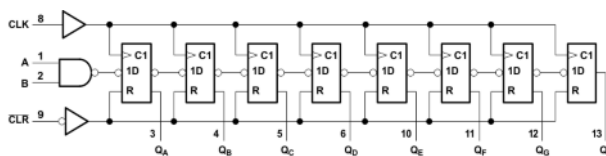
3 Description

The SN74LV164A devices are 8-bit parallel-out serial shift registers designed for 2 V to 5.5 V V_{CC} operation.

Package Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV164A	D (SOIC, 14)	8.65 mm × 3.91 mm
	DB (SSOP, 14)	6.20 mm × 5.30 mm
	DGV (TVSOP, 14)	3.60 mm × 4.40 mm
	NS (SOP, 14)	10.30 mm × 5.30 mm
	PW (TSSOP, 14)	5.00 mm × 4.40 mm
	RGY (VQFN, 14)	3.50 mm × 3.50 mm
	BQA (WQFN, 14)	3.00 mm × 2.50 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	7 Parameter Measurement Information	10
2 Applications	1	8 Detailed Description	11
3 Description	1	8.1 Overview.....	11
4 Revision History	2	8.2 Functional Block Diagram.....	11
5 Pin Configuration and Functions	3	8.3 Feature Description.....	11
6 Specifications	4	8.4 Device Functional Modes.....	11
6.1 Absolute Maximum Ratings.....	4	9 Application and Implementation	12
6.2 ESD Ratings.....	4	9.1 Application Information.....	12
6.3 Recommended Operating Conditions.....	5	9.2 Typical Application.....	12
6.4 Thermal Information.....	5	9.3 Power Supply Recommendations.....	13
6.5 Electrical Characteristics.....	6	9.4 Layout.....	13
6.6 Timing Requirements: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	10 Device and Documentation Support	15
6.7 Timing Requirements: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	10.1 Documentation Support.....	15
6.8 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	7	10.2 Receiving Notification of Documentation Updates..	15
6.9 Switching Characteristics: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	7	10.3 Support Resources.....	15
6.10 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	7	10.4 Trademarks.....	15
6.11 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	10.5 Electrostatic Discharge Caution.....	15
6.12 Noise Characteristics.....	8	10.6 Glossary.....	15
6.13 Operating Characteristics.....	8	11 Mechanical, Packaging, and Orderable Information	15
6.14 Typical Characteristics.....	9		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (December 2022) to Revision K (March 2023)	Page
• Updated the structural layout of document.....	1
• Updated thermal values for D package from R θ JA = 92.6 to 112.9, R θ JC(top) = 53.9 to 68.7, R θ JB = 46.8 to 69.4, Ψ JT = 18.9 to 30, Ψ JB = 46.6 to 69, all values in °C/W.....	5

Changes from Revision I (February 2015) to Revision J (December 2022)	Page
• Updated the format of tables, figures, and cross-references throughout the document.....	1

Changes from Revision H (April 2005) to Revision I (February 2015)	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1

5 Pin Configuration and Functions

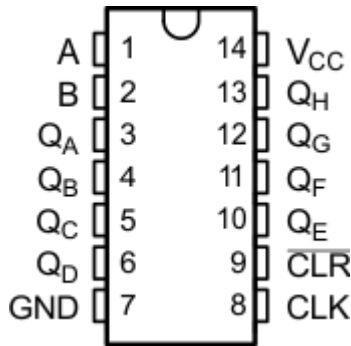


Figure 5-1. D, DB, DGV, NS, or PW Package 14-PIN SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)

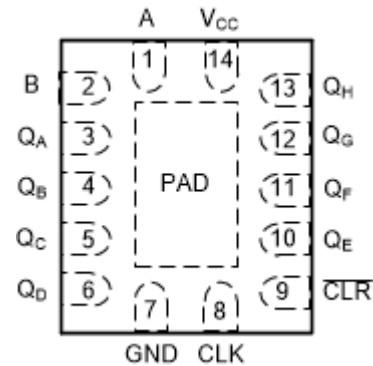


Figure 5-2. RGY or BQA Package 14-PIN VQFN or WQFN Top View

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	A	I	Serial input A
2	B	I	Serial input B
3	Q _A	O	Output A
4	Q _B	O	Output B
5	Q _C	O	Output C
6	Q _D	O	Output D
7	GND	—	Ground pin
8	CLK	I	Storage clock
9	$\overline{\text{CLR}}$	I	Storage clear
10	Q _E	O	Output E
11	Q _F	O	Output F
12	Q _G	O	Output G
13	Q _H	O	Output H
11	Q _H '	O	Q _H inverted
14	V _{CC}	—	Power pin
-	PAD	—	Thermal Pad ⁽²⁾

(1) I = input, O = output

(2) RGY and BQA packages only

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
V_I	Input voltage ⁽¹⁾	-0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽¹⁾	-0.5	7	V
V_O	Output voltage ^{(1) (2)}	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-20 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25 mA
	Continuous current through V_{CC} or GND			±50 mA
T_{stg}	Storage temperature	-65	150	°C

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV164A		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	
		V _{CC} = 3 V to 3.6 V	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	
		V _{CC} = 3 V to 3.6 V	6	
		V _{CC} = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV164A							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	92.6	104.4	126.7	89.3	138.7	74.8	88.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	53.9	57	50	46.9	69.1	81.1	90.9	
R _{θJB}	Junction-to-board thermal resistance	46.8	51.7	59.6	48	81.8	49.5	56.8	
ψ _{JT}	Junction-to-top characterization parameter	18.9	18.6	5.8	13.7	20.3	15	9.9	
ψ _{JB}	Junction-to-board characterization parameter	46.6	51.2	58.9	47.7	81.3	49.5	56.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	32.5	33.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV164A –40°C to 85°C			SN74LV164A –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1			V
	I _{OL} = 2 mA	2.3 V				0.4			
	I _{OL} = 6 mA	3 V				0.44			
	I _{OL} = 12 mA	4.5 V				0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V				±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5				20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0				5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.2			2.2			pF

6.6 Timing Requirements: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T _A = 25°C		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL _R low	6		6.5		6.5		ns
		CLK high or low	6.5		7.5		7.5		
t _{su}	Setup time	Data before CLK↑	6.5		8.5		8.5		ns
		CL _R inactive	3		3		3		
t _h	Hold time	Data after CLK↑	–0.5		0		0		ns

6.7 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T _A = 25°C		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CL _R low	5		5		5		ns
		CLK high or low	5		5		5		
t _{su}	Setup time	Data before CLK↑	5		6		6		ns
		CL _R inactive	2.5		2.5		2.5		
t _h	Hold time	Data after CLK↑	0		0		0		ns

6.8 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time	Data before CLK \uparrow	4.5		4.5		4.5		ns
		$\overline{\text{CLR}}$ inactive	2.5		2.5		2.5		
t_h	Hold time	Data after CLK \uparrow	1		1		1		ns

6.9 Switching Characteristics: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	55 ⁽¹⁾	105 ⁽¹⁾		50		50		MHz
			$C_L = 50\text{ pF}$	45	85		40		40		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		9.2 ⁽¹⁾	17.6 ⁽¹⁾	1	20	1	21	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			8.6 ⁽¹⁾	16 ⁽¹⁾	1	18	1	18.5	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		11.5	21.1	1	24	1	25	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			10.8	19.5	1	22	1	22.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80 ⁽¹⁾	155 ⁽¹⁾		65		65		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		6.4 ⁽¹⁾	12.8 ⁽¹⁾	1	15	1	16	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			6 ⁽¹⁾	12.8 ⁽¹⁾	1	15	1	16	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		8.3	16.3	1	18.5	1	19.5	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			7.9	16.3	1	18.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.11 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV164A –40°C to 85°C		SN74LV164A –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	125 ⁽¹⁾	220 ⁽¹⁾		105		95		MHz
			$C_L = 50\text{ pF}$	85	165		75		65		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$		4.5 ⁽¹⁾	9 ⁽¹⁾	1	10.5	1	11.5	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			4.2 ⁽¹⁾	8.6 ⁽¹⁾	1	10	1	11	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$		6	11	1	12.5	1	13	ns
t_{PHL}	$\overline{\text{CLR}}$	Q			5.8	10.6	1	12.5	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV164A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.28	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.22	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.09		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	48.1	pF
				5 V	47.5	

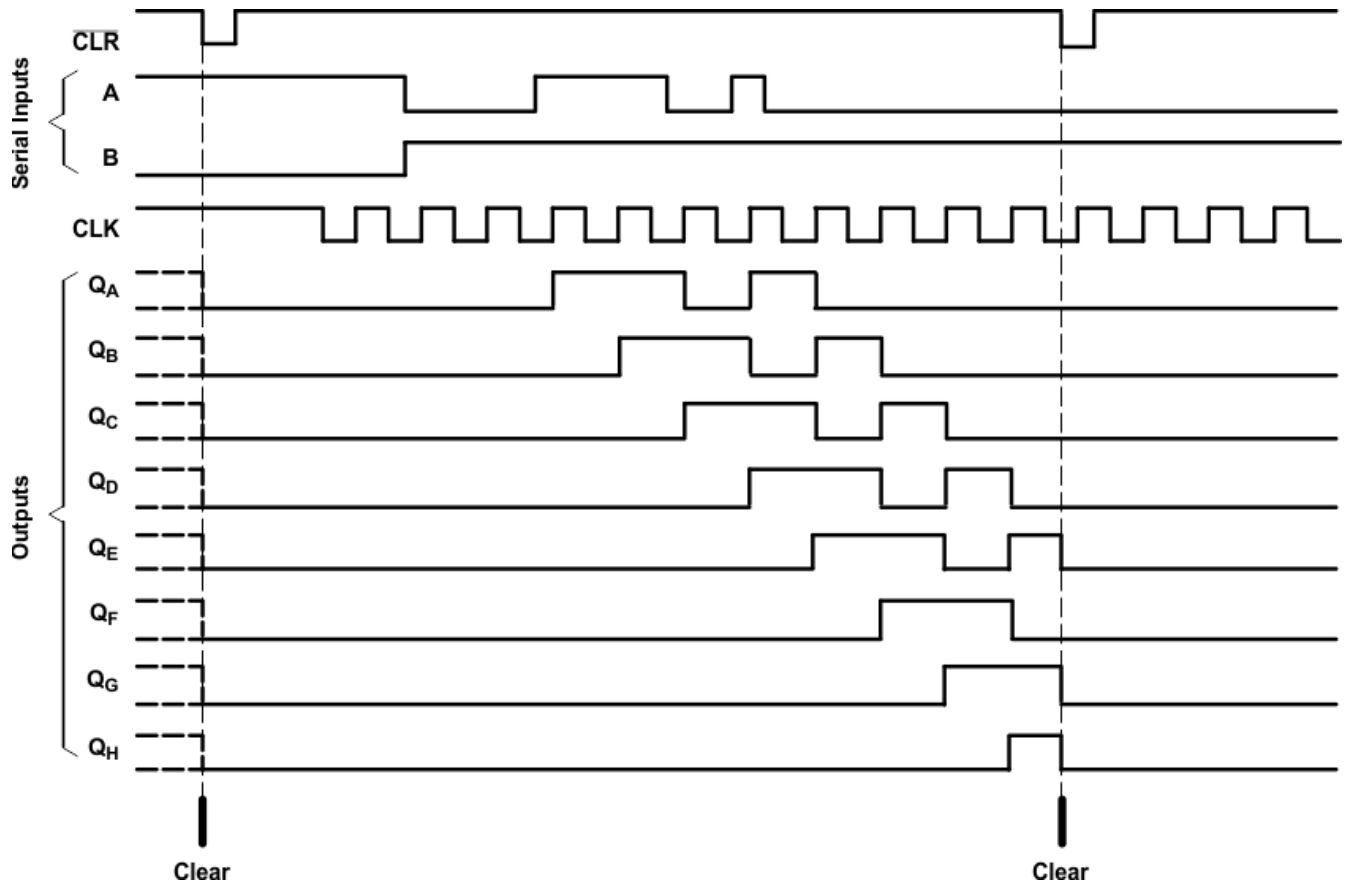
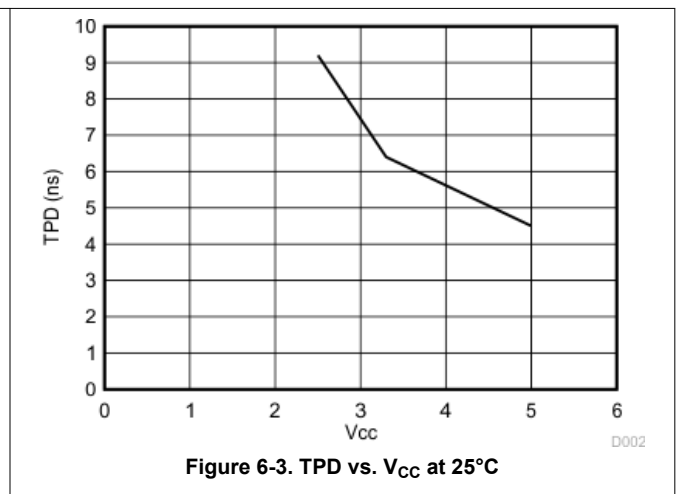
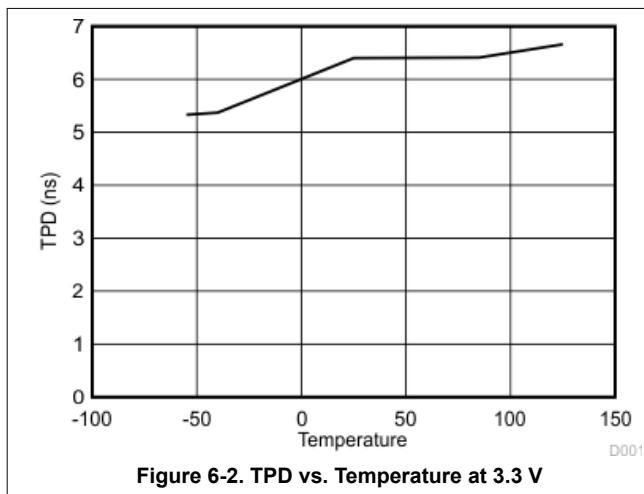
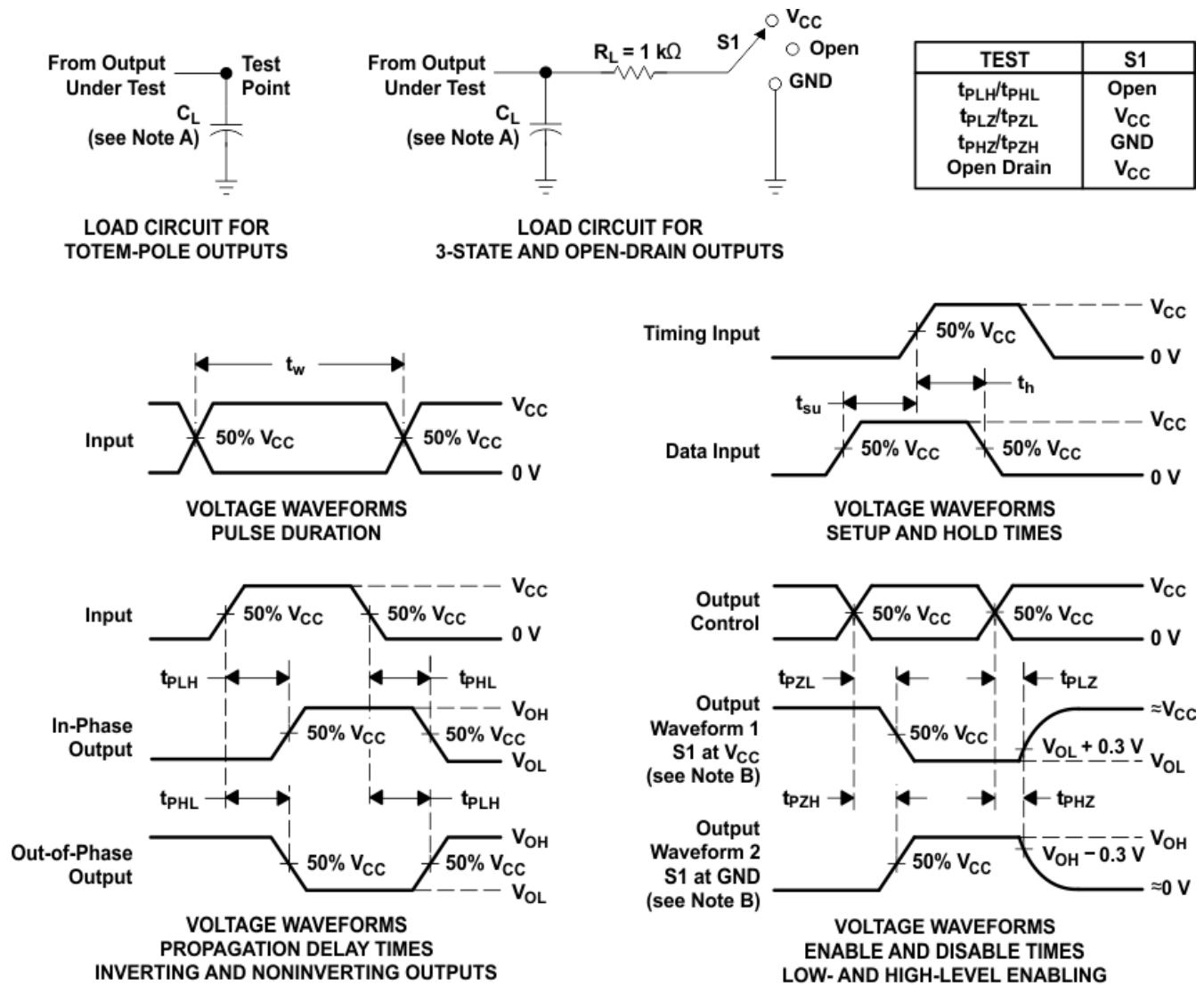


Figure 6-1. Typical Clear, Shift, and Clear Sequences

6.14 Typical Characteristics



7 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

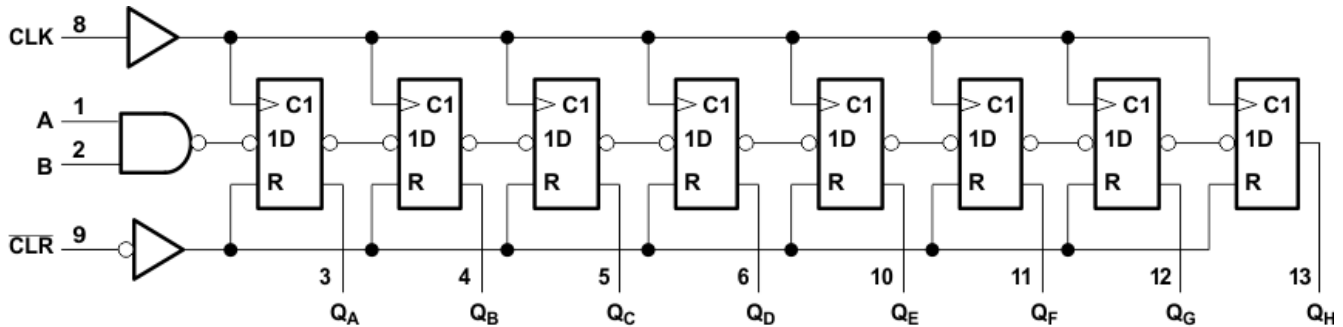
8 Detailed Description

8.1 Overview

The SNx4LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices feature NAND-gated serial (A and B) inputs and an asynchronous clear (\overline{CLR}) input. The gated serial inputs permit complete control over incoming data, as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 8-1. Function Table⁽¹⁾⁽²⁾

INPUTS				OUTPUTS			
CLR	CLK	A	B	Q _A	Q _B	...	Q _H
L	X	X	X	L	L		L
H	L	X	X	Q _{A0}	Q _{B0}		Q _{H0}
H	↑	H	H	H	Q _{An}		Q _{Gn}
H	↑	L	X	L	Q _{An}		Q _{Gn}
H	↑	X	L	L	Q _{An}		Q _{Gn}

- (1) Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
- (2) Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a 1-bit shift.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV164A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

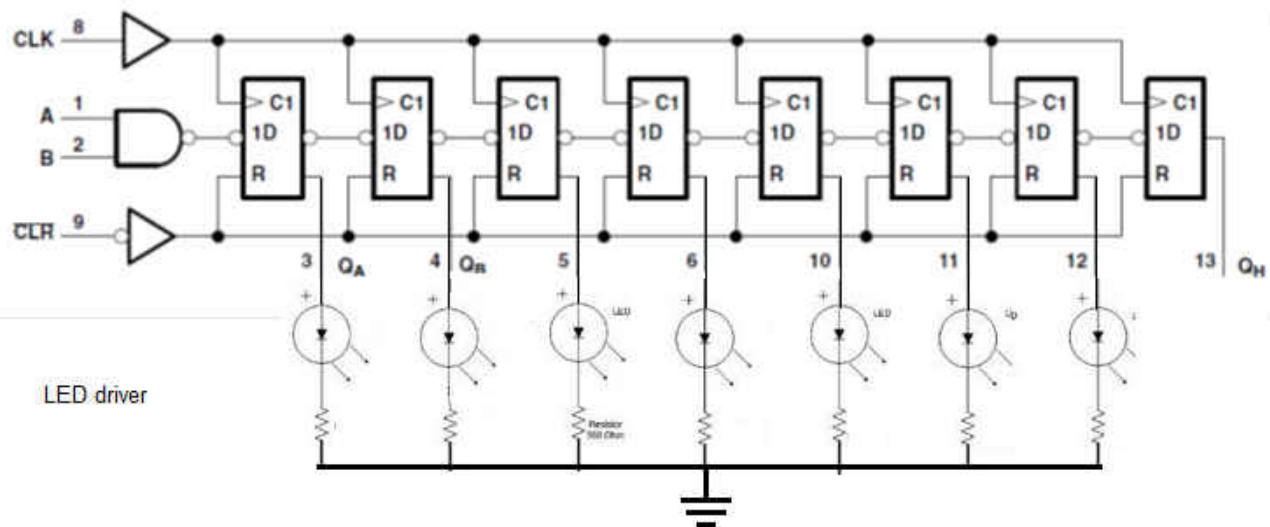


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in [Section 6.3](#).
 - Specified high and low level. See $(V_{IH}$ and $V_{IL})$ in [Section 6.3](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

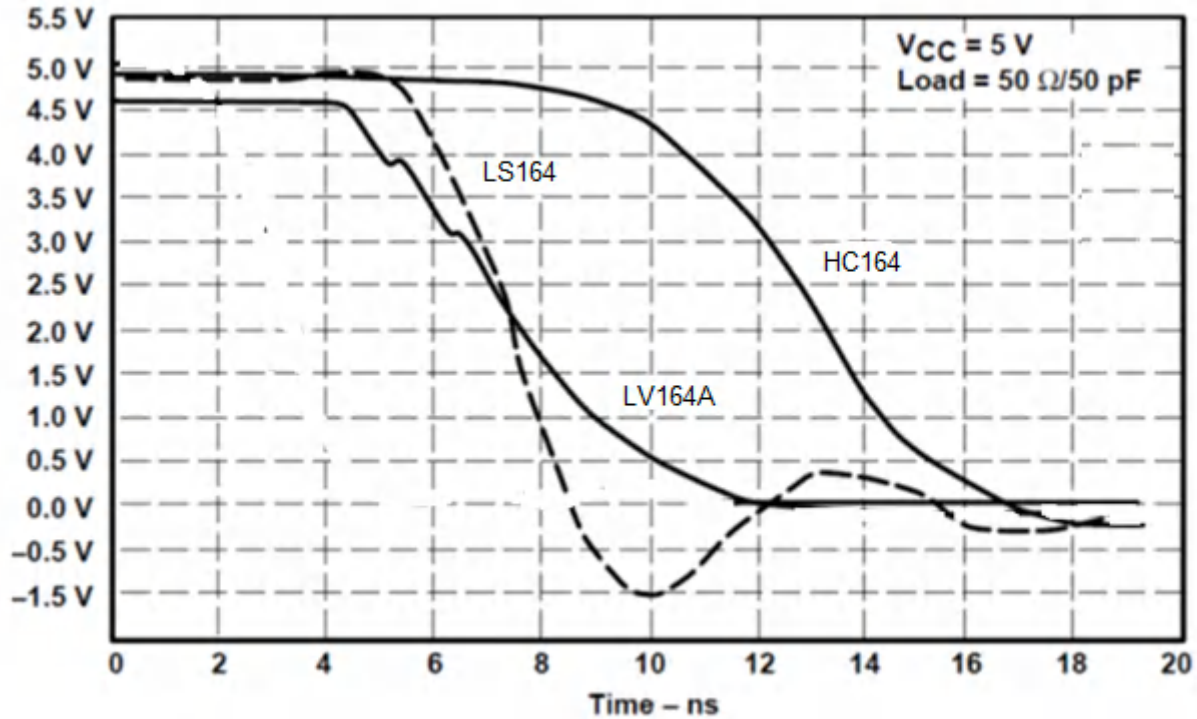


Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 6.3](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μF or 0.022- μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

9.4.2 Layout Example

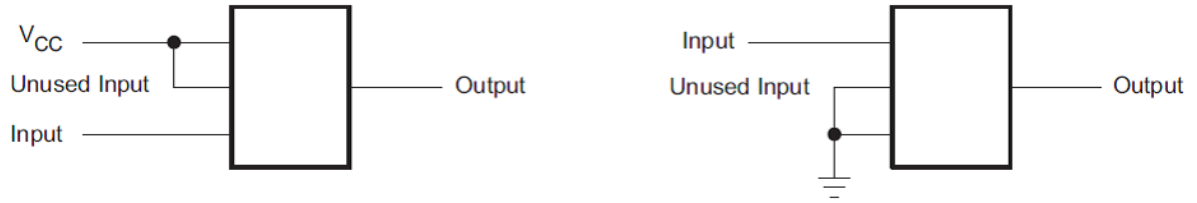


Figure 9-3. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV164A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV164ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVA164	Samples
SN74LV164AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LV164A	
SN74LV164ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV164A	Samples
SN74LV164APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV164A	
SN74LV164APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples
SN74LV164APWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV164A	
SN74LV164ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV164A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV164A :

- Automotive : [SN74LV164A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV164ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LV164ADBDR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV164ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV164ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV164ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV164ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV164APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV164APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV164ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV164ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LV164ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV164ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV164ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV164ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV164ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV164APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV164APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV164ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

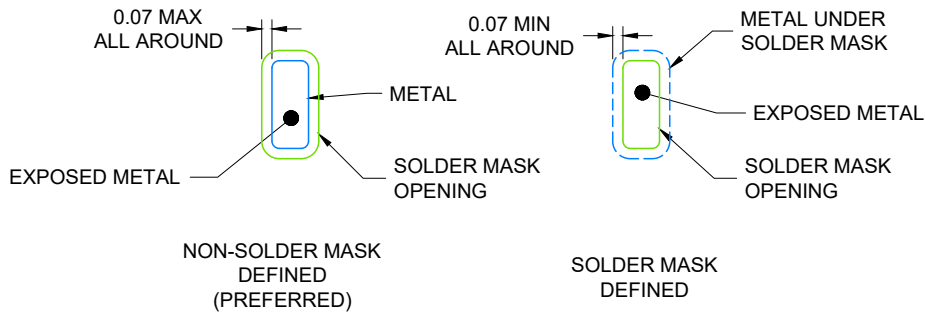
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated