

# SN5474, SN54LS74A, SN54S74 SN7474, SN74LS74A, SN74S74

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

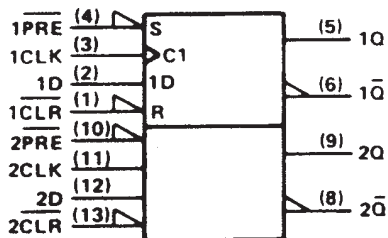
The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

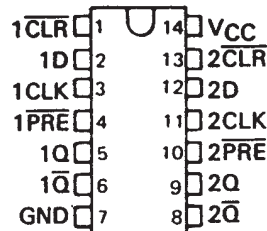
### logic symbol<sup>‡</sup>



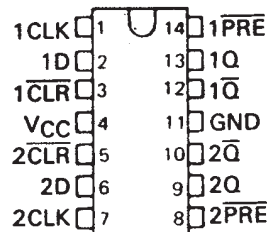
<sup>‡</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

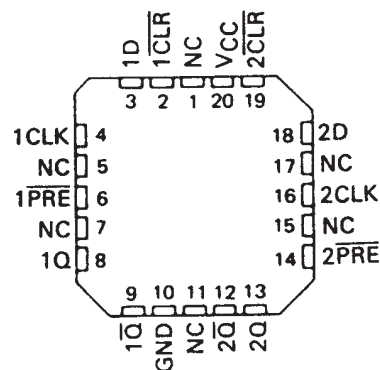
SN5474 . . . J PACKAGE  
SN54LS74A, SN54S74 . . . J OR W PACKAGE  
SN7474 . . . N PACKAGE  
SN74LS74A, SN74S74 . . . D OR N PACKAGE  
(TOP VIEW)



SN5474 . . . W PACKAGE  
(TOP VIEW)

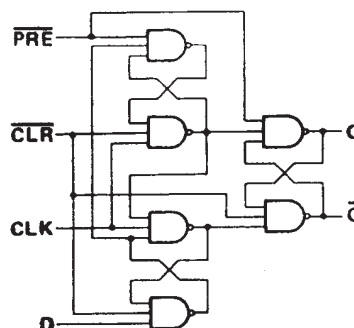


SN54LS74A, SN54S74 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

### logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

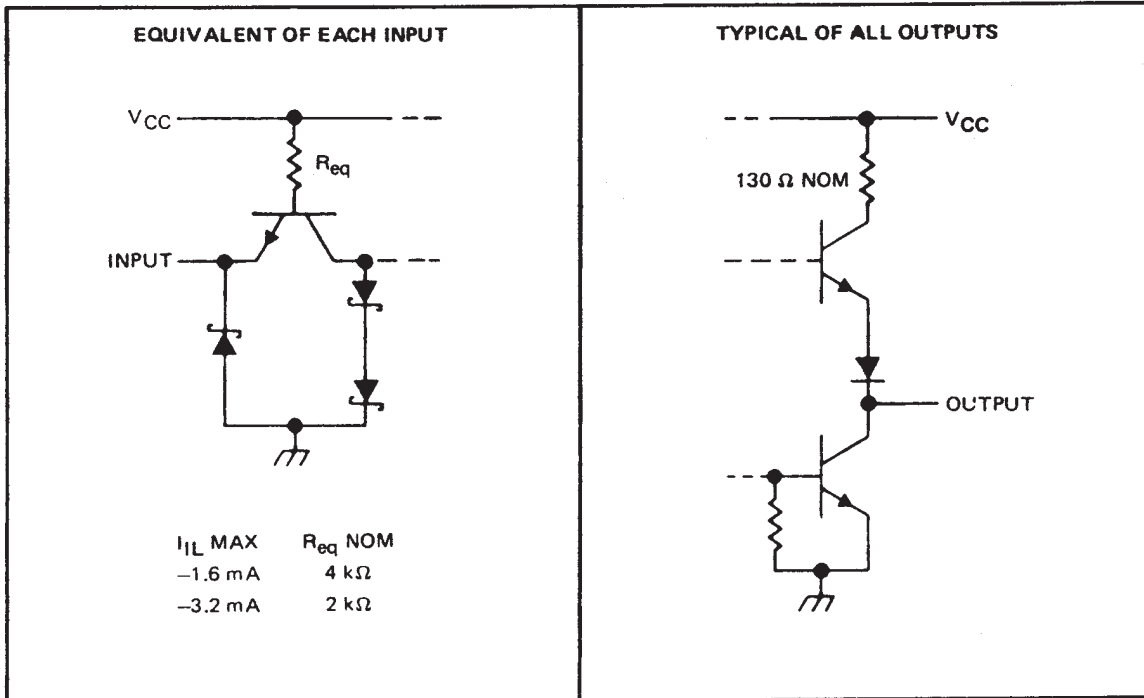
**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

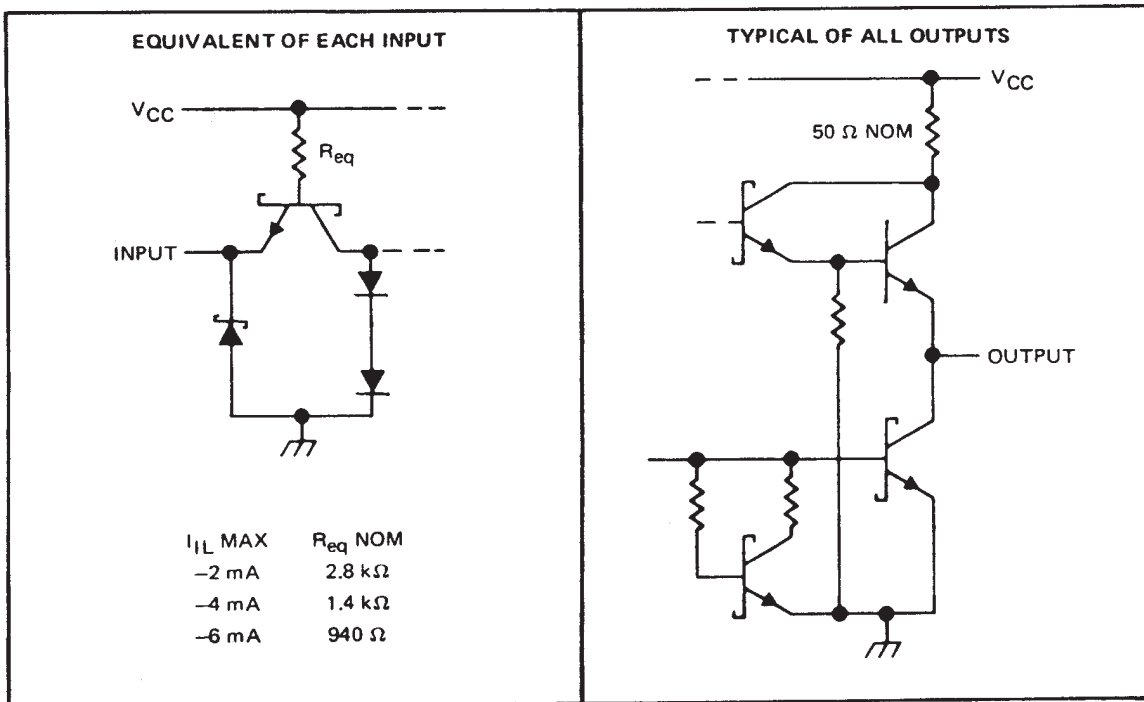
Copyright © 1988, Texas Instruments Incorporated

schematics of inputs and outputs

74



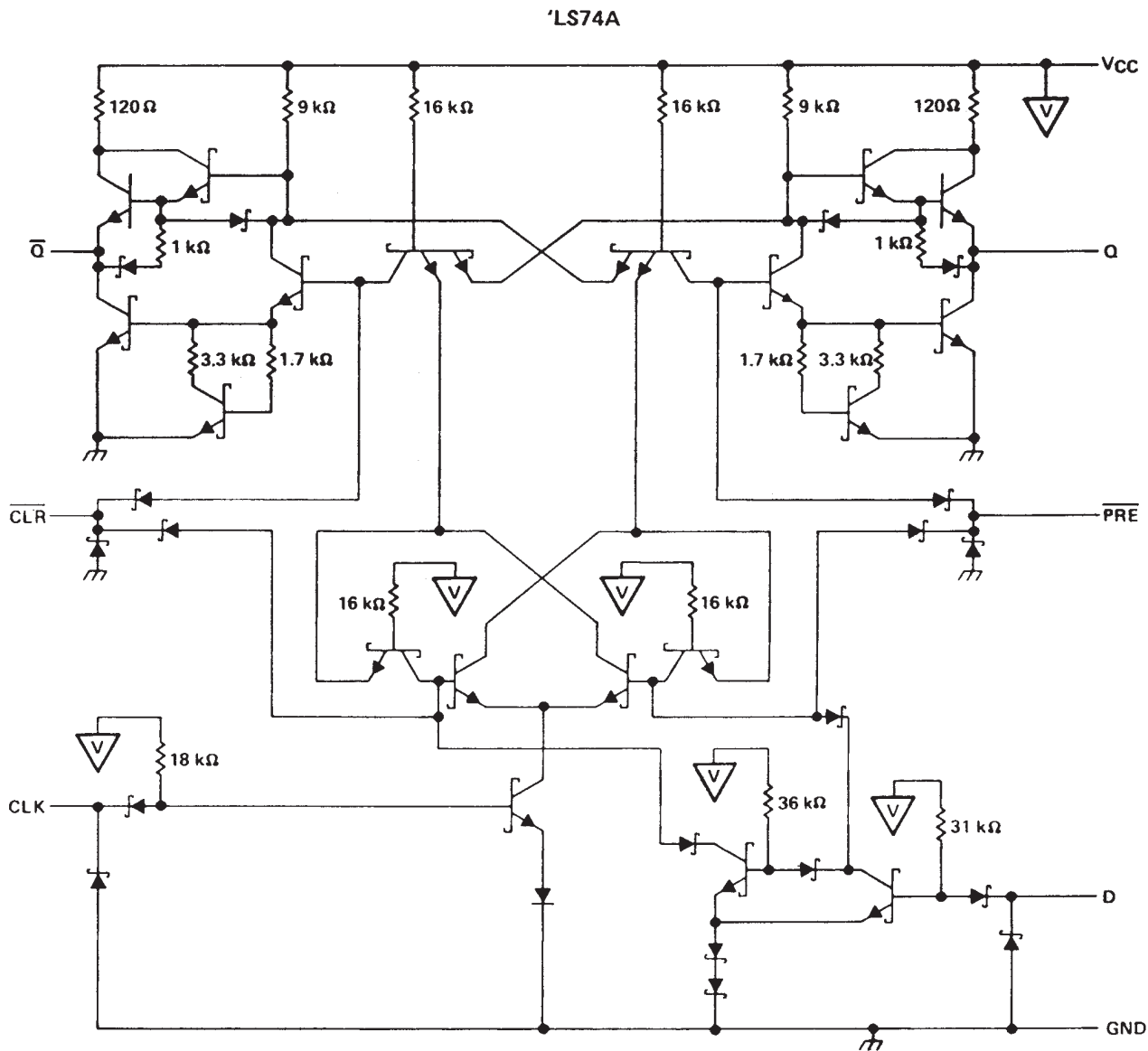
'S74



**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: '74, 'S74 .....	5.5 V
'LS74A .....	7 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



**SN5474, SN54LS74A, SN54S74**

**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

		SN5474			SN7474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
t <sub>w</sub>	Pulse duration	CLK high		30	30		ns	
		CLK low		37	37			
		PRE or CLR low		30	30			
t <sub>SU</sub>	Input setup time before CLK ↑	20			20			ns
t <sub>H</sub>	Input hold time-data after CLK ↑	5			5			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		SN5474		SN7474		UNIT		
				MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IK</sub>		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -12 mA			-1.5		-1.5	V	
V <sub>OH</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA	2.4	3.4	2.4	3.4		V	
V <sub>OL</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA		0.2 0.4		0.2 0.4		V	
I <sub>I</sub>		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V					1	mA	
I <sub>IH</sub>	D	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4 V					40	μA	
	CLR							120		
	All Other							80		
I <sub>IL</sub>	D	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V					-1.6	mA	
	PRE‡							-1.6		
	CLR‡									-3.2
	CLK									-3.2
I <sub>OS</sub> †		V <sub>CC</sub> = MAX		-20		-57	-18		-57	mA
I <sub>CC</sub> #		V <sub>CC</sub> = MAX,	See Note 2		8.5	15		8.5	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§Clear is tested with preset high and preset is tested with clear high.

†Not more than one output should be shown at a time.

#Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
f <sub>max</sub>					15	25		MHz	
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	R <sub>L</sub> = 400 Ω,	C <sub>L</sub> = 15 pF			25	ns	
t <sub>PHL</sub>							40	ns	
t <sub>PLH</sub>	CLK	Q or Q̄					14	25	ns
t <sub>PHL</sub>							20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

		SN54LS74A			SN74LS74A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V	
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA	
I <sub>OL</sub>	Low-level output current			4			8	mA	
f <sub>clock</sub>	Clock frequency	0		25	0		25	MHz	
t <sub>w</sub>	Pulse duration	CLK high		25	25			ns	
		PRE or CLR low		25	25				
t <sub>su</sub>	Setup time-before CLK ↑	High-level data		20	20			ns	
		Low-level data		20	20				
t <sub>h</sub>	Hold time-data after CLK ↑	5			5			ns	
T <sub>A</sub>	Operating free-air temperature	-55		125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS74A			SN74LS74A			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V	
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.35	0.5		
I <sub>I</sub>	D or CLK	0.1			0.1			mA	
	CLR or PRE	0.2			0.2				
I <sub>IH</sub>	D or CLK	20			20			μA	
	CLR or PRE	40			40				
I <sub>IL</sub>	D or CLK	-0.4			-0.4			mA	
	CLR or PRE	-0.8			-0.8				
I <sub>OS</sub> §	V <sub>CC</sub> = MAX, See Note 4	-20		-100	-20		-100	mA	
I <sub>CC</sub> (Total)	V <sub>CC</sub> = MAX, See Note 2	4		8		4		8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
f <sub>max</sub>					25	33		MHz	
t <sub>PLH</sub>	CLR, PRE or CLK	Q or Q̄	R <sub>L</sub> = 2 kΩ,	C <sub>L</sub> = 15 pF			13	25	ns
t <sub>PHL</sub>							25	40	ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.



**SN5474, SN54LS74A, SN54S74**

**SN7474, SN74LS74A, SN74S74**

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

**recommended operating conditions**

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage	0.8			0.8			V
I <sub>OH</sub>	High-level output current	-1			-1			mA
I <sub>OL</sub>	Low-level output current	20			20			mA
t <sub>w</sub>	Pulse duration	CLK high		6	6		ns	
		CLK low		7.3	7.3			
		CLR or PRE low		7	7			
t <sub>su</sub>	Setup time, before CLK ↑	High-level data		3	3		ns	
		Low-level data		3	3			
t <sub>h</sub>	Input hold time - data after CLK ↑	2			2			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	SN54S74			SN74S74			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA,	-1.2			-1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	0.5			0.5			V
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA
I <sub>IH</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	50			50			μA
	CLR		150			150			
	PRE or CLK		100			100			
I <sub>IL</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	-2			-2			mA
	CLR†		-6			-6			
	PRE†		-4			-4			
	CLK		-4			-4			
I <sub>OS</sub> ‡		V <sub>CC</sub> = MAX	-40	-100		-40	-100	mA	
I <sub>CC</sub> #		V <sub>CC</sub> = MAX, See Note 2	15	25		15	25	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

†Clear is tested with preset high and preset is tested with clear high.

#Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF	75	110		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄		4	6		ns
t <sub>PHL</sub>	PRE or CLR (CLK high)	Q̄ or Q		9	13.5		ns
	PRE or CLR (CLK low)			5	8		ns
t <sub>PLH</sub>	CLK	Q or Q̄		6	9		ns
t <sub>PHL</sub>				6	9		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BCA	<a href="#">Samples</a>
JM38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BDA	<a href="#">Samples</a>
JM38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BDA	<a href="#">Samples</a>
JM38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102B2A	<a href="#">Samples</a>
JM38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102B2A	<a href="#">Samples</a>
JM38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BCA	<a href="#">Samples</a>
JM38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BCA	<a href="#">Samples</a>
JM38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BDA	<a href="#">Samples</a>
JM38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BDA	<a href="#">Samples</a>
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S CA	<a href="#">Samples</a>
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S CA	<a href="#">Samples</a>
JM38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S DA	<a href="#">Samples</a>
JM38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S DA	<a href="#">Samples</a>
M38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BCA	<a href="#">Samples</a>
M38510/07101BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BCA	<a href="#">Samples</a>
M38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BDA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/07101BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07101BDA	<a href="#">Samples</a>
M38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102B2A	<a href="#">Samples</a>
M38510/30102B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102B2A	<a href="#">Samples</a>
M38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BCA	<a href="#">Samples</a>
M38510/30102BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BCA	<a href="#">Samples</a>
M38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BDA	<a href="#">Samples</a>
M38510/30102BDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30102BDA	<a href="#">Samples</a>
M38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S CA	<a href="#">Samples</a>
M38510/30102SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S CA	<a href="#">Samples</a>
M38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S DA	<a href="#">Samples</a>
M38510/30102SDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/30102S DA	<a href="#">Samples</a>
SN54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS74AJ	<a href="#">Samples</a>
SN54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS74AJ	<a href="#">Samples</a>
SN54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S74J	<a href="#">Samples</a>
SN54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S74J	<a href="#">Samples</a>
SN74LS74AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS74A	
SN74LS74AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	LS74A	
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS74A	<a href="#">Samples</a>
SN74LS74AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	<a href="#">Samples</a>
SN74LS74AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	<a href="#">Samples</a>
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	<a href="#">Samples</a>
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS74AN	<a href="#">Samples</a>
SN74LS74ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	<a href="#">Samples</a>
SN74LS74ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	<a href="#">Samples</a>
SN74LS74ANSRG4	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	<a href="#">Samples</a>
SN74LS74ANSRG4	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS74A	<a href="#">Samples</a>
SN74S74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S74	<a href="#">Samples</a>
SN74S74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S74	<a href="#">Samples</a>
SN74S74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S74N	<a href="#">Samples</a>
SN74S74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S74N	<a href="#">Samples</a>
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 74AFK	<a href="#">Samples</a>
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 74AFK	<a href="#">Samples</a>
SNJ54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AJ	<a href="#">Samples</a>
SNJ54LS74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AJ	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS74AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AW	<a href="#">Samples</a>
SNJ54LS74AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS74AW	<a href="#">Samples</a>
SNJ54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74J	<a href="#">Samples</a>
SNJ54S74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74J	<a href="#">Samples</a>
SNJ54S74W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74W	<a href="#">Samples</a>
SNJ54S74W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S74W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS74A, SN54LS74A-SP, SN54S74, SN74LS74A, SN74S74 :**

- Catalog : [SN74LS74A](#), [SN54LS74A](#), [SN74S74](#)
- Military : [SN54LS74A](#), [SN54S74](#)
- Space : [SN54LS74A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS74ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS74ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS74ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS74ANSR	SOP	NS	14	2000	367.0	367.0	38.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
JM38510/07101BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30102BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30102SDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/07101BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30102BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30102SDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS74ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74S74D	D	SOIC	14	50	506.6	8	3940	4.32
SN74S74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74S74N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS74AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S74W	W	CFP	14	25	506.98	26.16	6220	NA



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

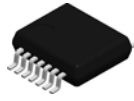
W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

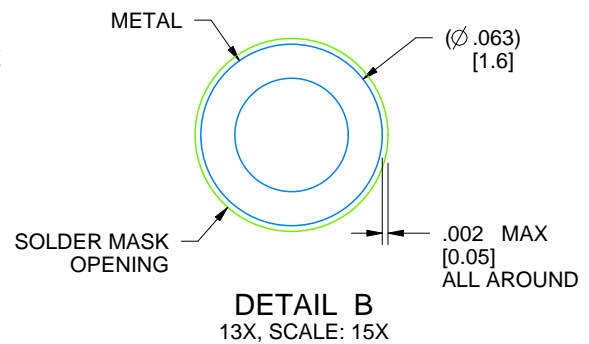
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated