SNx4HC244 Octal Buffers and Line Drivers With 3-State Outputs

1 Features

- Wide operating voltage range of 2V to 6V
- High-current outputs drive up to 15 LSTTL loads
- 3-state outputs drive bus lines or buffer memory address registers
- Low power consumption: I_{CC}, 80µA (maximum)
- Typical t_{pd} = 11ns
- ±6mA output drive at 5V
- Low input current of 1µA (maximum)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

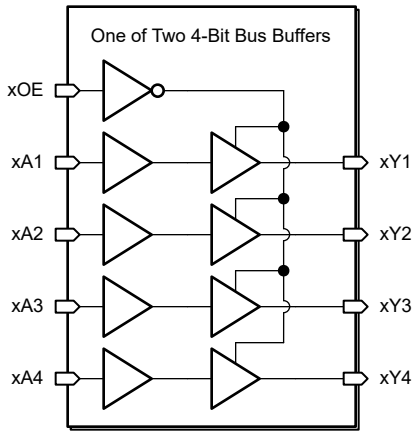
3 Description

The SNx4HC244 octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SNx4HC244 devices are organized as two 4-bit buffers and drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN54HC244	J (CDIP, 20)	24.38mm × 7.62mm	24.38mm × 6.92mm
	W (CFP, 20)	13.72mm × 8.13mm	13.72mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74HC244	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.3mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	N (PDIP, 20)	24.33mm x 9.4mm	24.33mm × 6.35mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

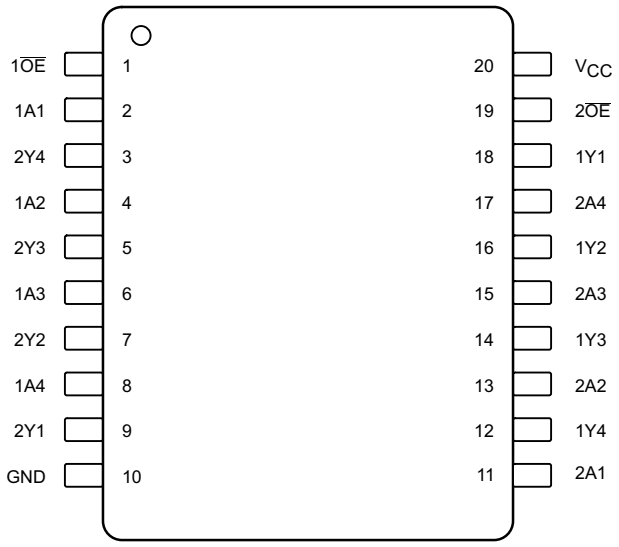

Figure 4-1. DB, DW, J, N, NS, PW, W Package 20-Pin SSOP, SOIC, CDIP, PDIP, SOP, TSSOP, or CFP Top View

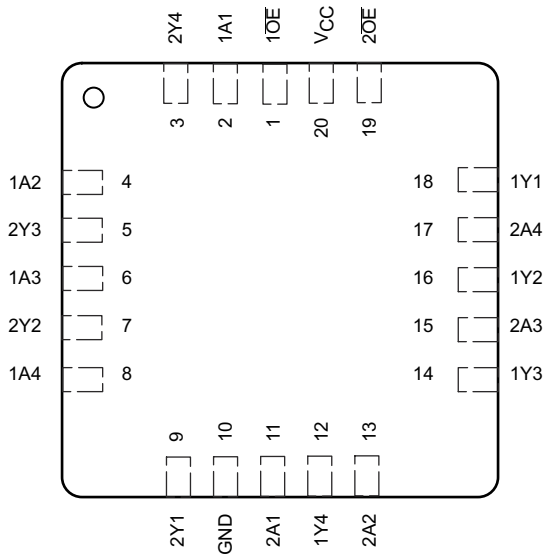

Figure 4-2. FK Package 20-Pin LCCC Top View

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable
2	1A1	I	Input
3	2Y4	O	Output
4	1A2	I	Input
5	2Y3	O	Output
6	1A3	I	Input
7	2Y2	O	Output
8	1A4	I	Input
9	2Y1	O	Output
10	GND	—	Ground
11	2A1	I	Input
12	1Y4	O	Output
13	2A2	I	Input
14	1Y3	O	Output
15	2A3	I	Input
16	1Y2	O	Output
17	2A4	I	Input
18	1Y1	O	Output
19	2 $\overline{OE}$	I	Output Enable
20	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		–0.5	7	V
Input clamp current, I_{IK}	$V_I < 0$ or $V_I > V_{CC}$ (2)		±20	mA
Output clamp current, I_{OK}	$V_O < 0$ or $V_O > V_{CC}$ (2)		±20	mA
Continuous output current, I_O	$V_O = 0$ or V_{CC}		±35	mA
Continuous current through V_{CC} or GND			±70	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

SN74HC244			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns/V
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
C_{pd}	Power dissipation capacitance per buffer or driver (no load)			35		pF
T_A	Operating free-air temperature	SN54HC244	–55		125	°C
		SN74HC244	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the Texas Instruments application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC		SN74HC244					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	109.1	122.7	84.6	113.4	131.8	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9	1.998		V
			V_{CC} = 4.5 V	4.4	4.499		
			V_{CC} = 6 V	5.9	5.999		
		I_{OH} = –6 mA, V_{CC} = 4.5 V		3.98	4.3		
		I_{OH} = –7.8 mA, V_{CC} = 6 V		5.48	5.8		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
			V_{CC} = 4.5 V		0.001	0.1	
			V_{CC} = 6 V		0.001	0.1	
		I_{OL} = 6 mA, V_{CC} = 4.5 V			0.17	0.26	
		I_{OL} = 7.8 mA, V_{CC} = 6 V			0.15	0.26	
I_I	V_I = V_{CC} or 0, V_{CC} = 6 V				±0.1	±100	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}, V_{CC} = 6 V				±0.01	±0.5	µA
I_{CC}	V_I = V_{CC} or 0, I_O = 0, V_{CC} = 6 V					8	µA
C_i	V_{CC} = 2 V to 6 V				3	10	pF

5.6 Electrical Characteristics – SN54HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9			V
			V_{CC} = 4.5 V	4.4			
			V_{CC} = 6 V	5.9			
		I_{OH} = –6 mA, V_{CC} = 4.5 V		3.7			
		I_{OH} = –7.8 mA, V_{CC} = 6 V		5.2			

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V			0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6 V			0.1	
		I_{OL} = 6 mA, V_{CC} = 4.5 V				0.4	
		I_{OL} = 7.8 mA, V_{CC} = 6 V				0.4	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V					±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}, V_{CC} = 6 V					±10	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					160	µA
C_i	V_{CC} = 2 V to 6 V					10	pF

5.7 Electrical Characteristics – SN74HC244

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9			V
			V_{CC} = 4.5 V	4.4			
			V_{CC} = 6 V	5.9			
		I_{OH} = –6 mA, V_{CC} = 4.5 V		3.7			
		I_{OH} = –7.8 mA, V_{CC} = 6 V		5.2			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V			0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6 V			0.1	
		I_{OL} = 6 mA, V_{CC} = 4.5 V				0.4	
		I_{OL} = 7.8 mA, V_{CC} = 6 V				0.4	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V					±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}, V_{CC} = 6 V					±10	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					160	µA
C_i	V_{CC} = 2 V to 6 V					10	pF

5.8 Switching Characteristics

T_A = 25°C (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	V_{CC} = 2 V	C_L = 50 pF		40	115	ns
			C_L = 150 pF		56	165	
		V_{CC} = 4.5 V	C_L = 50 pF		13	23	
			C_L = 150 pF		18	33	
		V_{CC} = 6 V	C_L = 50 pF		11	20	
			C_L = 150 pF		15	28	
t_{en}	From $\overline{OE}$ (input) to Y (output)	V_{CC} = 2 V	C_L = 50 pF		75	150	ns
			C_L = 150 pF		100	200	
		V_{CC} = 4.5 V	C_L = 50 pF		15	30	
			C_L = 150 pF		20	40	
		V_{CC} = 6 V	C_L = 50 pF		13	26	
			C_L = 150 pF		17	34	

T_A = 25°C (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{dis}	From $\overline{OE}$ (input) to Y (output)	V_{CC} = 2 V	C_L = 50 pF		75	150	ns
		V_{CC} = 4.5 V	C_L = 50 pF		15	30	
		V_{CC} = 6 V	C_L = 50 pF		13	26	
t_t	To Y (output)	V_{CC} = 2 V	C_L = 50 pF		28	60	ns
			C_L = 150 pF		45	210	
		V_{CC} = 4.5 V	C_L = 50 pF		8	12	
			C_L = 150 pF		17	42	
		V_{CC} = 6 V	C_L = 50 pF		6	10	
			C_L = 150 pF		13	36	

5.9 Switching Characteristics – C_L = 50 pF

over recommended operating free-air temperature range (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	V_{CC} = 2 V	SN54HC244			170	ns
			SN74HC244			170	
		V_{CC} = 4.5 V	SN54HC244			34	
			SN74HC244			34	
		V_{CC} = 6 V	SN54HC244			29	
			SN74HC244			29	
t_{en}	From $\overline{OE}$ (input) to Y (output)	V_{CC} = 2 V	SN54HC244			225	ns
			SN74HC244			225	
		V_{CC} = 4.5 V	SN54HC244			45	
			SN74HC244			45	
		V_{CC} = 6 V	SN54HC244			38	
			SN74HC244			38	
t_{dis}	From $\overline{OE}$ (input) to Y (output)	V_{CC} = 2 V	SN54HC244			225	ns
			SN74HC244			225	
		V_{CC} = 4.5 V	SN54HC244			45	
			SN74HC244			45	
		V_{CC} = 6 V	SN54HC244			38	
			SN74HC244			38	
t_t	To Y (output)	V_{CC} = 2 V	SN54HC244			90	ns
			SN74HC244			90	
		V_{CC} = 4.5 V	SN54HC244			18	
			SN74HC244			18	
		V_{CC} = 6 V	SN54HC244			15	
			SN74HC244			15	

5.10 Switching Characteristics – C_L = 150 pF

over recommended operating free-air temperature range (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	V_{CC} = 2 V	SN54HC244			245	ns
			SN74HC244			245	
		V_{CC} = 4.5 V	SN54HC244			49	
			SN74HC244			49	
		V_{CC} = 6 V	SN54HC244			42	
			SN74HC244			42	
t_{en}	From $\overline{OE}$ (input) to Y (output)	V_{CC} = 2 V	SN54HC244			300	ns
			SN74HC244			300	
		V_{CC} = 4.5 V	SN54HC244			60	
			SN74HC244			60	
		V_{CC} = 6 V	SN54HC244			51	
			SN74HC244			51	
t_t	To Y (output)	V_{CC} = 2 V	SN54HC244			315	ns
			SN74HC244			315	
		V_{CC} = 4.5 V	SN54HC244			63	
			SN74HC244			63	
		V_{CC} = 6 V	SN54HC244			53	
			SN74HC244			53	

5.11 Typical Characteristic

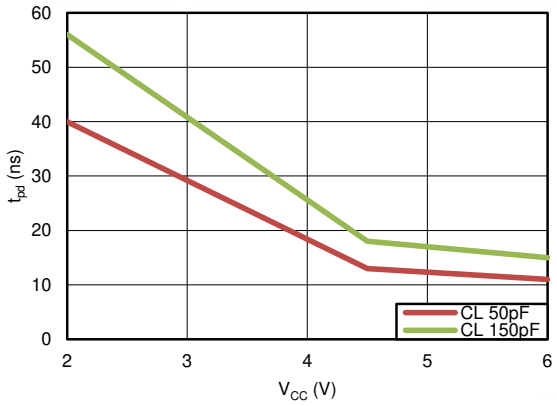

Figure 5-1. Propagation Delay

6 Parameter Measurement Information

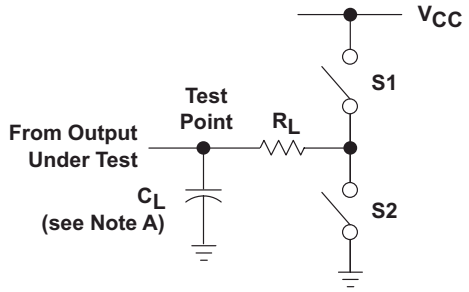

Figure 6-1. Load Circuit

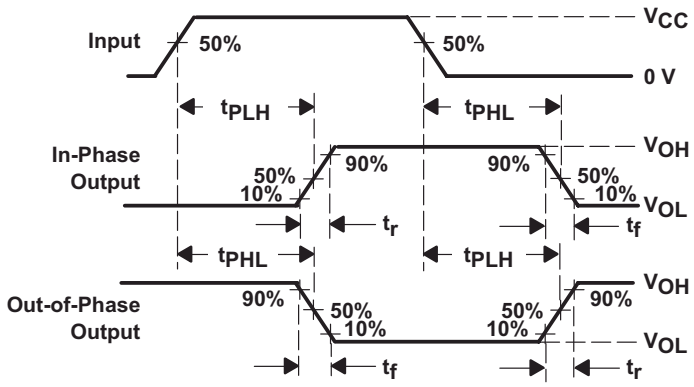

Figure 6-2. Propagation Delay and Output Transition Times

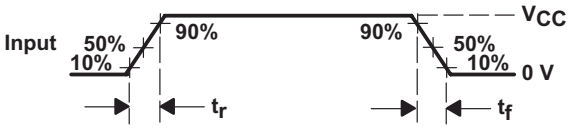

Figure 6-3. Input Rise and Fall Times

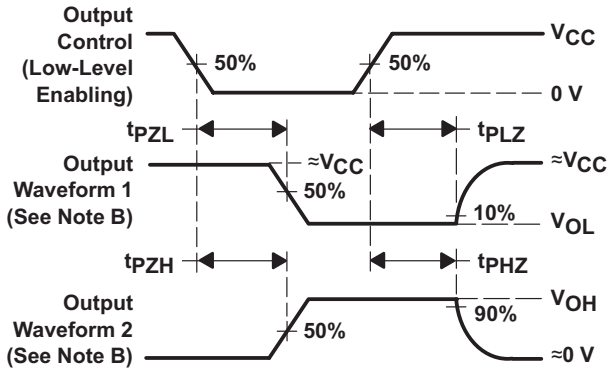

Figure 6-4. Enable and Disable Times for 3-State Outputs

Note

NOTE:

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Table 6-1. Switching Information Table

PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}	1 kΩ	50 pF or 150 pF	Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}	1 kΩ	50 pF	Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open

7 Detailed Description

7.1 Overview

The SNx4HC244 contains 8 individual high speed CMOS buffers with Schmitt-trigger inputs and 3-state outputs.

Each buffer performs the boolean logic function xYn = xAn, with *x* being the bank number and *n* being the channel number.

Each output enable (x$\overline{OE}$) controls four buffers. When the x$\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the x$\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

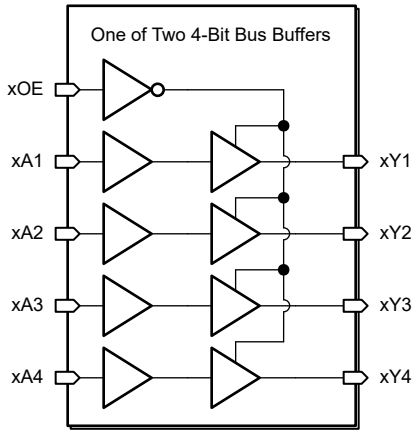

Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4HC244.

Table 7-1. Function Table

INPUTS[1]		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application

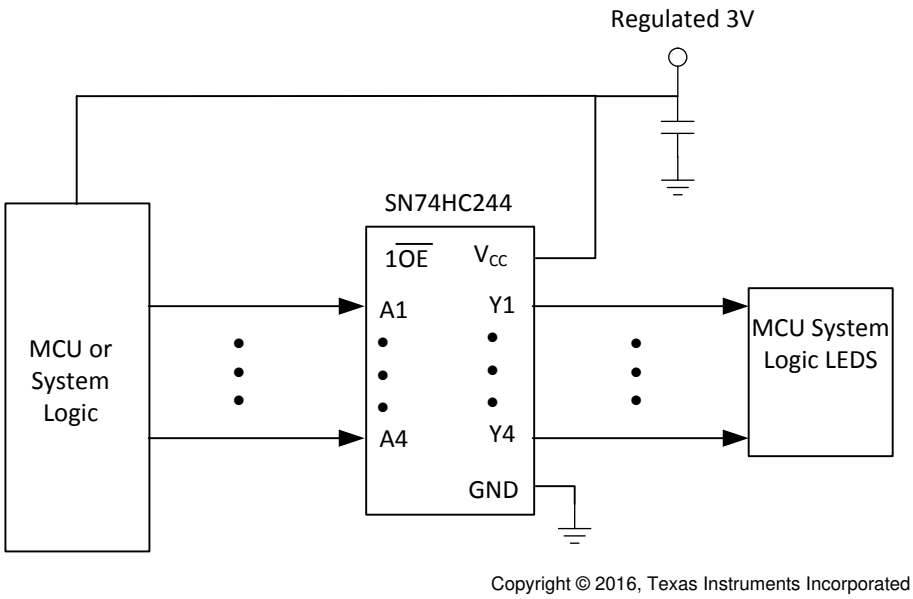

Figure 8-1. SN74HC244 Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see Δt/ΔV in *Section 5.3*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 5.3*.
2. Recommend output conditions:
   - Load currents should not exceed I_O max per output and should not exceed the continuous current through V_{CC} or GND total current for the part. These limits are located in *Section 5.1*.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curve

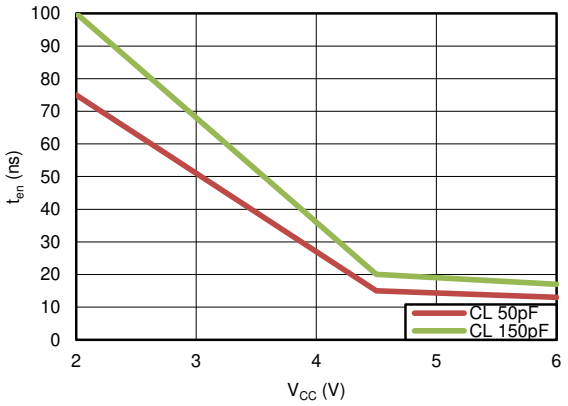

Figure 8-2. Enable Time

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

8.4.1 Layout Example

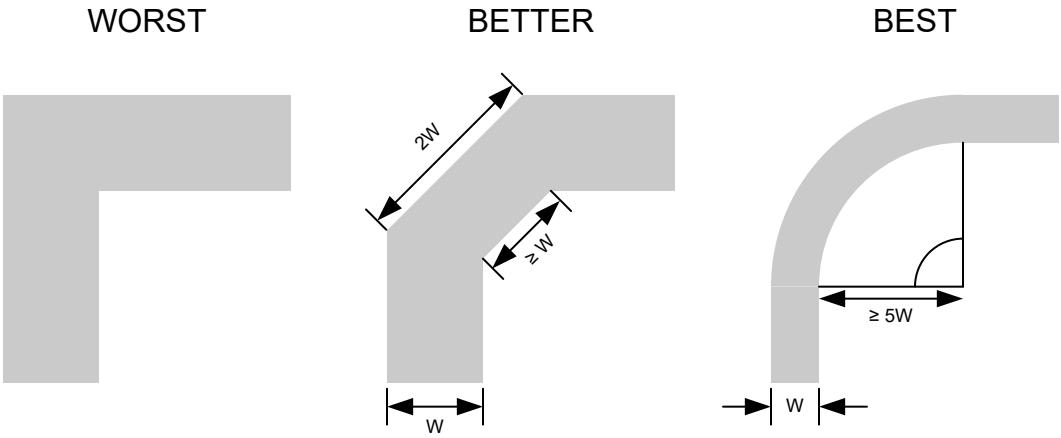

Figure 8-3. Example Trace Corners for Improved Signal Integrity

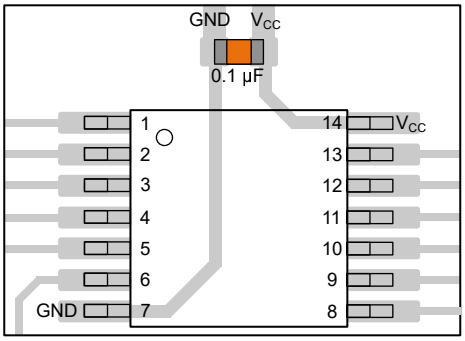

Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

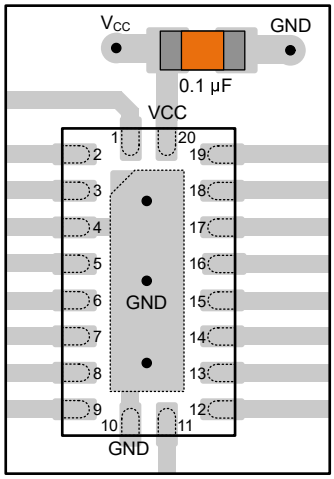

Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

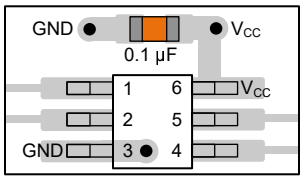

Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

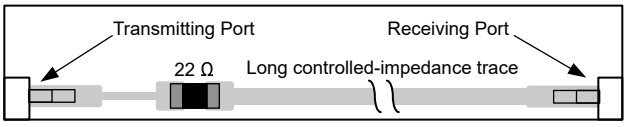

Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

Table 9-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC244	Click here	Click here	Click here	Click here	Click here
SN74HC244	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2025) to Revision H (February 2025) — **Page**

- Updated SN74HC244 operating temperature to 125°C and respective values in *Electrical Characteristics* table, *Recommended Operating Conditions* table, and *Switching Characteristics* tables..... 1

Changes from Revision F (May 2022) to Revision G (January 2025) — **Page**

- Added package size to *Device Information* table and updated structural layout of data sheet to current standards..... 1
- Updated *Features Description* and corrected *Functional Block Diagram* image and *Device Functional Modes* table 11

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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