TEXAS INSTRUMENTS

SN74AHCT594
SCLS417K – JUNE 1998 – REVISED JULY 2024

SN74AHCT594 8-Bit Shift Registers With Output Registers

1 Features

- Inputs are TTL-voltage compatible
- 8-bit serial-in, parallel-out shift registers with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for both shift and storage registers
- Latch-up performance exceeds 100mA per JESD, 78 class II
- ESD protection exceeds JESD 22
  - ±3500V human-body model
  - ±200V machine model

2 Applications

- Network Switches
- Power Infrastructure
- PCs, Notebooks
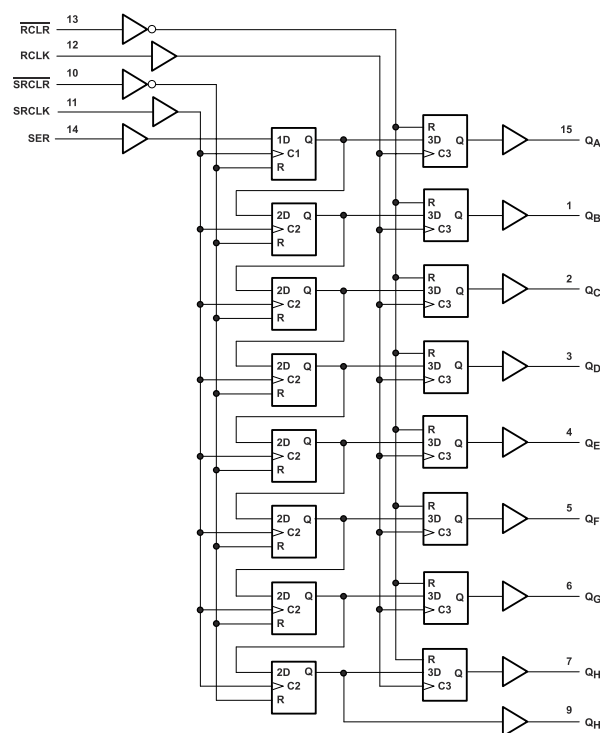- Health and Fitness, Wearables
- Tests and Measurements

3 Description

The SN74AHCT594 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]	BODY SIZE[3]
SN74AHCT594	N (PDIP, 16)	19.3mm × 9.4mm	19.32mm x 6.35mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.20mm x 5.30mm
	PW (TSSOP , 16)	5mm × 6.4mm	5.00mm x 4.40mm
	NS (SOP, 16)	10.2mm x 7.8mm	10.20mm x 5.30mm
	D (SOIC, 16)	9.9mm × 6mm	9.90mm x 3.90mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.
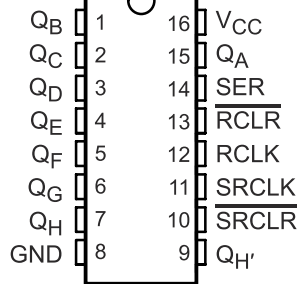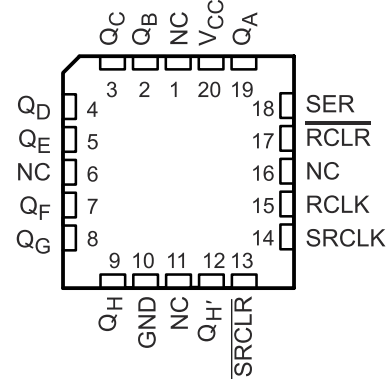

Simplified Schematic

Table of Contents

Product Folder Links: *SN74AHCT594*

4 Pin Configuration and Functions

SN54AHCT594 . . . J OR W PACKAGE
SN74AHCT594 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

SN54AHCT594 . . . FK PACKAGE
(TOP VIEW)

NC – No internal connection

Figure 4-1.

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	Q_B	O	Output B
2	Q_C	O	Output C
3	Q_D	O	Output D
4	Q_E	O	Output E
5	Q_F	O	Output F
6	Q_G	O	Output G
7	Q_H	O	Output H
8	GND	—	Ground Pin
9	$Q_{H'}$	I	QH inverted
10	$\overline{SRCLR}$	I	Serial Clear
11	SRCLK	I	Serial Clock
12	RCLK	I	Storage Clock
13	$\overline{RCLR}$	I	Storage Clear
14	SER	I	Serial Input
15	Q_A	O	Output A
16	V_{CC}	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Output voltage range[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage Temperature Range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		SN74AHCT594		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise and fall time		20	ns/V
T_A	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT594					UNIT
		D	DB	N	NS	PW	
		16 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.8	129.6	47.5	79.1	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	90	34.9	35.4	70.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	92.7	27.5	39.9	81.3	
ψ_{JT}	Junction-to-top characterization parameter	20.8	46.1	19.8	5.4	22.5	
ψ_{JB}	Junction-to-board characterization parameter	50.7	91.7	27.4	39.5	80.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	4.5V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[1]		±1[1]	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC} [2]	One input at 3.5 V, Other inputs at V_{CC} or GND	5.5 V			2		2.2		2.2	mA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER			T_A = 25°C		−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5		5.5		6.5		ns
		RCLR or SRCLR low	5.2		5.5		6		
t_{su}	Setup time	SER before SRCLK↑	3		3		3.5		ns
		SRCLK↑ before RCLK↑[1]	5		5		5.5		
		SRCLR low before RCLK↑	5		5		5.5		
		SRCLR high (inactive) before SRCLK↑	2.9		3.3		4		
		RCLR high (inactive) before RCLK↑	3.4		3.8		4.5		
t_h	Hold time	SER after SRCLK↑	2		2		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	135[1]	170[1]		115		115		MHz
			C_L = 50 pF	120	140		95		95		
t_{PLH}	RCLK	Q_A – Q_H	C_L = 15 pF		3.3[1]	6.2[1]	1	6.5	1	7.5	ns
t_{PHL}					3.7[1]	6.5[1]	1	6.9	1	7.8	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF		3.7[1]	6.8[1]	1	7.2	1	8	ns
t_{PHL}					4.1[1]	7.2[1]	1	7.6	1	8.5	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 15 pF		4.5[1]	7.6[1]	1	8.2	1	9.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF		4.1[1]	7.1[1]	1	7.6	1	8.5	
t_{PLH}	RCLK	Q_A – Q_H	C_L = 50 pF		4.9	7.8	1	8.3	1	9.5	ns
t_{PHL}					5.8	8.9	1	9.7	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF		5.5	8.6	1	9.7	1	10	ns
t_{PHL}					6	9.2	1	10.1	1	11	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	C_L = 50 pF		6.6	10	1	10.7	1	11.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF		6	9.2	1	10.1	1	11	ns

(1)   On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		SN74AHCT594			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1)   Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	112	pF

5.10 Typical Characteristics
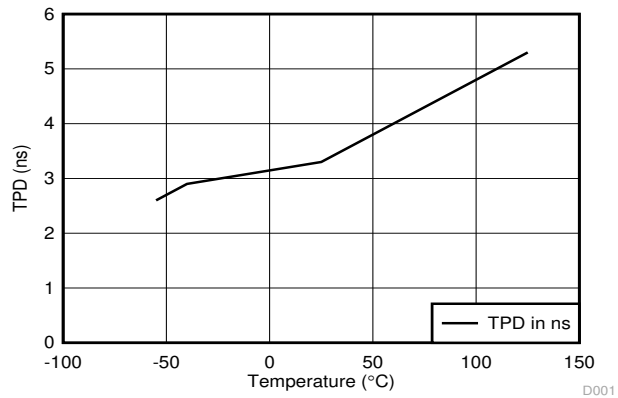
Figure 5-1. TPD vs Temperature

Product Folder Links: *SN74AHCT594*

6 Parameter Measurement Information

From Output Under Test — Test Point
C_L (see Note A)

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

From Output Under Test — $R_L = 1\ k\Omega$ — S1 — V_{CC} / Open / GND
C_L (see Note A)

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Input — t_W — 1.5 V — 1.5 V — 3 V / 0 V

VOLTAGE WAVEFORMS PULSE DURATION

Timing Input — 1.5 V — 3 V / 0 V
t_{su} — t_h
Data Input — 1.5 V — 1.5 V — 3 V / 0 V

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

Input — 1.5 V — 1.5 V — 3 V / 0 V
t_{PLH} — t_{PHL}
In-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}
t_{PHL} — t_{PLH}
Out-of-Phase Output — 50% V_{CC} — 50% V_{CC} — V_{OH} / V_{OL}

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

Output Control — 1.5 V — 1.5 V — 3 V / 0 V
t_{PZL} — t_{PLZ}
Output Waveform 1 S1 at V_{CC} (see Note B) — 50% V_{CC} — V_{OL} + 0.3 V — ≈V_{CC} / V_{OL}
t_{PZH} — t_{PHZ}
Output Waveform 2 S1 at GND (see Note B) — 50% V_{CC} — V_{OH} − 0.3 V — V_{OH} / ≈0 V

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

Product Folder Links: *SN74AHCT594*

7 Detailed Description

7.1 Overview

The 'AHCT594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{SRCLR}$, $\overline{RCLR}$) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

7.2 Functional Block Diagram
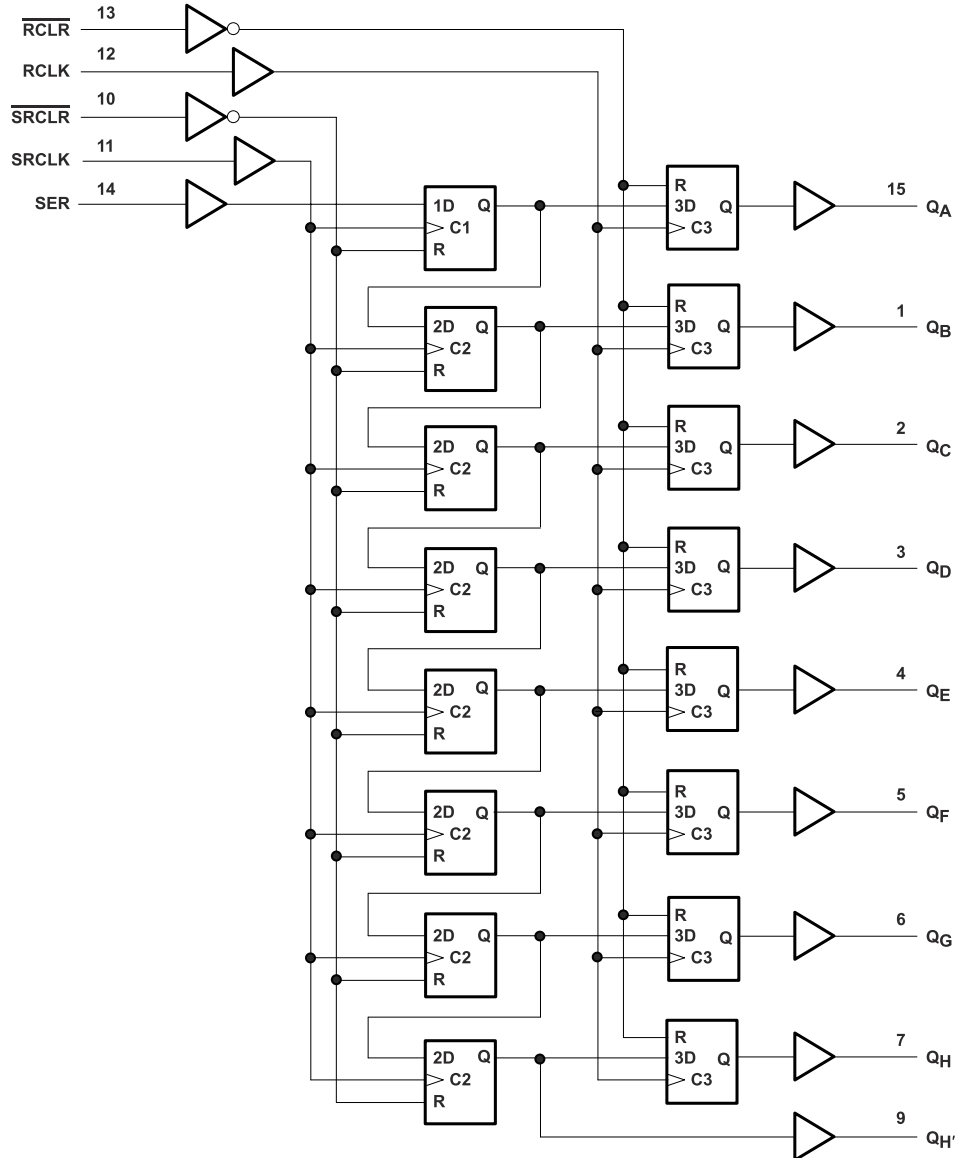
7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allow Up voltage translation from 3.3 V to 5 V
  - Inputs accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift-register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage-register state is not changed.

Product Folder Links: *SN74AHCT594*

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHCT594 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2 V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V. Figure 8-2 shows this type of translation.
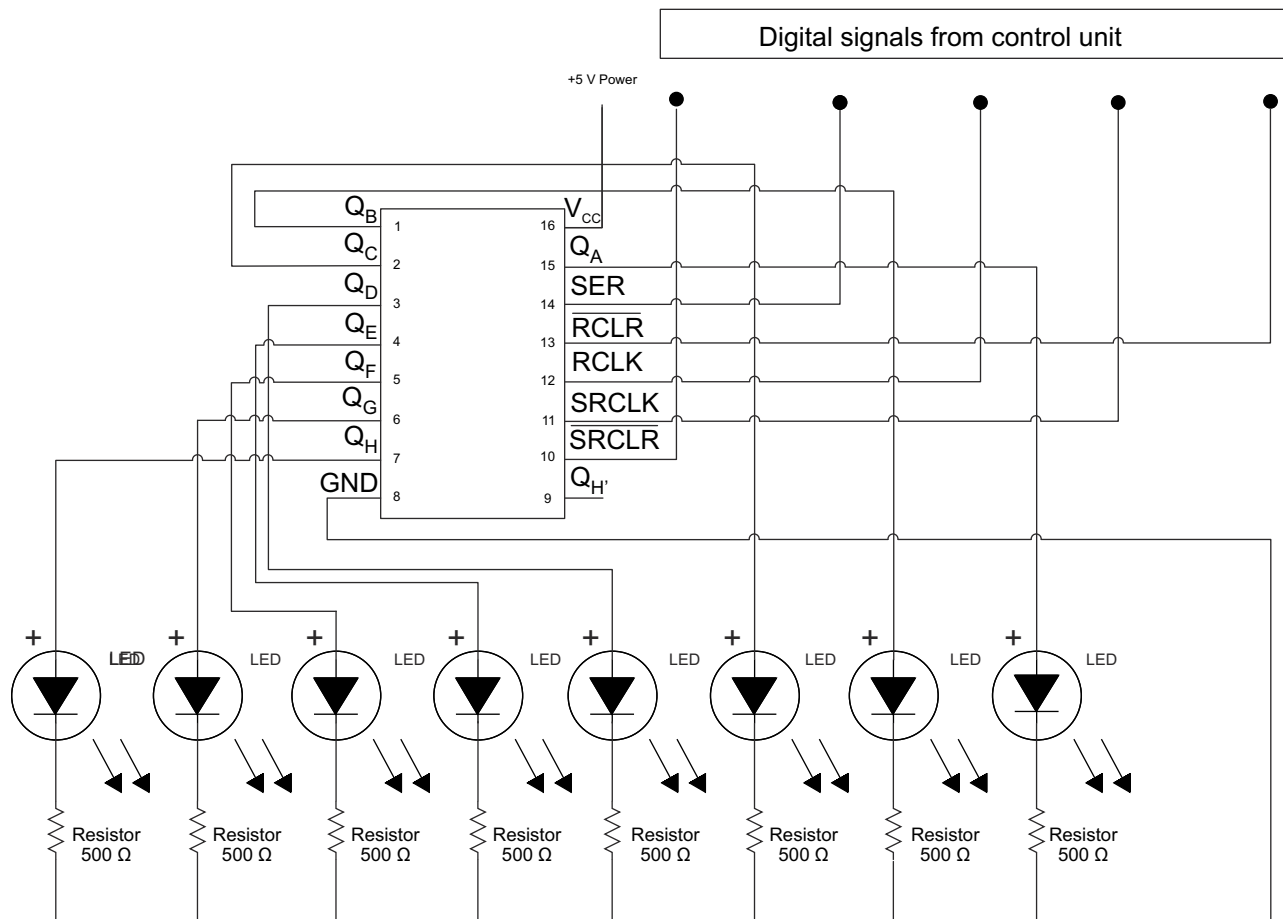
8.2 Typical Application


Figure 8-1. Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Product Folder Links: *SN74AHCT594*

8.2.2 Detailed Design Procedure

1. Recommended Input conditions
    *   Rise time and fall time specs see (Δt/ΔV) in *Section 5.3* table.
    *   Specified High and low levels. See (V_{IH} and V_{IL}) in *Section 5.3* table.
    *   Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid Vcc
2. Recommend output conditions
    *   Load currents should not exceed 25 mA per output and 75 mA total for the part
    *   Outputs should not be pulled above V_{CC}

8.2.3 Application Curves

Figure 8-2. Typical Application Curve
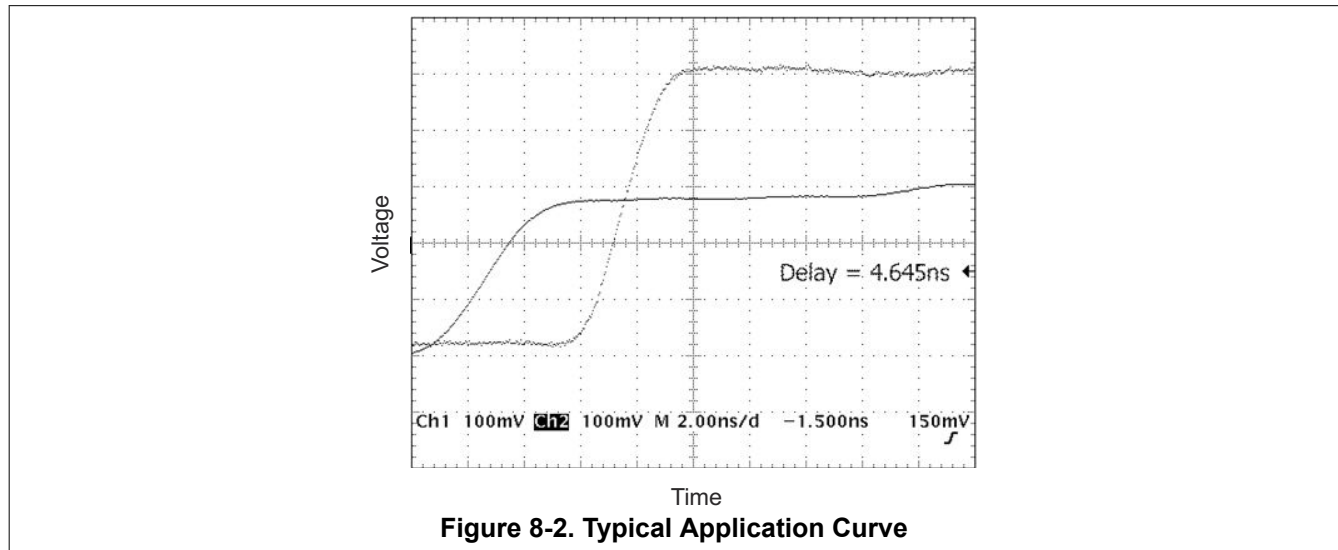
8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.
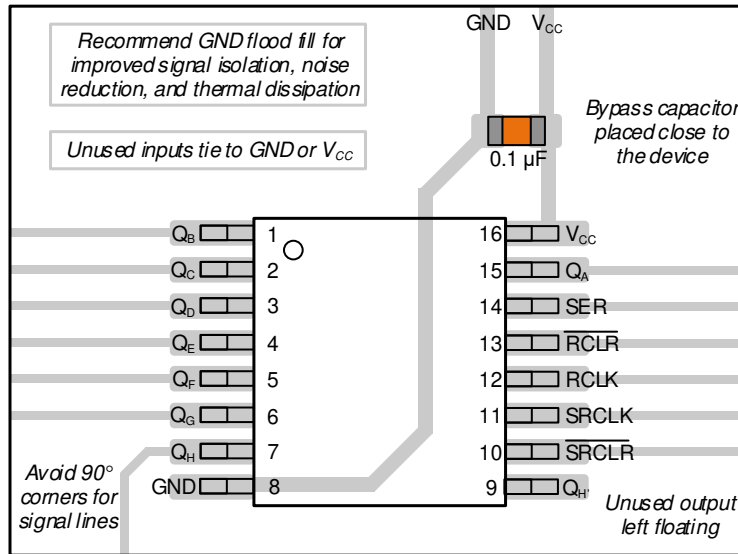
8.4.2 Layout Example

Figure 8-3. Example Layout for the SN74AHCT594

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT594	Click here	Click here	Click here	Click here	Click here

9.2 Trademarks

All trademarks are the property of their respective owners.

9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision J (April 2024) to Revision K (July 2024)   **Page**

- Updated thermal values for D package from $R\theta JA$ = 80.2 to 93.8, $R\theta JC(top)$ = 39.1 to 54.7, $R\theta JB$ = 27.7 to 50.9, ΨJT = 9.9 to 20.8, ΨJB = 37.4 to 50.7, $R\theta JC(bot)$ = N/A, all values in °C/W 5

Changes from Revision I (December 2014) to Revision J (April 2024)   **Page**

- Deleted references to machine model throughout the data sheet and updated structural layout of data sheet to current standard.. 1
- Updated $R\theta JA$ values: DB = 97.5 to 129.6, PW = 105.7 to 135.9; Updated DB and PW packages for $R\theta JC(top)$, $R\theta JB$, ΨJT, ΨJB, and $R\theta JC(bot)$, all values in °C/W 5
- Updated layout image 13

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *SN74AHCT594*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT594D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AHCT594	
SN74AHCT594DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB594	Samples
SN74AHCT594DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594	Samples
SN74AHCT594N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT594N	Samples
SN74AHCT594NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT594	Samples
SN74AHCT594PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 125	HB594	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT594 :

• Automotive : SN74AHCT594-Q1

NOTE: Qualified Version Definitions:

    • Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT594DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT594DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT594NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT594PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHCT594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT594DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHCT594DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHCT594DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT594DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT594DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT594NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74AHCT594PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT594PWR	TSSOP	PW	16	2000	366.0	364.0	50.0
SN74AHCT594PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHCT594N	N	PDIP	16	25	506	13.97	11230	4.32

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

NS0016A

SOP

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

16X (1.85)

1

16X (0.6)

16

SYMM

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AC.

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6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ 0.1Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0°-8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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PW0016A

TSSOP - 1.2 mm max height

16X (1.5)

SYMM

(R0.05) TYP

1

16X (0.45)

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

4220763/A   05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

16X (1.85)

1

16X (0.45)

SYMM
℄

(R0.05) TYP

16

SYMM
℄

14X (0.65)

8

9

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A   05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G**)　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

1,27

0,51
0,35

⌖ 0,25 Ⓜ

14

8

5,60
5,00

8,20
7,40

1

7

A

0,15 NOM

Gage Plane

0°–10°

0,25

1,05
0,55

0,15
0,05

2,00 MAX

Seating Plane

⬓ 0,10

DIM ╲ PINS **	14	16	20	24
A　MAX	10,50	10,50	12,90	15,30
A　MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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