SN74AHC594-Q1 Automotive 8-Bit Shift Register With Output Registers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN (WBQA) package
- Operating range 2V to 5.5V V_{CC}
- Low delay, 12ns (V_{CC} = 5V, C_L = 50pF)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Increase the number of outputs on a microcontroller
- Store up to 8 bits of data temporarily

3 Description

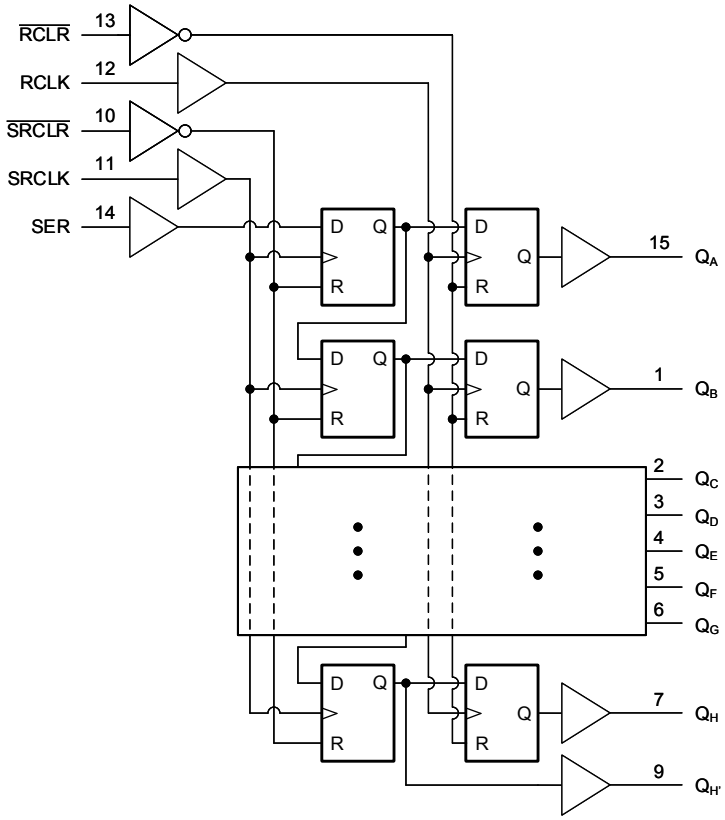
The SN74AHC594-Q1 is an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74AHC594-Q1	WBQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

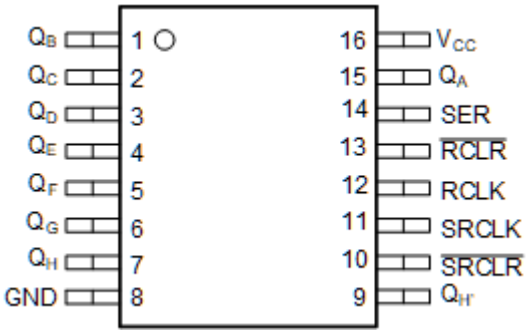


Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

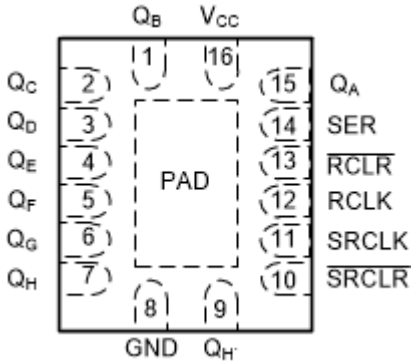


Figure 4-2. WBQB Package, 16-Pin WQFN (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Q_B	1	O	Q_B output
Q_C	2	O	Q_C output
Q_D	3	O	Q_D output
Q_E	4	O	Q_E output
Q_F	5	O	Q_F output
Q_G	6	O	Q_G output
Q_H	7	O	Q_H output
GND	8	G	Ground
$Q_{H'}$	9	O	Serial output, can be used for cascading
$\overline{SRCLR}$	10	I	Shift register clear, active low
SRCLK	11	I	Shift register clock, rising edge triggered
RCLK	12	I	Output register clock, rising edge triggered
$\overline{RCLR}$	13	I	Storage register clear, active low
SER	14	I	Serial input
Q_A	15	O	Q_A output
V_{CC}	16	P	Positive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.
(2) WBQB package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5 V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-Level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input Voltage		0	5.5	V
V_O	Ouptut Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		-50	µA
		V_{CC} = 3.3 V ± 0.3 V		-4	mA
		V_{CC} = 5 V ± 0.5 V		-8	mA
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	ns/V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		WBQB (WQFN) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.6	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.4	81.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.1	22.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.4	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	56.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC}-0.1	V_{CC}		V_{CC}-0.1	V_{CC}		V
	I_{OH} = −4mA	3 V	2.58			2.48			
	I_{OH} = −8mA	4.5 V	3.94			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 4mA	3 V			0.36			0.44	
	I_{OL} = 8mA	4.5 V			0.36			0.44	
I_I	V_I = 5.5 V or GND and V_{CC} = 0 V to 5.5 V	0 V to 5.5 V			±0.1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0, and V_{CC} = 5.5 V	5.5 V			4			40	µA
C_I	V_I = V_{CC} or GND	5 V		2	10			10	pF
C_{PD}	No load, F = 1 MHz	5 V		128					pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_H	Hold time	SER after SRCLK↑	3.3 V ± 0.3 V	1.5		1.5		1.5		ns
t_{SU}	Setup time	$\overline{RCLR}$ high	3.3 V ± 0.3 V	2.5		2.5		2.5		ns
		SER before SRCLK↑	3.3 V ± 0.3 V	3.5		3.5		3.5		ns
		SRCLK↑ before RCLK↑	3.3 V ± 0.3 V	8		8.5		8.5		ns
		$\overline{SRCLR}$ high before SRCLK↑	3.3 V ± 0.3 V	3		3		4		ns
		$\overline{SRCLR}$ low before RCLK↑	3.3 V ± 0.3 V	8		9		9		ns

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	$\overline{RCLR}$ low	3.3 V ± 0.3 V	5		5		5		ns
		RCLK or SRCLK high or low	3.3 V ± 0.3 V	5		5		5.5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	3.3 V ± 0.3 V	5		5		5		ns
t_H	Hold time	SER after SRCLK↑	5 V ± 0.5 V	2		2		2		ns
t_{SU}	Setup time	$\overline{RCLR}$ high	5 V ± 0.5 V	2.5		2.5		2.5		ns
		SER before SRCLK↑	5 V ± 0.5 V	3		3		3		ns
		SRCLK↑ before RCLK↑	5 V ± 0.5 V	5		5		5		ns
		$\overline{SRCLR}$ high before SRCLK↑	5 V ± 0.5 V	2.5		2.5		3.3		ns
		$\overline{SRCLR}$ low before RCLK↑	5 V ± 0.5 V	5		5		5		ns
t_W	Pulse duration	$\overline{RCLR}$ low	5 V ± 0.5 V	5		5		5		ns
		RCLK or SRCLK high or low	5 V ± 0.5 V	5		5		5		ns
		$\overline{RCLR}$ or $\overline{SRCLR}$ low	5 V ± 0.5 V	5		5		5.2		ns

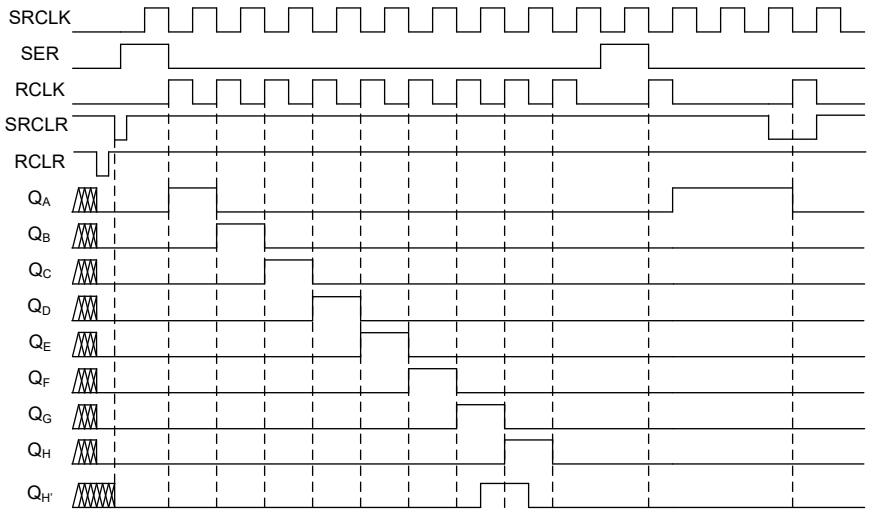


Figure 5-1. Timing Diagram

5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
F_{MAX}	-	-	C_L = 15 pF	3.3 V ± 0.3 V	95	170		80		0	70			MHz
T_{PLH}	RCLK	Q_A-Q_H	C_L = 15 pF	3.3 V ± 0.3 V		6	11.9	1		13.5	1		14.9	ns
T_{PHL}	RCLK	Q_A-Q_H	C_L = 15 pF	3.3 V ± 0.3 V		6	11.9	1		13.5	1		14.9	ns
T_{PHL}	$\overline{RCLR}$	Q_A-Q_H	C_L = 15 pF	3.3 V ± 0.3 V		6	9.8	1		12.9	1		13.6	ns
T_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF	3.3 V ± 0.3 V		6.6	13	1		15	1		16.4	ns

5.7 Switching Characteristics (continued)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
T_{PHL}	SRCLK	$Q_{H'}$	C_L = 15 pF	3.3 V ± 0.3 V		6.6	13	1		15	1		16.4	ns
T_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF	3.3 V ± 0.3 V		6.2	12.8	1		13.7	1		15	ns
F_{MAX}	-	-	C_L = 50 pF	3.3 V ± 0.3 V	55	130		50			50			MHz
T_{PLH}	RCLK	Q_A-Q_H	C_L = 50 pF	3.3 V ± 0.3 V		7.9	15.4	1		17	1		18.6	ns
T_{PHL}	RCLK	Q_A-Q_H	C_L = 50 pF	3.3 V ± 0.3 V		7.9	15.4	1		17	1		18.6	ns
T_{PHL}	$\overline{RCLR}$	Q_A-Q_H	C_L = 50 pF	3.3 V ± 0.3 V		9.1	13.5	1		16	1		16	ns
T_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF	3.3 V ± 0.3 V		9.2	16.5	1		18.5	1		20	ns
T_{PHL}	SRCLK	$Q_{H'}$	C_L = 50 pF	3.3 V ± 0.3 V		9.2	16.5	1		18.5	1		20	ns
T_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF	3.3 V ± 0.3 V		9	16.3	1		17.2	1		18.7	ns
F_{MAX}	-	-	C_L = 15 pF	5 V ± 0.5 V	135	240		115			115			MHz
T_{PLH}	RCLK	Q_A-Q_H	C_L = 15 pF	5 V ± 0.5 V		4.3	7.4	1		8.5	1		9.5	ns
T_{PHL}	RCLK	Q_A-Q_H	C_L = 15 pF	5 V ± 0.5 V		4.3	7.4	1		8.5	1		9.5	ns
T_{PHL}	$\overline{RCLR}$	Q_A-Q_H	C_L = 15 pF	5 V ± 0.5 V		4.5	7.6	1		8.9	1		9.2	ns
T_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF	5 V ± 0.5 V		4.5	8.2	1		9.4	1		10.4	ns
T_{PHL}	SRCLK	$Q_{H'}$	C_L = 15 pF	5 V ± 0.5 V		4.5	8.2	1		9.4	1		10.4	ns
T_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF	5 V ± 0.5 V		4.5	8	1		9.1	1		10.1	ns
F_{MAX}	-	-	C_L = 50 pF	5 V ± 0.5 V	120	180		95			95			MHz
T_{PLH}	RCLK	Q_A-Q_H	C_L = 50 pF	5 V ± 0.5 V		5.6	9.4	1		10.5	1		11.5	ns
T_{PHL}	RCLK	Q_A-Q_H	C_L = 50 pF	5 V ± 0.5 V		5.6	9.4	1		10.5	1		11.5	ns
T_{PHL}	$\overline{RCLR}$	Q_A-Q_H	C_L = 50 pF	5 V ± 0.5 V		6.6	10	1		11.4	1		11.7	ns
T_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF	5 V ± 0.5 V		6.4	10.2	1		11.4	1		12.4	ns
T_{PHL}	SRCLK	$Q_{H'}$	C_L = 50 pF	5 V ± 0.5 V		6.4	10.2	1		11.4	1		12.4	ns
T_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF	5 V ± 0.5 V		6.4	10	1		11.1	1		12.1	ns

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.9	-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

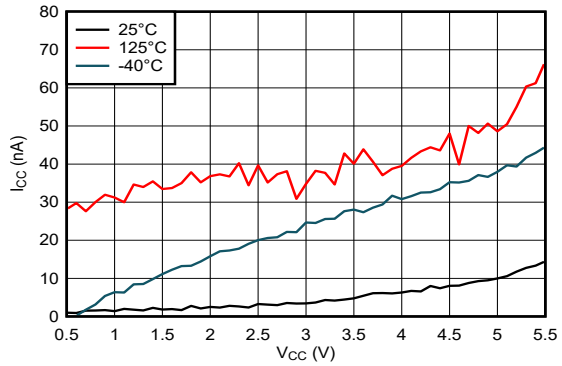


Figure 5-2. Supply Current Across Supply Voltage

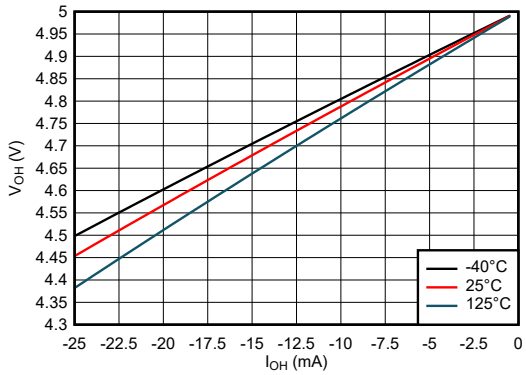


Figure 5-3. Output Voltage vs Current in HIGH State; 5V Supply

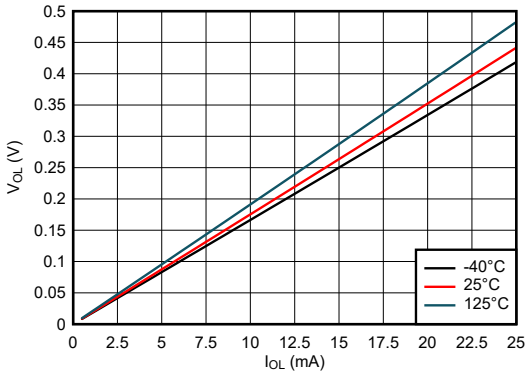


Figure 5-4. Output Voltage vs Current in LOW State; 5V Supply

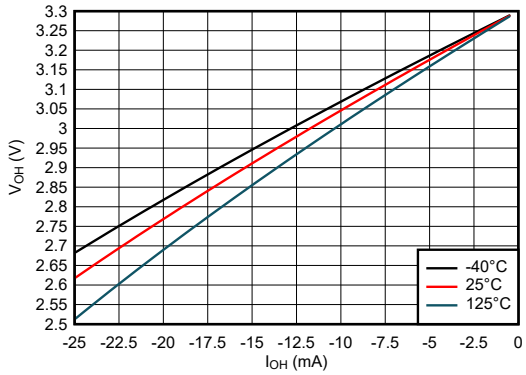


Figure 5-5. Output Voltage vs Current in HIGH State; 3.3V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

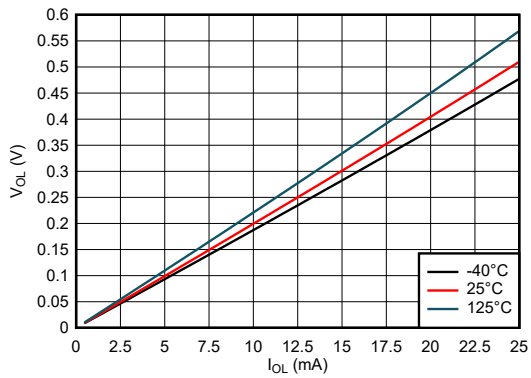


Figure 5-6. Output Voltage vs Current in LOW State; 3.3V Supply

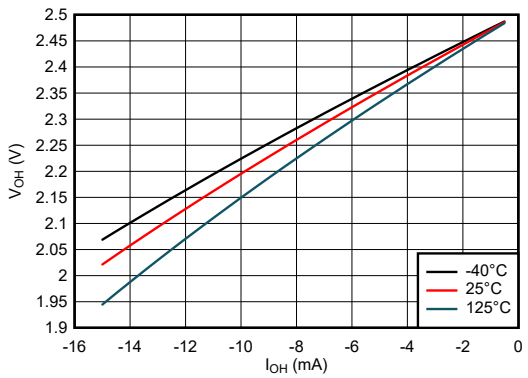


Figure 5-7. Output Voltage vs Current in HIGH State; 2.5V Supply

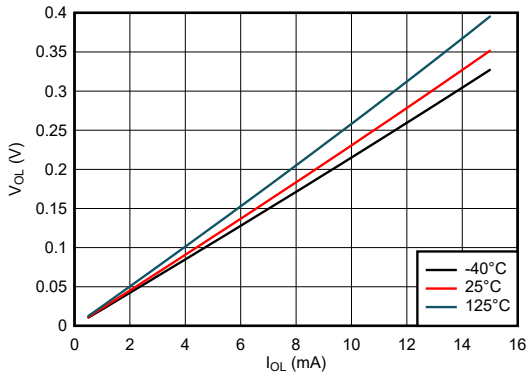


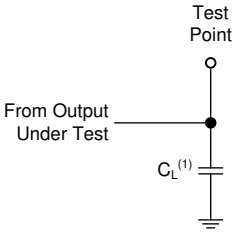
Figure 5-8. Output Voltage vs Current in LOW State; 2.5V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

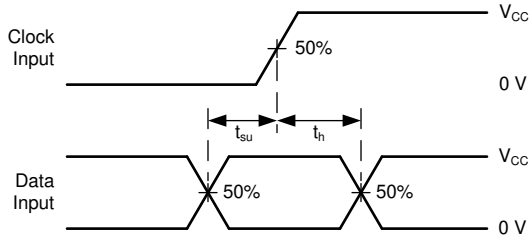
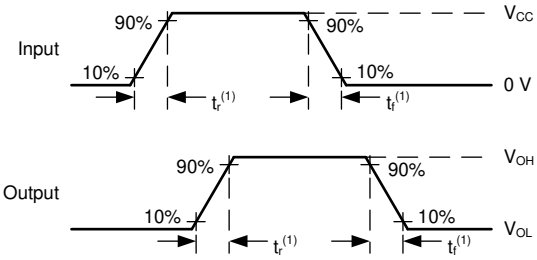


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

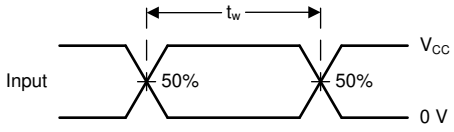
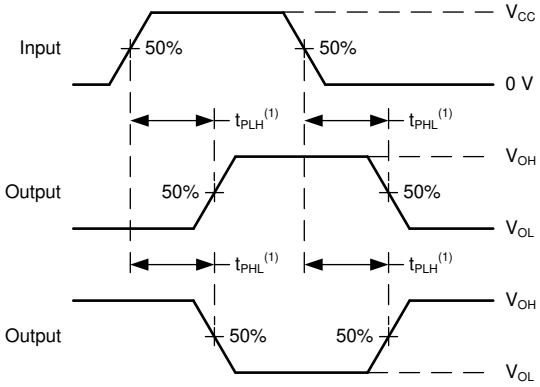
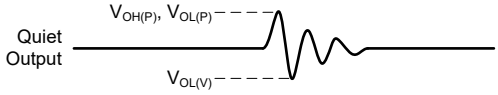


Figure 6-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



Noise values measured with all other outputs simultaneously switching.

Figure 6-6. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

The SN74AHC594-Q1 is an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, then the shift register always is one clock pulse ahead of the storage register.

The internal shift register has an active-low asynchronous clear input ($\overline{\text{SRCLR}}$) to force all registers into the low state.

The output register has an active-low asynchronous clear input ($\overline{\text{RCLR}}$) to force all registers into the low state.

The $Q_{H'}$ output provides a direct connection to the last stage of the internal shift register. This signal can be fed into another shift register device as the serial data input to create a cascade of shift registers.

7.2 Functional Block Diagram

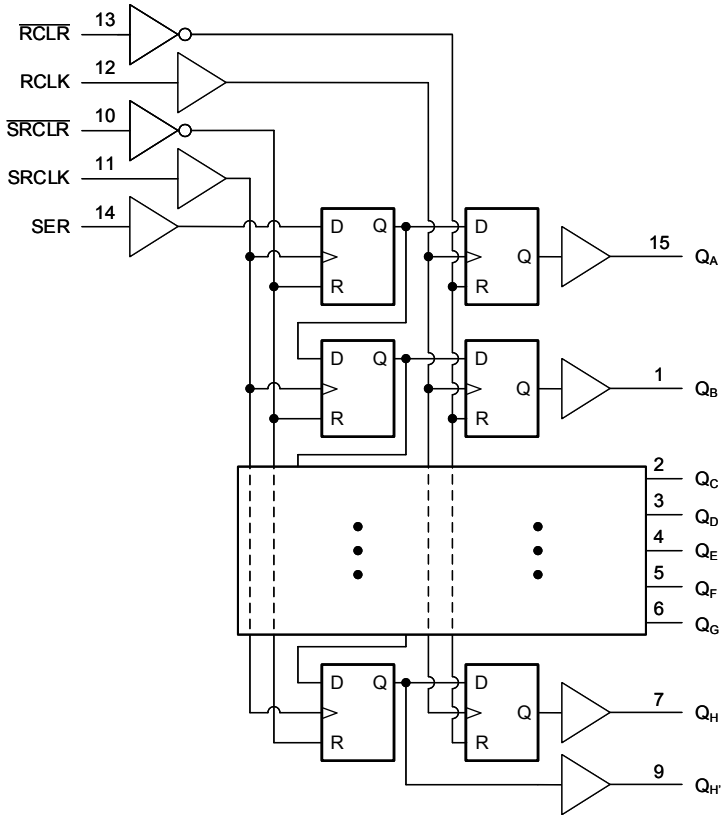


Figure 7-1. Logic Diagram (Positive Logic) for SN74AHC594-Q1

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

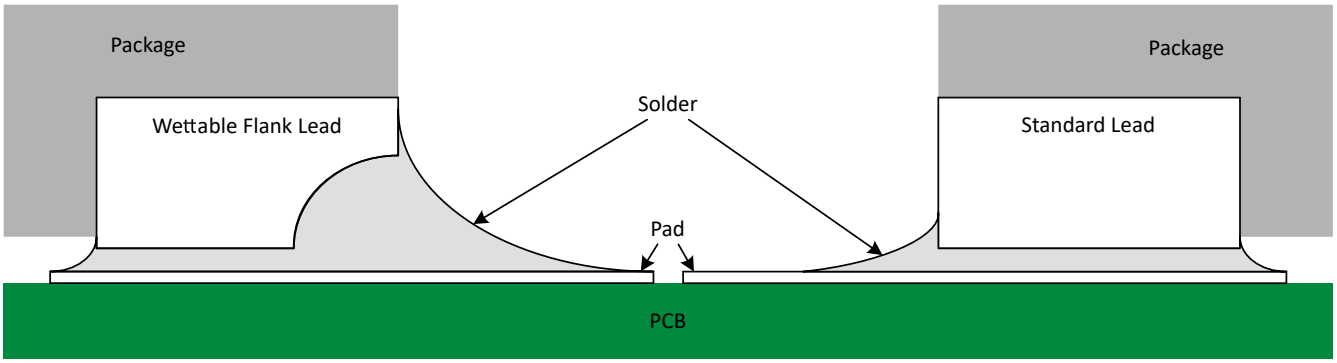


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 Clamp Diode Structure

As Figure 7-3 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

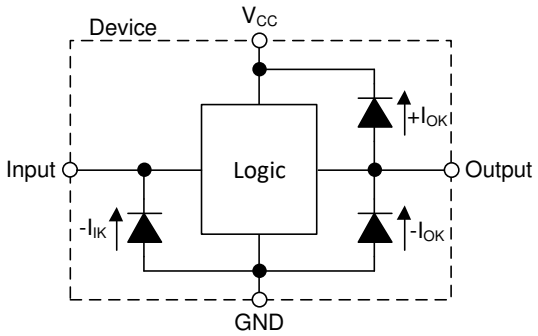


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AHC594-Q1.

Table 7-1. Function Table

INPUTS[1]					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	X	X	L	Output register is cleared
X	X	L	X	X	Internal shift register is cleared
H/L	↑	H	X	X	SER Data is loaded into first shift bit as H/L, data shifts from bit to bit within the internal shift register
X	X	H	↑	H	Data is transferred from internal shift register to output register
H/L	↑	H	↑	H	When SRCLK and RCLK are synchronous, Data is transferred from internal shift register to output register, internal shift register first bit is loaded with SER data H/L and data shifts from bit to bit within internal shift register
X	↓, L, H	H	X	X	Internal shift register remains in previous state
X	X	H	↓, L, H	H	Output register remains in previous state

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74AHC594-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74AHC594-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

There is no practical limitation to how many SN74AHC594-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register. See the application note, *Designing with Shift Registers*, for solutions to common design challenges around cascading shift registers.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, both registers need to be cleared. An RC network can be connected to the $\overline{\text{SRCLR}}$ and $\overline{\text{RCLR}}$ pins as shown to initialize the shift and output registers to all zeros.

8.2 Typical Application

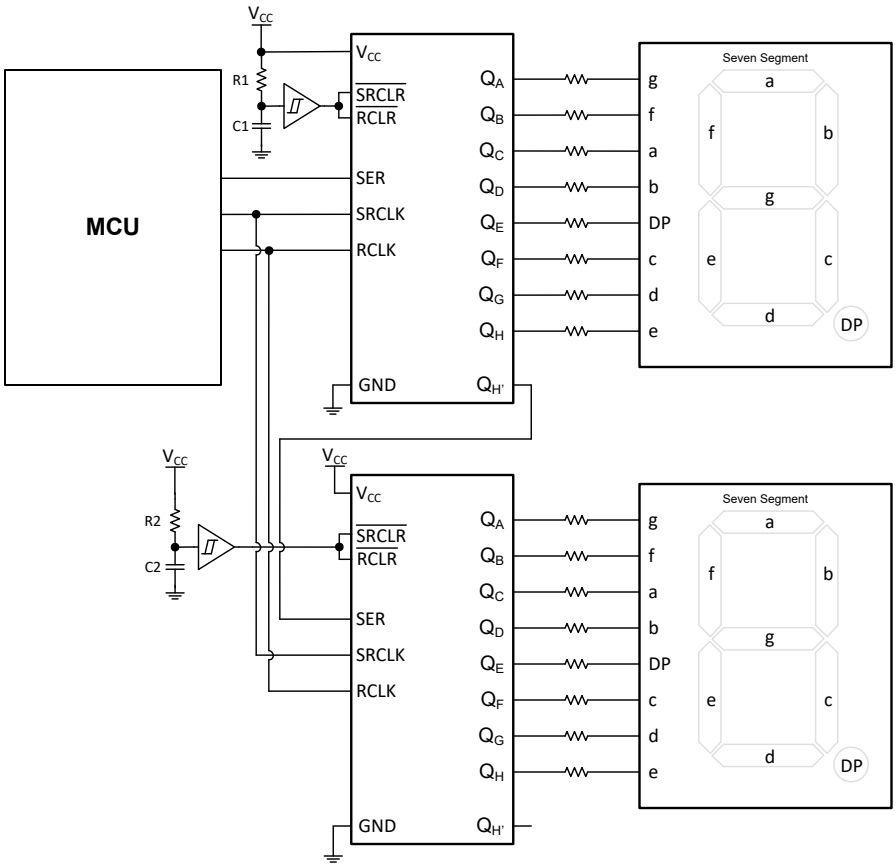


Figure 8-1. Typical Application Block Diagram

8.3 Design Requirements

8.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC594-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC594-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC594-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC594-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC594-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AHC594-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground

voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC594-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.5 Application Curves

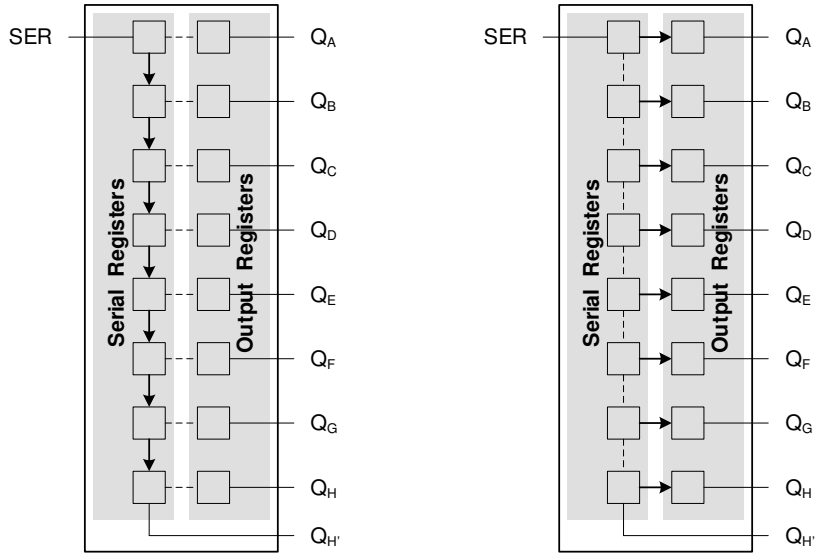


Figure 8-2. Simplified Functional Diagram Showing Clock Operation

8.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass

capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.7 Layout

8.7.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.7.2 Layout Example

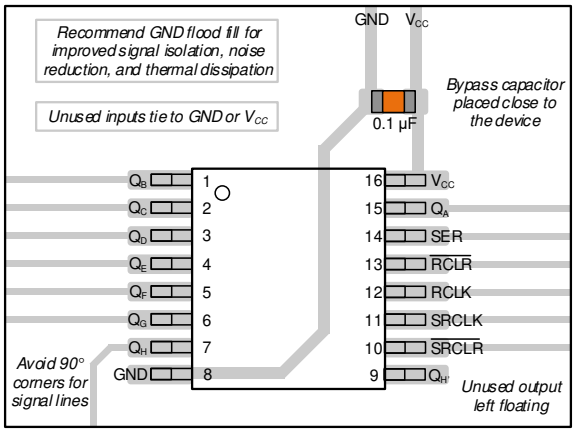


Figure 8-3. Example Layout for the SN74AHC594-Q1 in the PW Package

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC594QPWRQ1	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594Q	Samples
SN74AHC594QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH594Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHC594-Q1 :

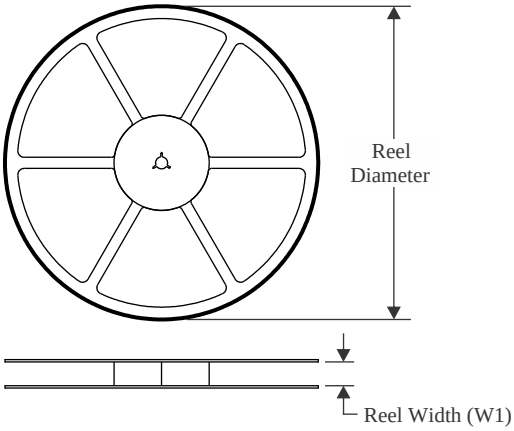
- Catalog : SN74AHC594

NOTE: Qualified Version Definitions:

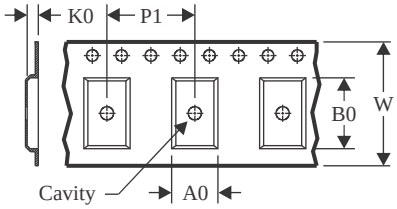
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

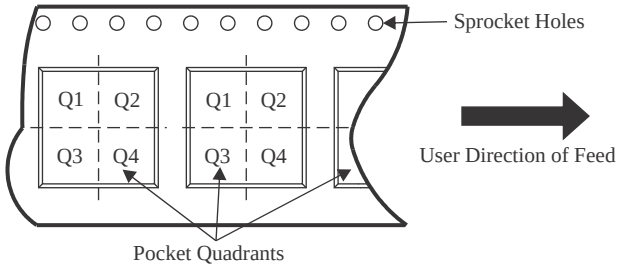


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

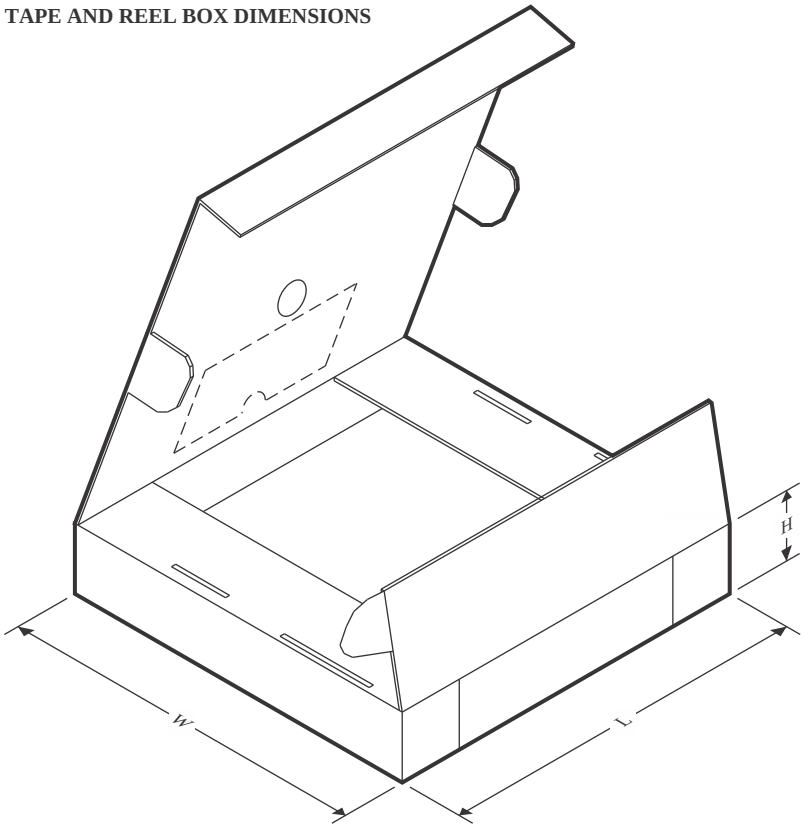
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC594QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC594QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC594QPWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0
SN74AHC594QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

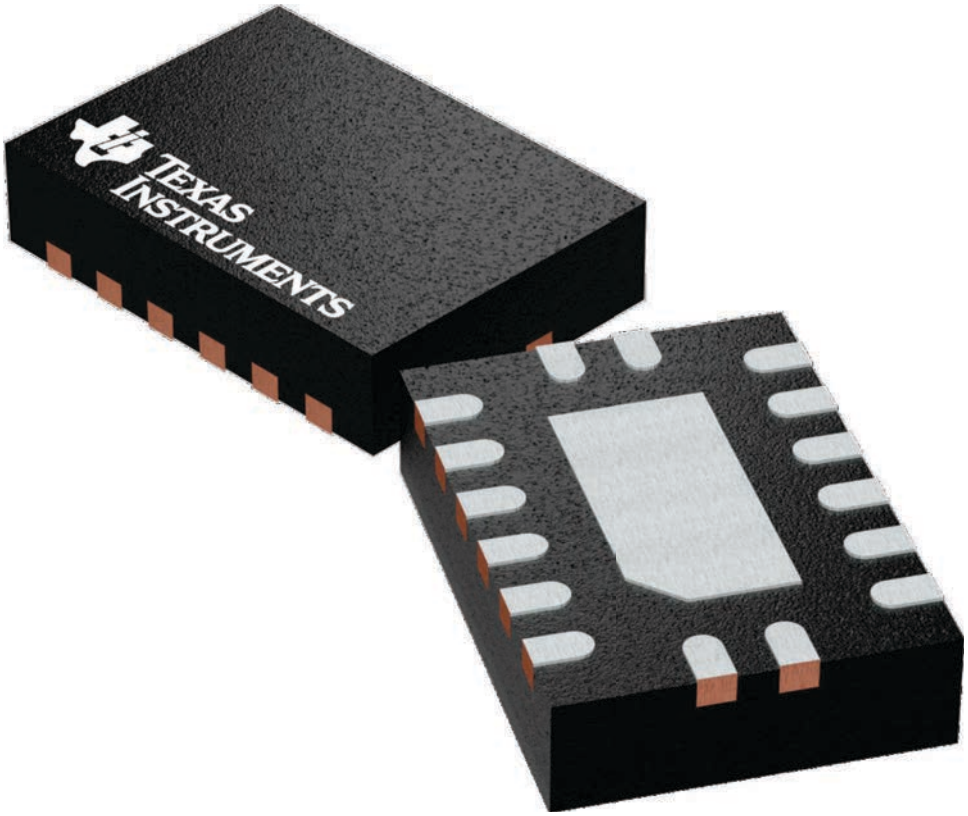
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



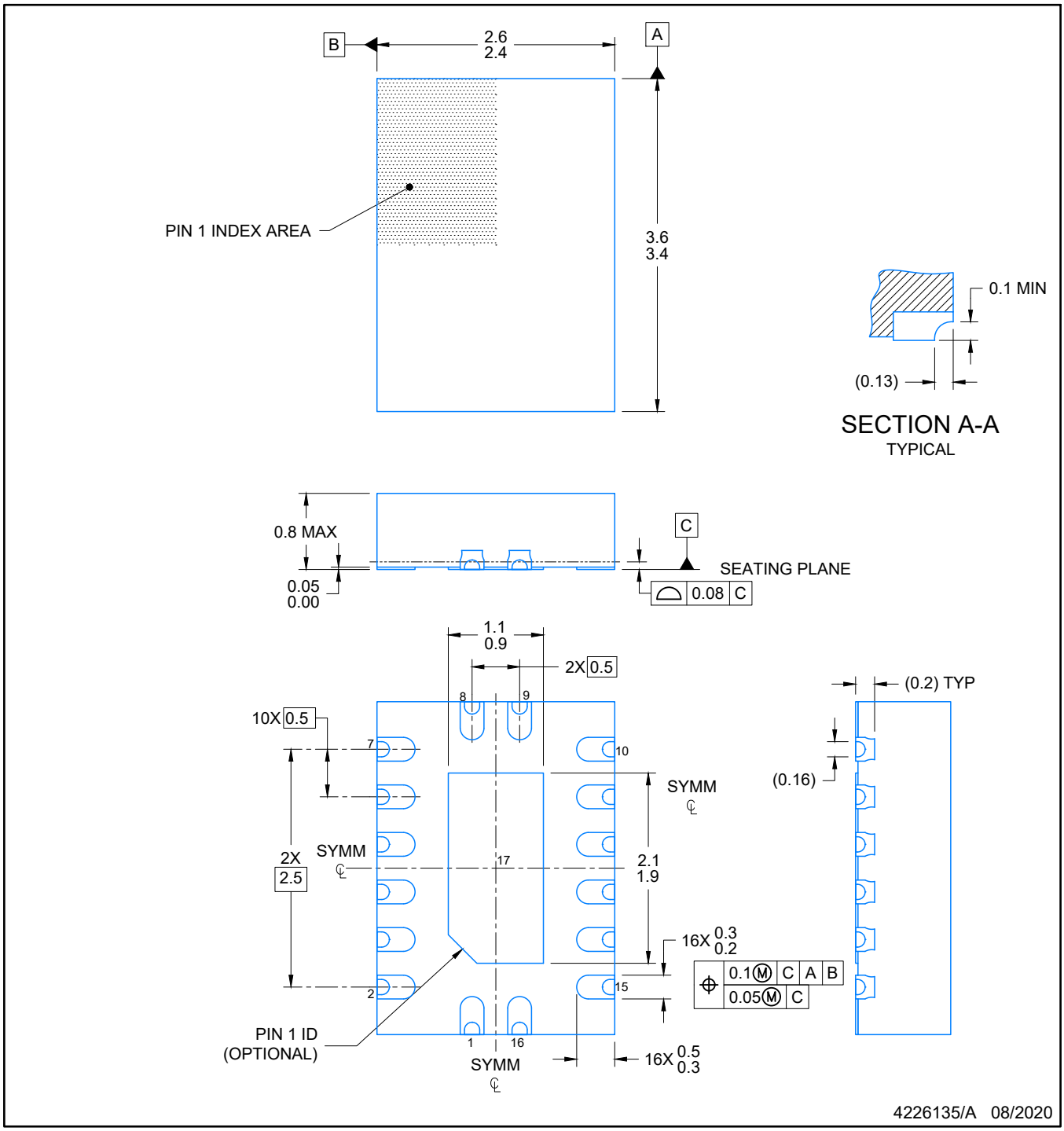
4226161/A

PACKAGE OUTLINE

BQB0016B

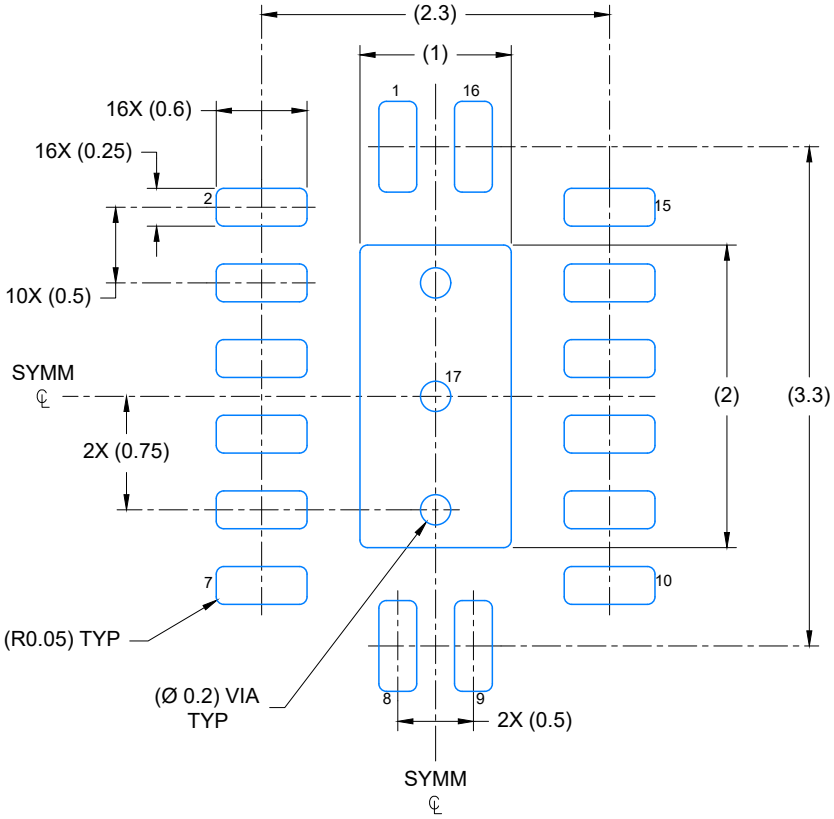
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

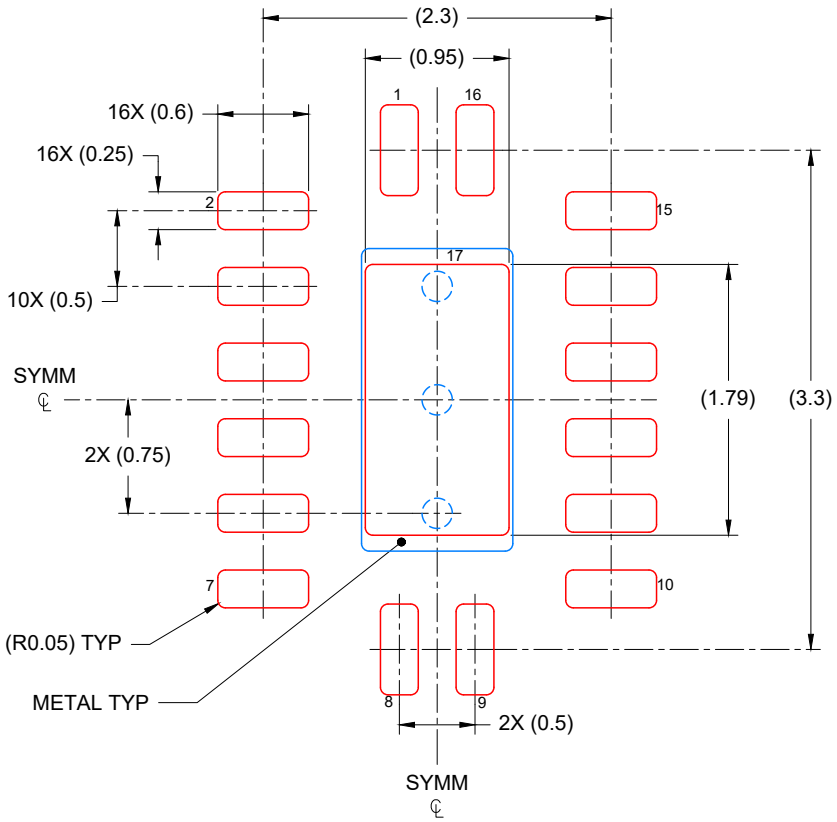


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

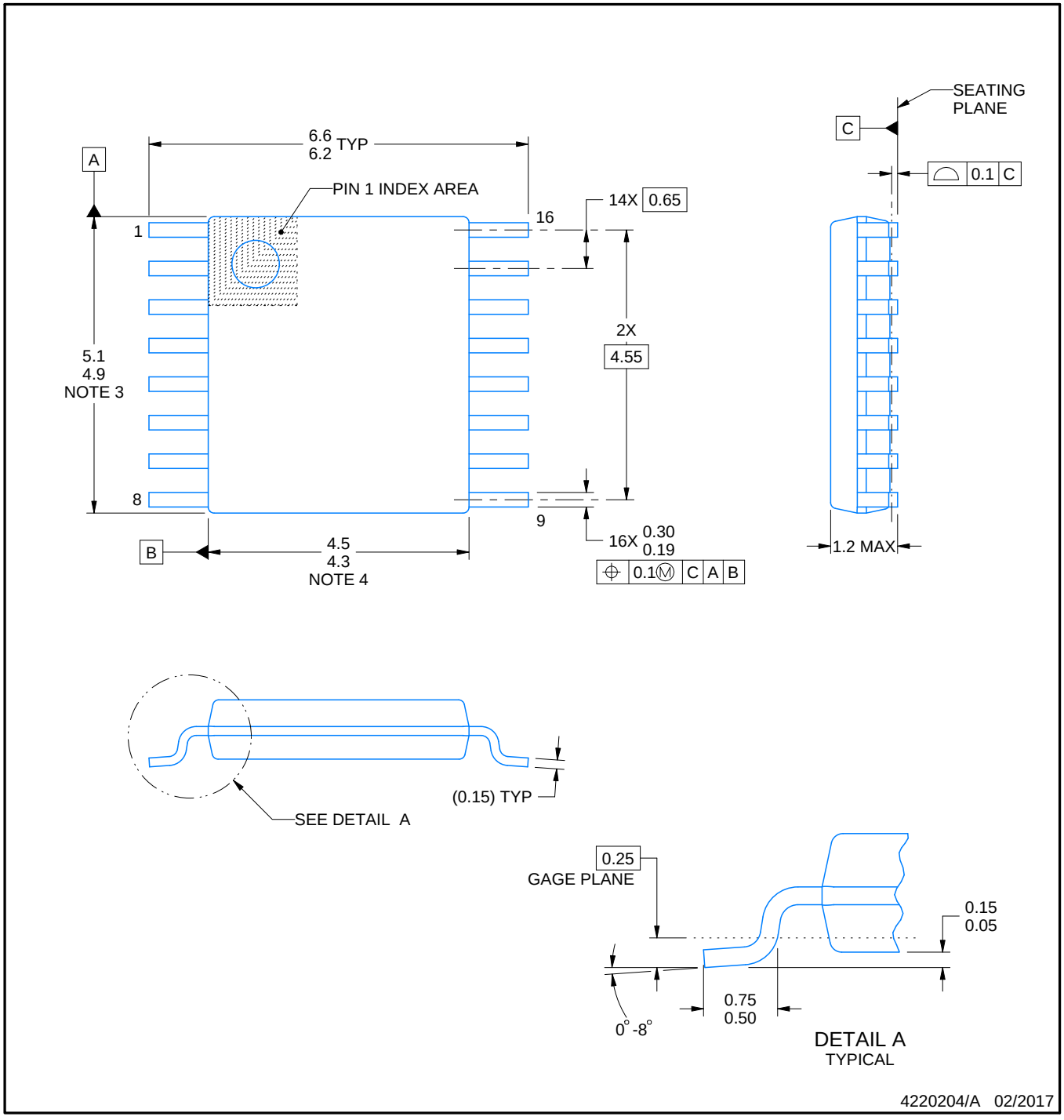
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

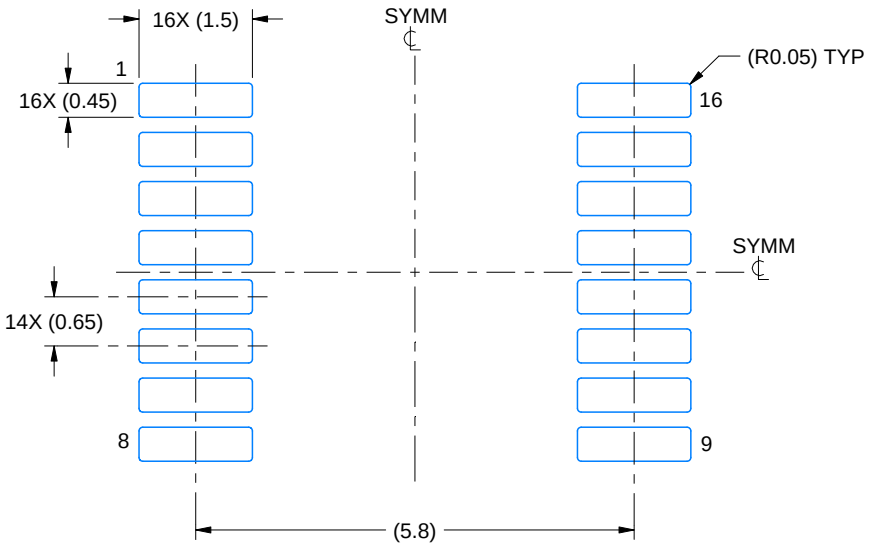
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

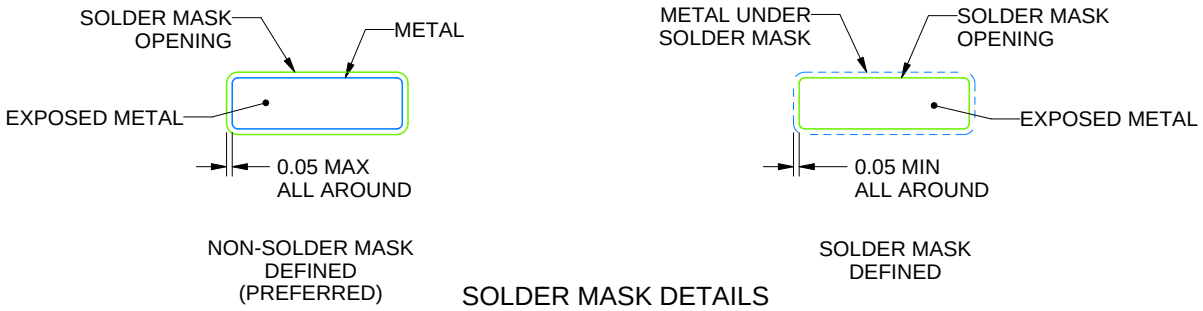


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

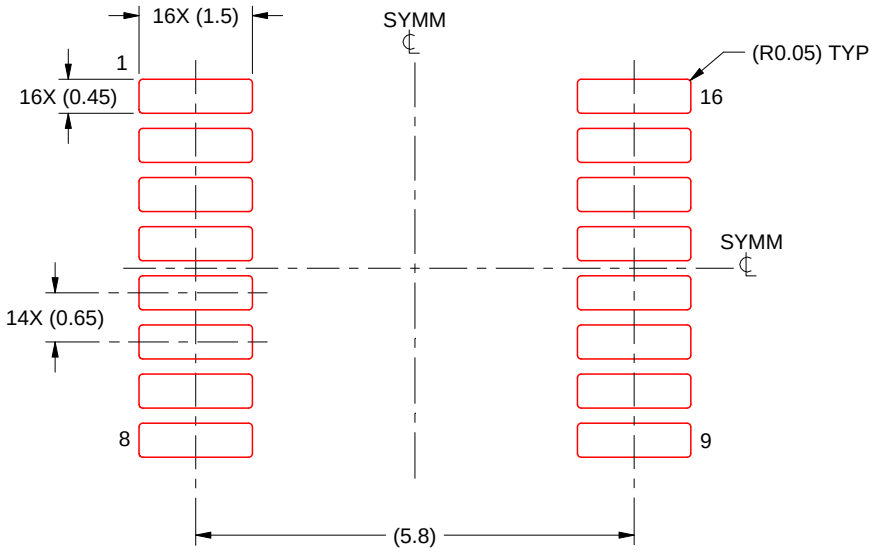


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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