SNx4AHC541 Octal Buffers/Drivers With 3-State Outputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points-of-Sale

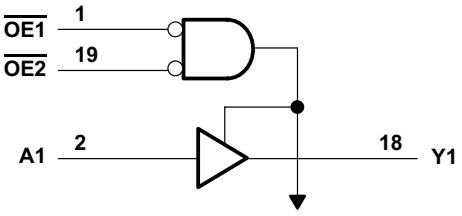
3 Description

The SNx4AHC541 octal buffers and drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4AHC541	N (PDIP, 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	NS (SOP, 20)	12.6mm x 7.8mm	12.6mm x 5.3mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm x 5.30mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm x 4.40mm
	DGV (TVSOP, 20)	5.00mm x 6.4mm	5.00mm x 4.40mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm x 7.50mm
	J (CDIP, 20)	24.2mm x 7.62mm	24.2mm x 6.92mm
	W (CFP, 20)	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK (LCCC, 20)	8.89mm x 8.89mm	8.89mm x 8.89mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Block Diagram

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4 Pin Configuration and Functions

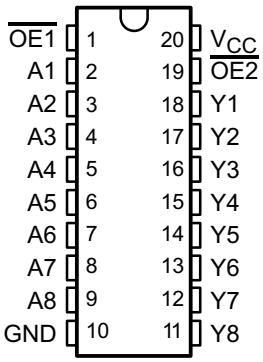


Figure 4-1. DB, PW, DGV, DW, N, or NS Package; 20-Pin, SSOP, TSSOP, TVSOP, SOIC, PDIP, or SOP (Top View)

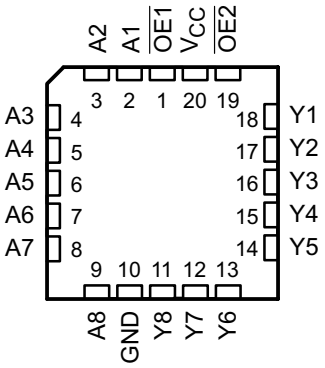


Figure 4-2. FK Package 20-Pin LCCC (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	$\overline{OE2}$	I	Output Enable 2
20	V_{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AHC541		SN74AHC541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level Input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHC541						UNIT
		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.9	119.2	81.1	68.5	77.6	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.7	34.5	48.6	48.5	42.7	58.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	55.2	60.7	53.8	44.9	45.7	78.7	
ψ_{JT}	Junction-to-top characterization parameter	22.6	1.2	19.5	28.0	10.2	12.6	
ψ_{JB}	Junction-to-board characterization parameter	54.8	60.0	53.1	44.5	45.2	77.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC541		SN74AHC541		SN74AHC541 –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I_{OH} = 4 mA	3 V			0.36		0.5		0.44		0.5	
	I_{OH} = 8 mA	4.5 V			0.36		0.5		0.44		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[1]		±1		±1	µA
I_{OZ} [2]	$V_O = V_{CC}$ or GND V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5		±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND I_O = 0	5.5 V			4		40		40		20	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10			pF
C_O	$V_O = V_{CC}$ or GND	5 V		4								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) For input and output pins, I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		SN54AHC541		SN74AHC541		SN74AHC541 T_A = –40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF	5(1)	7(1)	1(1)	8.5(1)	1	8.5	1	8.5	ns
t_{PHL}				5(1)	7(1)	1(1)	8.5(1)	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF	6(1)	10.5(1)	1(1)	11(1)	1	11	1	11	ns
t_{PZL}				6(1)	10.5(1)	1(1)	11(1)	1	11	1	11	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF	7(1)	11(1)	1(1)	12(1)	1	12	1	12	ns
t_{PLZ}				7(1)	11(1)	1(1)	12(1)	1	12	1	12	
t_{PLH}	A	Y	C_L = 50 pF	7.5	10.5	1	12	1	12	1	12	ns
t_{PHL}				7.5	10.5	1	12	1	12	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF	8	14	1	16	1	16	1	16	ns
t_{PZL}				8	14	1	16	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF	9	15.4	1	17.5	1	17.5	1	17.5	ns
t_{PLZ}				9	15.4	1	17.5	1	17.5	1	17.5	
$t_{sk(o)}$			C_L = 50 pF		1.5(2)				1.5			ns
t_{PLH}	A or B	Y	C_L = 50 pF	6.3	8.8	1	10	1	10	1	10	ns
t_{PHL}				6.3	8.8	1	10	1	10	1	10	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		SN54AHC541		SN74AHC541		T_A = –40°C to 125°C SN74AHC541		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF	3.5(1)	5(1)	1(1)	6(1)	1	6	1	6	ns
t_{PHL}				3.5(1)	5(1)	1(1)	6(1)	1	6	1	6	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF	4.7(1)	7.2(1)	1(1)	8.5(1)	1	8.5	1	8.5	ns
t_{PZL}				4.7(1)	7.2(1)	1(1)	8.5(1)	1	8.5	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF	5(1)	7.5(1)	1(1)	8(1)	1	8	1	8	ns
t_{PLZ}				5(1)	7.5(1)	1(1)	8(1)	1	8	1	8	
t_{PLH}	A	Y	C_L = 50 pF	5	7	1	8	1	8	1	8	ns
t_{PHL}				5	7	1	8	1	8	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF	6.2	9.2	1	10.5	1	10.5	1	10.5	ns
t_{PZL}				6.2	9.2	1	10.5	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF	6	8.8	1	10	1	10	1	10	ns
t_{PLZ}				6	8.8	1	10	1	10	1	10	
$t_{sk(o)}$			C_L = 50 pF		1(2)	1			1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SN74AHC541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

5.10 Typical Characteristics

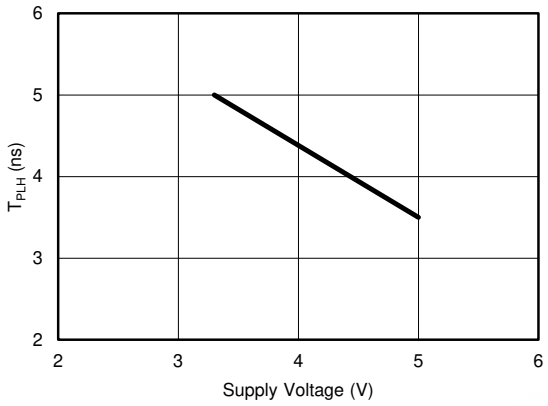
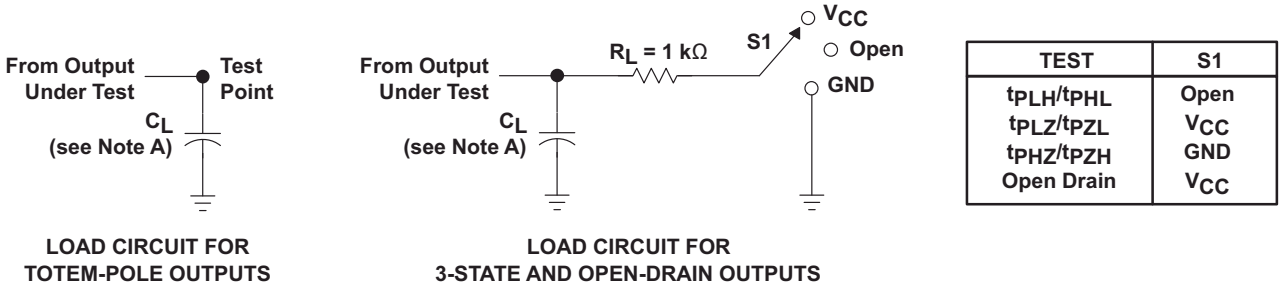


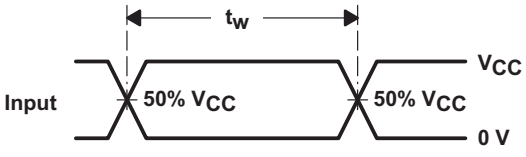
Figure 5-1. T_{PD} (Typical) vs V_{CC} at C_L = 15pF & T_A = 25°C

6 Parameter Measurement Information

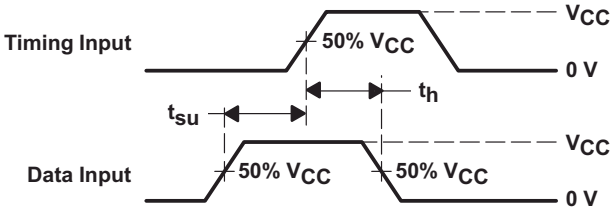


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

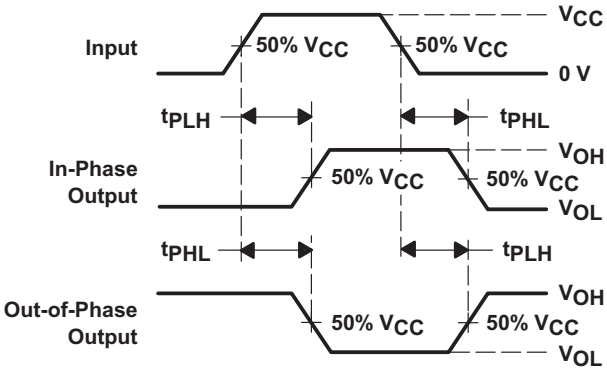
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



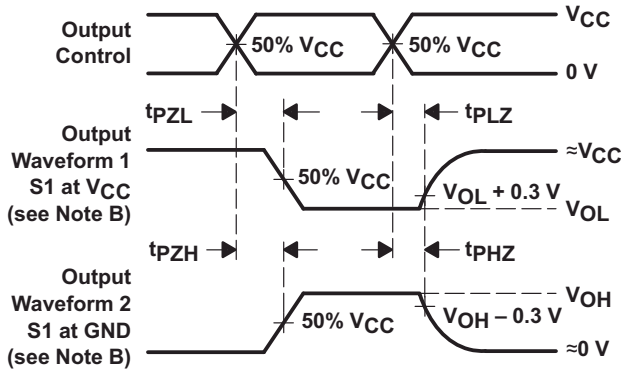
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

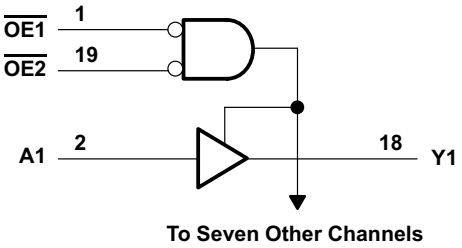
7.1 Overview

The SNx4AHC541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

The SNx4AHC541 has a wide operating voltage range of 2 V to 5.5 V. It allows down voltage translations while accepting input voltages of up to 5.5 V. The slow edges of the SNx4AHC541 enables the reduction of output ringing.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for the SNx4AHC541 devices.

Table 7-1. Function Table (Each Buffer/Driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC541 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V, which allows down translation to the V_{CC} level. Figure 8-2 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

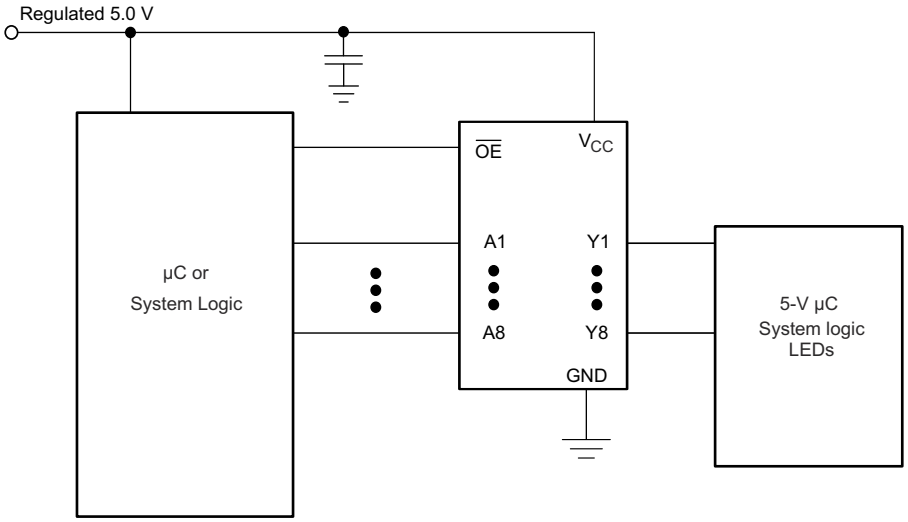


Figure 8-1. Typical Application Schematic

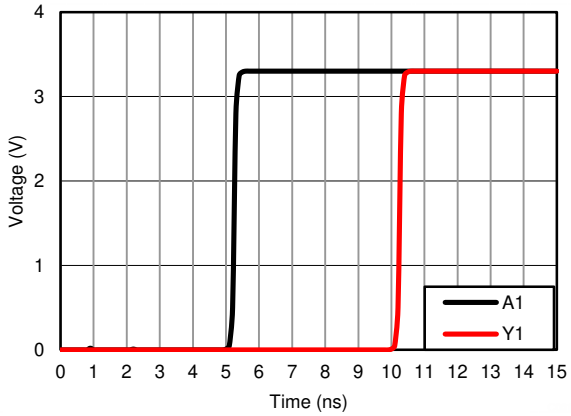
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/ΔV in the *Section 5.3* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Section 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curve



V_{cc} = 3.3 V, C_L = 15 pF, T_A = 25°C

Figure 8-2. Simulated Propagation Delay From Input (A1) to Output (Y1)

8.3 Power Supply Recommendations

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

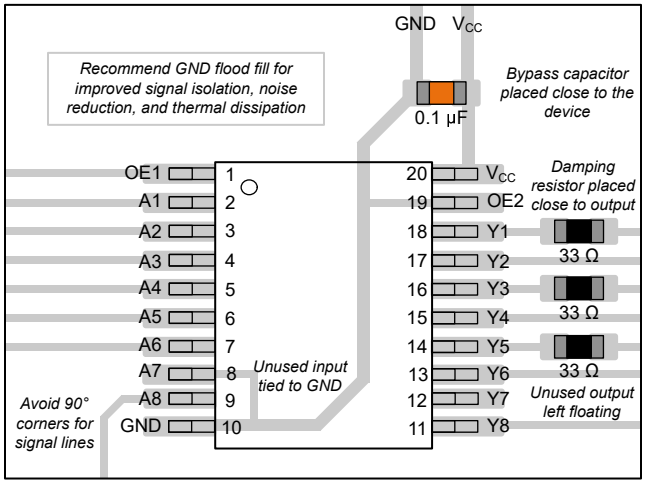


Figure 8-3. Example Layout for the SN74AHC541

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC541	Click here	Click here	Click here	Click here	Click here
SN54AHC541	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision P (August 2024) to Revision Q (January 2025)	Page
• Updated HBM and CDM values in *ESD Ratings* table	4

Changes from Revision O (September 2015) to Revision P (August 2024)	Page
• Added package size to *Device Information* table	1
• Updated structural layout of data sheet to current standards	1
• Updated RθJA values: PW = 105.4 to 116.8, DW = 83.0 to 81.1, N = 54.9 to 68.5, NS = 80.4 to 77.6; Updated PW, DW, N, and NS packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	5
• Updated *Layout Example* image	11

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685701Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701Q2A SNJ54AHC541FK	Samples
5962-9685701QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701QRA SNJ54AHC541J	Samples
5962-9685701QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701QSA SNJ54AHC541W	Samples
SN74AHC541DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA541	Samples
SN74AHC541DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA541	Samples
SN74AHC541DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHC541	
SN74AHC541DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC541	Samples
SN74AHC541DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC541	Samples
SN74AHC541N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC541N	Samples
SN74AHC541NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC541	Samples
SN74AHC541PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	HA541	
SN74AHC541PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(AHC541, HA541)	Samples
SN74AHC541PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA541	Samples
SN74AHC541PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA541	Samples
SNJ54AHC541FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701Q2A SNJ54AHC541FK	Samples
SNJ54AHC541J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701QRA SNJ54AHC541J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC541W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685701QSA SNJ54AHC541W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC541, SN74AHC541 :

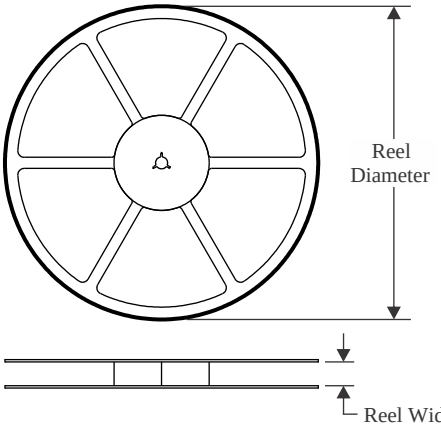
- Catalog : SN74AHC541
- Automotive : SN74AHC541-Q1, SN74AHC541-Q1
- Military : SN54AHC541

NOTE: Qualified Version Definitions:

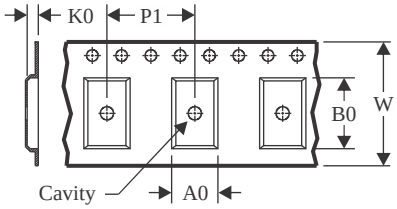
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

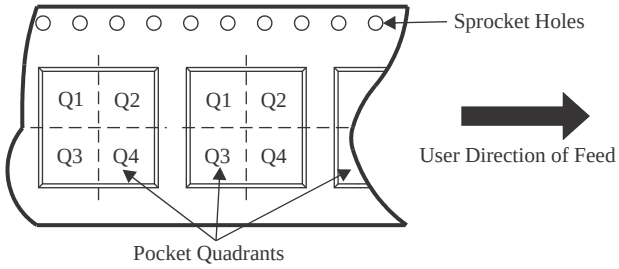


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

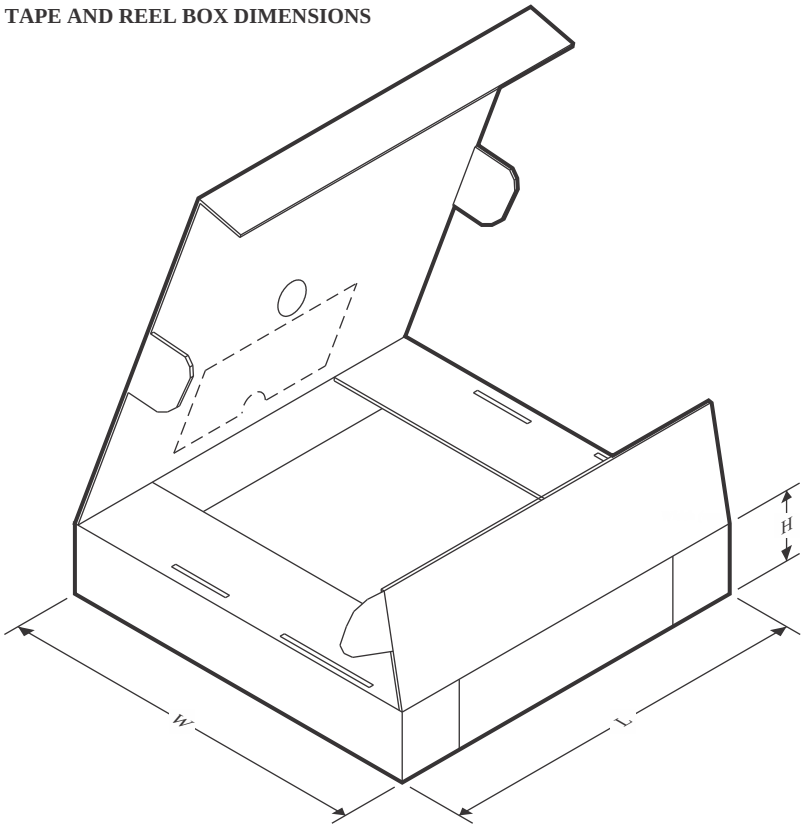
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC541DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

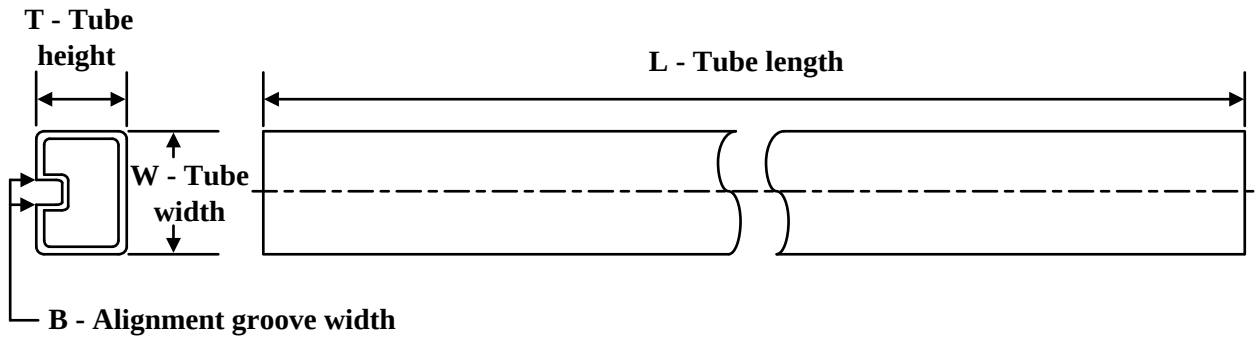
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC541DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHC541DGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74AHC541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC541NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHC541NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHC541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC541PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC541PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

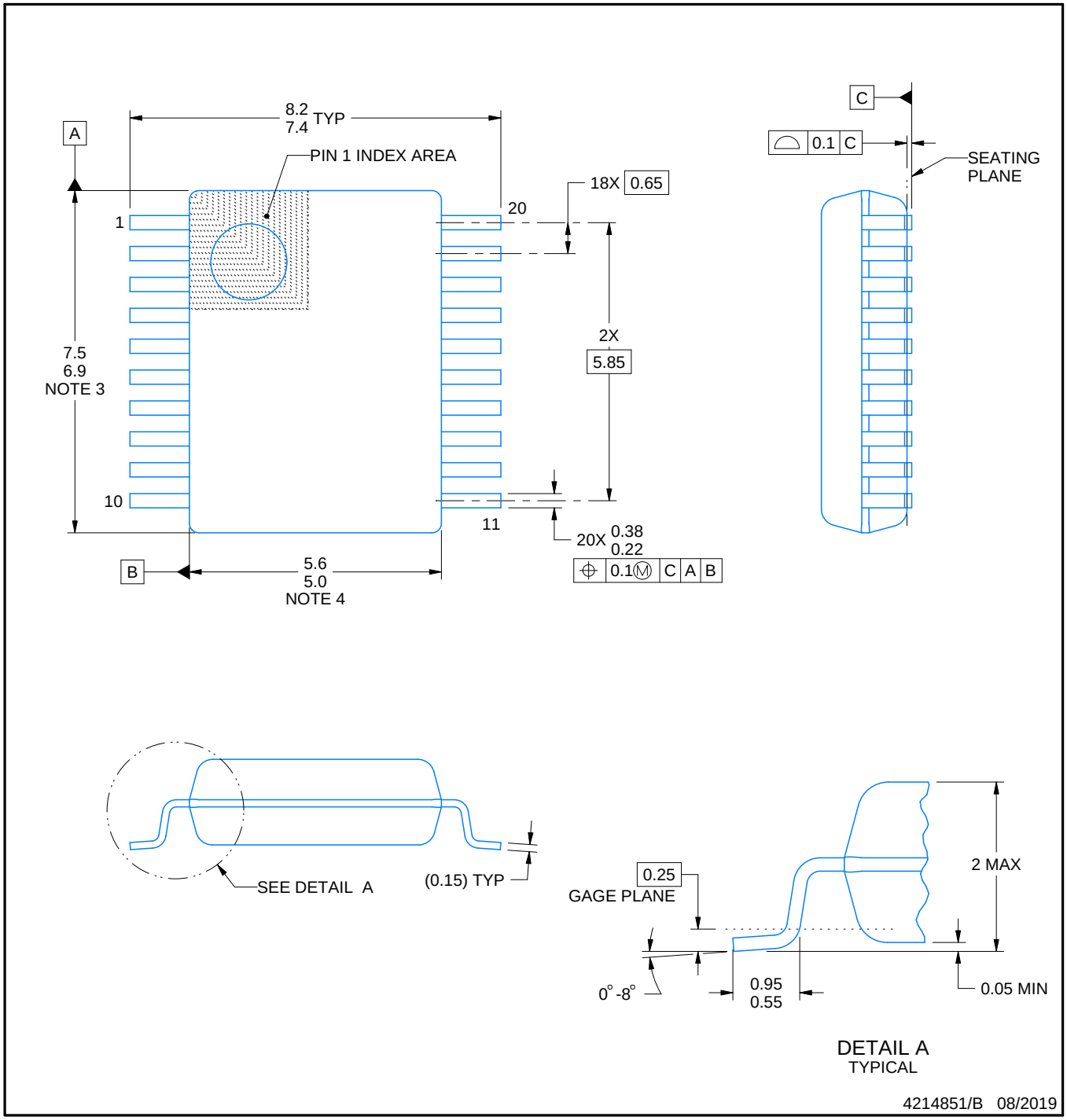
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9685701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC541N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC541FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC541W	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

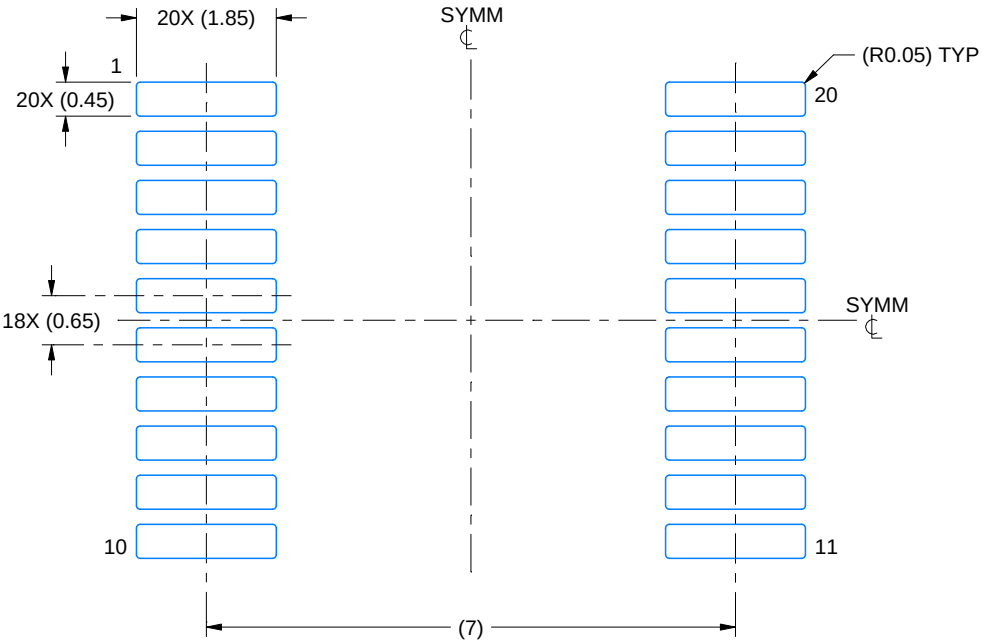
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

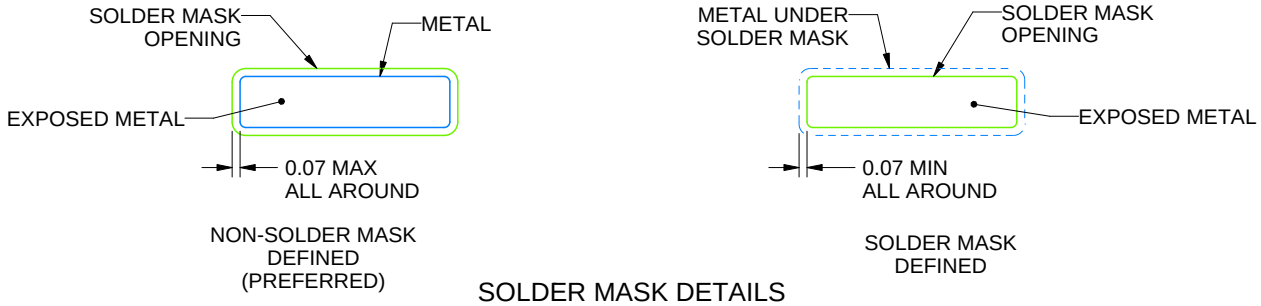


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

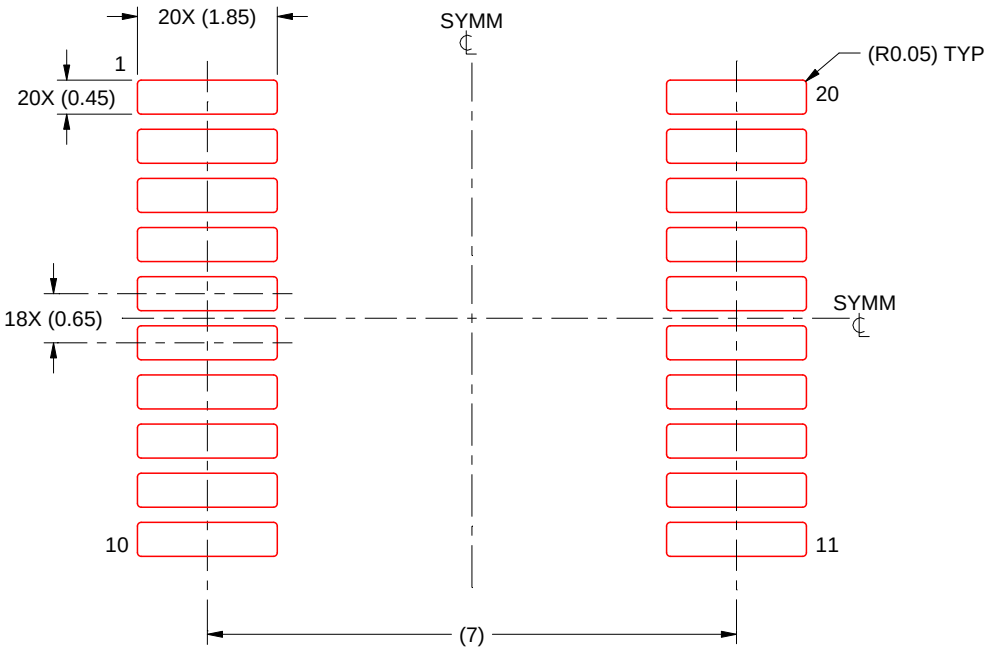
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

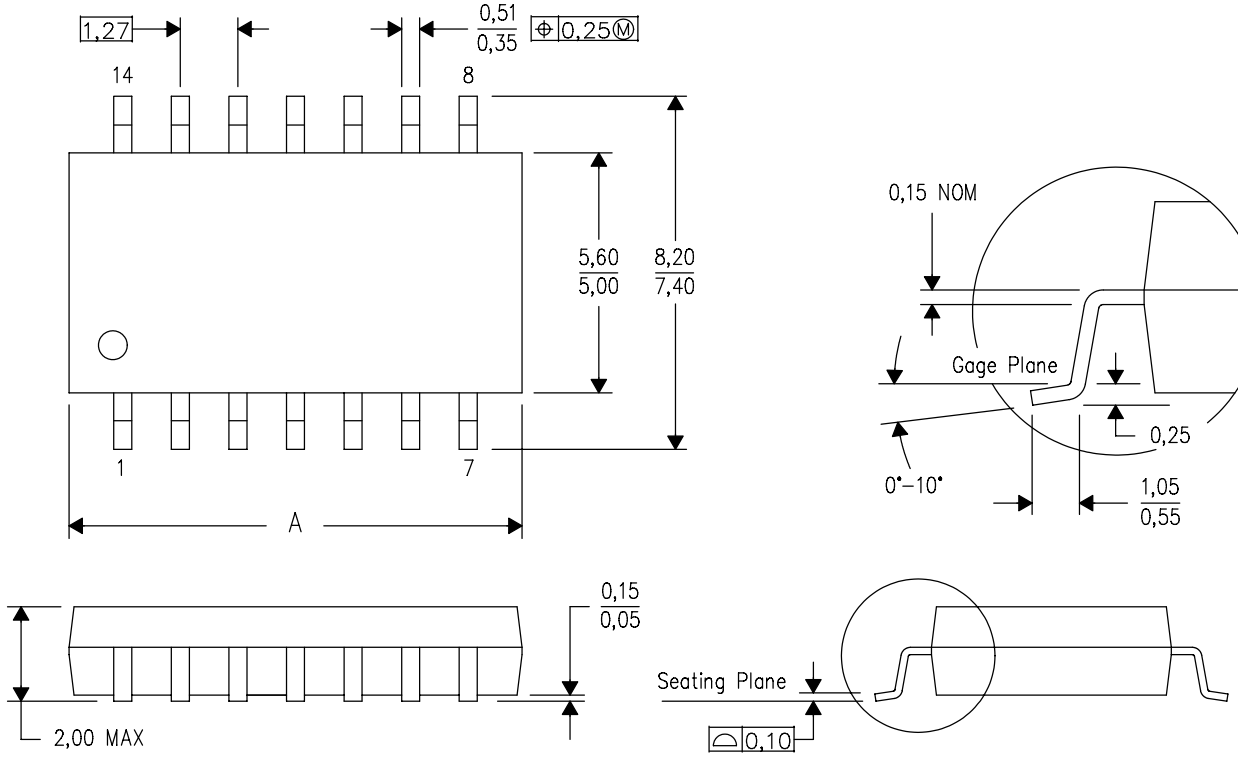
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

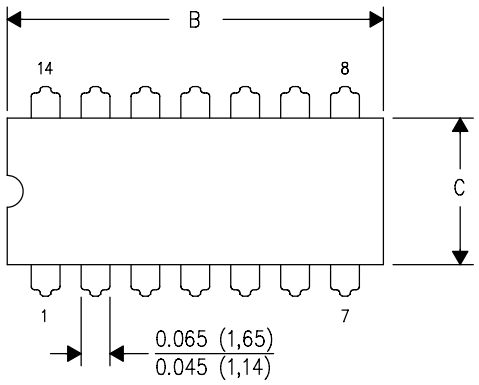
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

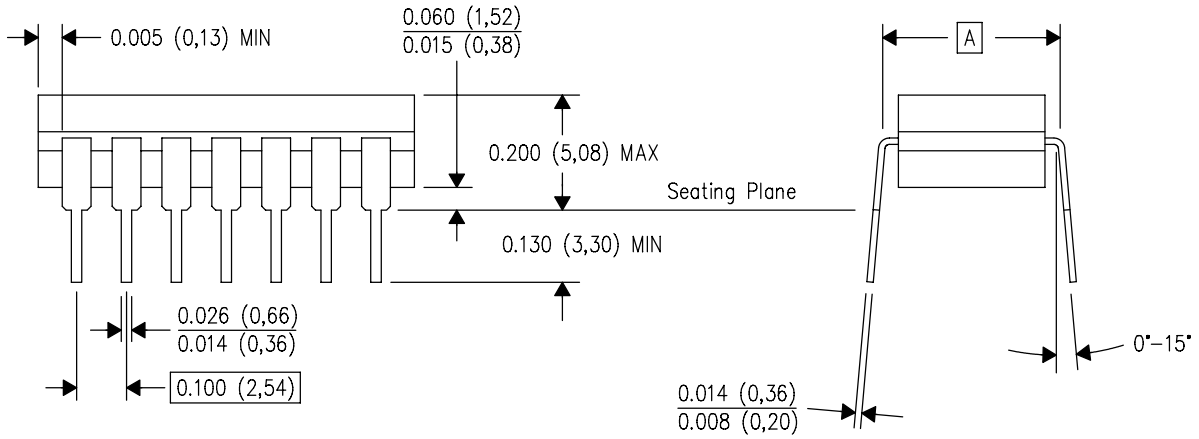
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

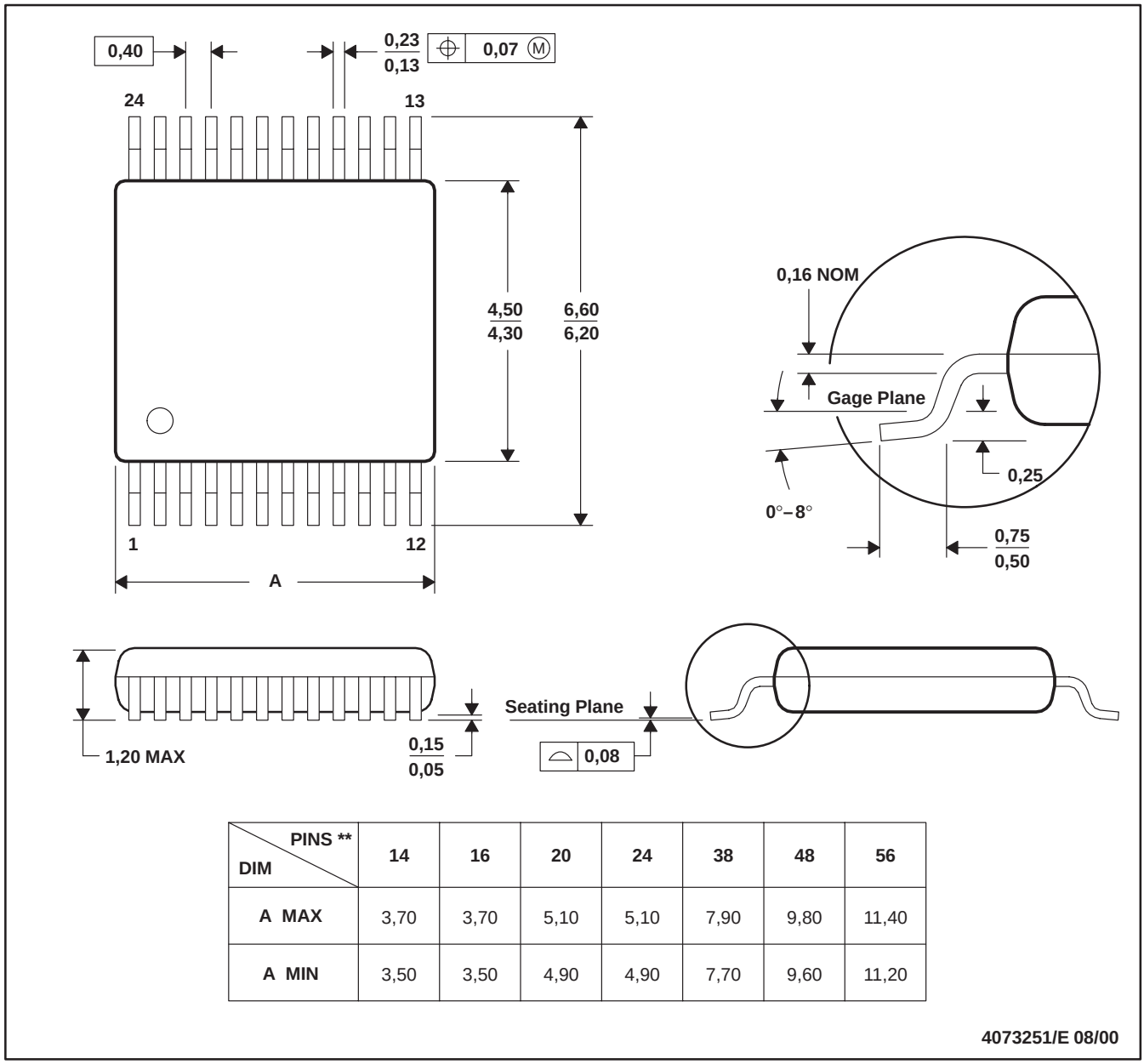


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

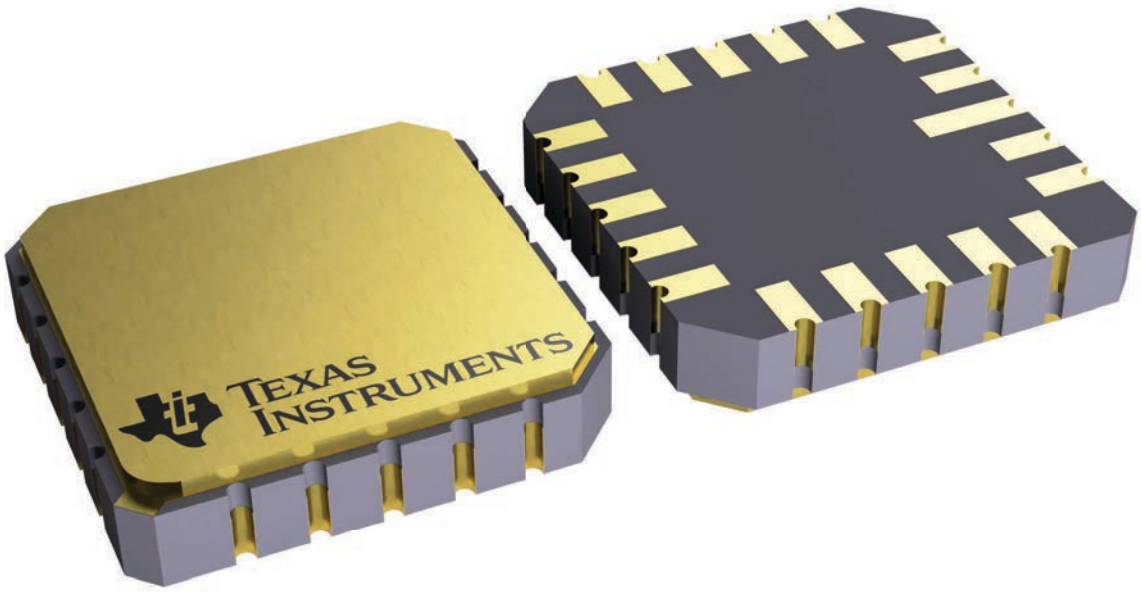
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

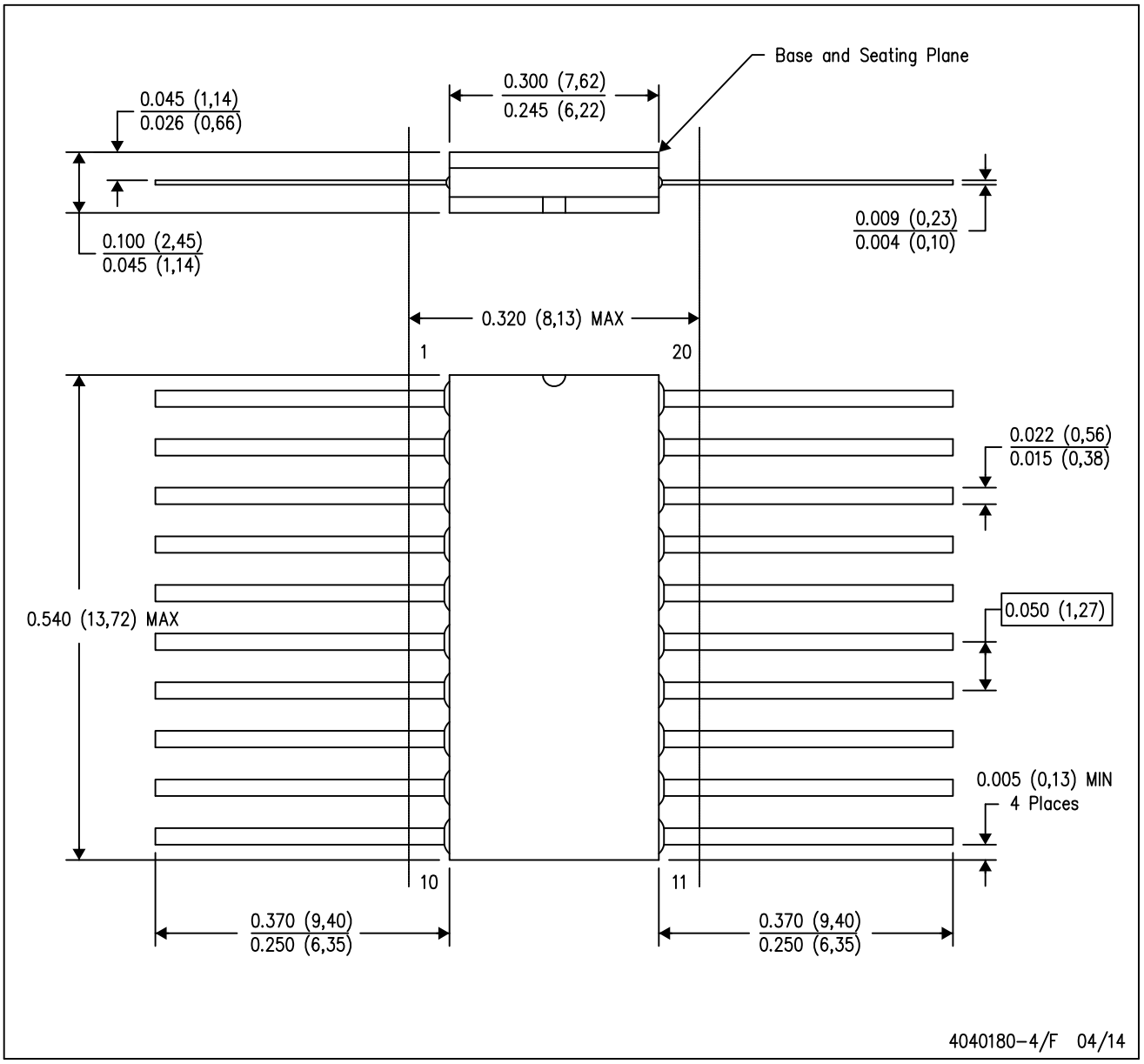
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



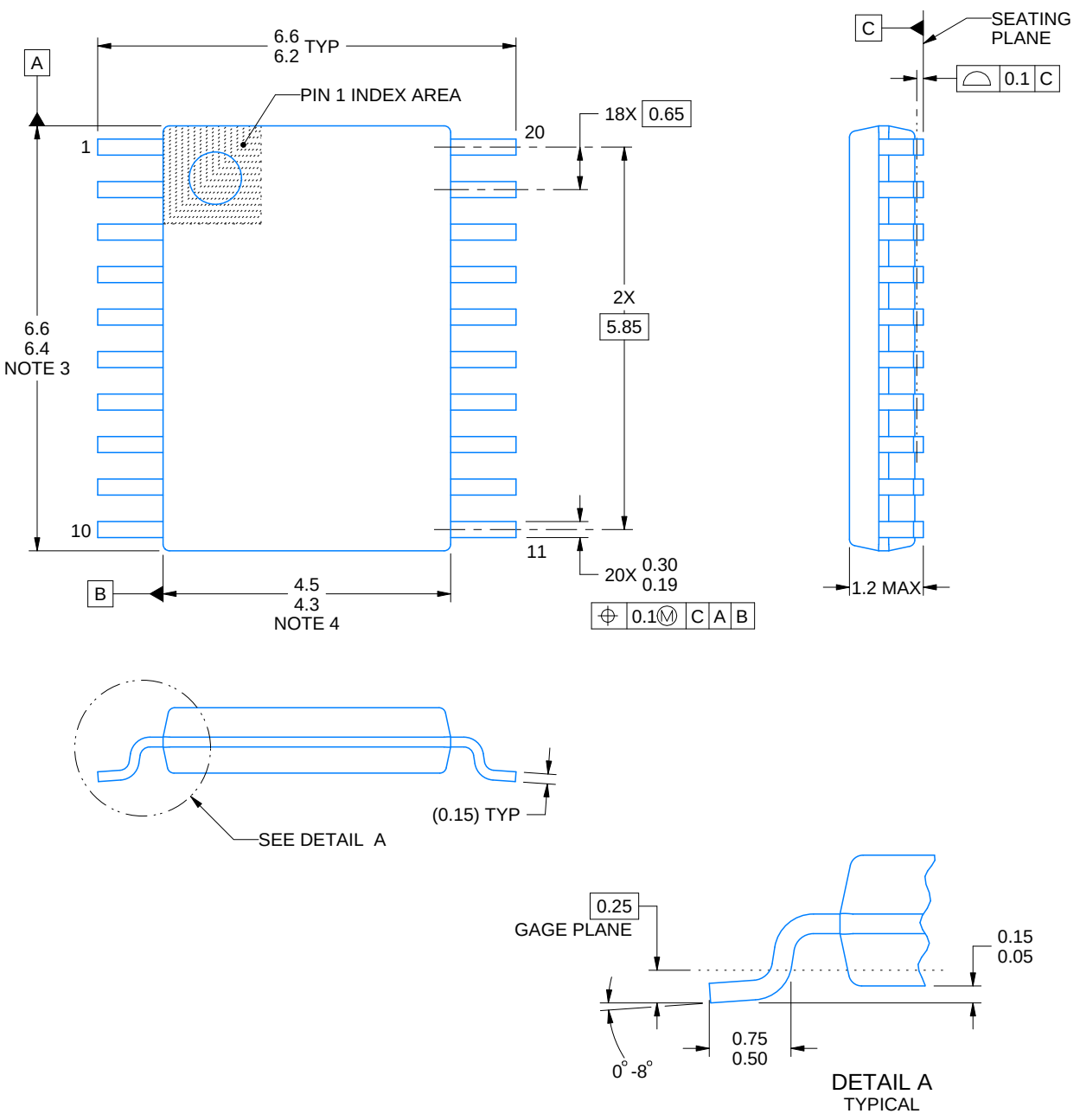
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

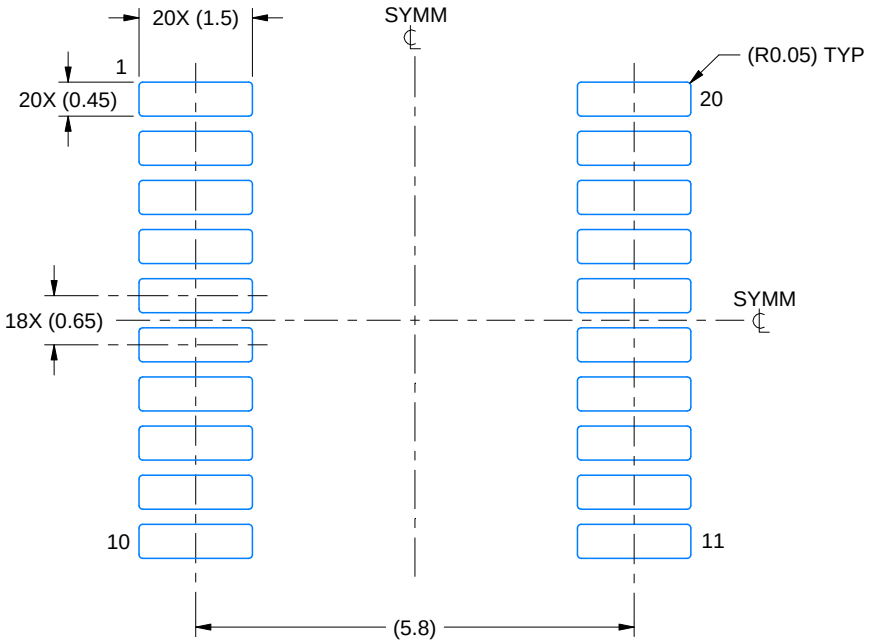
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



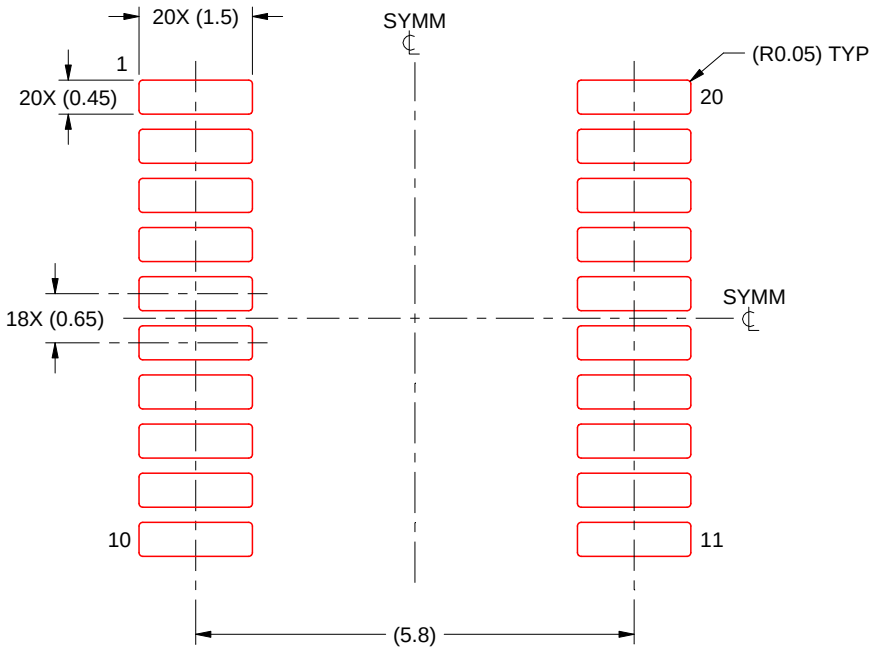
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

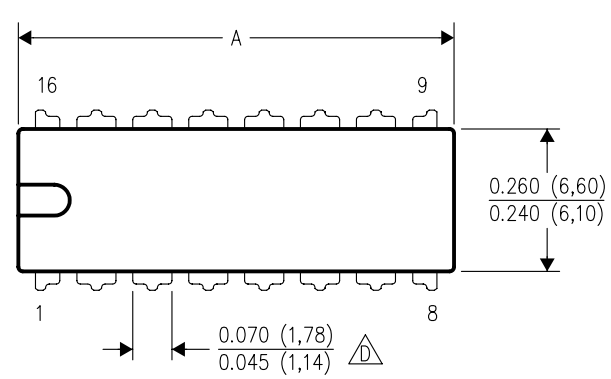
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

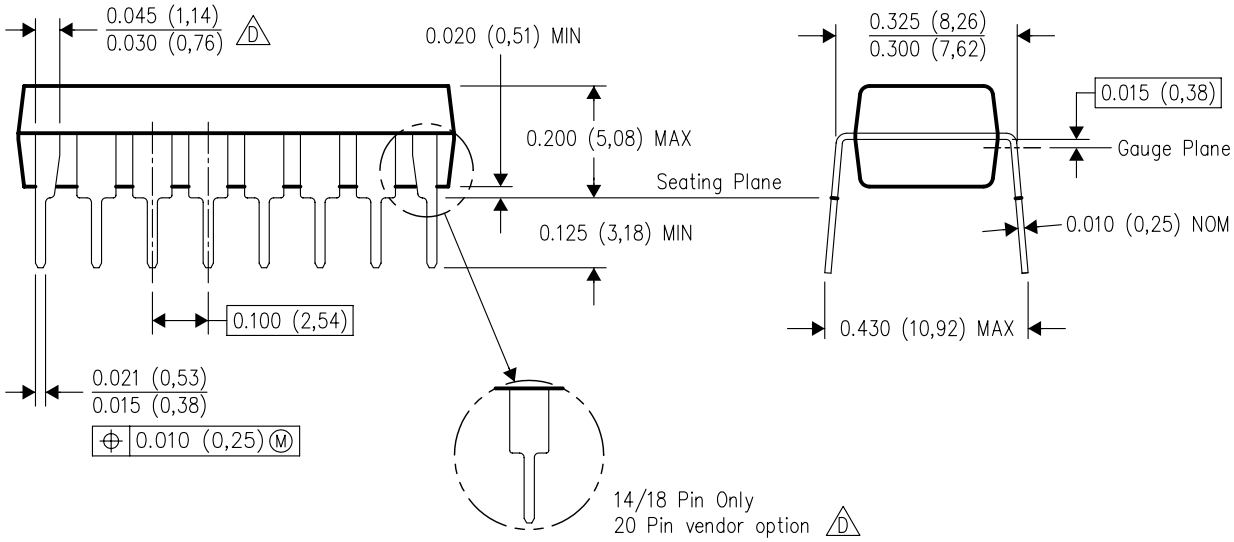
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

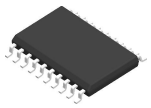


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

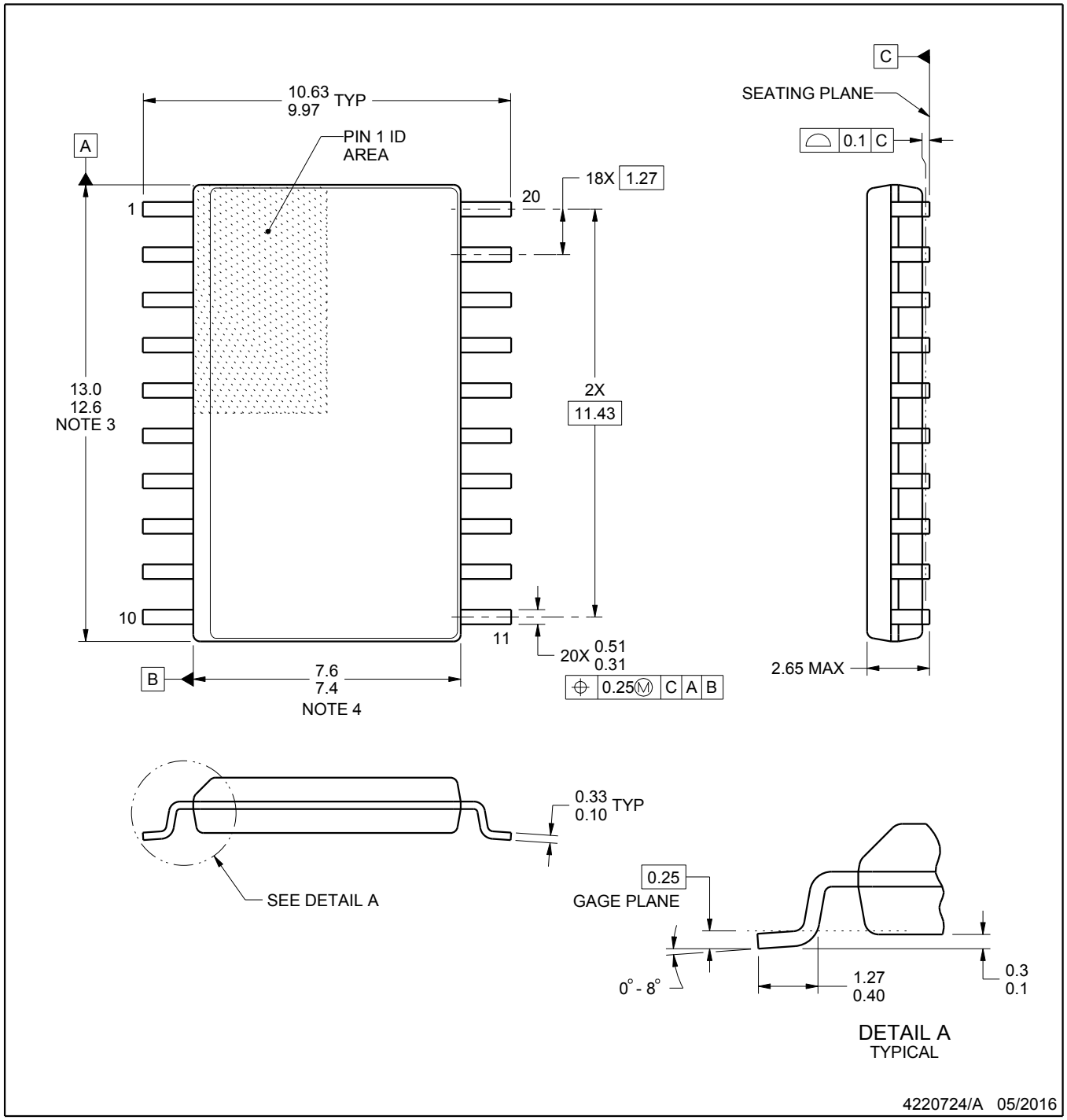


PACKAGE OUTLINE

DW0020A

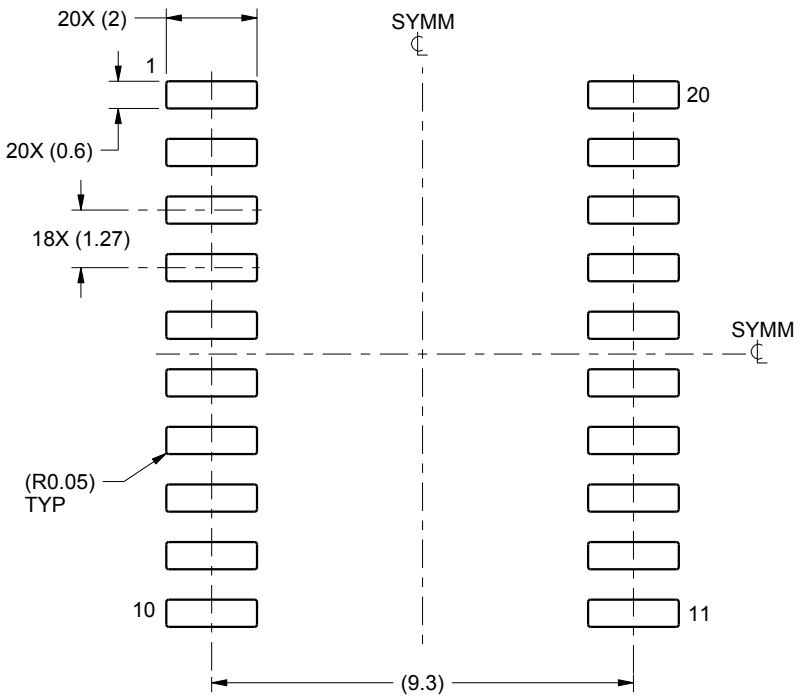
SOIC - 2.65 mm max height

SOIC

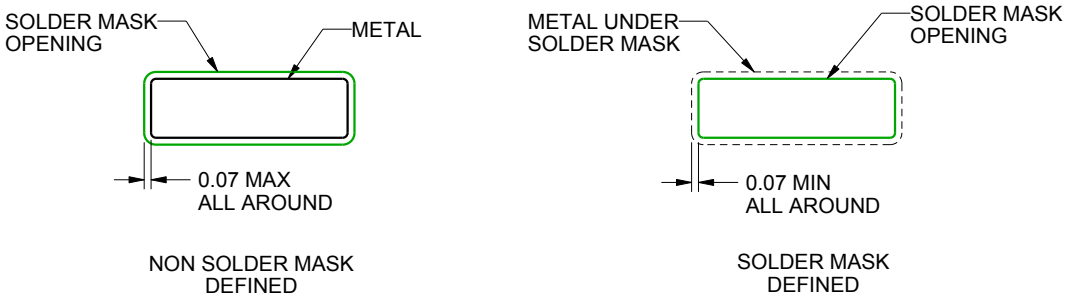


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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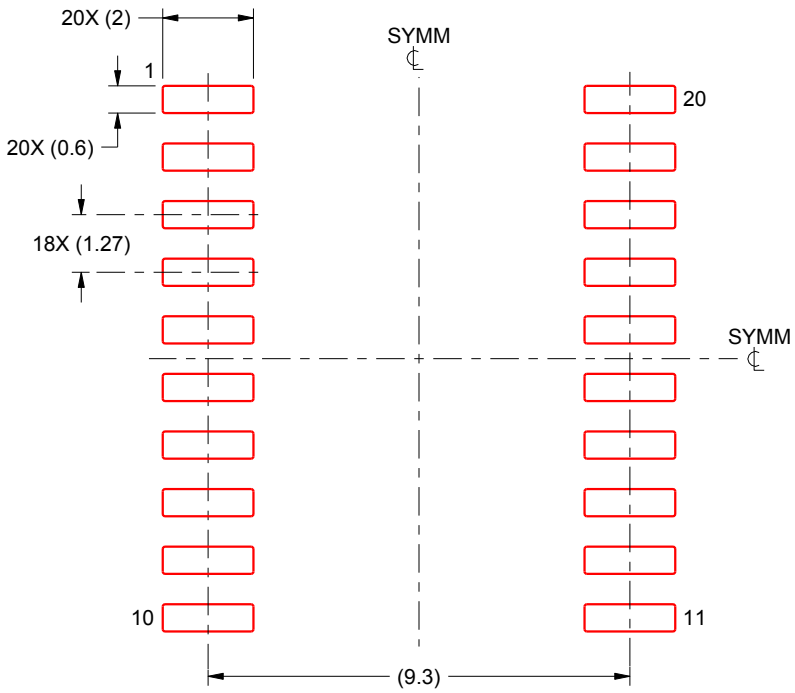
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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