SN74AHC1G86-Q1 Automotive Single 2-Input Exclusive-OR Gate

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - ±4000V Human-Body Model (HBM) ESD Classification Level 3A
  - ±1000V Charged-Device Model (CDM) ESD Classification Level C5
- Operating range of 2V to 5.5V
- Maximum t_{pd} of 10ns at 5V
- Low power consumption, 10μA maximum I_{CC}
- ±8mA output drive at 5V
- Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time

2 Applications

- Wireless headsets
- Motor drives and controls
- TVs
- Set-top boxes
- Audio

3 Description

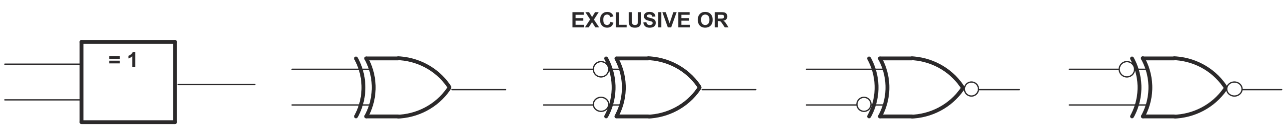
The SN74AHC1G86-Q1 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (3)
SN74AHC1G86-Q1	DBV (SOT-23, 5)	2.90mm × 2.8mm	2.90mm x 1.60mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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4 Pin Configuration and Functions

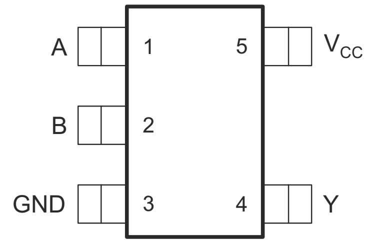


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground
4	Y	O	Output Y
5	V_{CC}	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[(2)]		–0.5	7	V
V_O	Output voltage range applied in the high- or low-state[(2)]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0V)		–20	V
I_{OK}	Output clamp current	(V_O < 0V or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0V to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 3V	2.1		
		V_{CC} = 5.5V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2V		0.5	V
		V_{CC} = 3V		0.9	
		V_{CC} = 5.5V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2V		–50	µA
		V_{CC} = 3.3V ±0.3V		–4	mA
		V_{CC} = 5V ±0.5V		–8	
I_{OL}	Low-level output current	V_{CC} = 2V		50	µA
		V_{CC} = 3.3V ±0.3V		4	mA
		V_{CC} = 5V ±0.5V		8	
Δt/ΔV	Input transition rise or fall rate	V_{CC} = 3.3V ±0.3V		100	ns/V
		V_{CC} = 5V ±0.5V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC1G86-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	115.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	183.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
V_{OH}	I_{OH} = –50µA	2V	1.9	2		1.9		V
		3V	2.9	3		2.9		
		4.5V	4.4	4.5		4.4		
	I_{OH} = –4mA	3V	2.58			2.48		
	I_{OH} = –8mA	4.5V	3.94			3.8		
V_{OL}	I_{OL} = 50µA	2V			0.1		0.1	V
		3V			0.1		0.1	
		4.5V			0.1		0.1	
	I_{OL} = 4mA	3V			0.36		0.44	
	I_{OL} = 8mA	4.5V			0.36		0.44	
I_I	V_I = 5.5V or GND	0V to 5.5V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0 A	5.5V			1		10	µA
C_I	V_I = V_{CC} or GND	5V		4	10		10	pF

5.6 Switching Characteristics, V_{CC} = 3.3V ±0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ±0.3V, T_A = –40°C to 125°C, see Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 50pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	

5.7 Switching Characteristics, V_{CC} = 5V ±0.5 V

over recommended operating free-air temperature range, V_{CC} = 5V ±0.5V, T_A = –40°C to 125°C, see Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 50pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

5.8 Operating Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1MHz	18	pF

5.9 Typical Characteristics

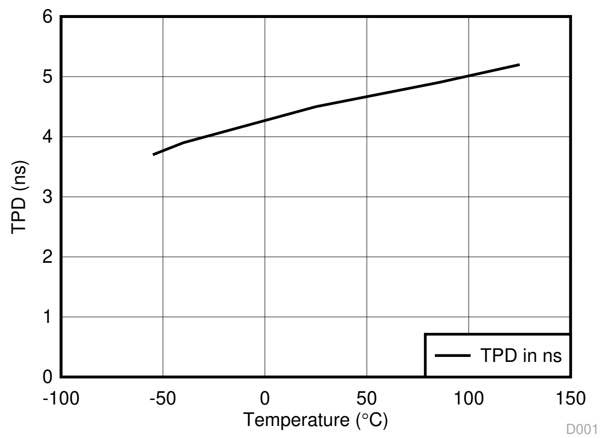


Figure 5-1. TPD vs Temperature

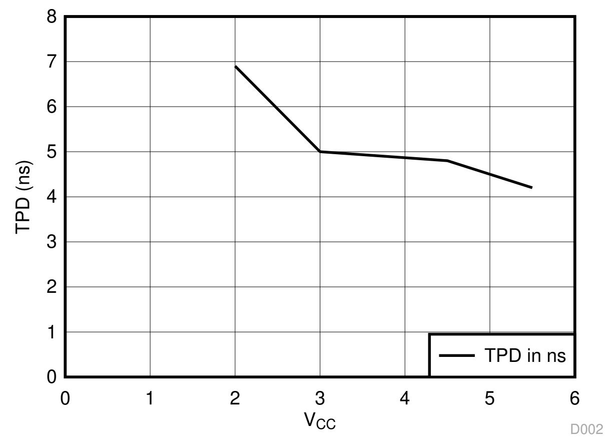
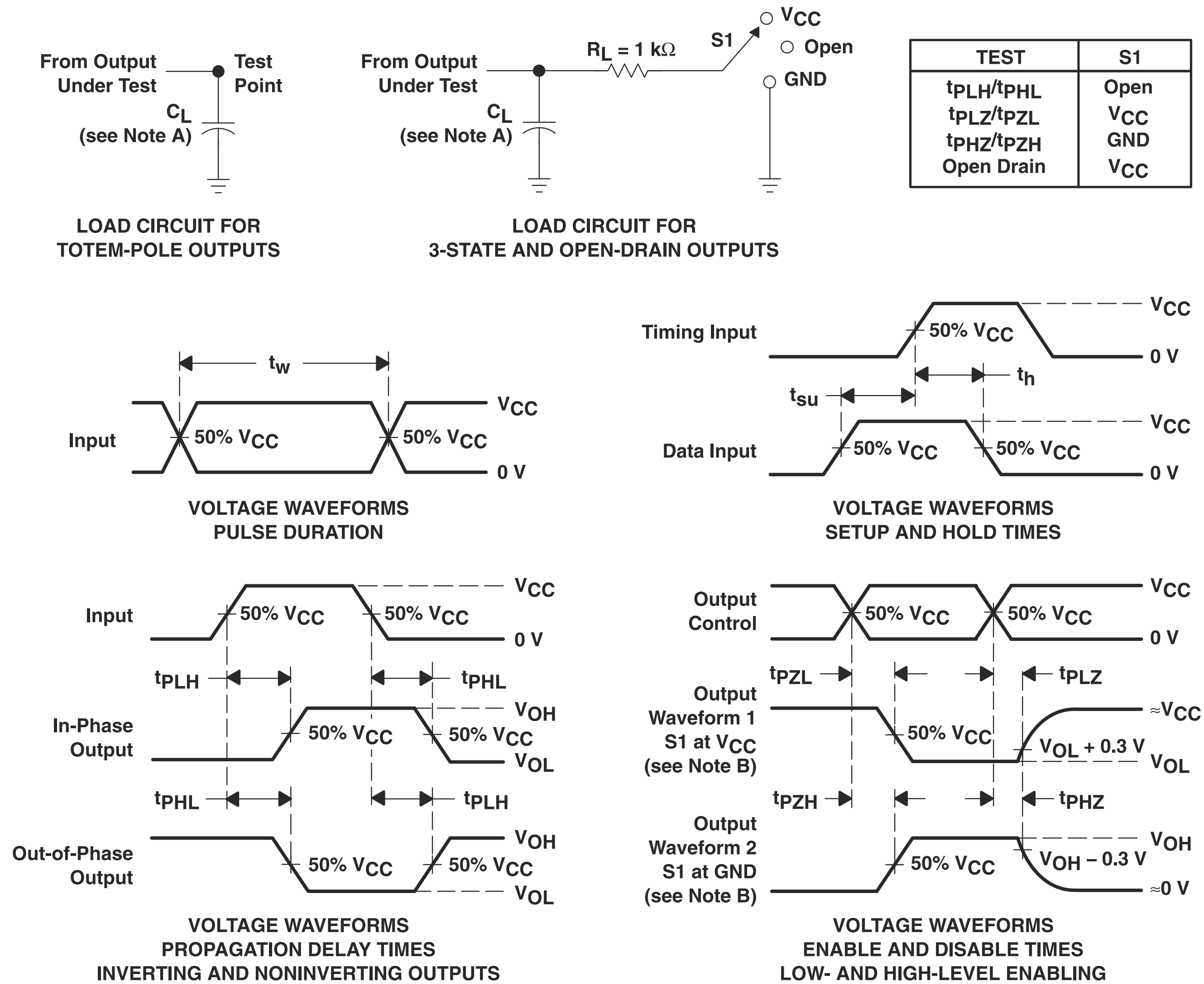


Figure 5-2. TPD vs V_{CC} at 25°C

6 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

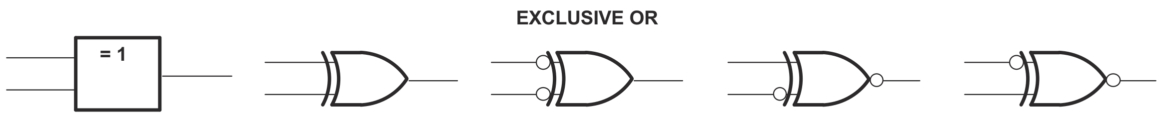
7 Detailed Description

7.1 Overview

The SN74AHC1G86-Q1 is an automotive qualified device that performs the Boolean function $Y = \overline{A}B + A\,\overline{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 2V to 5.5V V_{CC} operation.

A common application is as a true or complementary element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

7.2 Functional Block Diagram



These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86-Q1 gate in positive logic; negation may be shown at any two ports.

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the . The worst case resistance is calculated with the maximum input voltage, given in the , and the maximum input leakage current, given in the , using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamping Diodes

The inputs have negative clamping diodes, and the outputs have positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

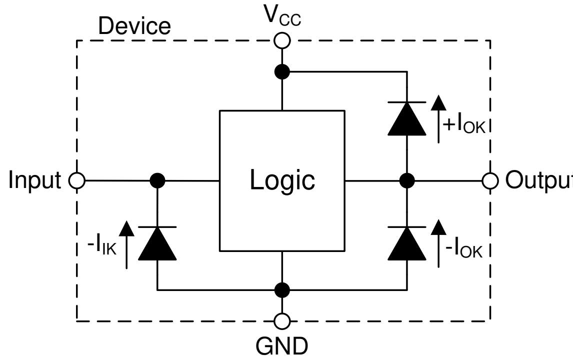


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the .

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AHC1G86-Q1 device.

Table 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC1G86-Q1 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5V at any valid V_{CC} making it ideal for down translation.

8.2 Typical Application

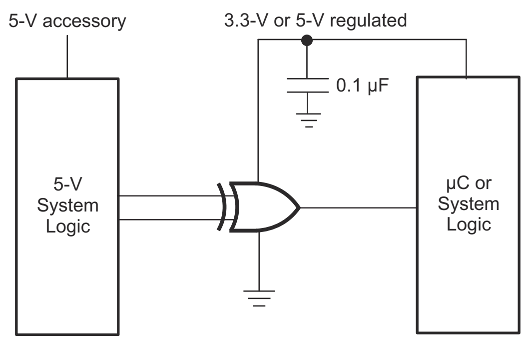


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed 8mA per output.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curve

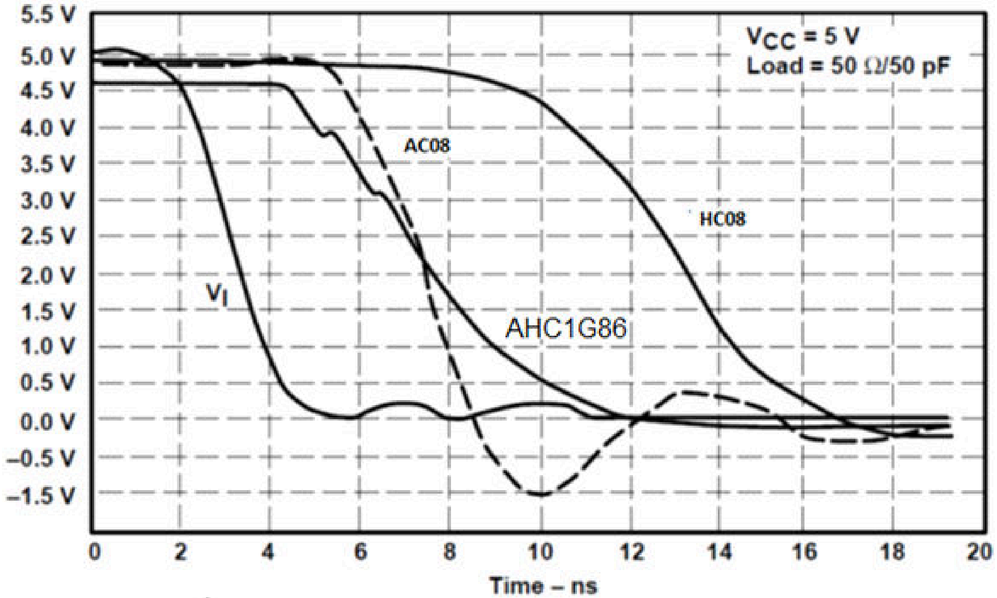


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF is recommended. If there are multiple V_{CC} pins, 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

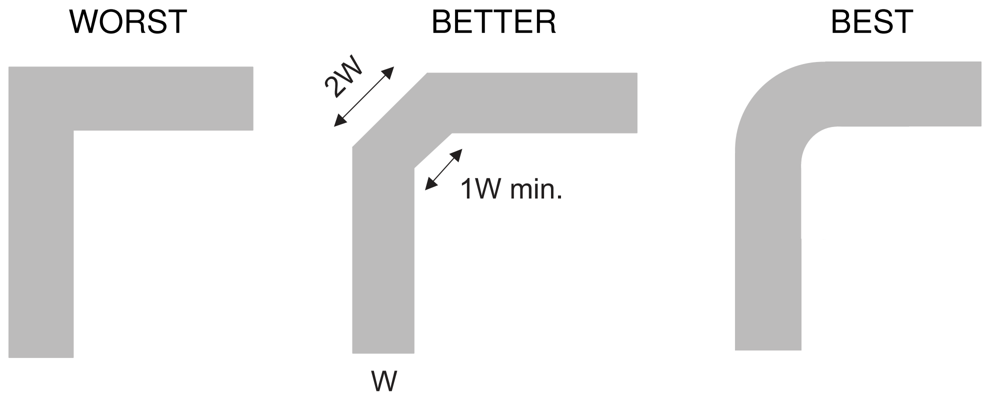


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Community Resources

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2019) to Revision B (February 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Updated thermal values for DBV package from RθJA = 224.1 to 278, RθJC(top) = 152.8 to 180.5, RθJB = 131.8 to 184.4, ΨJT = 65.7 to 115.4, ΨJB = 131.0 to 183.4, RθJC(bot) = N/A, all values in °C/W 5

Changes from Revision * (April 2011) to Revision A (May 2019) **Page**

- Changed Features section 1
- Added Applications section 1
- Changed Description section.......... 1
- Changed Pin Configuration and Functions section.......... 3
- Added T_J spec to Absolute Maximum Ratings table.......... 4
- Changed T_{stg} to -65° (min) and 150°C (max) from -40°C (min) and 125°C (max).......... 4
- Added ESD Ratings table.......... 4
- Added Thermal Information table.......... 5
- Added Typical Characteristics section.......... 6
- Added Application and Implementation section 10
- Added Power Supply Recommendations section 11

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G86QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(39KH, ACYU)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC1G86-Q1 :

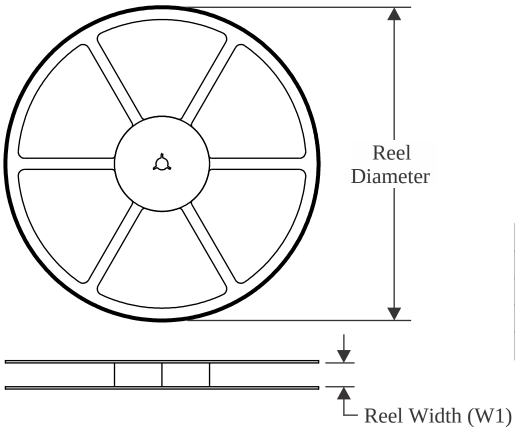
- Catalog : SN74AHC1G86
- Enhanced Product : SN74AHC1G86-EP

NOTE: Qualified Version Definitions:

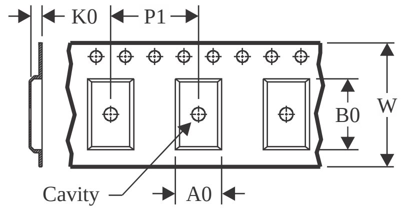
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

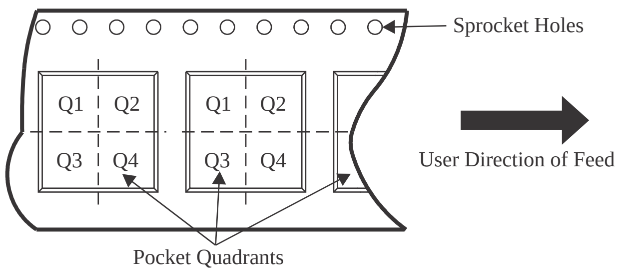


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

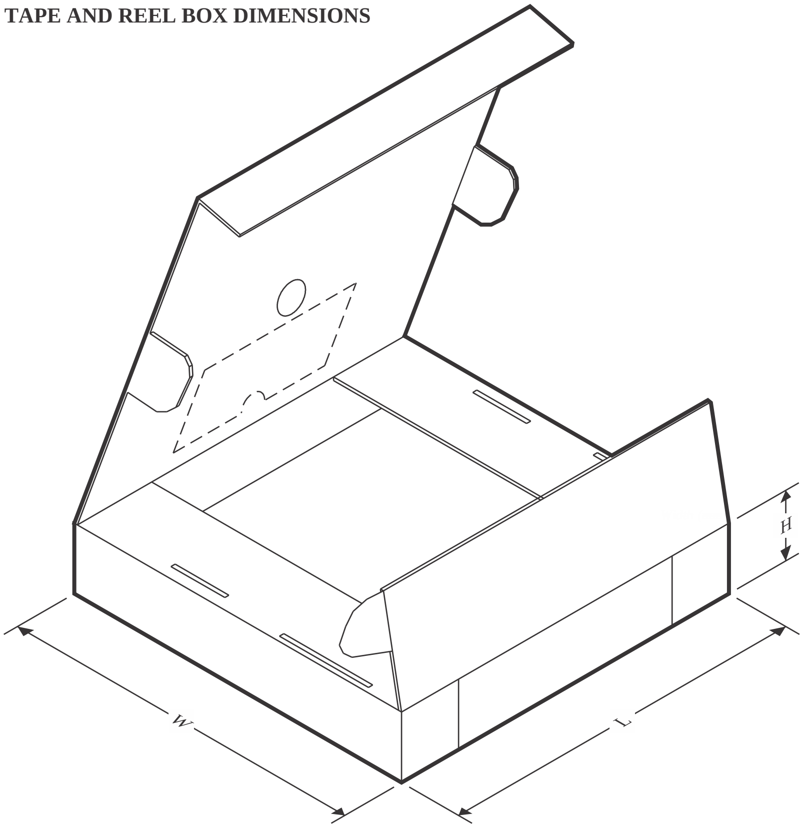
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



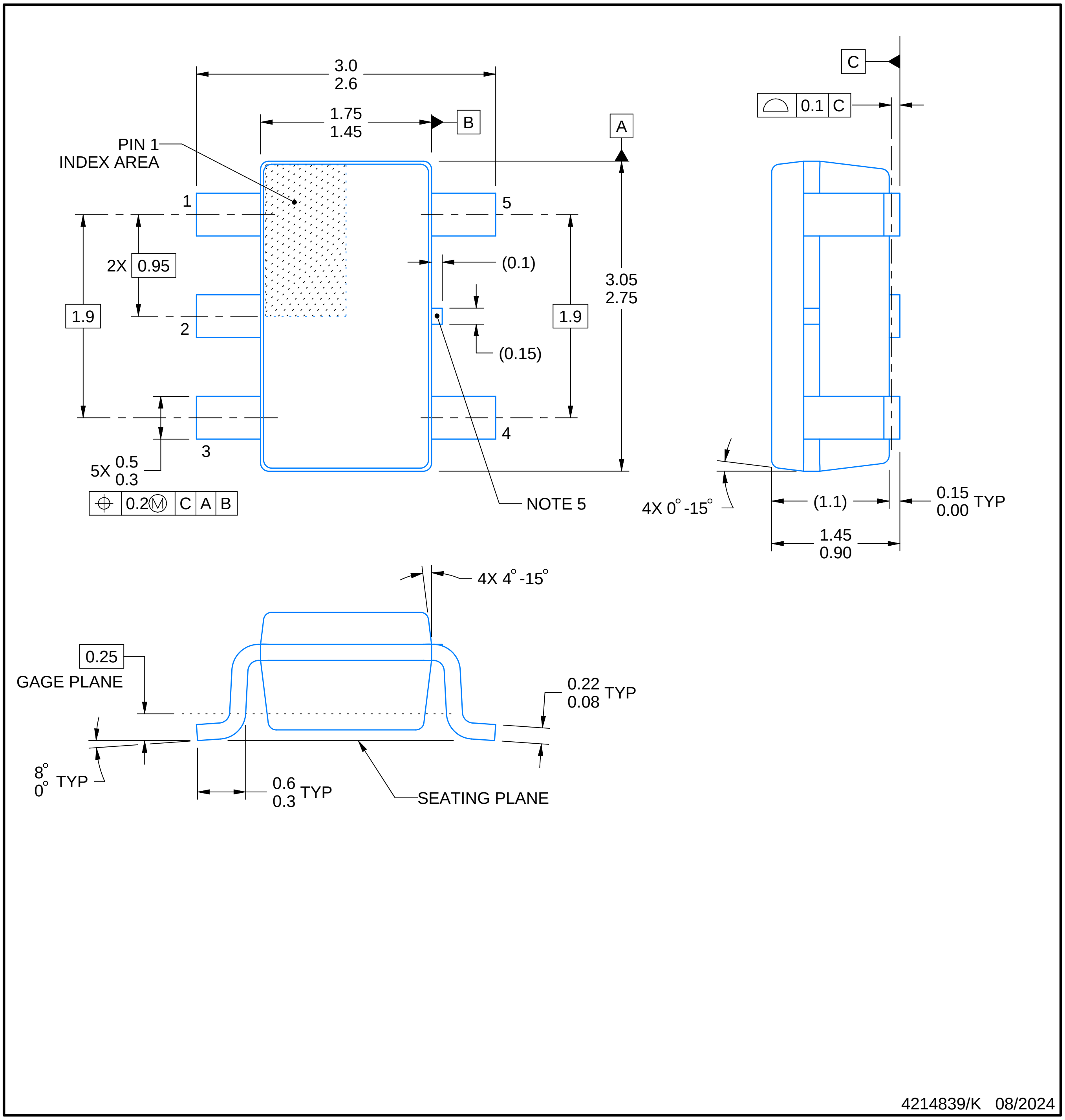
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

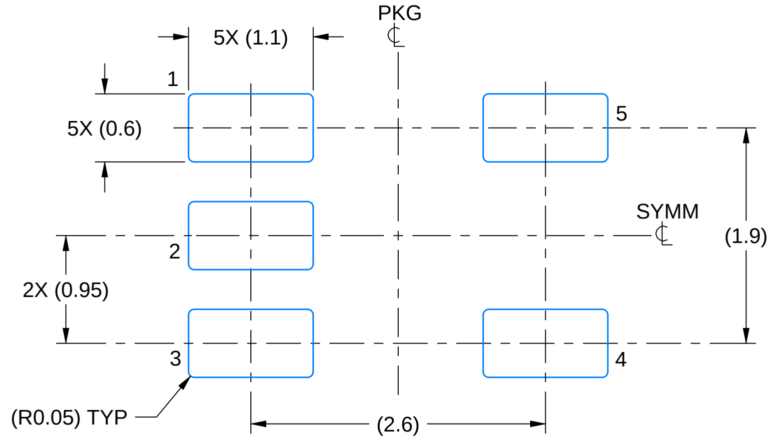
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

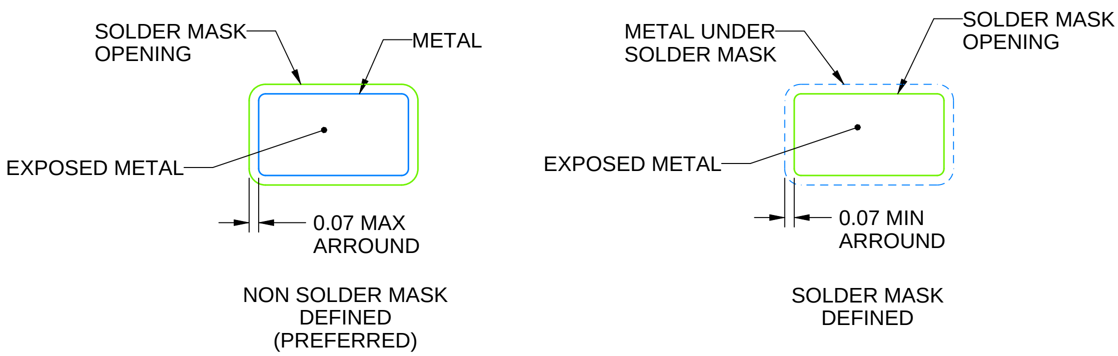


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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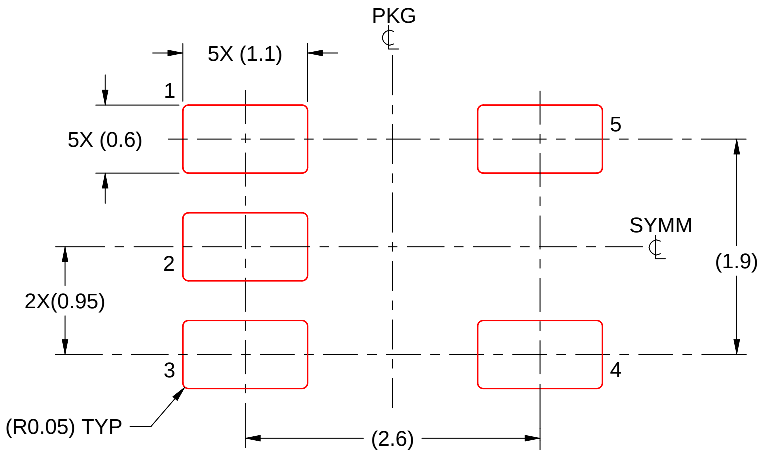
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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