# SN74AHC1G126 Single Bus Buffer Gate With 3-State Output

## 1 Features

- Operating range of 2V to 5.5V
- Max $t_{pd}$ of 6ns at 5V
- Low power consumption, 10µA max $I_{CC}$
- ±8mA output drive at 5V
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- Projectors
- TVs
- Servers
- Motor Controls
- Patient Monitoring
- Electronic Points of Sale

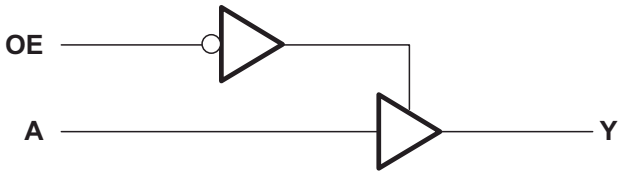
## 3 Description

The SN74AHC1G126 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74AHC1G126 | DBV (SOT-23, 5) | 2.9mm x 2.8mm | 2.9mm x 1.6mm |
| | DCK (SC-70, 5) | 2mm x 2.1mm | 2mm × 1.25mm |
| | DRL (SOT-553, 5) | 1.6mm x 1.6mm | 1.6mm × 1.2mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

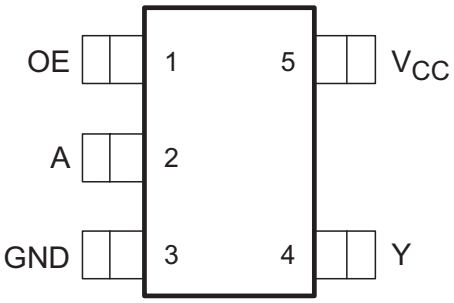



**Simplified Schematic**

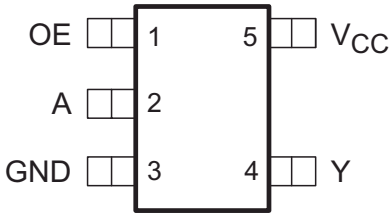
# Table of Contents

## 4 Pin Configuration and Functions

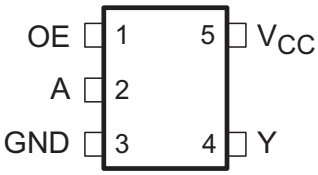
**DBV PACKAGE**
**(TOP VIEW)**




**DCK PACKAGE**
**(TOP VIEW)**




**DRL PACKAGE**
**(TOP VIEW)**




See mechanical drawings for dimensions.

**Table 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | OE | I | Output Enable |
| 2 | A | I | Input A |
| 3 | GND | — | Ground Pin |
| 4 | Y | O | Output Y |
| 5 | $V_{CC}$ | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ (2) | Input voltage range | | –0.5 | 7 | V |
| $V_O$ (2) | Output voltage range | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | –20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous channel current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $T_J$ | Junction Temperature | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC1G126 | | | UNIT |
|---|---|---|---|---|---|
| | | DBV(SOT-23) | DCK(SC-70) | DRL(SOT-553) | |
| | | 5 PINS | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 289.2 | 328.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 180.5 | 205.8 | 105.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 184.4 | 176.2 | 150.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 115.4 | 117.6 | 6.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 183.4 | 175.1 | 148.4 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bot) thermal resistance | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | Off-State (High-Impedance State) Output Current (of a 3-State Output) | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | | 10 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | | 10 | pF |
| $C_o$ | Output capacitance | $V_O$ = $V_{CC}$ or GND | 5 V | | 10 | | | | | | pF |

## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8 | 1 | 9.5 | 1 | 10 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | 1 | 10 | ns |
| $t_{PZL}$ | | | | | 5.4 | 8 | 1 | 9.5 | 1 | 10 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | 1 | 14 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | 1 | 14 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | 1 | 14 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | 1 | 16 | |

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | 1 | 7 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | 1 | 6.5 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | 1 | 6.5 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | 1 | 9.5 | |
| $t_{PZH}$ | OE | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | 1 | 9 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | 1 | 9 | |
| $t_{PHZ}$ | OE | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | 1 | 11 | |

## 5.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## 5.9 Typical Characteristics

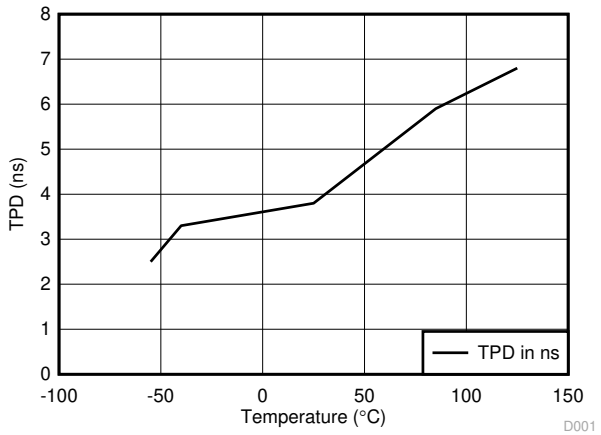



**Figure 5-1. TPD vs Temperature**

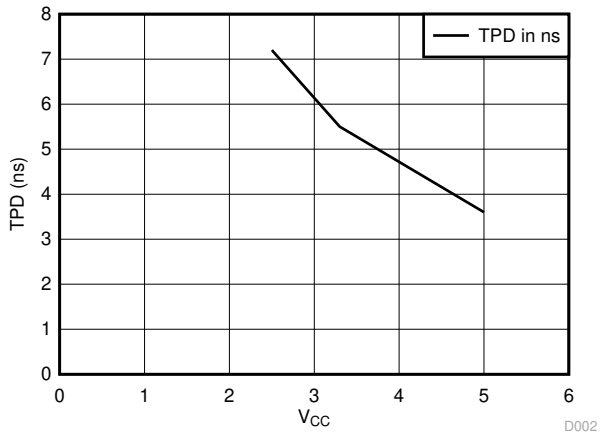
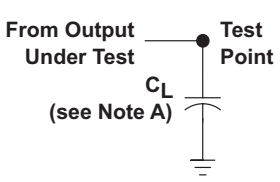
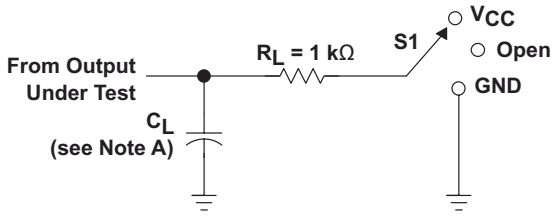



**Figure 5-2. TPD vs $V_{CC}$ at 25°C**

## 6 Parameter Measurement Information

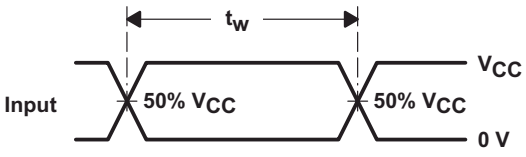



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

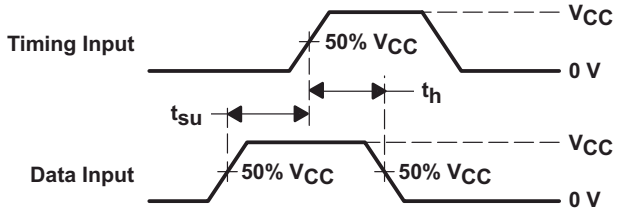



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

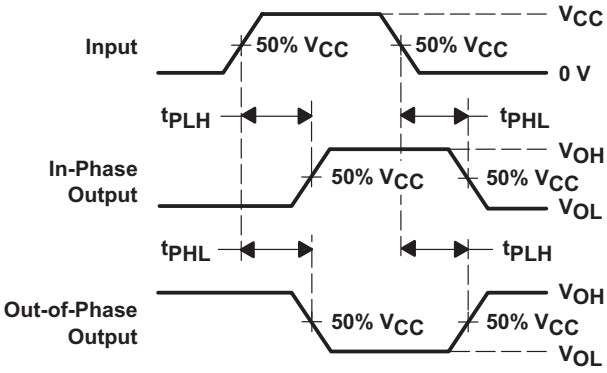
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



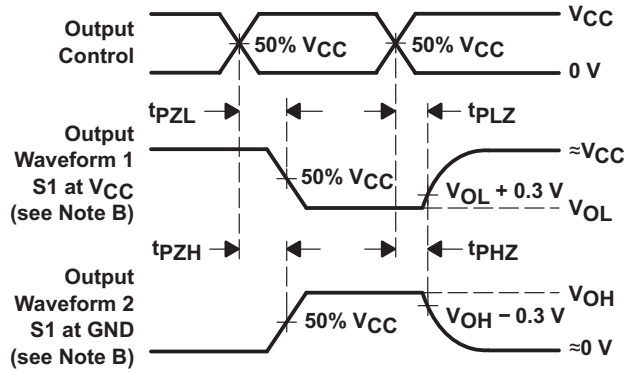

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The SN74AHC1G126 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## 7.2 Functional Block Diagram

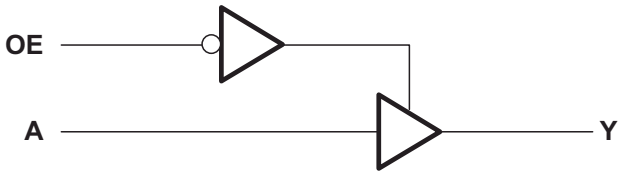



**Figure 7-1. Logic Diagram (Positive Logic)**

## 7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS(1) | | OUTPUT(2) |
|---|---|---|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74AHC1G126 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are 5.5-V tolerant at any valid $V_{CC}$, making it Ideal for translating down to $V_{CC}$.

## 8.2 Typical Application

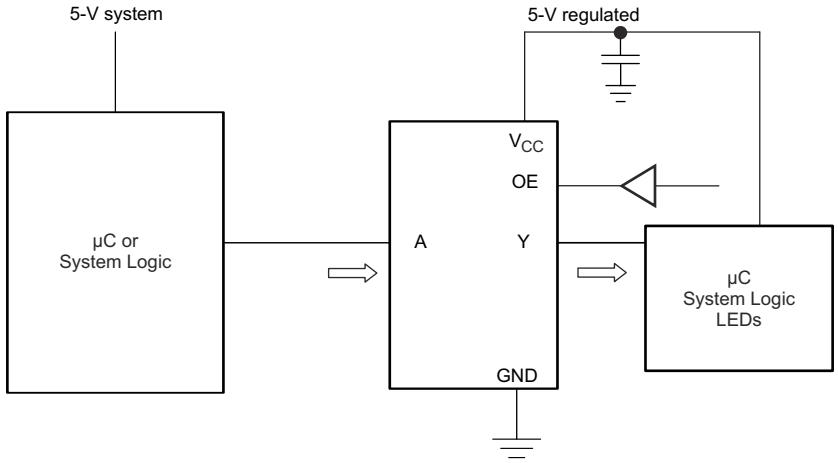



**Figure 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Section 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *Section 5.3* table.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 8.2.3 Application Curves

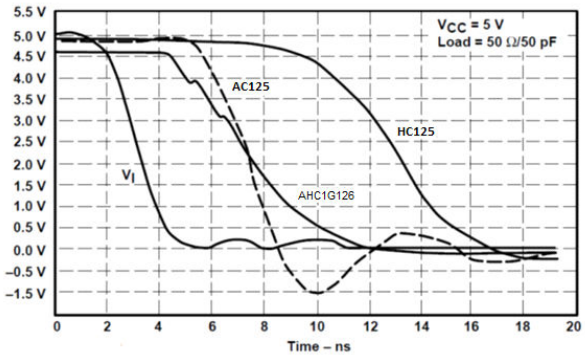



**Figure 8-2. Output Turn-off Waveform**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

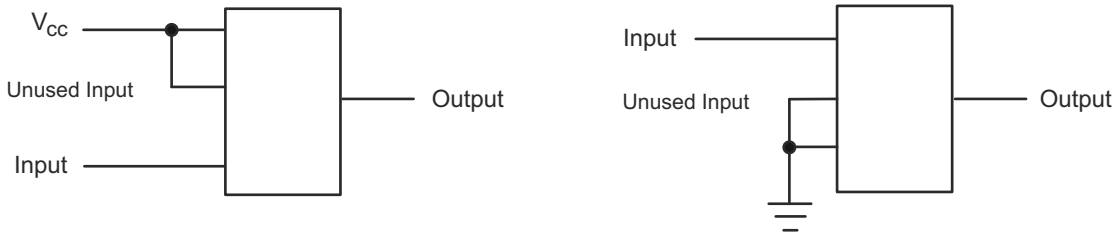



**Figure 8-3. Layout Diagram**

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

| Changes from Revision L (October 2023) to Revision M (February 2024) | Page |
|---|---|
| • Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB = 60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W | 5 |

| Changes from Revision K (December 2014) to Revision L (October 2023) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W | 5 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AHC1G126DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A26G | Samples |
| 74AHC1G126DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AN3 | Samples |
| 74AHC1G126DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AN3 | Samples |
| 74AHC1G126DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AN3 | Samples |
| SN74AHC1G126DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | (39LH, 3BZF, A263, A26G, A26J, A 26S) | Samples |
| SN74AHC1G126DBVT | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI | -40 to 125 | (A263, A26G, A26J, A26S) | |
| SN74AHC1G126DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | (1RE, AN3, ANG, AN J, ANS) | Samples |
| SN74AHC1G126DCKT | OBSOLETE | SC70 | DCK | 5 | | TBD | Call TI | Call TI | -40 to 125 | (AN3, ANG, ANJ, AN S) | |
| SN74AHC1G126DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN74AHC1G126 :**

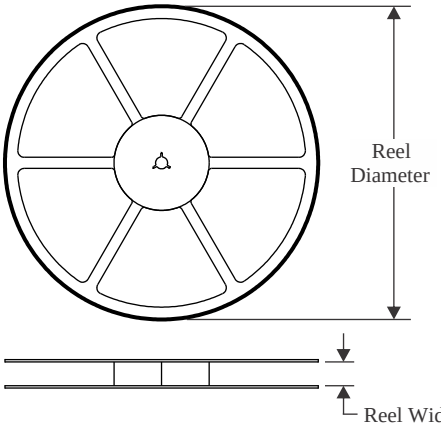
- Automotive : SN74AHC1G126-Q1
- Enhanced Product : SN74AHC1G126-EP

NOTE: Qualified Version Definitions:

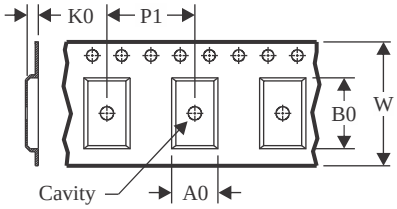
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

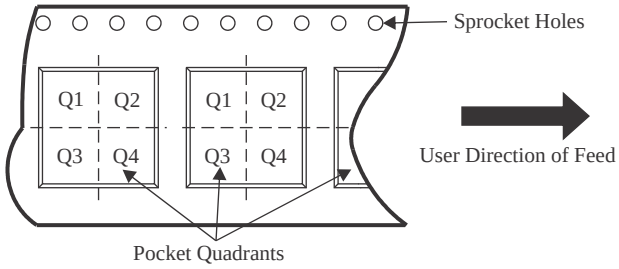



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

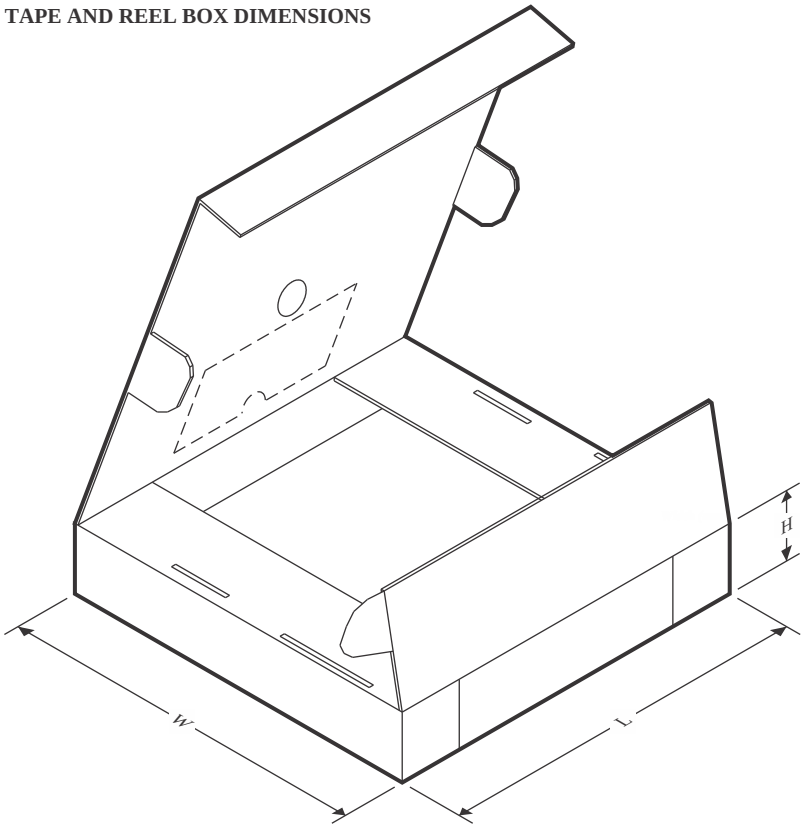
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AHC1G126DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74AHC1G126DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G126DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G126DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G126DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

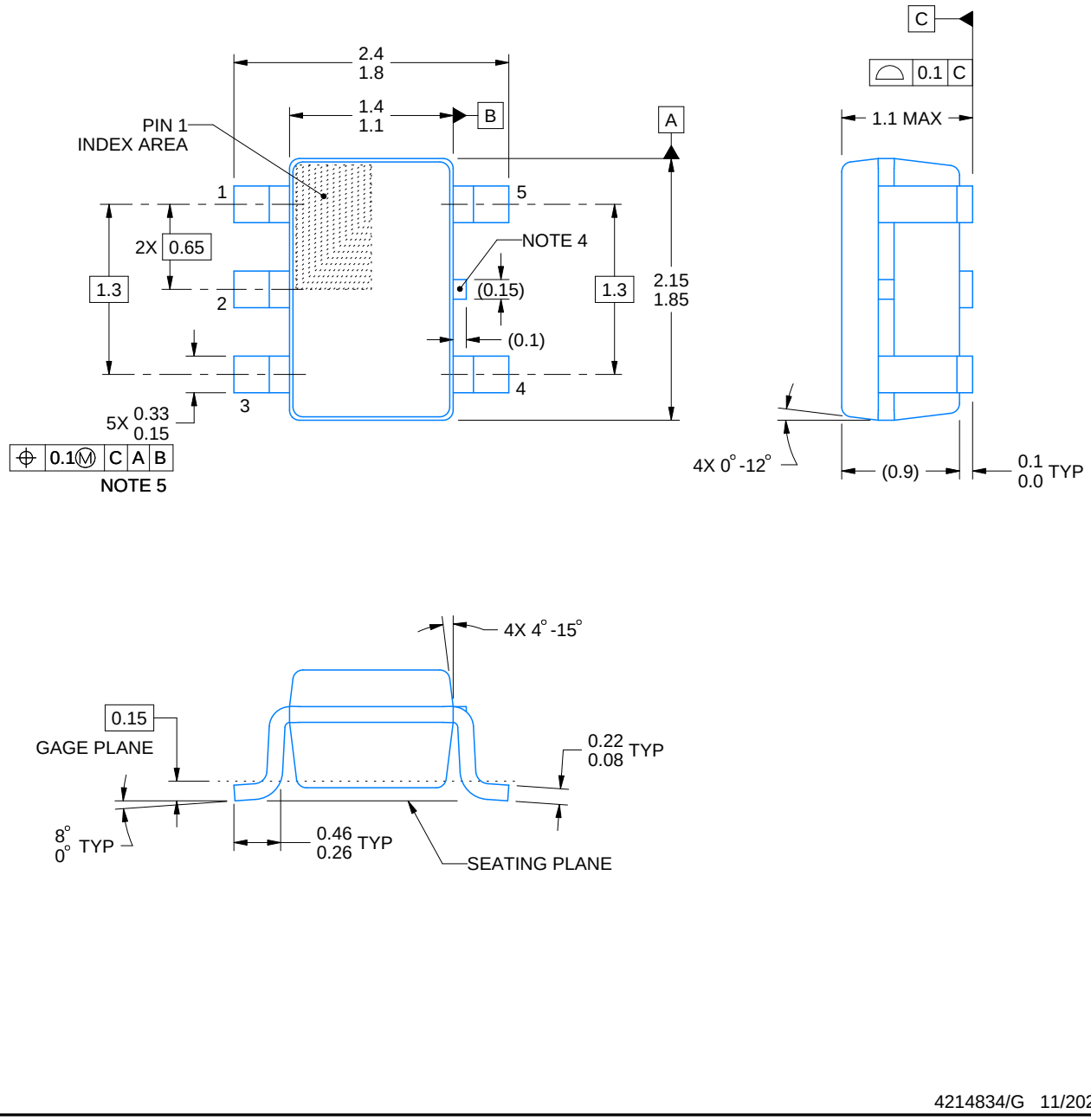
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AHC1G126DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| 74AHC1G126DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G126DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G126DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G126DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

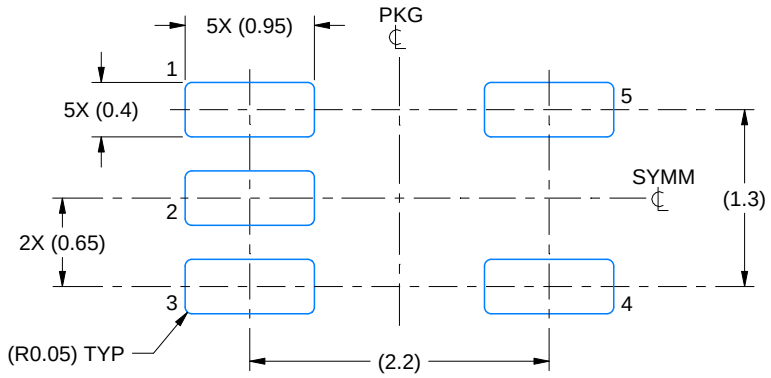
SMALL OUTLINE TRANSISTOR



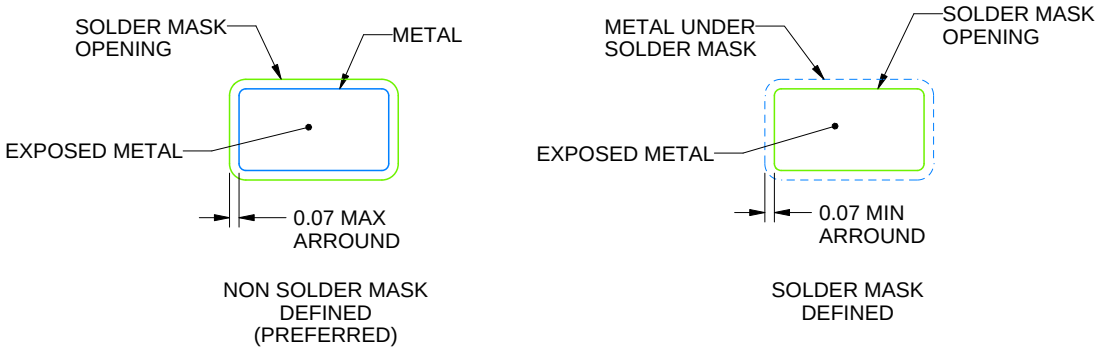

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

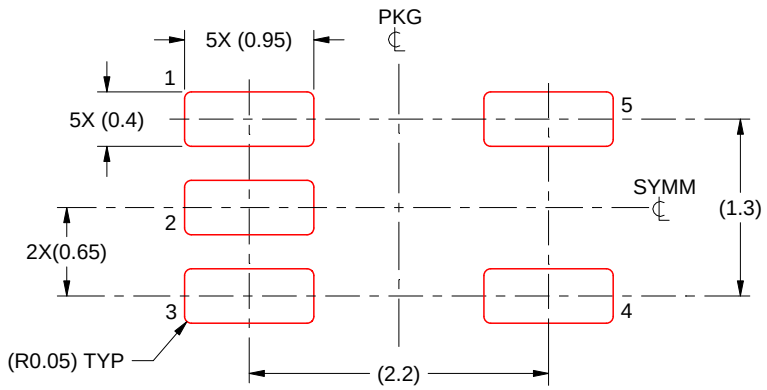



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

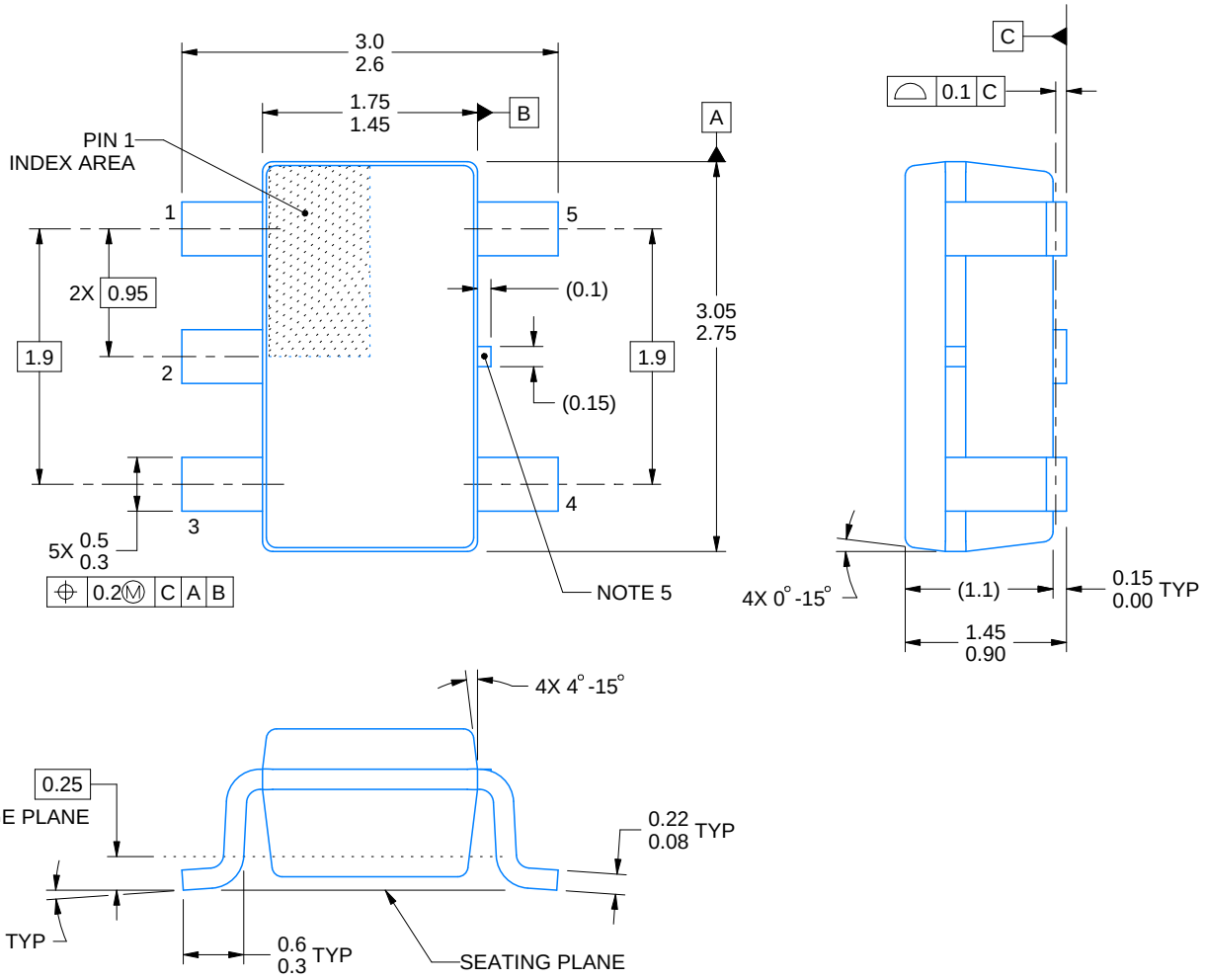
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

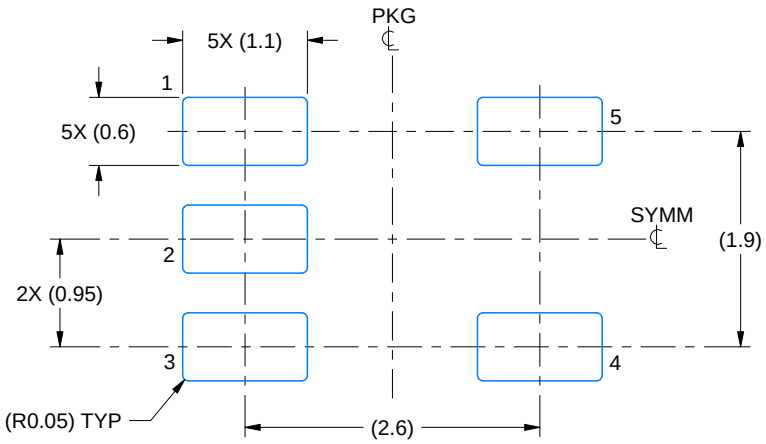
SMALL OUTLINE TRANSISTOR



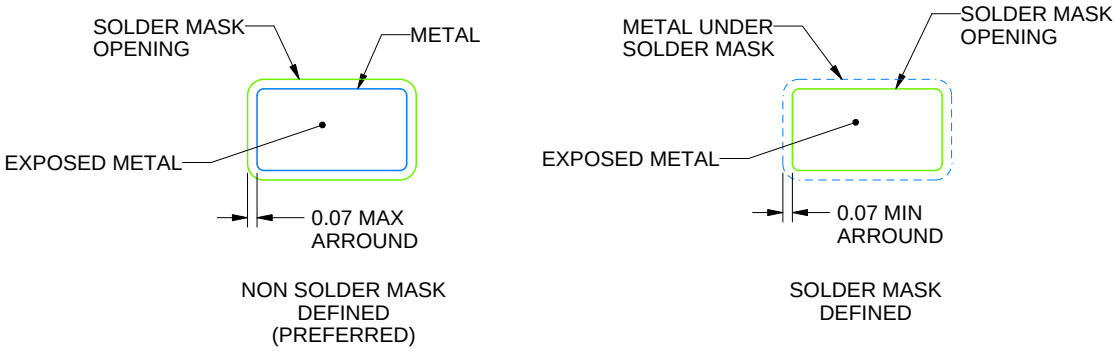

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

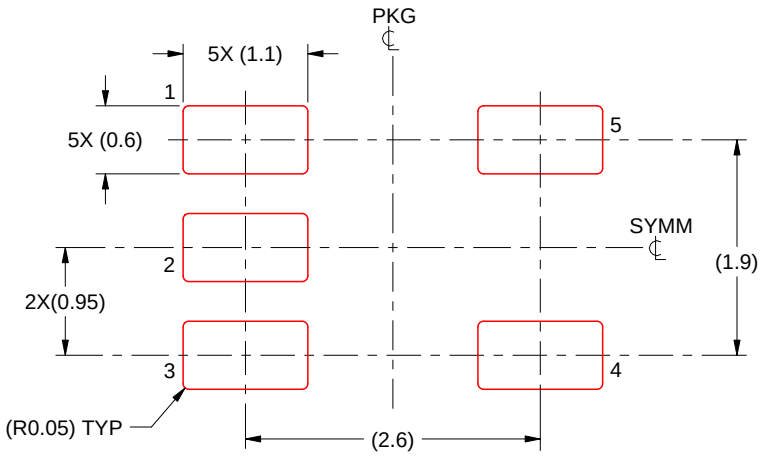



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

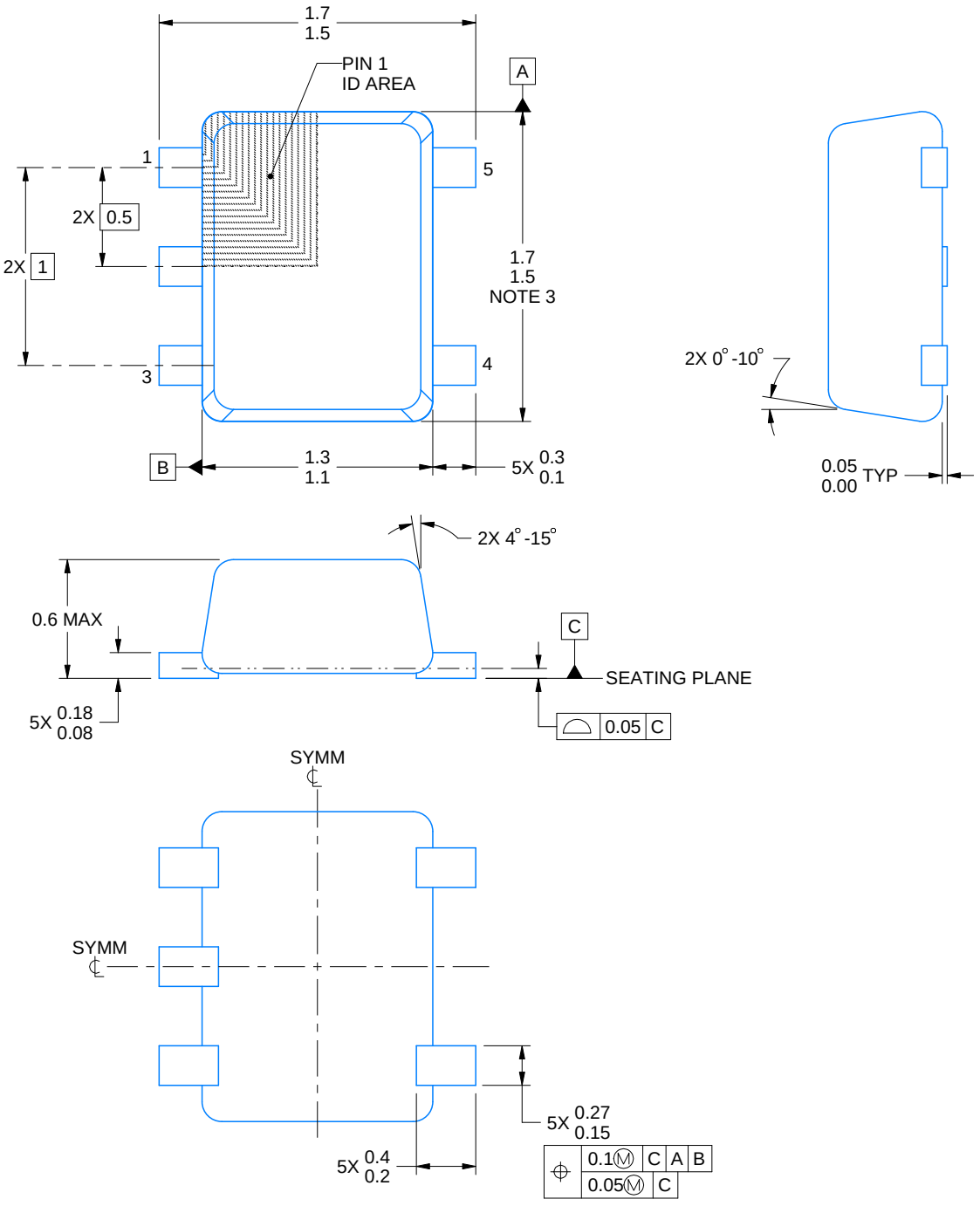
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DRL0005A

## SOT - 0.6 mm max height

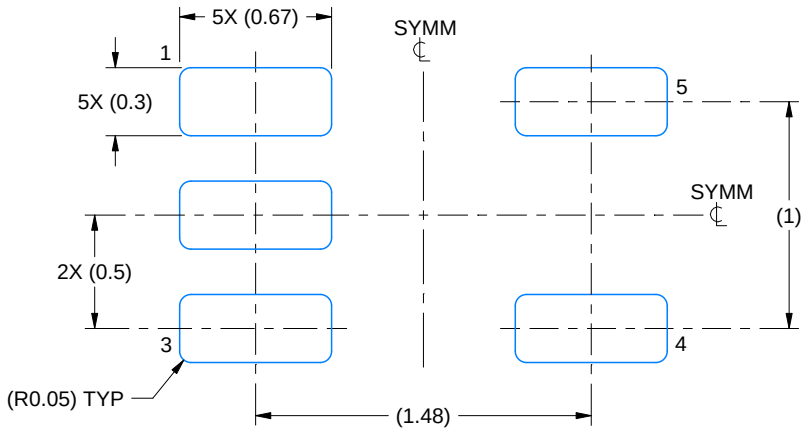
PLASTIC SMALL OUTLINE



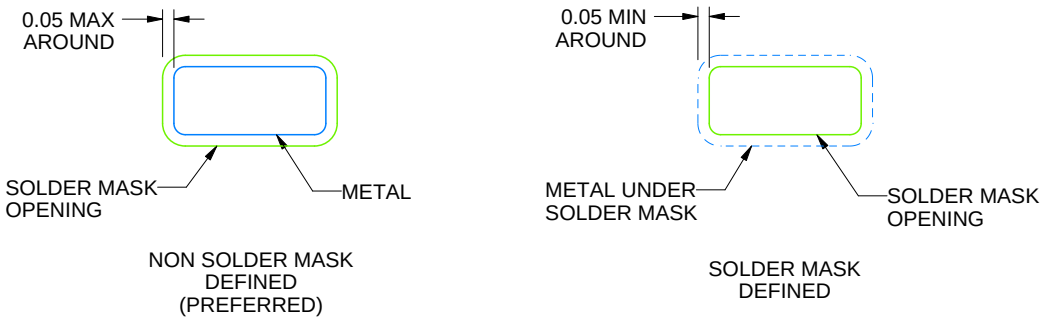

4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

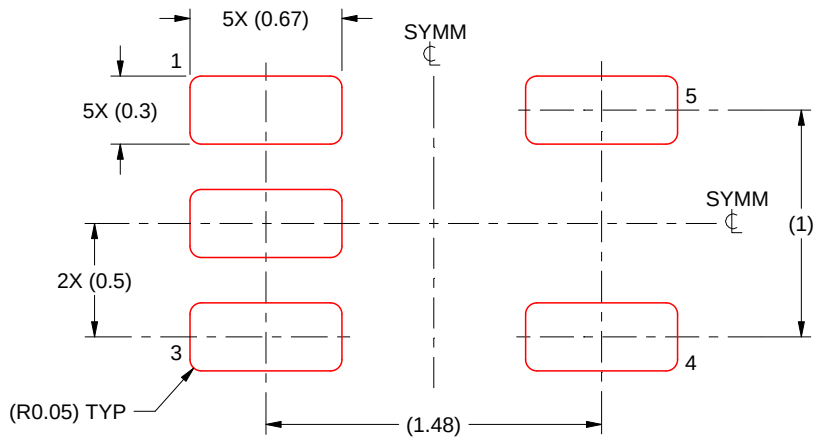



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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