TEXAS INSTRUMENTS
SN65MLVD200A, SN65MLVD202A
SN65MLVD204A, SN65MLVD205A
SLLS573E – DECEMBER 2003 – REVISED MARCH 2024

SN65MLVD20xx Multipoint-LVDS Line Driver and Receiver

1 Features

- Low-Voltage Differential 30Ω to 55Ω Line Drivers and Receivers for Signaling Rates [1] up to 100Mbps, Clock Frequencies up to 50MHz
- Type-1 Receivers Incorporate 25mV of Hysteresis (SN65MLVD200A, SN65MLVD202A)
- Type-2 Receivers Provide an Offset (100mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions (SN65MLVD204A, SN65MLVD205A)
- Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- –1V to 3.4V of Common-Mode Voltage Range Allows Data Transfer With 2V of Ground Noise
- Bus Pins High Impedance When Disabled or V_{CC} ≤ 1.5V
- 200Mbps Devices Available (SN65MLVD201, SN65MLVD203, SN65MLVD206, SN65MLVD207)
- Bus Pin ESD Protection Exceeds 8kV
- Packages Available:
  - 8-Pin SOIC SN65MLVD200A, SN65MLVD204A
  - 14-Pin SOIC SN65MLVD202A, SN65MLVD205A
- Improved Alternatives to the SN65MLVD200, SN65MLVD202A, SN65MLVD204A, and SN65MLVD205A Devices

2 Applications

- Low-Power, High-Speed, Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central Office Switches
- Network Switches and Routers

3 Description

The SN65MLVD20xx devices are multipoint low-voltage differential (M-LVDS) line drivers and receivers that are optimized to operate at signaling rates up to 100 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899.

The SN65MLVD20xx devices have enhancements over their predecessors. Improved features include controlled slew rate on the driver output to help minimize reflections from unterminated stubs, which results in better signal integrity. Additionally, 8-kV ESD protection on the bus pins for more robustness. The same footprint definition was maintained making for an easy drop-in replacement for a system performance upgrade.

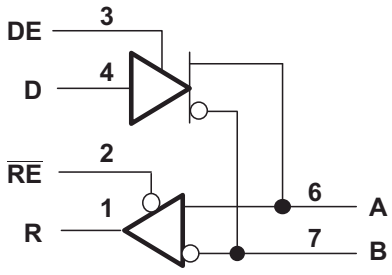
The devices are characterized for operation from –40°C to 85°C.

Device Information

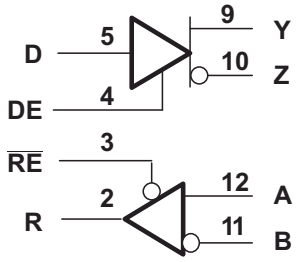
PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65MLVD200A SN65MLVD204A	SOIC (8)	4.90 mm × 3.91 mm
SN65MLVD202A SN65MLVD205A	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN65MLVD200A, SN65MLVD204A



SN65MLVD202A, SN65MLVD205A



Logic Diagrams (Positive Logic)

[1] The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

Table of Contents

4 Device Comparison Table

PART NUMBER	FOOTPRINT	RECEIVER TYPE
SN65MLVD200AD	SN75176	Type 1
SM65MLVD202AD	SN75ALS180	Type 1
SN65MLVD204AD	SN75176	Type 2
SM65MLVD205AD	SN75ALS180	Type 2

5 Pin Configuration and Functions

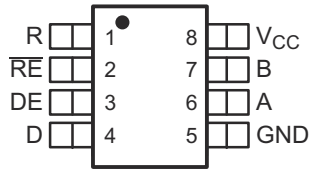


Figure 5-1. D Package 8-Pin SOIC Top View

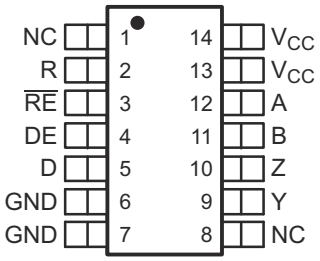


Figure 5-2. D Package 14-Pin SOIC Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC-8	SOIC-14		
A	6	12	I/O	Differential I/O
B	7	11	I/O	Differential I/O
D	4	5	I	Driver input
DE	3	4	I	Driver enable pin: High = Enable, Low = Disable
GND	5	6, 7	Power	Supply ground
NC	—	1, 8	NC	No internal connection
R	1	2	O	Receiver output
$\overline{RE}$	2	3	I	Receiver enable pin: High = Disable, Low = Enable
V_{CC}	8	13, 14	Power	Power supply, 3.3 V
Y	—	9	I/O	Differential I/O
Z	—	10	I/O	Differential I/O

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage(2), V_{CC}		–0.5	4	V
Input voltage	D, DE, $\overline{RE}$	–0.5	4	V
	A, B (SN65MLVD200A and SN65MLVD204A)	–1.8	4	V
	A, B (SN65MLVD202A, SN65MLVD205A)	–4	6	V
Output voltage range	R	–0.3	4	V
	Y, Z, A, or B	–1.8	4	V
Continuous power dissipation		See *Section 6.4*		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	All pins except A, B, Y, and Z	±4000	V
			A, B, Y, and Z	±8000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal V_A V_B V_Y or V_Z	–1.4		3.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage			V_{CC}	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			100	Mbps
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN65MLVD200A, SN65MLVD204A	SN65MLVD202A, SN65MLVD205A	UNIT
		D (SOIC)	D (SOIC)	
		8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.9	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.6	39	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.5	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.1	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.9	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current	Driver only	$\overline{RE}$ and DE at V_{CC}, R_L = 50 Ω, All others open		13	22	mA
		Both disabled	$\overline{RE}$ at V_{CC}, DE at 0 V, R_L = No Load, All others open		1	4	
		Both enabled	$\overline{RE}$ at 0 V, DE at V_{CC}, R_L = 50 Ω, All others open		16	24	
		Receiver only	$\overline{RE}$ at 0 V, DE at 0 V, All others open		4	13	
P_D	Device power dissipation		R_L = 50 Ω, Input to D is a 50-MHz 50% duty cycle square wave, DE = high, $\overline{RE}$ = low, T_A = 85°C			94	mW

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

6.6 Electrical Characteristics – Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX	UNIT
$\lvert V_{AB}\rvert$ or $\lvert V_{YZ}\rvert$	Differential output voltage magnitude	See Figure 7-2	480		650	mV
$\Delta\lvert V_{AB}\rvert$ or $\Delta\lvert V_{YZ}\rvert$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 7-3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$ or $V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7-7	0		2.4	V
$V_{Z(OC)}$ or $V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 7-5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		–0.2 V_{SS}			V
I_{IH}	High-level input current (D, DE)	V_{IH} = 2 V to V_{CC}	0		10	µA
I_{IL}	Low-level input current (D, DE)	V_{IL} = GND to 0.8 V	0		10	µA
$\lvert I_{OS}\rvert$	Differential short-circuit output current magnitude	See Figure 6-4			24	mA
I_{OZ}	High-impedance state output current (driver only)	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V	–15		10	µA
$I_{O(OFF)}$	Power-off output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V, 0 V ≤ V_{CC}≤ 1.5 V	–10		10	µA

6.6 Electrical Characteristics – Driver (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
C_Y or C_Z	Output capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V,(3) Other input at 1.2 V, driver disabled		3		pF
C_{YZ}	Differential output capacitance	V_{AB} = 0.4 sin(30E6πt) V, (3) Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, (C_Y/C_Z)		0.99		1.01	

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

6.7 Electrical Characteristics – Receiver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	Type 1	See Figure 6-9, Table 7-1, and Table 7-2			50	mV
		Type 2				150	
V_{IT-}	Negative-going differential input voltage threshold	Type 1		–50			mV
		Type 2		50			
V_{HYS}	Differential input voltage hysteresis, (V_{IT+} – $V_{IT–}$)	Type 1			25		mV
		Type 2			0		
V_{OH}	High-level output voltage (R)		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage (R)		I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current ($\overline{RE}$)		V_{IH} = 2 V to V_{CC}	–10		0	µA
I_{IL}	Low-level input current ($\overline{RE}$)		V_{IL} = GND to 0.8 V	–10		0	µA
I_{OZ}	High-impedance output current (R)		V_O = 0 V or 3.6 V	–10		15	µA
C_A or C_B	Input capacitance		V_I = 0.4 sin(30E6πt) + 0.5 V(2), Other input at 1.2 V		3		pF
C_{AB}	Differential input capacitance		V_{AB} = 0.4 sin(30E6πt) V(2)			2.5	pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)			0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

6.8 Electrical Characteristics – BUS Input and Output

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_A	Receiver or transceiver with driver disabled input current	V_A = 3.8 V,	V_B = 1.2 V,		0		32	µA
		V_A = 0 V or 2.4 V,	V_B = 1.2 V		–20		20	
		V_A = –1.4 V,	V_B = 1.2 V		–32		0	
I_B	Receiver or transceiver with driver disabled input current	V_B = 3.8 V,	V_A = 1.2 V		0		32	µA
		V_B = 0 V or 2.4 V,	V_A = 1.2 V		–20		20	
		V_B = –1.4 V,	V_A = 1.2 V		–32		0	
I_{AB}	Receiver or transceiver with driver disabled differential input current (I_A – I_B)	V_A = V_B,	1.4 ≤ V_A ≤ 3.8 V		–4		4	µA
$I_{A(OFF)}$	Receiver or transceiver power-off input current	V_A = 3.8 V,	V_B = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	0		32	µA
		V_A = 0 V or 2.4 V,	V_B = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	–20		20	
		V_A = –1.4 V,	V_B = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	–32		0	
$I_{B(OFF)}$	Receiver or transceiver power-off input current	V_B = 3.8 V,	V_A = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	0		32	µA
		V_B = 0 V or 2.4 V,	V_A = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	–20		20	
		V_B = –1.4 V,	V_A = 1.2 V,	0 V ≤ V_{CC} ≤ 1.5 V	–32		0	

6.8 Electrical Characteristics – BUS Input and Output (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current ($I_A - I_B$)	$V_A = V_B$, 0 V ≤ V_{CC} ≤ 1.5 V, –1.4 ≤ V_A ≤ 3.8 V	–4		4	µA
C_A	Transceiver with driver disabled input capacitance	V_A = 0.4 sin (30E6πt) + 0.5 V(2), V_B = 1.2 V		5		pF
C_B	Transceiver with driver disabled input capacitance	V_B = 0.4 sin (30E6πt) + 0.5 V(2), V_A = 1.2 V		5		pF
C_{AB}	Transceiver with driver disabled differential input capacitance	V_{AB} = 0.4 sin (30E6πt)V(2)			3	pF
$C_{A/B}$	Transceiver with driver disabled input capacitance balance, (C_A/C_B)		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

6.9 Switching Characteristics – Driver

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	See Figure 7-5	2	2.5	3.5	ns
t_{pHL}	Propagation delay time, high-to-low-level output		2	2.5	3.5	ns
t_r	Differential output signal rise time		2	2.6	3.2	ns
t_f	Differential output signal fall time		2	2.6	3.2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			30	150	ps
$t_{sk(pp)}$	Part-to-part skew (2)				0.9	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(3)	50-MHz clock input(4)		2	3	ps
$t_{jit(pp)}$	Peak-to-peak jitter(3) (6)	100 Mbps 2^{15} –1 PRBS input(5)		55	150	ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 7-6		4	7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			4	7	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			4	7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			4	7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) Part-to-part skew is defined as the difference in propagation delays between two devices that operate at the same V/T conditions.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) t_r = t_f = 0.5 ns (10% to 90%), measured over 30K samples.
(5) t_r = t_f = 0.5 ns (10% to 90%), measured over 100K samples.
(6) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

6.10 Switching Characteristics – Receiver

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 15 pF, See Figure 7-10	2	3.6	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2	3.6	6	ns
t_r	Output signal rise time			1		2.3	ns
t_f	Output signal fall time			1		2.3	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)	Type 1			100	300	ps
		Type 2			300	500	ps
$t_{sk(pp)}$	Part-to-part skew(2)					1	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(3)		50-MHz clock input(4)		4	7	ps
$t_{jit(pp)}$	Peak-to-peak jitter(3) (6)	Type 1	100 Mbps 2^{15} –1 PRBS input(5)		200	700	ps
		Type 2			225	800	ps

6.10 Switching Characteristics – Receiver (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 7-11		6	10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			6	10	ns
t_{PZH}	Enable time, high-impedance-to-high-level output			10	15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output			10	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) Part-to-part skew is defined as the difference in propagation delays between two devices that operate at the same V/T conditions.
(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(4) V_{ID} = 200 mV_{pp} (MLVD200A, 202A), V_{ID} = 400 mV_{pp} (MLVD204A, 205A), V_{cm} = 1 V, t_r = t_f = 0.5 ns (10% to 90%), measured over 30K samples.
(5) V_{ID} = 200 mV_{pp} (MLVD200A, 202A), V_{ID} = 400 mV_{pp} (MLVD204A, 205A), V_{cm} = 1 V, t_r = t_f = 0.5 ns (10% to 90%), measured over 100K samples.
(6) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$)

6.11 Typical Characteristics

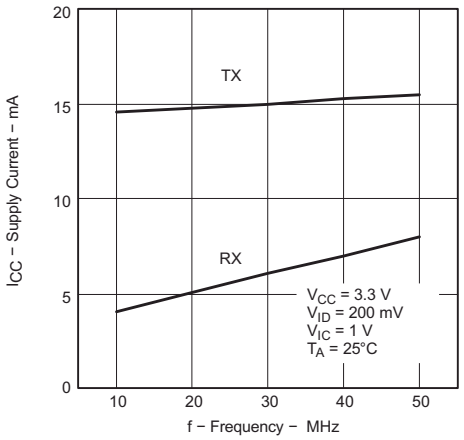


Figure 6-1. Supply Current vs Frequency

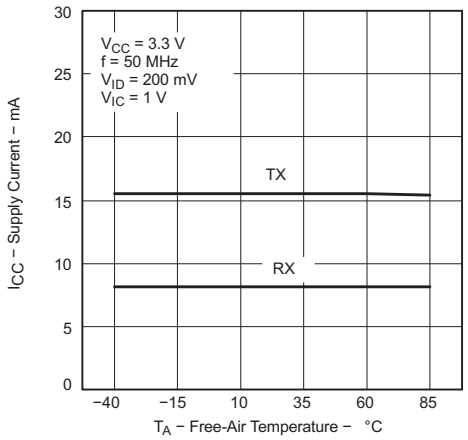


Figure 6-2. Supply Current vs Free-Air Temperature

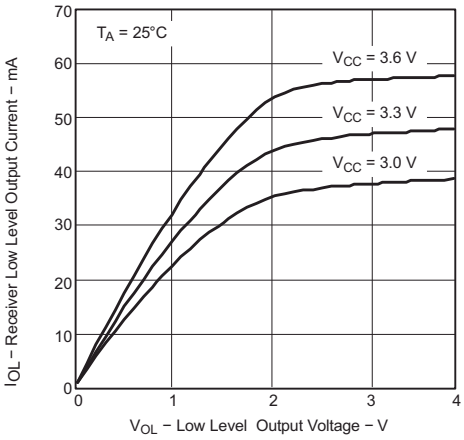


Figure 6-3. Receiver Low-Level Output Current vs Low-Level Output Voltage

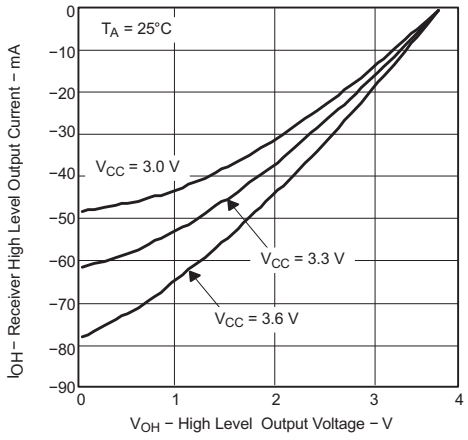


Figure 6-4. Receiver High-Level Output Current vs High-Level Output Voltage

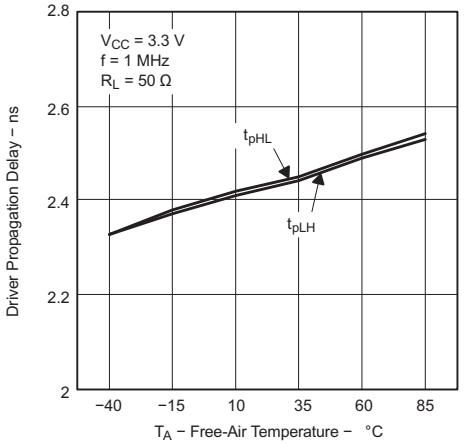


Figure 6-5. Driver Propagation Delay vs Free-Air Temperature

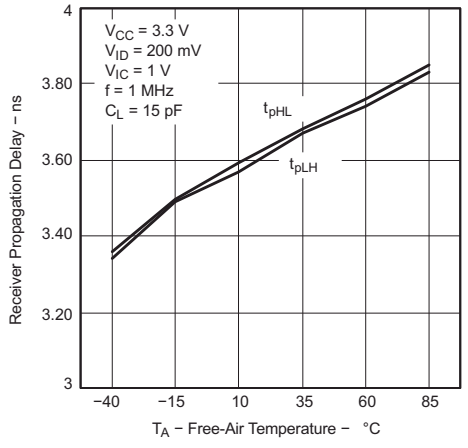


Figure 6-6. Receiver Propagation Delay vs Free-Air Temperature

6.11 Typical Characteristics (continued)

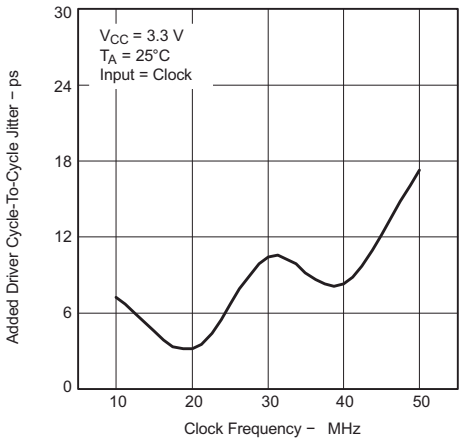


Figure 6-7. Added Driver Cycle-to-Cycle Jitter vs Clock Frequency

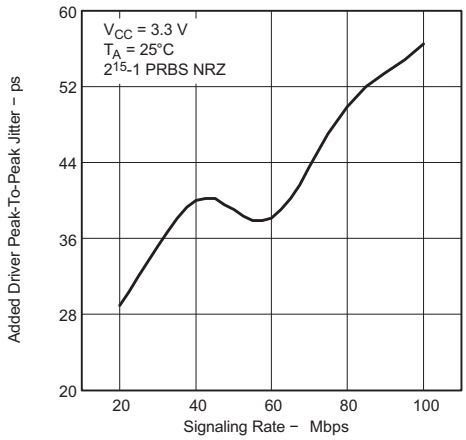


Figure 6-8. Added Driver Peak-to-Peak Jitter vs Signaling Rate

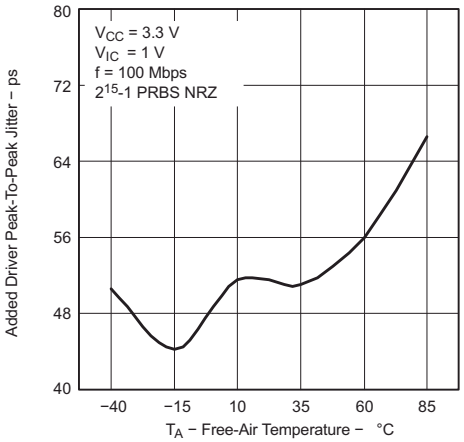


Figure 6-9. Added Driver Peak-to-Peak Jitter vs Free-Air Temperature

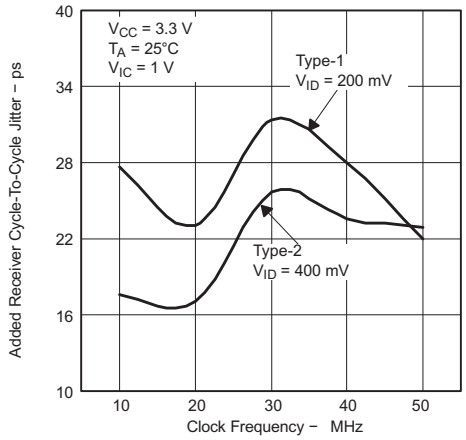


Figure 6-10. Added Receiver Cycle-to-Cycle Jitter vs Clock Frequency

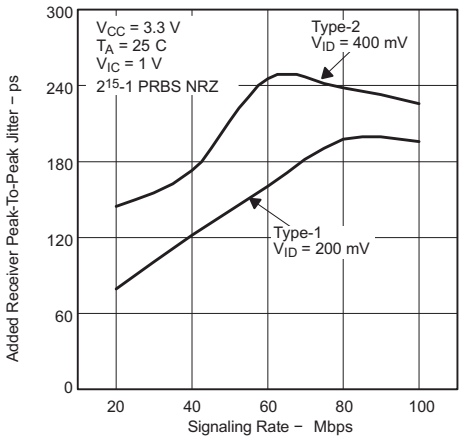


Figure 6-11. Added Receiver Peak-to-Peak Jitter vs Signaling Rate

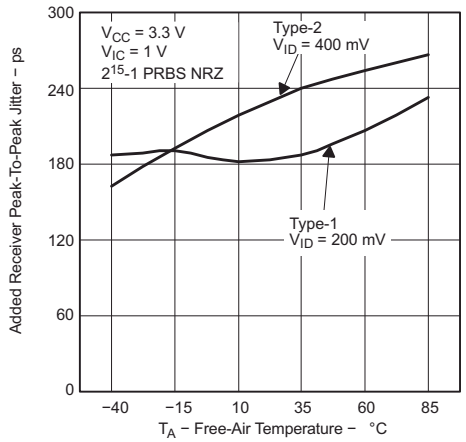


Figure 6-12. Added Receiver Peak-to-Peak Jitter vs Free-Air Temperature

7 Parameter Measurement Information

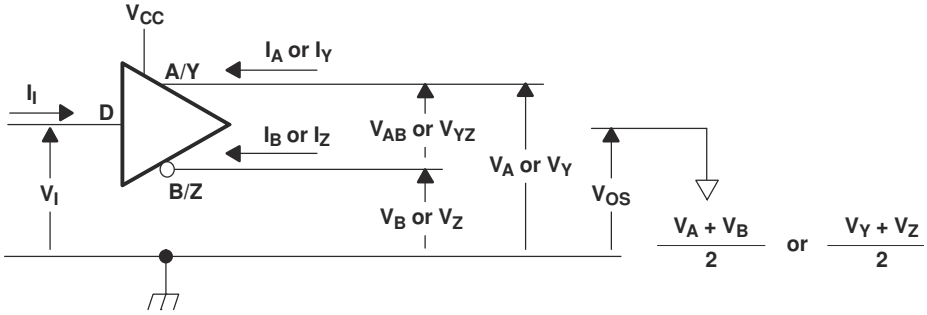
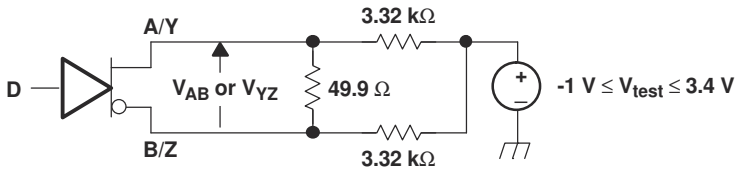
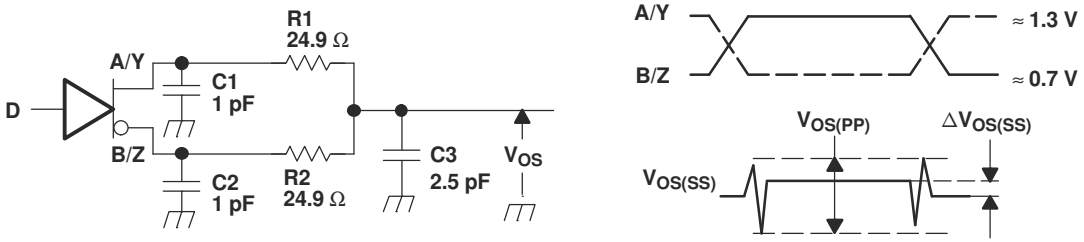


Figure 7-1. Driver Voltage and Current Definitions



A. All resistors are 1% tolerance.

Figure 7-2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 7-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

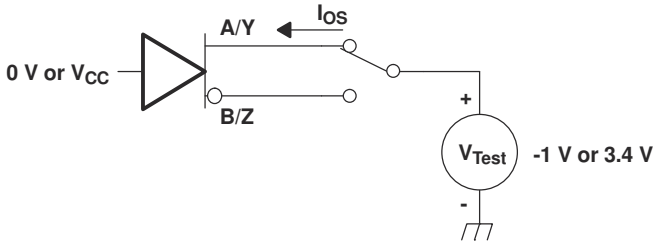
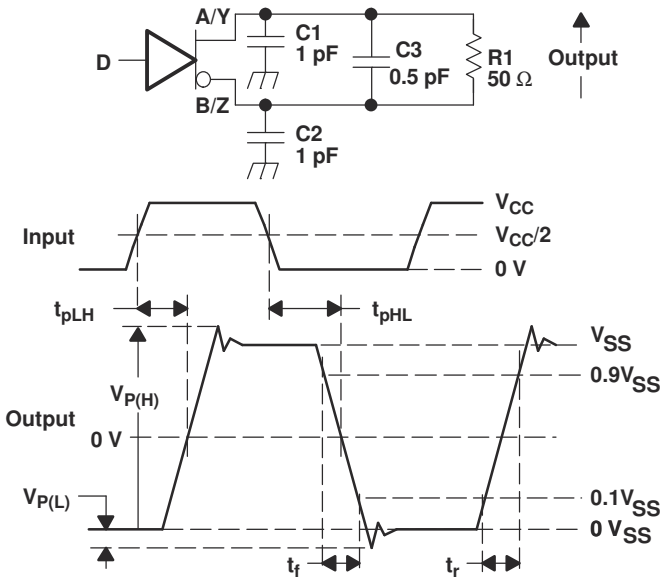
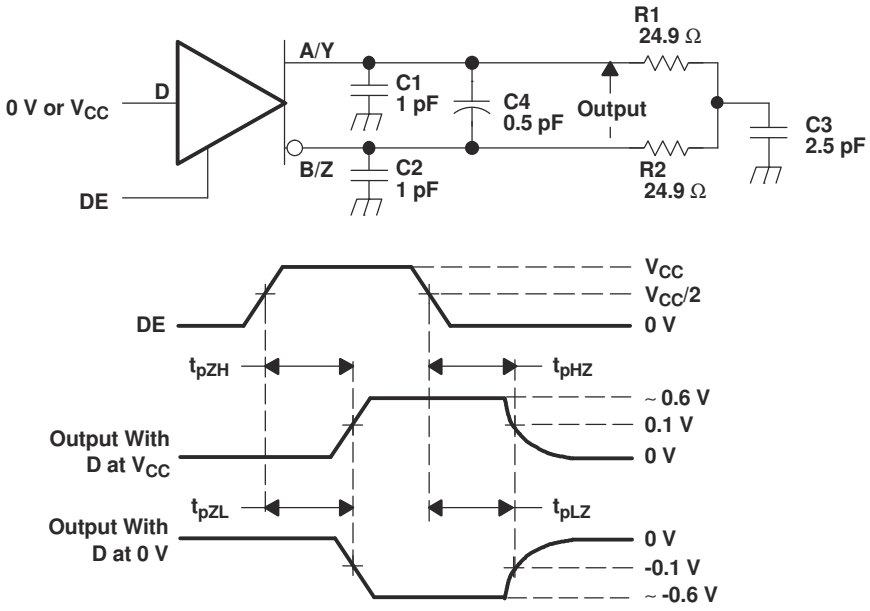


Figure 7-4. Driver Short-Circuit Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 7-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 7-6. Driver Enable and Disable Time Circuit and Definitions

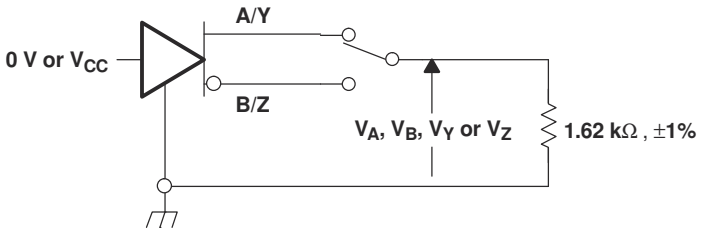
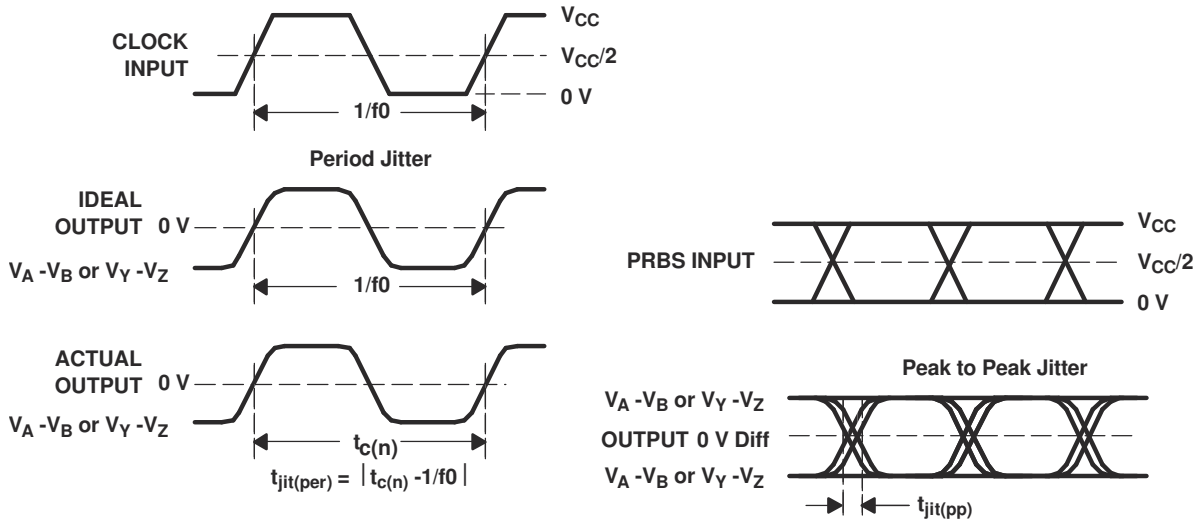


Figure 7-7. Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 81250 Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 50 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 100 Mbps 2^{15} –1 PRBS input.

Figure 7-8. Driver Jitter Measurement Waveforms

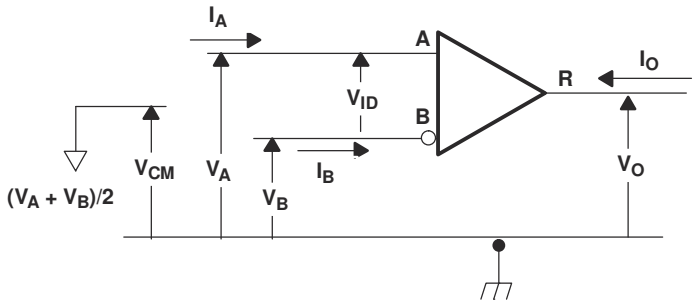


Figure 7-9. Receiver Voltage and Current Definitions

Table 7-1. Type-1 Receiver Input Threshold Test Voltages

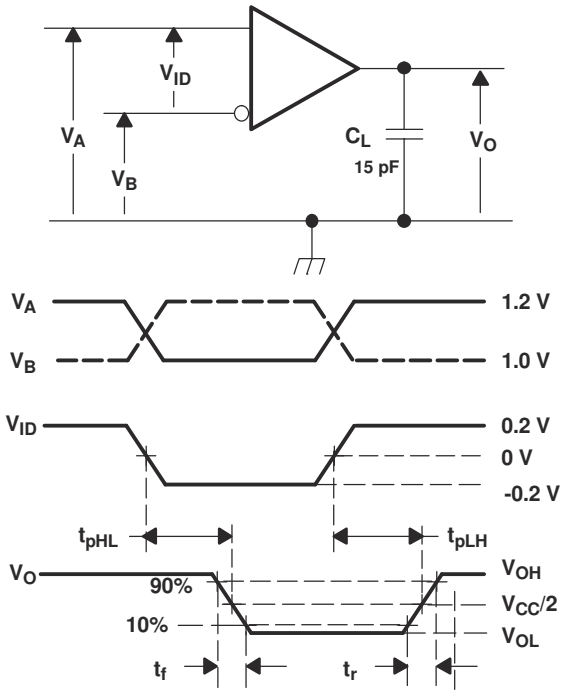
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER [(1)]OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.425	3.335	0.050	3.4	H
3.375	3.425	–0.050	3.4	L
–0.975	–1.025	0.050	–1	H
–1.025	–0.975	–0.050	–1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

Table 7-2. Type-2 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT[(1)]
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.475	3.325	0.150	3.4	H
3.425	3.375	0.050	3.4	L
–0.925	–1.075	0.150	–1	H
–0.975	–1.025	0.050	–1	L

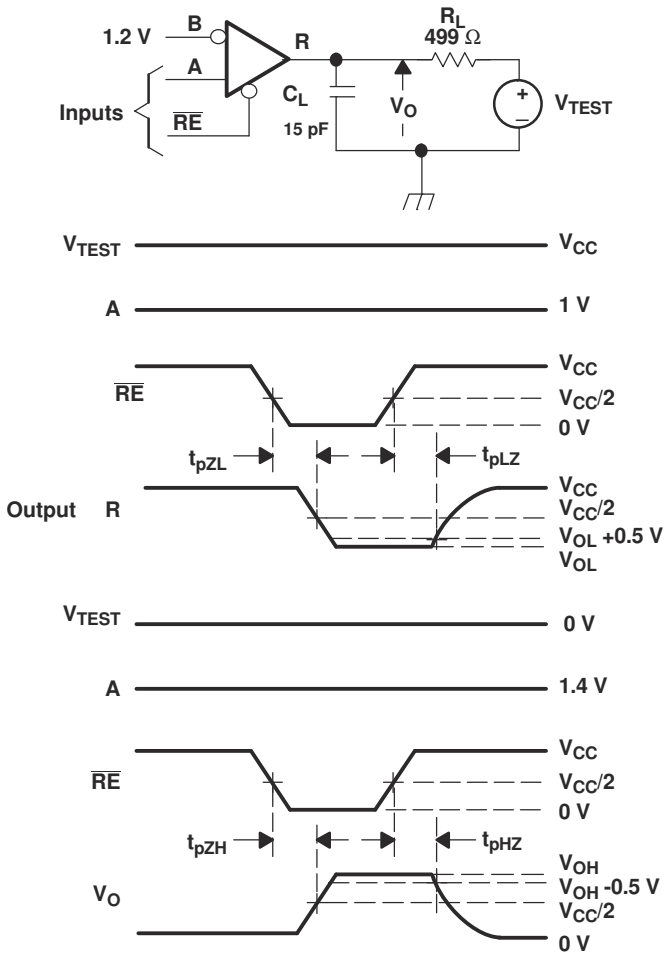
(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

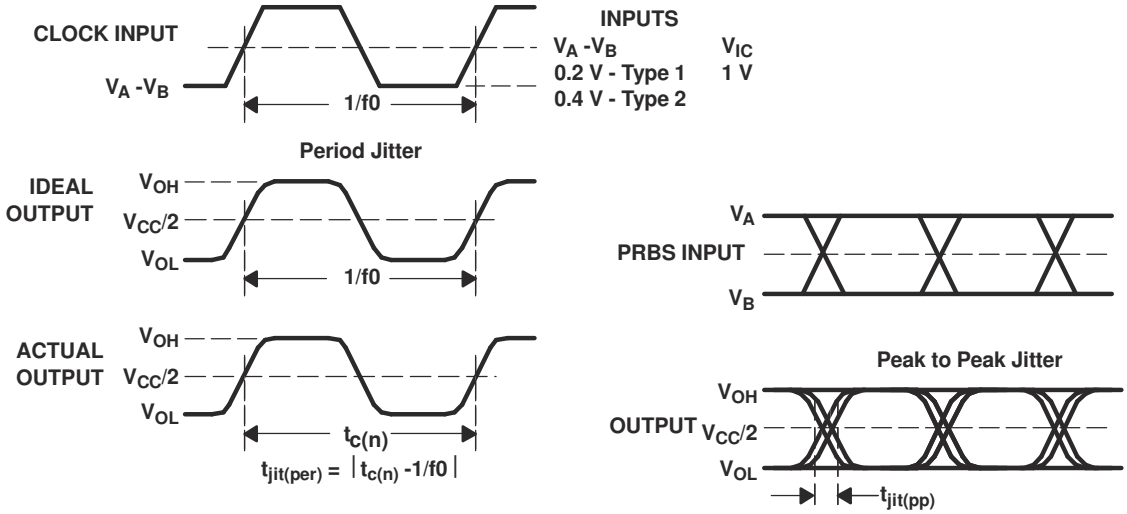
B. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 7-10. Receiver Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and ±20%.

Figure 7-11. Receiver Enable and Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 50 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 100 Mbps 2^{15} –1 PRBS input.

Figure 7-12. Receiver Jitter Measurement Waveforms

8 Detailed Description

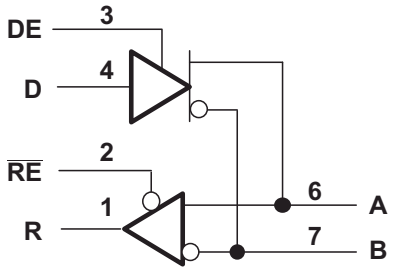
8.1 Overview

The SN65MLVD20xA family of devices are multipoint-low-voltage differential (M-LVDS) line drivers and receivers that are optimized to operate at signaling rates up to 100 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV (for Type-1) or 150 mV (for Type-2) of differential input voltage over a common-mode voltage range of –1 V to 3.4 V. The Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a known output state under open-circuit and bus-idle fault conditions.

8.2 Functional Block Diagram

SN65MLVD200A, SN65MLVD204A



SN65MLVD202A, SN65MLVD205A

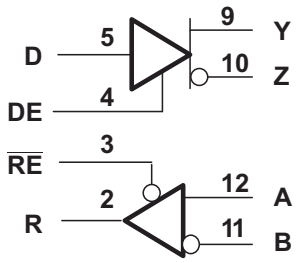


Figure 8-1. Logic Diagrams (Positive Logic)

8.3 Feature Description

8.3.1 Power-On Reset

This family of devices operates and meets all the specified performance requirements for supply voltages in the range of 3 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry sets the driver output to a high-impedance state.

8.3.2 ESD Protection

The bus terminals of the SN65MLVD20xA devices possess on-chip ESD protection against ±8-kV human body model (HBM) and ±8 kV.

8.4 Device Functional Modes

8.4.1 Device Function Tables

Table 8-1. Type-1 Receiver (SN65MLVD200A)(1)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
-50 mV < V_{ID} < 50 mV	L	?
$V_{ID} \leq -50$ mV	L	L
X	H	Z
X	Open	Z

(1) H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

Table 8-2. Type-2 Receiver (SN65MLVD204A)(1)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 150$ mV	L	H
50 mV < V_{ID} < 150 mV	L	?
$V_{ID} \leq 50$ mV	L	L
X	H	Z
X	Open	Z

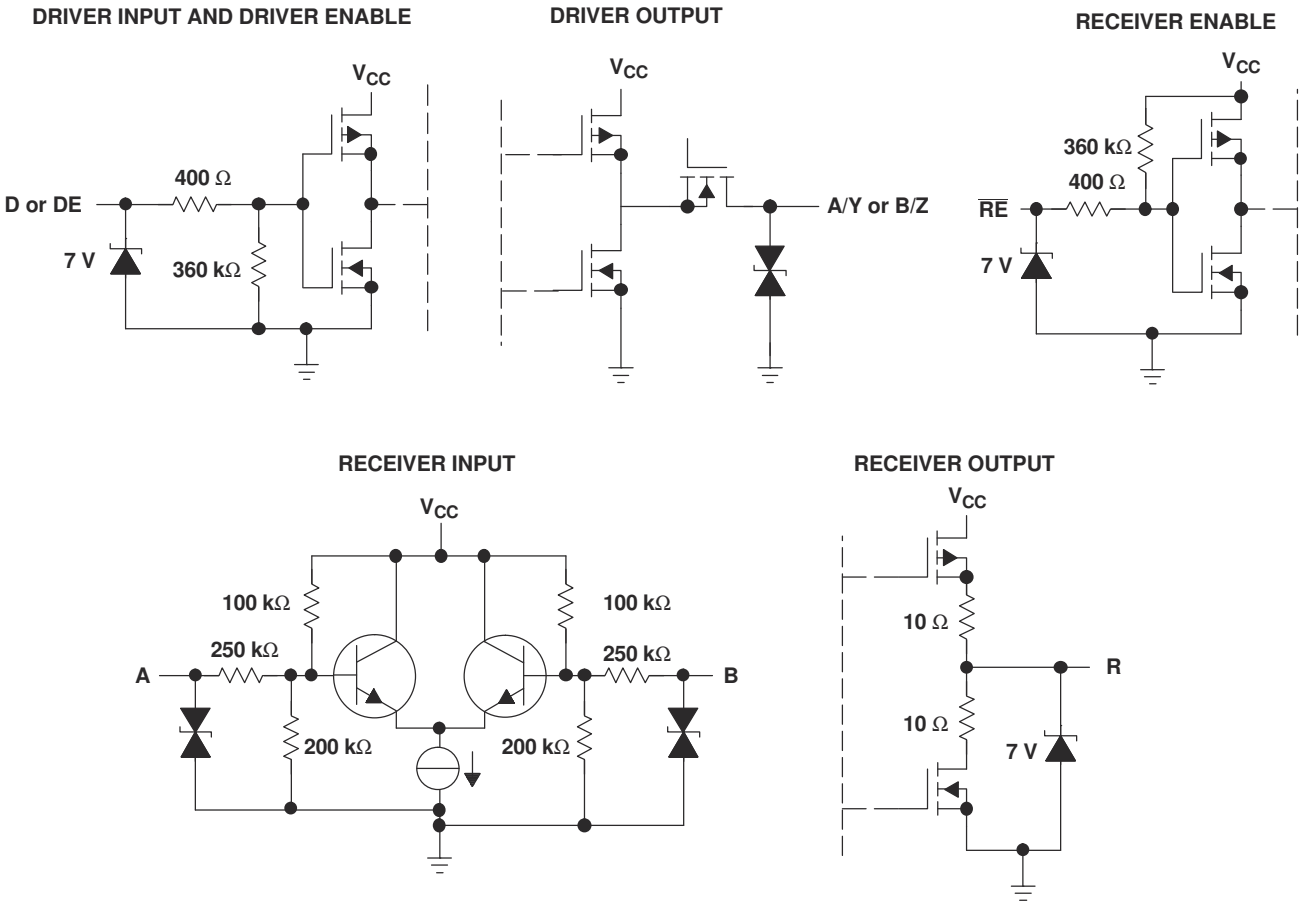
(1) H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

Table 8-3. Driver(1)

INPUTS	ENABLE	OUTPUTS	
D	DE	A	B
L	H	L	H
H	H	H	L
Open	H	L	H
X	Open	Z	Z
X	L	Z	Z

(1) H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

8.4.2 Equivalent Input and Output Schematic Diagrams



9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65MLVD20xA family of devices are multipoint line drivers and receivers. The functionality of these devices is simple, yet extremely flexible, thus leading to their use in designs ranging from wireless base stations to desktop computers.

9.2 Typical Application

Figure 9-1 shows a multipoint configuration. In a multipoint configuration, many transmitters and many receivers can be interconnected on one transmission line. The key difference compared to multidrop is the presence of two or more drivers. Such a situation creates contention issues that must not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over one balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.

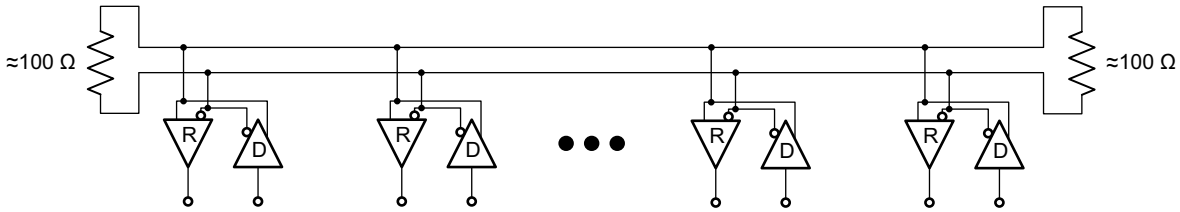


Figure 9-1. Multipoint Configuration

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 V to 3.6 V
Driver input voltage	0.8 V to 3.3 V
Driver signaling rate	DC to 100 Mbps
Interconnect characteristic impedance (differential)	100 Ω
Termination resistance	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 V to 3.6 V
Receiver input voltage	0 to (V_{CC} – 0.8) V
Receiver signaling rate	DC to 100 Mbps
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Supply Voltage

The SN65MLVD20xA devices are operated from one supply. The SN65MLVD20xA devices can support operation with a supply as low as 3 V and as high as 3.6 V.

9.2.2.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to µF range) must be installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with M-LVDS chips can be determined by Equation 1 and Equation 2, according to *High Speed Digital Design – A Handbook of Black Magic* by Howard Johnson and Martin Graham (1993). A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of M-LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 100 mV; however, this figure varies depending on the noise budget available for the design.

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{MLVDS} = \left(\frac{100\ \text{mA}}{100\ \text{mV}} \right) \times 4\,\text{ns} = 0.004\ \mu\text{F} \quad (2)$$

Figure 9-2 shows a configuration that lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.004 µF). Place the smallest value of capacitance as close as possible to the chip.

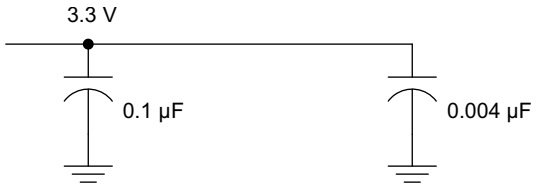


Figure 9-2. Recommended M-LVDS Bypass Capacitor Layout

9.2.2.3 Driver Input Voltage

The input stage accepts LVTTL signals. The driver will operate with a decision threshold of approximately 1.4 V.

9.2.2.4 Driver Output Voltage

The driver outputs a steady state common mode voltage of 1 V with a differential signal of 540 V under nominal conditions.

9.2.2.5 Termination Resistors

An M-LVDS communication channel employs a current source driving a transmission line that is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors must be matched to the characteristic impedance of the transmission line. The designer must ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistors must be between 90 Ω and 110 Ω. The line termination resistors are typically placed at the ends of the transmission line.

9.2.2.6 Receiver Input Signal

The M-LVDS receivers herein comply with the M-LVDS standard and correctly determine the bus state. These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential voltage over the common mode range of –1 V to 3.4 V.

9.2.2.7 Receiver Input Threshold (Failsafe)

The M-LVDS standard defines a Type-1 and a Type-2 receiver. Type-1 receivers have differential input voltage thresholds near zero volts. Type-2 receivers have differential input voltage thresholds offset from 0 V to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 9-2 and Figure 9-3.

Table 9-2. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\ V \le V_{ID} \le -0.05\ V$	$0.05\ V \le V_{ID} \le 2.4\ V$
Type 2	$-2.4\ V \le V_{ID} \le 0.05\ V$	$0.15\ V \le V_{ID} \le 2.4\ V$

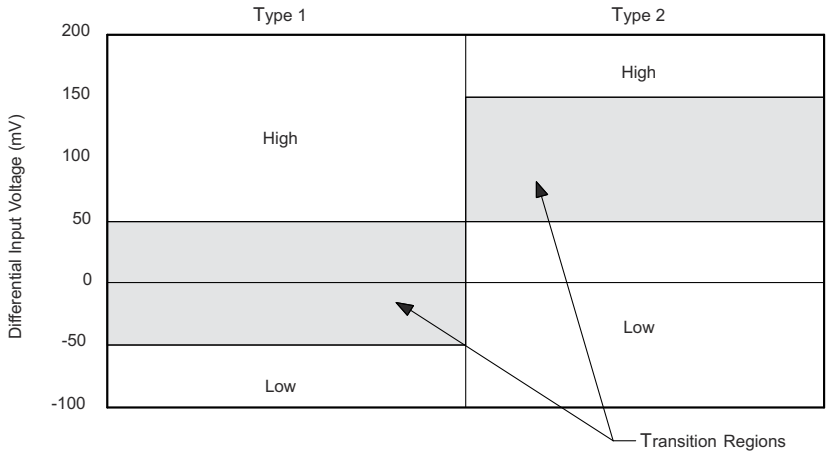


Figure 9-3. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

9.2.2.8 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

9.2.2.9 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced, paired metal conductors that meet the requirements of the M-LVDS standard—the key points are included in the following. The interconnecting media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect must be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

9.2.2.10 PCB Transmission Lines

The *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187), Figure 9-4 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer that is separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line, which is also called *controlled-impedance transmission line*.

When two signal lines are placed close together, they form a pair of coupled transmission lines. Figure 9-4 shows examples of edge-coupled microstrips and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called *odd-mode impedance*. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent (for example, if S is less than 2 × W) the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length and to maintain good symmetry between the two lines.

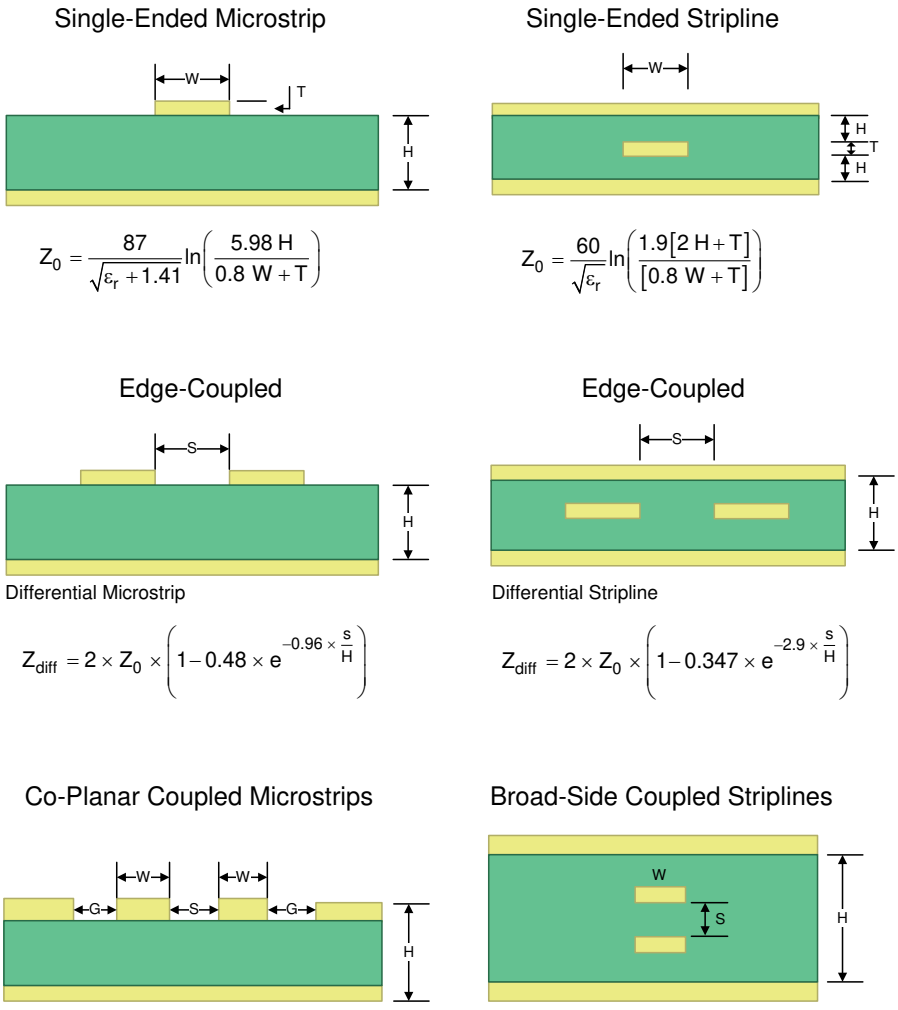


Figure 9-4. Controlled-Impedance Transmission Lines

9.2.3 Application Curves

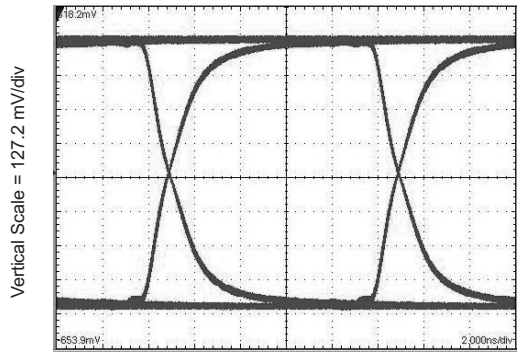


Figure 9-5. SN65MLVD200A Driver Output Eye Pattern

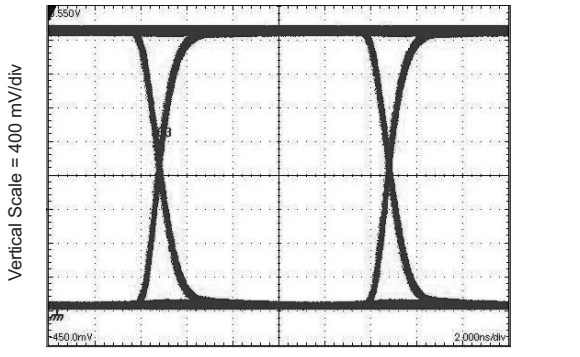


Figure 9-6. SN65MLVD200A Receiver Output Eye Pattern

10 Power Supply Recommendations

The M-LVDS drivers and receivers in this data sheet are designed to operate from one power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards or even separate equipment. In these cases, separate supplies must be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ±1 V. Board level and local device level bypass capacitance must be used and are covered supply bypass capacitance.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip Versus Stripline Topologies

According to the *LVDS Application and Data Handbook* (SLLD009), printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 11-1.

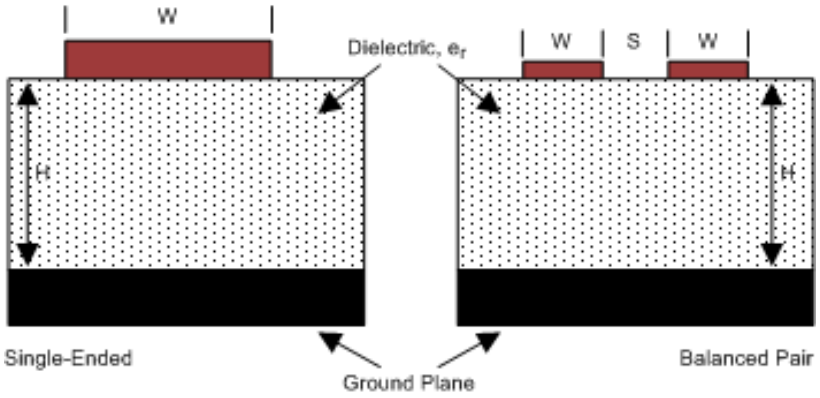


Figure 11-1. Microstrip Topology

Striplines are traces between two ground planes (see Figure 11-2). Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing M-LVDS signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[1], 2[2], and 3[3] provide the documentation for formulas for Z_O and t_{PD} for differential and single-ended traces. [2] [3] [4]

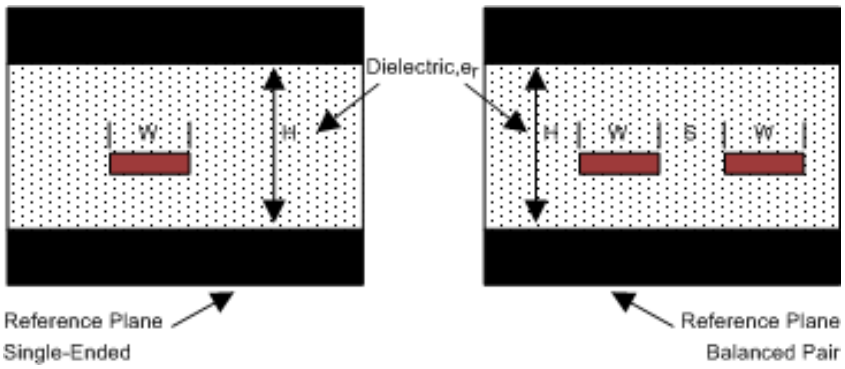


Figure 11-2. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with M-LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. When the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving M-LVDS devices:

- Copper weight: 15 g or ½ oz start, plated to 30 g or 1 oz
- All exposed circuitry must be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum)
- Copper plating must be 25.4 µm or 0.001 in (minimum) in plated-through-holes
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the TTL/CMOS to M-LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 11-3.

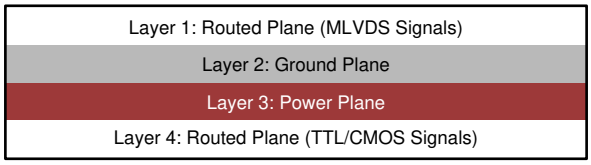


Figure 11-3. Four-Layer PCB Board

Note

The separation between layers 2 and 3 must be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

[2] Howard Johnson and Martin Graham.1993. *High Speed Digital Design – A Handbook of Black Magic.* Prentice Hall PRT. ISBN number 013395724.
[3] Mark I. Montrose. 1996. *Printed Circuit Board Design Techniques for EMC Compliance.* IEEE Press. ISBN number 0780311310.
[4] Clyde F. Coombs. 1995. *Printed Circuits Handbook.* McGraw Hill. ISBN number 0070127549.

One of the most common stack configurations is the six-layer board, as shown in Figure 11-4.

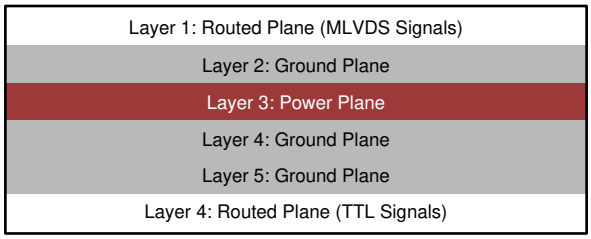


Figure 11-4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an M-LVDS link to benefit from the electromagnetic field cancellation. The traces must be 100-Ω differential and coupled in the manner that best fits this requirement. In addition, differential pairs must have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one must use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of one trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule must be applied to the separation between adjacent M-LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

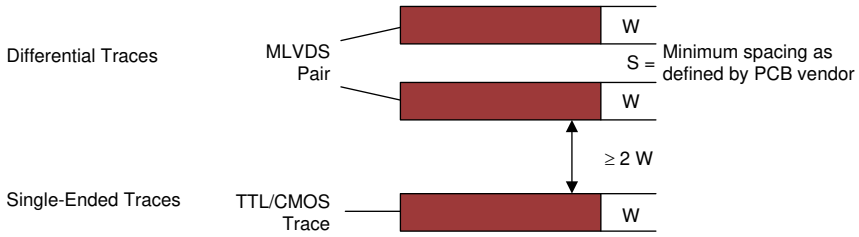


Figure 11-5. 3-W Rule for Single-Ended and Differential Traces (Top View)

Exercise caution when using autorouters because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and must be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device must be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

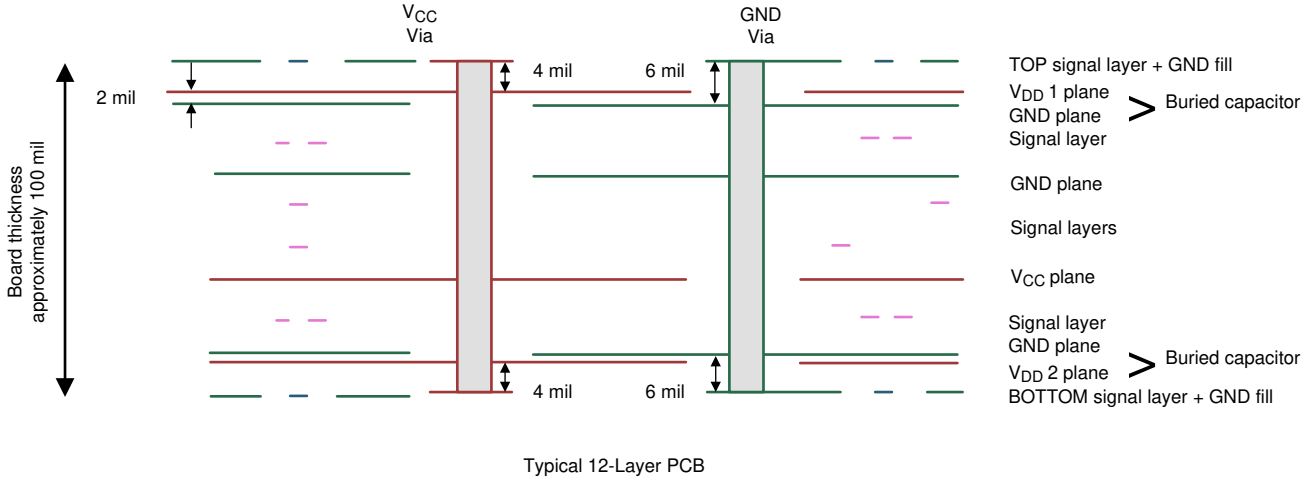


Figure 11-6. Low Inductance, High-Capacitance Power Connection

Bypass capacitors must be placed close to V_{DD} pins and can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small physical-size capacitors (such as 0402, 0201, or X7R surface-mount capacitors) must be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 11-7(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above about 30 MHz, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB.

Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small surface mount technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 9-4) creates multiple paths for heat transfer.

Thermal PCB issues are often the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases, the GND pad that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve, due to insufficient pad-to-pad spacing as shown in Figure 11-8(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum.

It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad into the via barrel, which results in a poor solder connection

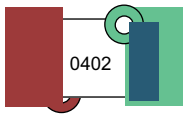


Figure 11-7. Typical Decoupling Capacitor Layout (a)

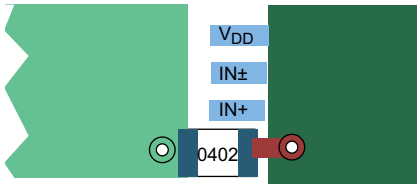


Figure 11-8. Typical Decoupling Capacitor Layout (b)

11.2 Layout Example

At least two or three times the width of an individual trace must separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 11-9.

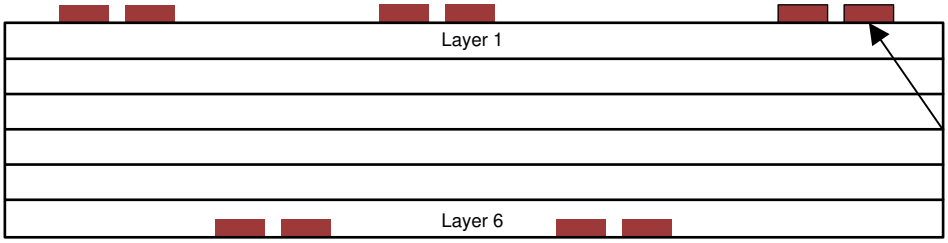


Figure 11-9. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 11-10.

Note

Vias create additional capacitance. For example, a typical via has a lumped capacitance effect of ½ pF to 1 pF in FR4.

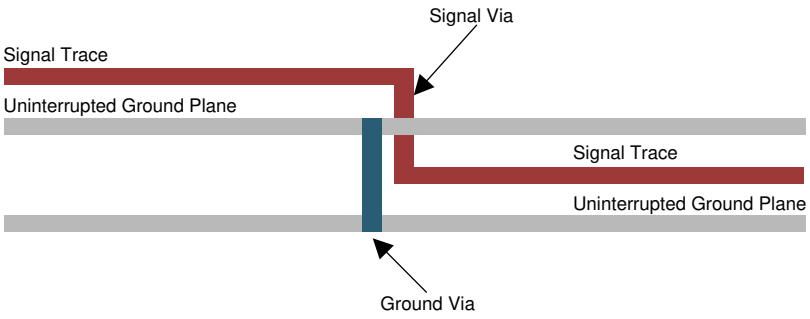


Figure 11-10. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Introduction to M-LVDS (TIA/EIA-899)* (SLLA108)
- *LVDS Application and Data Handbook* (SLLD009)
- *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- Howard Johnson and Martin Graham.1993. *High Speed Digital Design – A Handbook of Black Magic.* Prentice Hall PRT. ISBN number 013395724.
- Mark I. Montrose. 1996. *Printed Circuit Board Design Techniques for EMC Compliance.* IEEE Press. ISBN number 0780311310.
- Clyde F. Coombs. 1995. *Printed Circuits Handbook.* McGraw Hill. ISBN number 0070127549.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

Rogers™ is a trademark of Rogers Corporation.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

Changes from Revision D (December 2015) to Revision E (March 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision C (September 2015) to Revision D (December 2015)	Page
• Deleted Features list item "Meets ±8-kV IEC 61000-4-2, Contact Discharge"	1

Changes from Revision B (June 2015) to Revision C (August 2015) **Page**

- Deleted row "Open Circuit" from Table 8-1 and Table 8-2 as redundant 18
- Changed from "V_{ID} ≥ 50 mV " to "V_{ID} ≥ 150 mV " in Table 8-2 18
- Changed from "–50 mV < V_{ID} < 150 mV" to "50 mV < V_{ID} < 150 mV" in Table 8-2 18

Changes from Revision A (December 2003) to Revision B (June 2015) **Page**

- *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed SN65MLVD204B from the data sheet..... 1
- Changed *Ordering Information* to *Device Comparison Table* 3
- Deleted |V_{ID}| MIN value in *Recommended Operating Conditions* 4
- Changed *Multipoint Configuration* image..... 20

Changes from Revision * (December 2003) to Revision A (December 2003) **Page**

- Deleted duplicate Note from Figure 7-11 11

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD200AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	Samples
SN65MLVD200ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	Samples
SN65MLVD200ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	Samples
SN65MLVD200ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	Samples
SN65MLVD202AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD202A	Samples
SN65MLVD202ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD202A	Samples
SN65MLVD204AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	Samples
SN65MLVD204ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	Samples
SN65MLVD204ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	Samples
SN65MLVD205AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	Samples
SN65MLVD205ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	Samples
SN65MLVD205ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

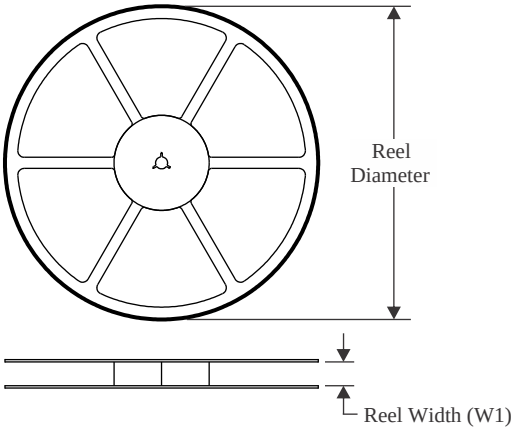
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

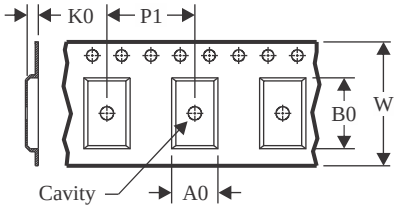
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

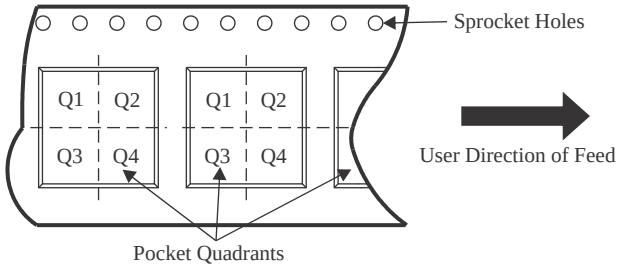


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

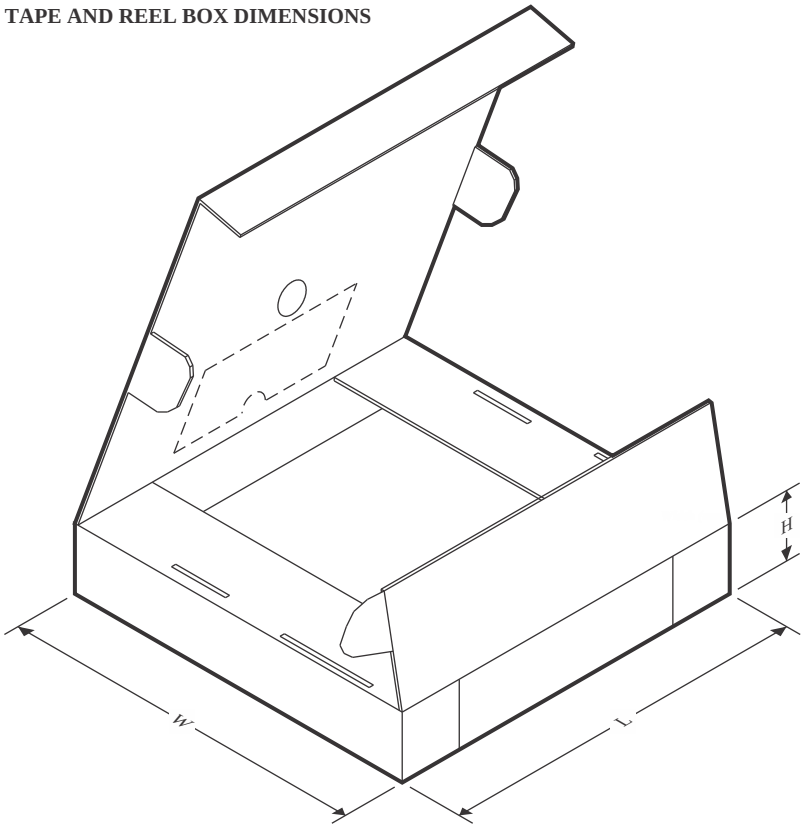
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD200ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD202ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65MLVD204ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD205ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

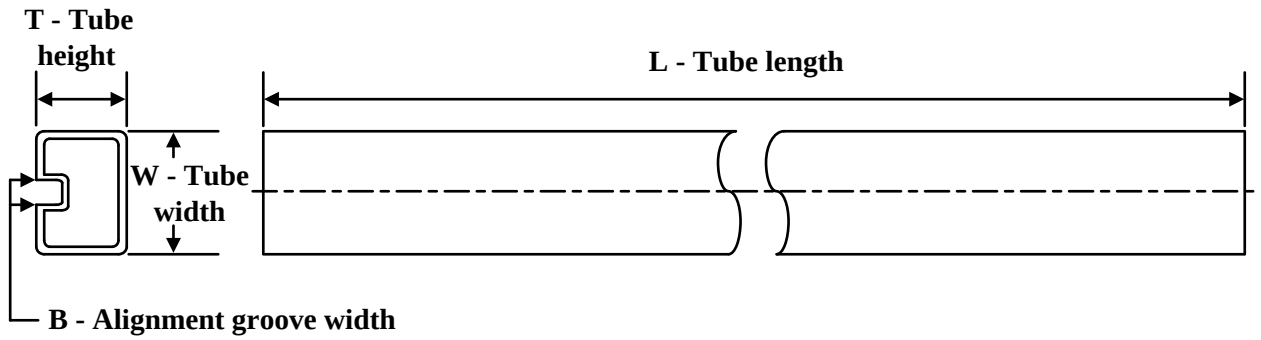
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

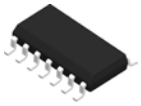
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD200ADR	SOIC	D	8	2500	353.0	353.0	32.0
SN65MLVD202ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN65MLVD204ADR	SOIC	D	8	2500	353.0	353.0	32.0
SN65MLVD205ADR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65MLVD200AD	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD200ADG4	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD202AD	D	SOIC	14	50	507	8	3940	4.32
SN65MLVD204AD	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD204ADG4	D	SOIC	8	75	507	8	3940	4.32
SN65MLVD205AD	D	SOIC	14	50	507	8	3940	4.32
SN65MLVD205ADG4	D	SOIC	14	50	507	8	3940	4.32

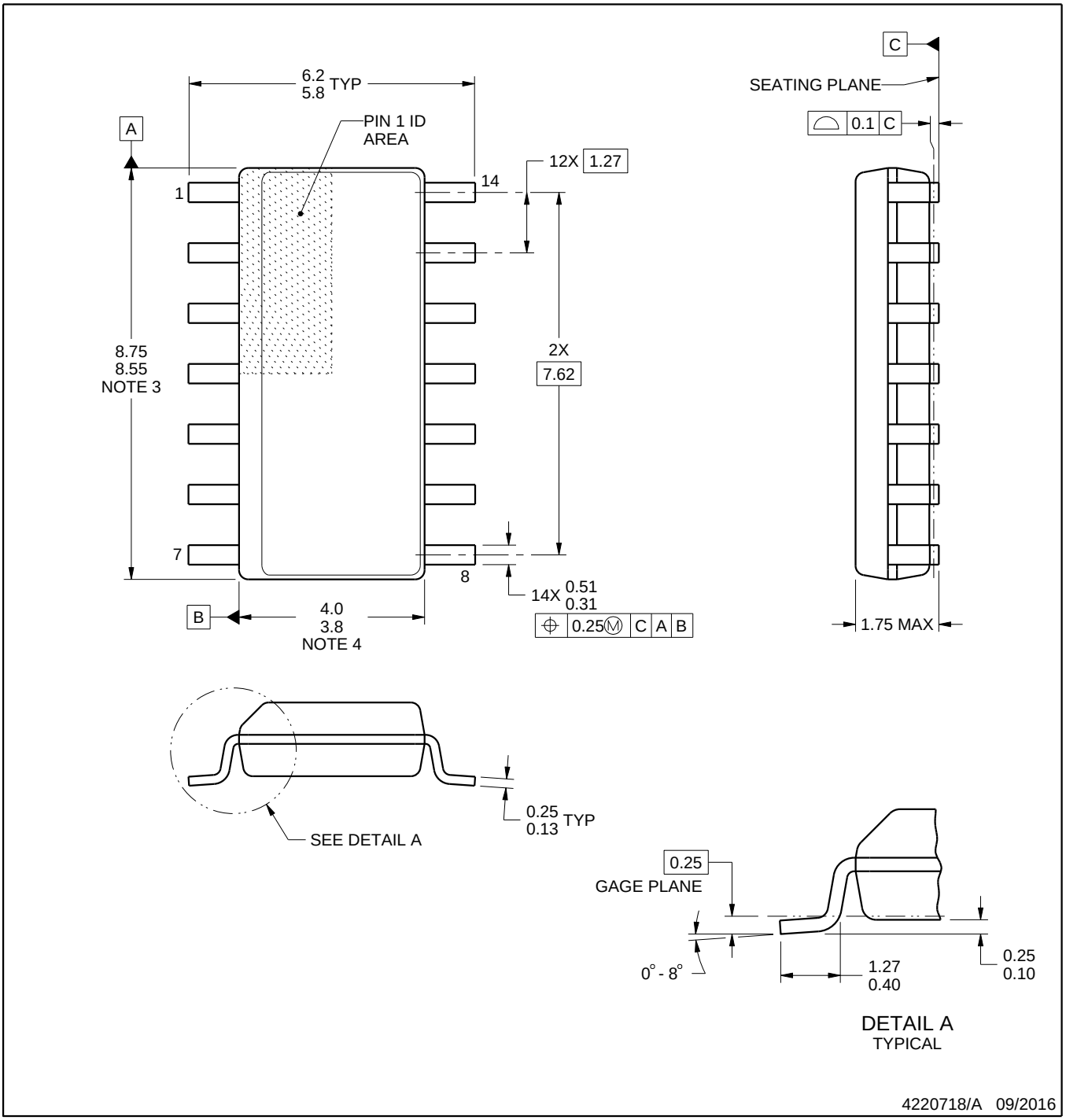


PACKAGE OUTLINE

D0014A

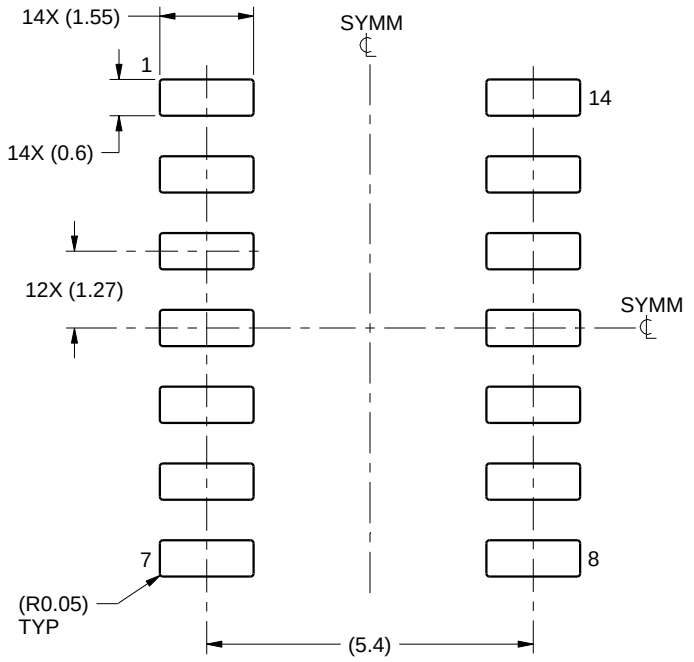
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

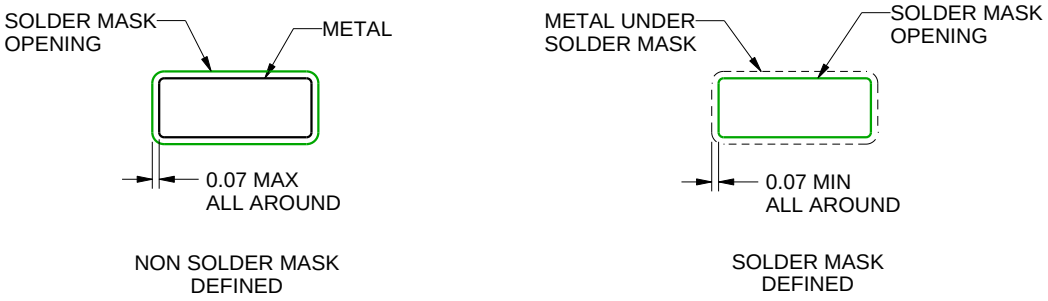


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

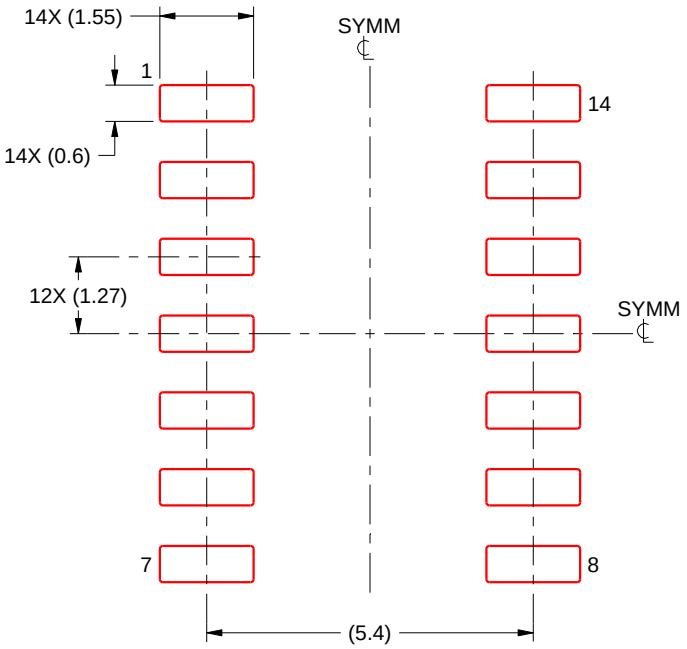
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

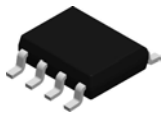


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

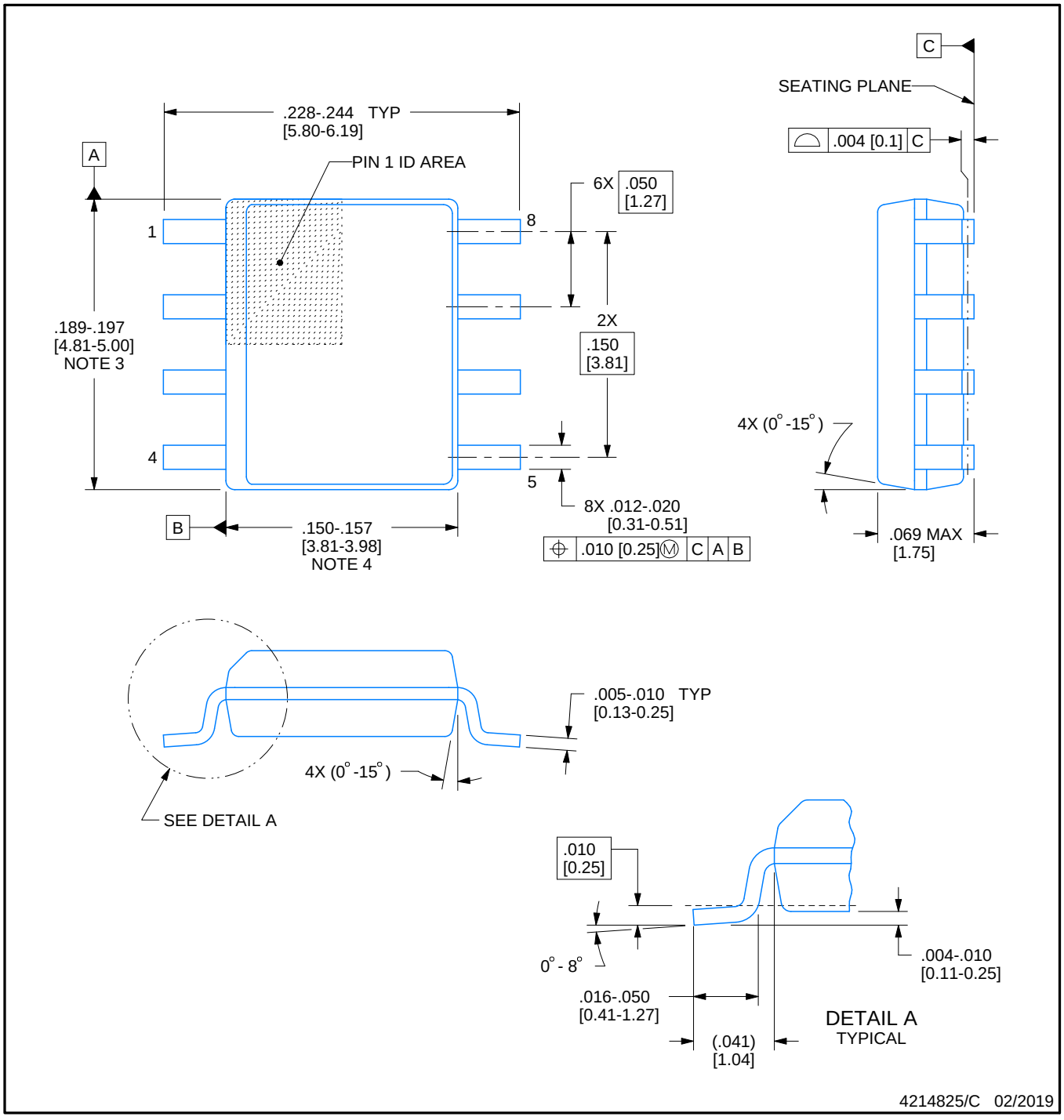


PACKAGE OUTLINE

D0008A

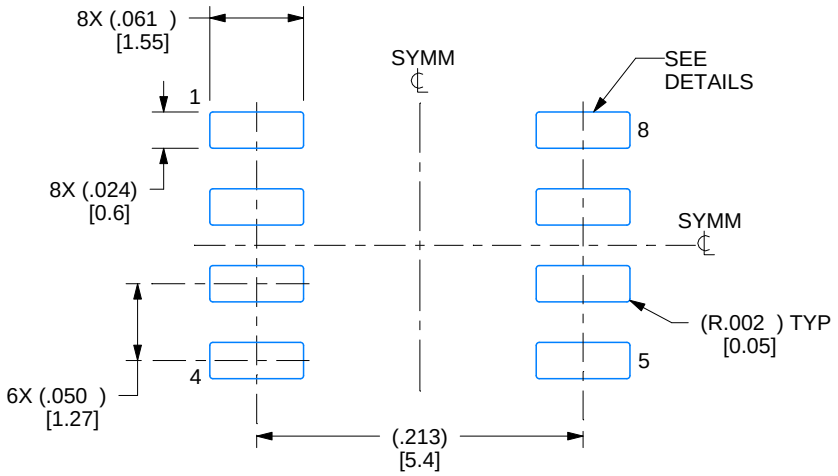
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

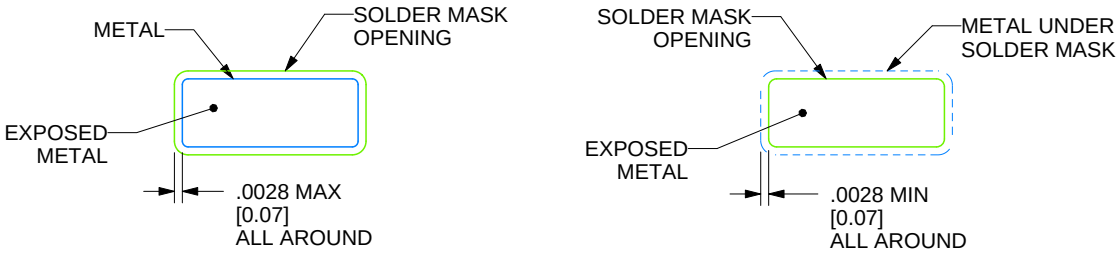


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

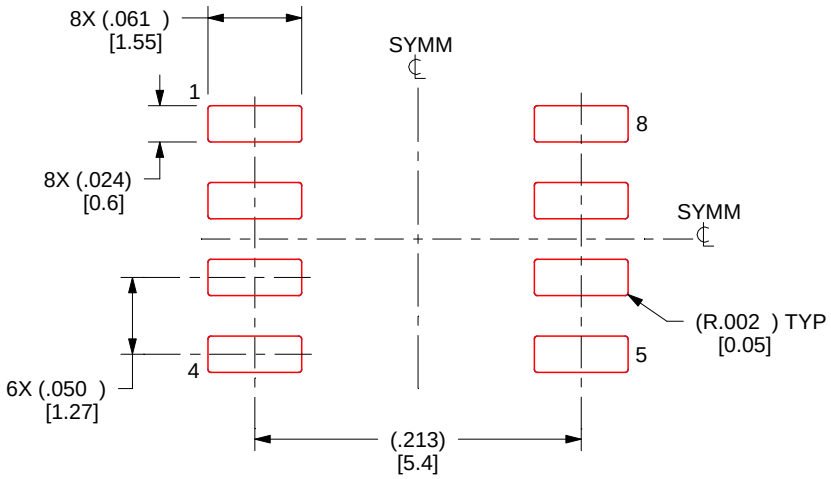
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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