OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers

1 Features

- Precision super-beta performance:
  - Low offset voltage: 200 µV (maximum)
  - Ultra-low drift: 1 µV/°C (maximum)
- Excellent efficiency:
  - Quiescent current: 580 µA (typical)
  - Gain-bandwidth product: 1 MHz
  - Low input voltage noise: 9 $\text{nV}/\sqrt{\text{Hz}}$
- Ease of use, design simplicity:
  - Heavy capacitive load drive: 5-µs settling time with 25 nF
  - Ultra-high input impedance: 3000 GΩ and 0.5 pF
  - EMI hardened, thermal, and short-circuit protection
- Stable Performance:
  - High CMRR and A_{OL}: 126 dB (minimum)
  - High PSRR: 126 dB (minimum)
- Low bias current: 2 nA (maximum)
- Low 0.1-Hz to 10-Hz noise: 0.2 μV_{PP}
- Wide supply voltage: ±2.25 V to ±18 V
- Replaces OP-07 and OP-27

2 Applications

- Data acquisition (DAQ)
- Lab and field instrumentation
- Merchant network and server PSU
- Multiparameter patient monitor
- String inverter

3 Description

The OPA202, OPA2202, and OPA4202 (OPAx202) are a family of devices built on TI's industry-leading precision super-beta, complementary, bipolar semiconductor process. This process offers ultra-low flicker noise, low offset voltage, low offset voltage temperature drift, and excellent linearity with common-mode and power-supply variation. These devices offer an exceptional combination of dc precision, heavy capacitive load drive, and protection against external EMI, thermal, and short-circuit events.

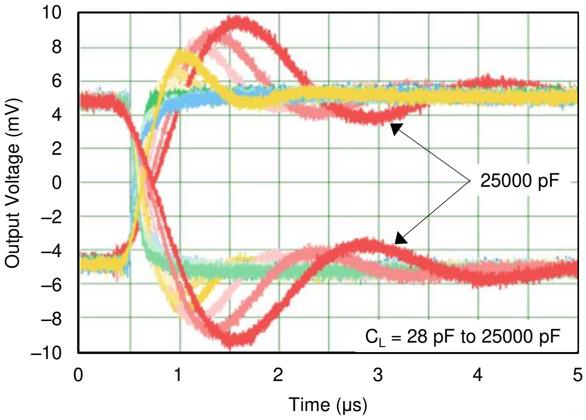
The supply current is 580 µA at ±18 V. The OPAx202 do not exhibit phase inversion, and the series is stable with high capacitive loads. The OPAx202 are fully specified with a temperature range from –40°C to +105°C.

Device Information[(1)]

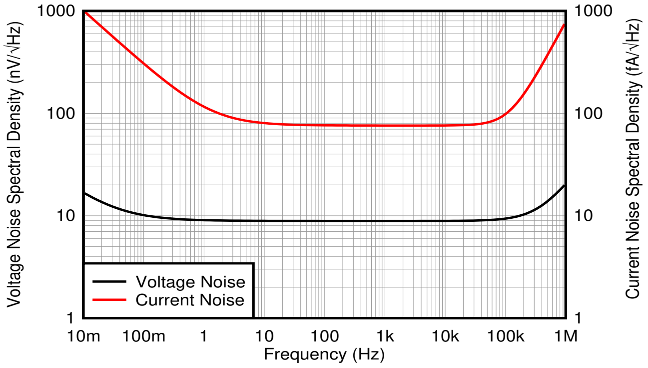
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA202	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2202	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA4202	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPAx202 Excel Even When Directly Driving Heavy Capacitive Loads



Input Voltage Noise and Current Noise Spectral Density vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2020) to Revision H	Page
• Changed OPA202 VSSOP (DGK) and OPA2202 SOIC (D) packages from preview to production data (active)	1

Changes from Revision F (February 2020) to Revision G	Page
• Changed OPA4202 14-pin TSSOP (PW) package from preview to production data (active)	1
• Added OPA2202 8-pin SOIC (D) preview package and associated content to data sheet	1

Changes from Revision E (February 2020) to Revision F	Page
• Added OPA4202 14-pin TSSOP (PW) preview package and associated content to data sheet	1
• Changed Figure 19, *Input Voltage Noise and Current Noise Spectral Density vs Frequency*, to more accurately represent the input current noise behavior of the device	15

Changes from Revision D (December 2019) to Revision E	Page
• Added OPA202 8-pin VSSOP (DGK) preview package and associated content to data sheet	1

Changes from Revision C (October 2018) to Revision D	Page
• Changed OPA2202 and OPA4202 devices from advanced information (preview) to production data (active)	1

Changes from Revision B (December 2018) to Revision C	Page
• Added OPA2202 and OPA4202 preview devices and associated content to data sheet	1
• Deleted *Operating Voltage* section; redundant information	20

Changes from Revision A (September 2018) to Revision B — Page

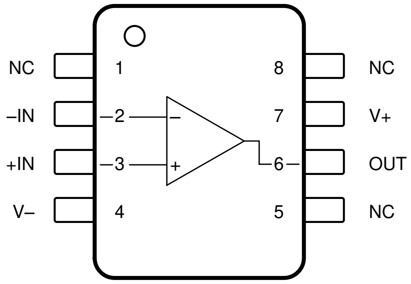
- Changed SOT-23 package from preview to production data 1

Changes from Original (October 2017) to Revision A — Page

- Added preview content for SOT-23 package offering 1

5 Pin Configuration and Functions

OPA202 D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



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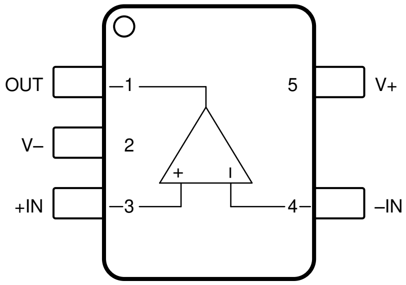
OPA202 DBV Package
5-Pin SOT-23
Top View



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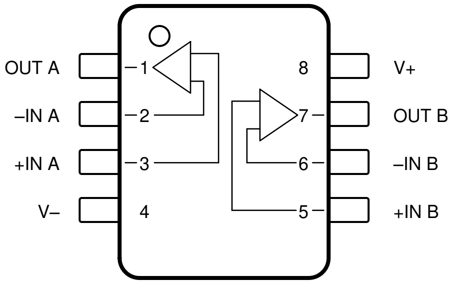
Pin Functions: OPA202

PIN			I/O	DESCRIPTION
NAME	NO.			
	D (SOIC) DGK (VSSOP)	DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Noninverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

OPA2202 D and DGK Packages
8-Pin SOIC VSSOP
Top View



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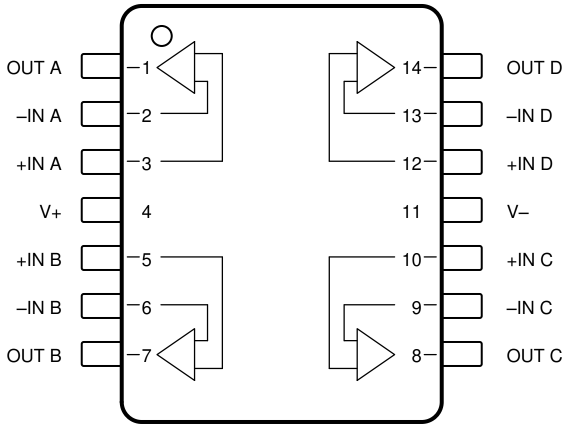
Pin Functions: OPA2202

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

OPA4202 D and PW Packages
14-Pin SOIC and 14-Pin TSSOP
Top View



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Pin Functions: OPA4202

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
–IN C	9	I	Inverting input channel C
+IN C	10	I	Noninverting input channel C
–IN D	13	I	Inverting input channel D
+IN D	12	I	Noninverting input channel D
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
OUT C	8	O	Output channel C
OUT D	14	O	Output channel D
V–	11	—	Negative supply
V+	4	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply			40	V
	Dual-supply			±20	
Signal input pins	Voltage	Common-mode(2)	(V–) – 0.5	(V+) + 0.5	
		Differential(3)		±0.5	
	Current			±10	mA
Output short current(4)			Continuous		
Operating temperature, T_A			–40	125	°C
Junction temperature, T_J				125	
Storage temperature, T_{stg}			–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Input terminals are anti-parallel diode-clamped to each other. Input signals that cause differential voltages of swing more than ± 0.5 V must be current-limited to 10 mA or less.
(4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, [(V+) – (V–)]	Single-supply	4.5		36	V
		Dual-supply	±2.25		±18	
T_A	Specified temperature		–40		105	°C

6.4 Thermal Information: OPA202

THERMAL METRIC(1)		OPA202			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT-23)	
		8 PINS	8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136	190.8	206.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	82.3	121.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	113.0	65.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	19.0	39.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	111.2	65.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2202

THERMAL METRIC(1)		OPA2202		UNIT
		DGK (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.1	121.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.4	65	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.5	18.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.8	64.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information: OPA4202

THERMAL METRIC(1)		OPA4202		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.9	116.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.7	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	61.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.1	60.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±18 V			±20	±200	µV
		V_S = ±18 V, T_A = –40°C to +105°C				±250	
dV_{OS}/dT	Input offset voltage drift	OPA202, OPA4202	T_A = –40°C to +105°C		±0.5	±1	µV/°C
		OPA2202	T_A = –40°C to +105°C		±0.5	±1.5	µV/°C
PSRR	Input offset voltage versus power supply	V_S = ±2.25 V to ±18 V			±0.1	±0.5	µV/V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +105°C				±0.5	
INPUT BIAS CURRENT							
I_B	Input bias current				±0.25	±2	nA
		T_A = –40°C to +105°C				±2.1	
I_{OS}	Input offset current	OPA202 (D, DBV)			±15	±150	pA
			T_A = –40°C to +105°C			±700	
		OPA202 (DGK), OPA2202, OPA4202			±25	±250	
			T_A = –40°C to +105°C			±700	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		µV_{PP}
					0.03		µV_{RMS}
e_n	Input voltage noise density	f = 10 Hz			9.5		nV/√Hz
		f = 100 Hz			9.1		
		f = 1 kHz			9		
i_n	Input current noise	f = 1 kHz			0.076		pA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V	114	131		dB
			(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to +105°C	114			
		V_S = ±18 V	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V	126	148		
			(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to +105°C	119			
INPUT CAPACITANCE							
	Differential				10 || 3.3		MΩ || pF
	Common-mode				3 || 0.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±2.25 V	(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 10 kΩ	120	135		dB
			(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 10 kΩ, T_A = –40℃ to +105℃	119			
		V_S = ±18 V	(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 10 kΩ	126	150		
			(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 10 kΩ, T_A = –40℃ to +105℃	126			
		V_S = ±2.25 V	(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 2 kΩ	120	133		
			(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 2 kΩ, T_A = –40℃ to +105℃	119			
		V_S = ±18 V	(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 2 kΩ	126	150		
			(V–) + 1.25 V ≤ V_O ≤ (V+) – 1.25 V, R_L = 2 kΩ, T_A = –40℃ to +105℃	126			

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1		MHz
SR	Slew rate	10-V step, G = 1			0.35		V/µs
t_S	Settling time	To 0.1%, 10-V step , G = 1			30		µs
		To 0.01%, 10-V step , G = 1			32		
	Overload recovery time	V_{IN} × gain > V_S			4		µs
THD+N	Total harmonic distortion + noise	V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ			0.0002%		
OUTPUT							
	Voltage output swing from rail	V_S = ±18 V	T_A = 25°C, No Load		650	750	mV
			T_A = 25°C, R_L = 10 kΩ		800	900	
			T_A = 25°C, R_L = 2 kΩ		1.05	1.15	V
			T_A = –40°C to +105°C, R_L = 10 kΩ			1	
			A_{OL} > 120 dB, R_L = 10 kΩ			1.05	
			A_{OL} > 120 dB, R_L = 2 kΩ			1.25	
I_{SC}	Short-circuit current	Sinking			35		mA
		Sourcing			35		
C_{LOAD}	Capacitive load drive				Figure 28		
Z_O	Open-loop output impedance	I_O = 0 mA, f = 1 MHz; see Figure 27			50		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			580	800	µA
		I_O = 0 mA, T_A = –40°C to +105°C				900	

6.8 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution From –40°C to +105°C	Figure 2
Input Bias Current Production Distribution	Figure 3
Input Offset Current Production Distribution	Figure 4
Offset Voltage vs Temperature	Figure 5
Offset Voltage vs Common-Mode Voltage	Figure 6
Offset Voltage vs Supply Voltage	Figure 7
Open-Loop Gain and Phase vs Frequency	Figure 8
Closed-Loop Gain vs Frequency	Figure 9
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Input Bias Current and Offset vs Temperature	Figure 11
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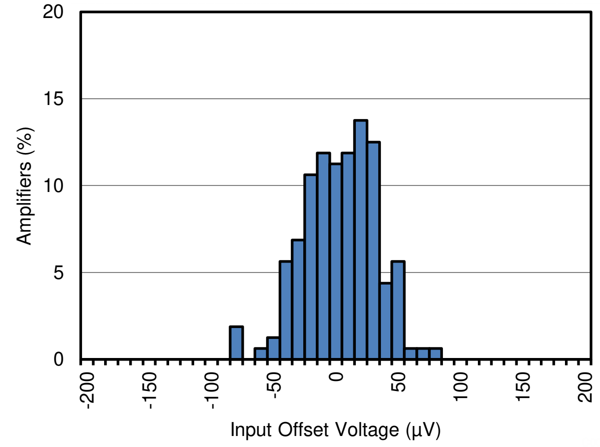
Settling Time (10-V Step)	Figure 36
Short-Circuit Current vs Temperature	Figure 37
Maximum Output Voltage vs Frequency	Figure 38
EMIRR vs Frequency	Figure 39

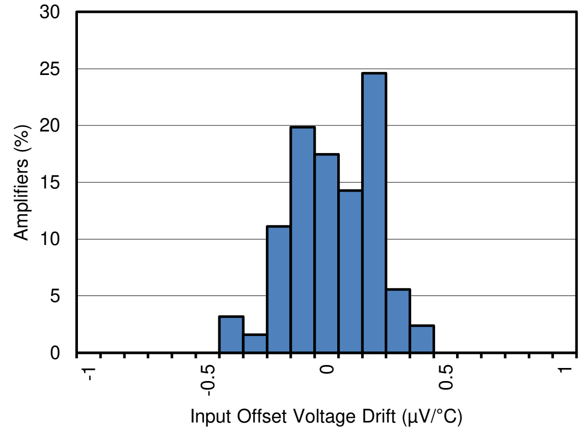
6.9 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



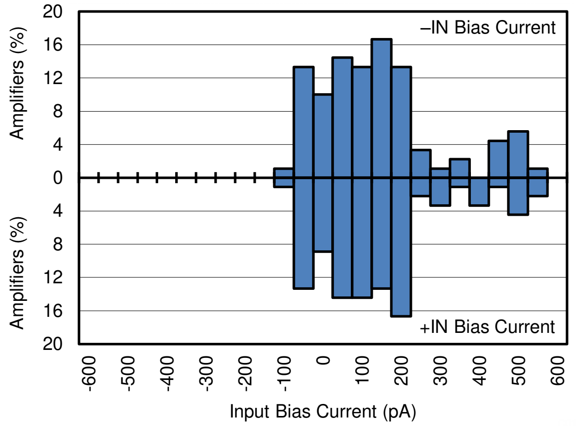
μ = –3.56 µV σ = 32.09 µV N = 252

Figure 1. Offset Voltage Production Distribution



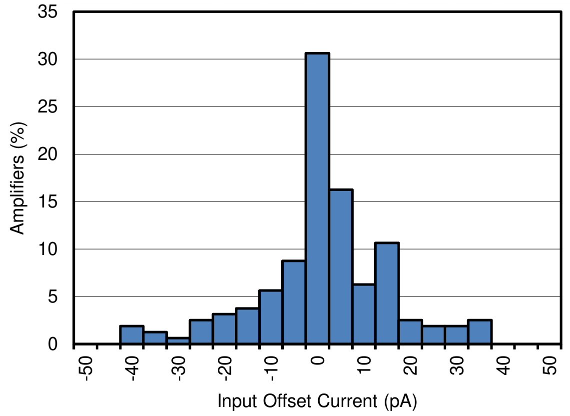
μ = –18.23 nV/°C σ = 177.41 nV/°C N = 252
T_A = –40°C to +105°C

Figure 2. Offset Voltage Drift Distribution



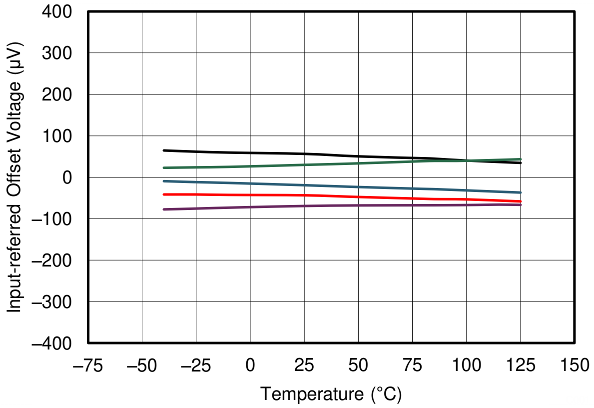
$μ_{–IN}$ = 112.335 pA $σ_{–IN}$ = 154.946 pA N = 90
$μ_{+IN}$ = 112.448 pA $σ_{+IN}$ = 152.739 pA

Figure 3. Input Bias Current Production Distribution



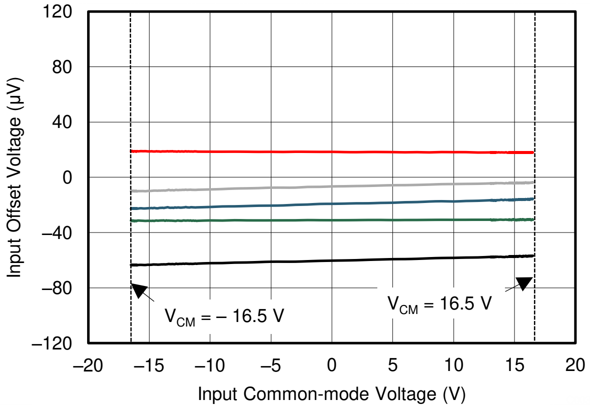
μ = 0.112 pA σ = 15.023 pA N = 90

Figure 4. Input Offset Current Production Distribution



5 typical units

Figure 5. Offset Voltage vs Temperature

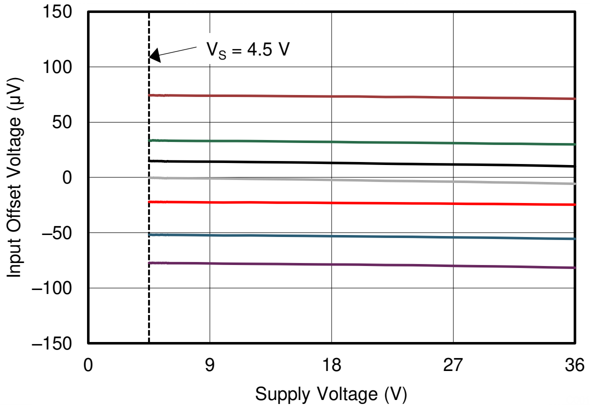


5 typical units

Figure 6. Offset Voltage vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



5 typical units

Figure 7. Offset Voltage vs Supply Voltage

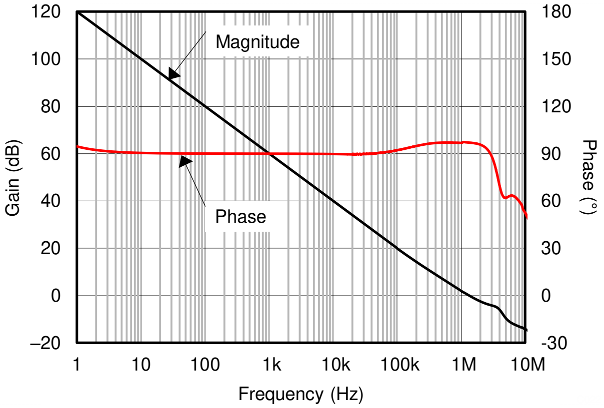


Figure 8. Open-Loop Gain and Phase vs Frequency

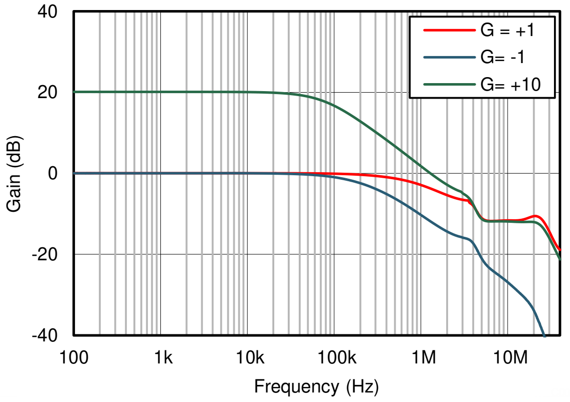


Figure 9. Closed-Loop Gain vs Frequency

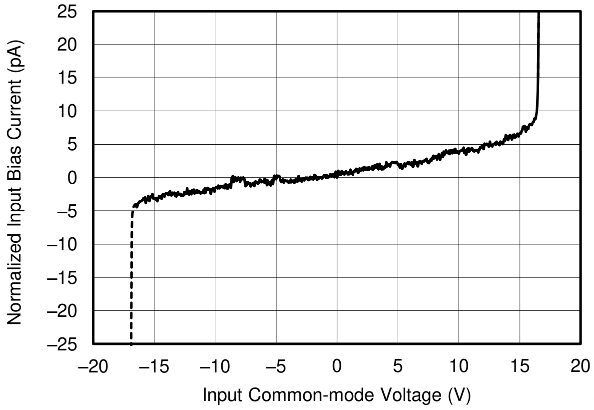


Figure 10. Input Bias Current vs Common-Mode Voltage

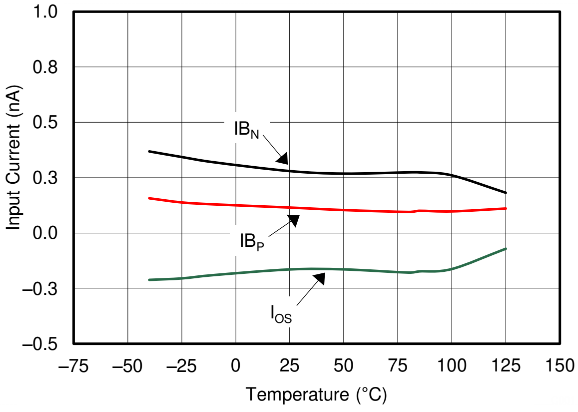


Figure 11. Input Bias Current and Offset vs Temperature

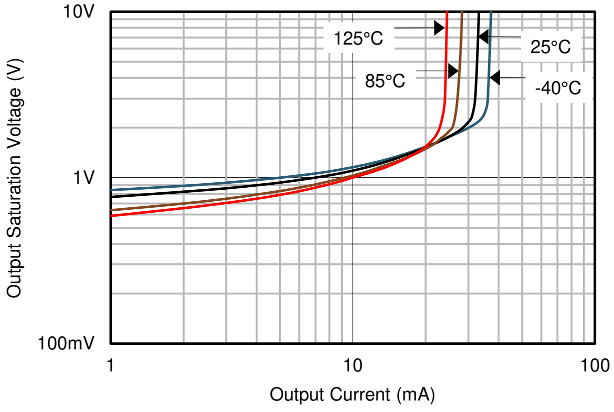


Figure 12. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

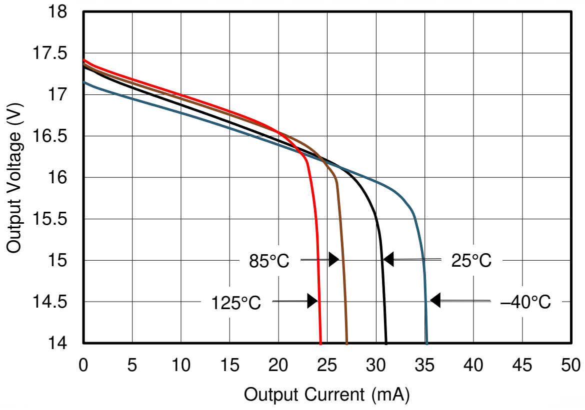


Figure 13. Output Voltage Swing vs Output Current (Sourcing)

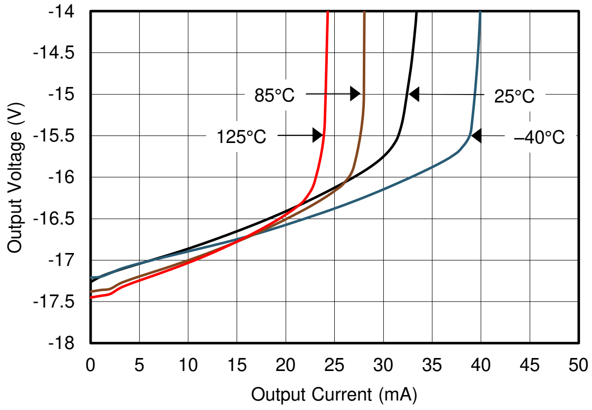


Figure 14. Output Voltage Swing vs Output Current (Sinking)

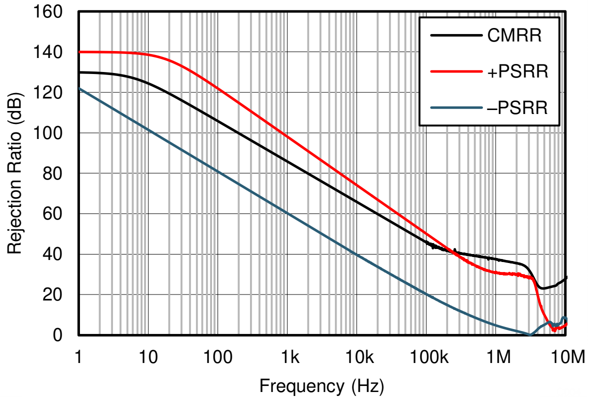


Figure 15. CMRR and PSRR vs Frequency

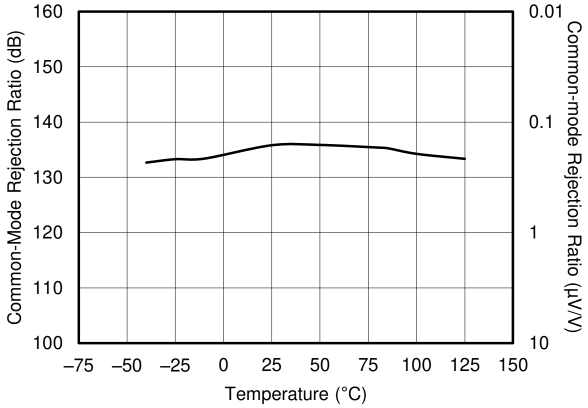


Figure 16. CMRR vs Temperature

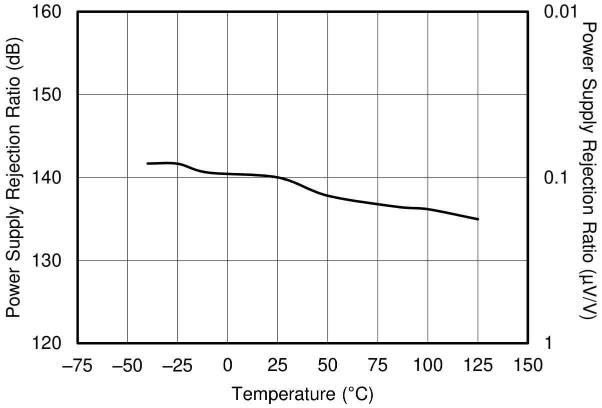


Figure 17. PSRR vs Temperature

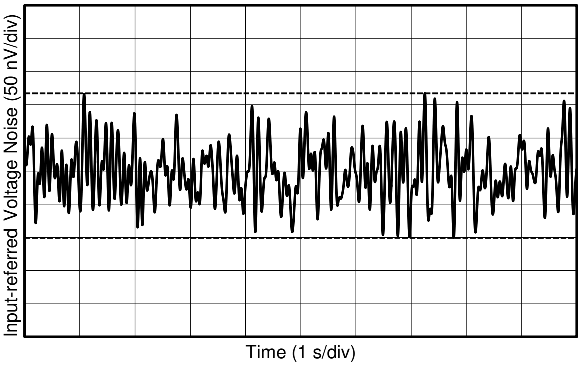


Figure 18. 0.1-Hz to 10-Hz Voltage Noise

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

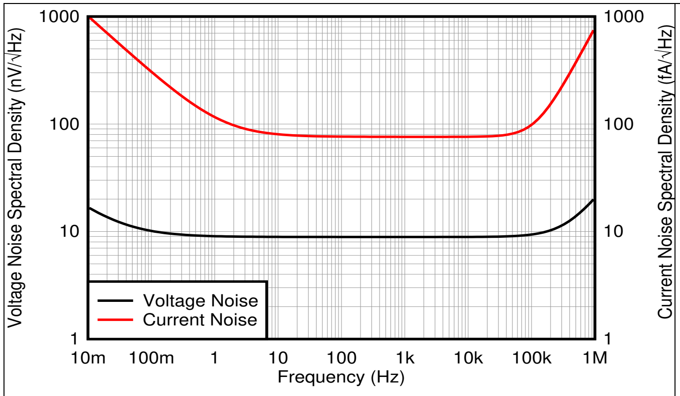
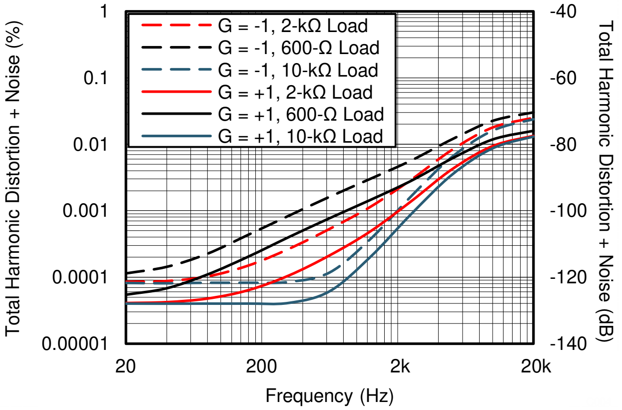
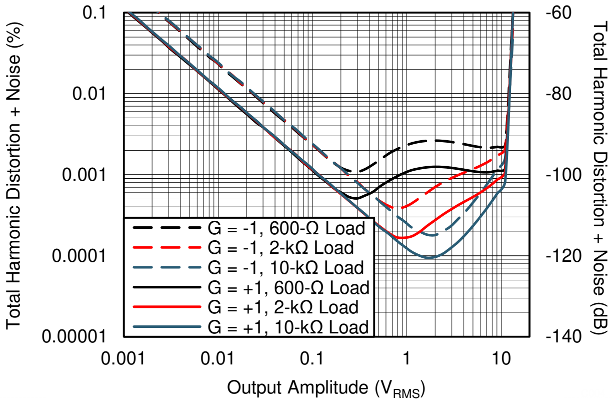


Figure 19. Input Voltage Noise and Current Noise Spectral Density vs Frequency



V_{OUT} = 3.5 V_{RMS} BW = 90 kHz

Figure 20. THD+N Ratio vs Frequency



f = 1 kHz BW = 90 kHz

Figure 21. THD+N vs Output Amplitude

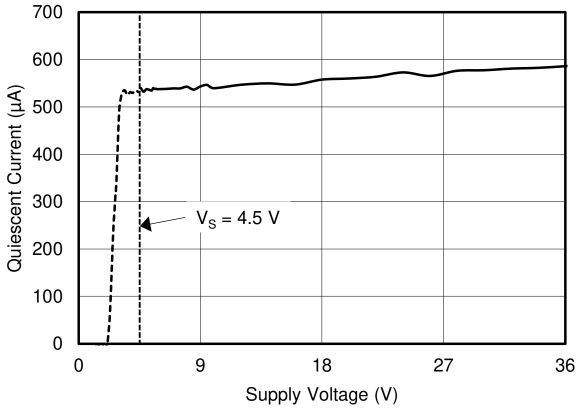


Figure 22. Quiescent Current vs Supply Voltage

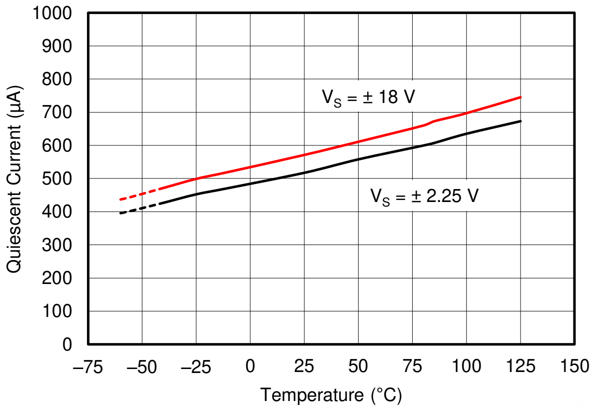


Figure 23. Quiescent Current vs Temperature

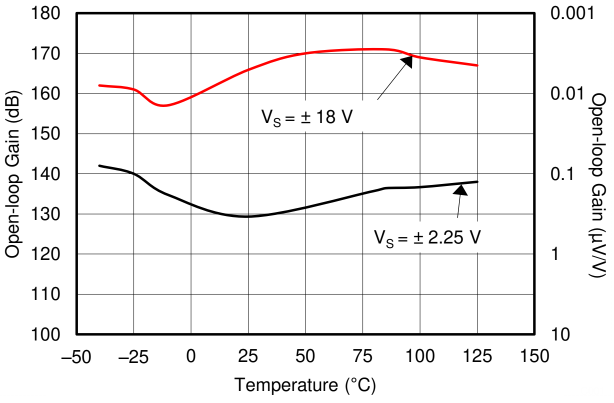
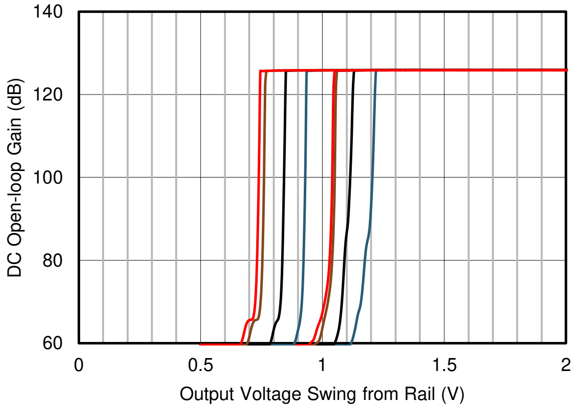


Figure 24. Open-Loop Gain vs Temperature (With 10-kΩ Load)

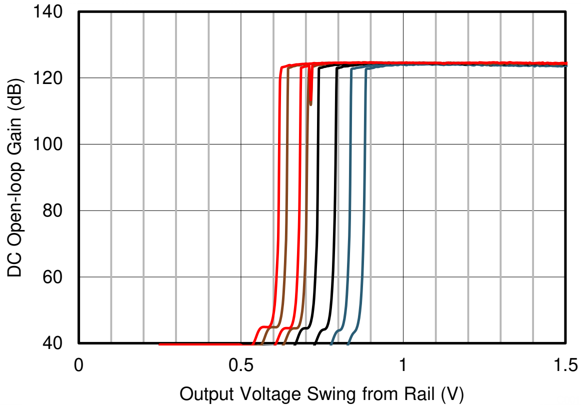
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



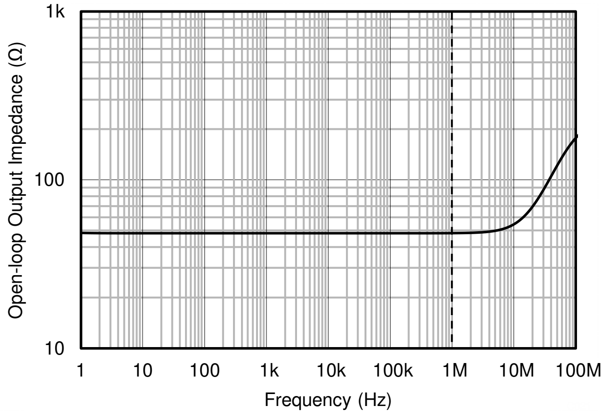
V_S = ±18 V

Figure 25. Open-Loop Gain vs Output Voltage Swing to Supply



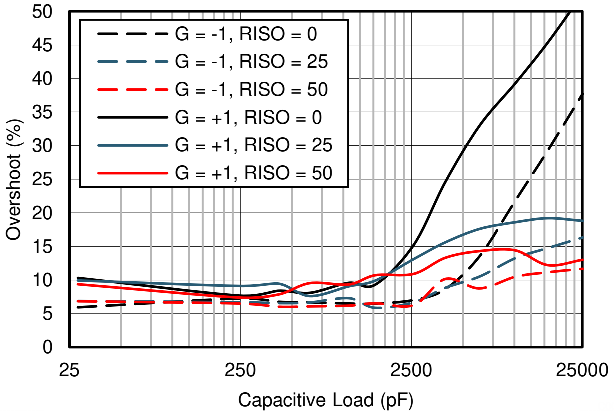
V_S = ±2.25 V

Figure 26. Open-Loop Gain vs Output Voltage Swing to Supply



Unity-gain bandwidth = 1 MHz

Figure 27. Open-Loop Output Impedance vs Frequency



10-mV step

Figure 28. Small-Signal Overshoot vs Capacitive Load

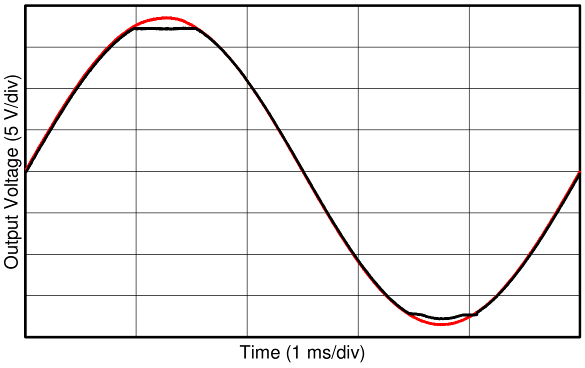


Figure 29. No Phase Reversal

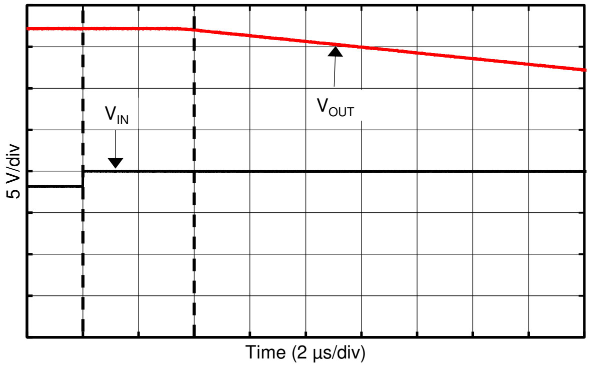


Figure 30. Positive Overload Recovery

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

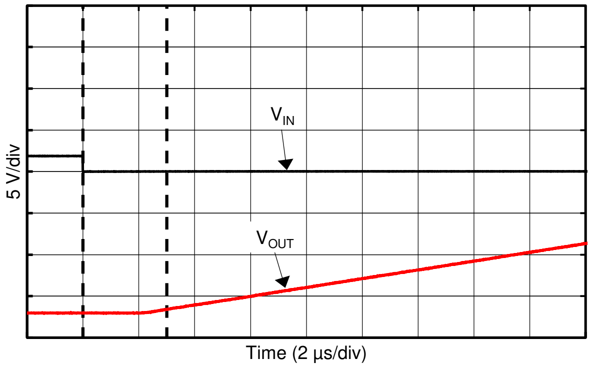
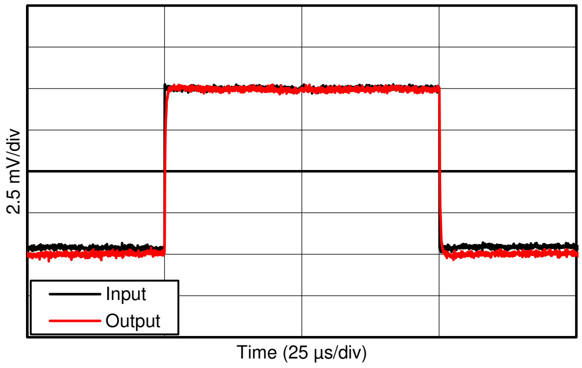
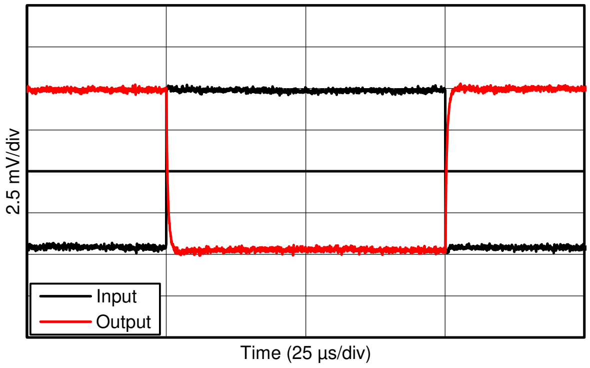


Figure 31. Negative Overload Recovery



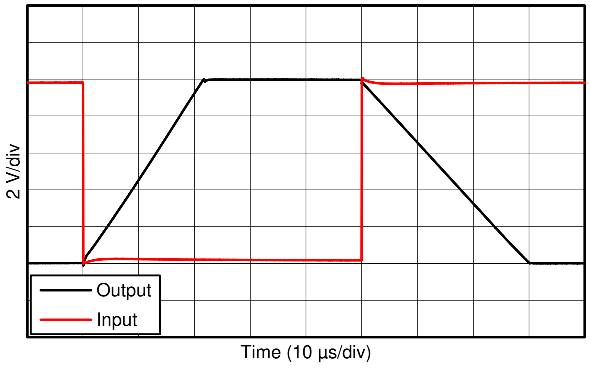
G = +1

Figure 32. Small-Signal Step Response (10-mV Step)



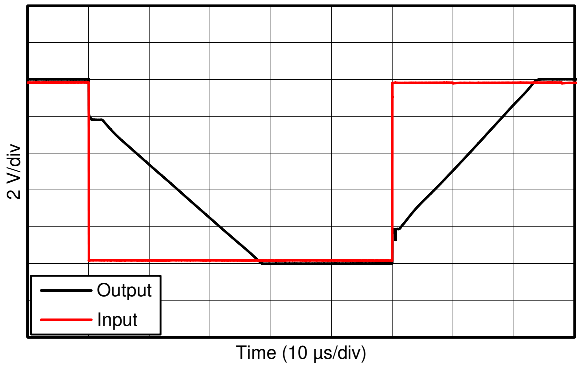
G = –1

Figure 33. Small-Signal Step Response (10-mV Step)



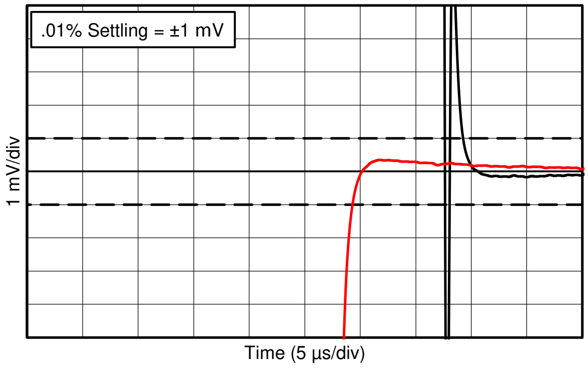
G = –1 10-V step

Figure 34. Large-Signal Step Response



G = +1 10-V step

Figure 35. Large-Signal Step Response



10-V step

Figure 36. Settling Time

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

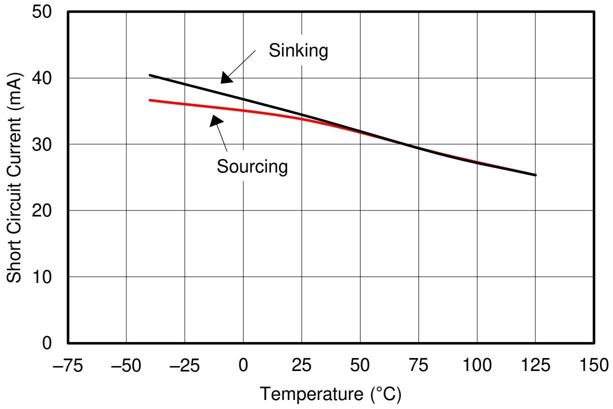


Figure 37. Short-Circuit Current vs Temperature

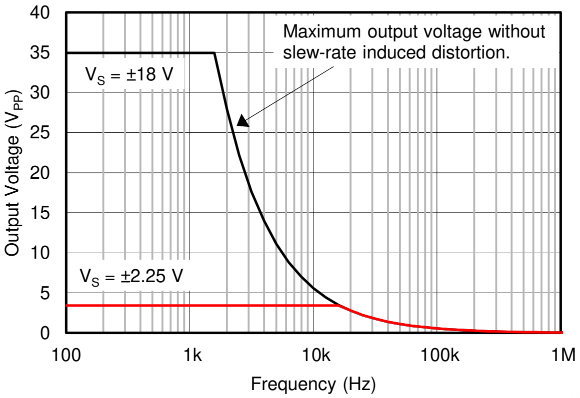
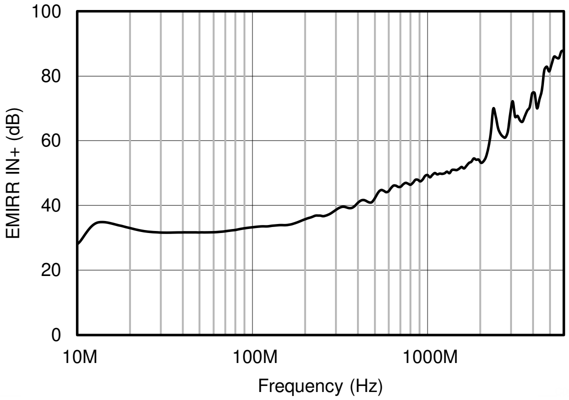


Figure 38. Maximum Output Voltage Amplitude vs Frequency



P_{RF} = –10 dBm

Figure 39. EMIRR vs Frequency

7 Detailed Description

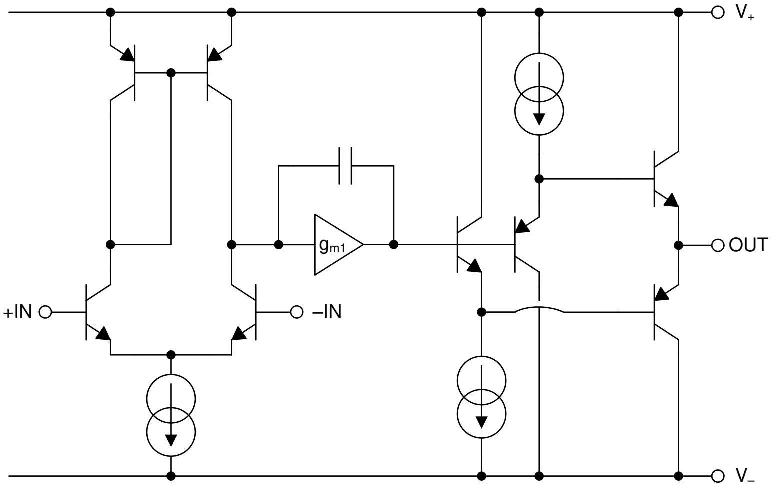
7.1 Overview

The OPA202, OPA2202, and OPA4202 (OPAx202) family of devices is a series of low-power, super-beta, bipolar junction transistor (super-β BJT), input amplifiers that features superior drift performance and low input bias current. The low output impedance and heavy capacitive load drive abilities allow designers to interface to modern, fast-acquisition, precision analog-to-digital converters (ADCs) and buffer precision voltage references and drive power supply decoupling capacitors. The OPAx202 achieve a 1-MHz gain-bandwidth product and a 0.35-V/µs slew rate, and consumes only 580 µA (typical) of quiescent current, making the devices a great choice for low-power applications. These devices operate on a single 4.5-V to 36-V supply, or dual ±2.25-V to ±18-V supplies.

All versions are fully specified from –40°C to +105°C for use in the most challenging environments. The single-channel OPA202 is available in 8-pin SOIC, 8-pin VSSOP, and 5-pin SOT-23 packages. The dual-channel OPA2202 is available in an 8-pin VSSOP package. The quad-channel OPA4202 is available in 14-pin SOIC and TSSOP packages.

The *Functional Block Diagram* shows the simplified diagram of the OPAx202.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Capacitive Load and Stability

The dynamic characteristics of the OPAx202 are optimized for commonly encountered gains, loads, and operating conditions. The OPAx202 feature a patented output stage capable of driving large capacitive loads. In a unity-gain configuration, the series is capable of directly driving to 25 nF of pure capacitive load. Increase the gain to enhance the ability of the devices to drive greater capacitive loads. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier, and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. Add a small resistor (R_{OUT} equal to 50 Ω, for example) in series with the output to achieve isolation. Figure 40 shows the effects on small-signal overshoot for several capacitive loads and combinations of isolation resistance. See the *Feedback Plots Define Op Amp AC Performance* application bulletin for details of analysis techniques and application circuits, available for download from the www.TI.com. By using isolation resistors, driving capacitive loads of 100 nF and beyond is possible.

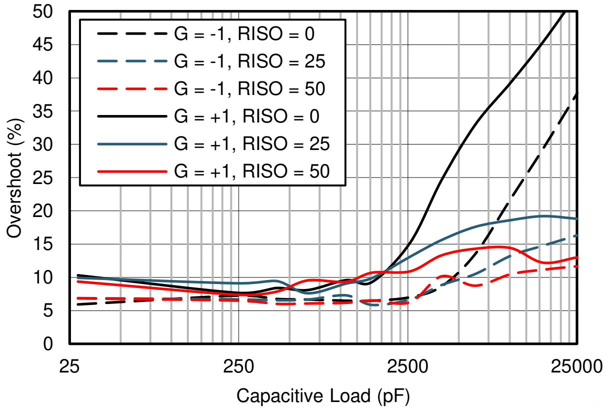


Figure 40. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step)

Feature Description (continued)

For additional drive capability in unity-gain configurations, insert a small (10 Ω to 20 Ω) resistor (R_{ISO}) in series with the output to improve capacitive load drive, as shown in Figure 41. This resistor reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, which introduces a gain error at the output and reduces the output swing. The error is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx202 a great choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 41 uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. Table 2 lists the results using the OPAx202. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIPD128 details complete design goals, simulation, and test results.

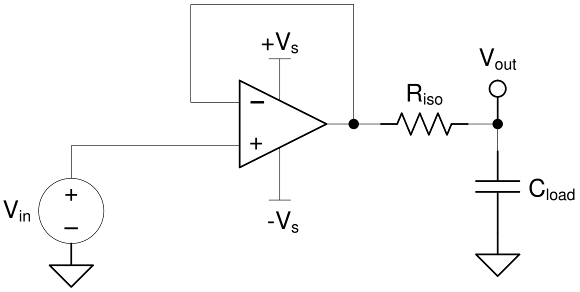


Figure 41. Extending Capacitive Load Drive With the OPAx202

Table 2. OPAx202 Capacitive Load Drive Solution Using Isolation Resistor Measured Results

PARAMETER	MEASURED OVERSHOOT (%)					
	INVERTING CONFIGURATION			NONINVERTING CONFIGURATION		
C_{LOAD} (pF)	R_{ISO} = 0 Ω	R_{ISO} = 25 Ω	R_{ISO} = 50 Ω	R_{ISO} = 0 Ω	R_{ISO} = 25 Ω	R_{ISO} = 50 Ω
31	8.6	6.6	6.6	9.3	9	9.4
251	6.7	6.4	6.7	8.9	8.9	8.9
421	6.4	6.3	6.6	8.8	8.8	8.7
641	6.7	6.3	6.5	8.1	8.8	8.5
1079	6.1	6.1	6.4	8.6	8.7	9.8
1539	6.4	6.3	6.1	8.9	10.3	10.1
2579	6.1	6.3	6.9	16	13.3	12
3949	8.1	7.9	8.3	25	16	14.1
6269	14.9	10.8	9.9	33.1	18.1	14.5
10139	21.8	13.5	10.8	40.2	19.1	15.4
15729	29.4	15.2	11.6	46.2	19.6	14.5
25069	37	16.5	12.3	52.6	19.2	13.9

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, see TIPD128, *Capacitive Load Drive Solution Using an Isolation Resistor* verified reference design.

7.3.2 Output Current Limit

The output current of the OPAx202 is limited by internal circuitry to ±35 mA (sinking or sourcing) to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as Figure 37 shows.

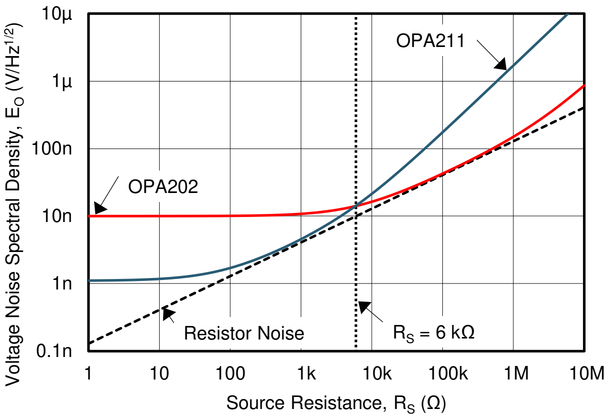
7.3.3 Noise Performance

Figure 42 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPAx202 and OPA211 are shown with total circuit noise calculated. The op amp itself contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise dominates. The OPAx202 have both low voltage noise and low current noise because of the super-beta bipolar junction transistor (super-β BJT) input of the op amp. As a result, the current noise contribution of the OPAx202 is negligible for most practical source impedances, which makes the series the better choice for applications with high source impedance.

The equation in Figure 42 shows the calculation of the total circuit noise with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in kelvins (K)

For more details on calculating noise, see *Basic Noise Calculations*.



NOTE: For source resistances (R_S) greater than 6 kΩ, the OPAx202 is a lower-noise option compared to the OPA211, as shown in Figure 42.

Figure 42. Noise Performance of the OPAx202 vs the OPA211 in a Unity-Gain Buffer Configuration

7.3.4 Phase-Reversal Protection

The OPAx202 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPAx202 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 29).

7.3.5 Thermal Protection

The OPAx202 family of op amps is capable of driving 2-kΩ loads with power-supply voltages of up to ±18 V across the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 1.1 kΩ at a supply voltage of 36 V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used as long as the output current does not exceed 35 mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPAx202 devices improves heat dissipation. Printed-circuit-board (PCB) layout helps reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heat sink. An increase in temperature is further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to midsupply, the typical short-circuit current of 35 mA leads to an internal power dissipation of over 600 mW at a supply of ±18 V.

To prevent excessive heating, the OPAx202 have an internal thermal shutdown circuit that shuts down the device if the die temperature exceeds approximately 135°C. When this thermal shutdown circuit activates, a built-in hysteresis of 10°C makes sure that the die temperature drops to approximately 125°C before the device switches on again. Additional consideration must be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type.

7.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event. See Figure 43 for an illustration of the ESD circuits contained in the OPAx202 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as the pulse discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to protect the core from damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx202 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (such as the one Figure 43 shows), the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 43 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

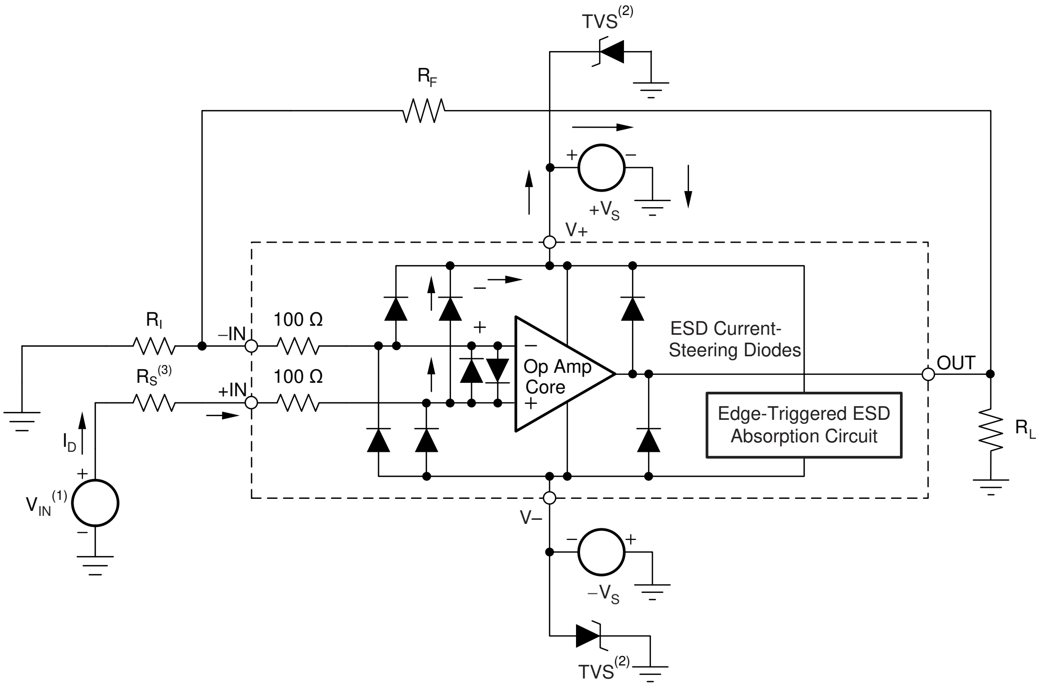
If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V.

It depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 43. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin rises above the safe operating supply voltage level.



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(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value is approximately 5 kΩ in overvoltage conditions.

Figure 43. Equivalent Internal ESD Circuitry in a Typical Application Circuit

7.3.7 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR is performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier may result in adverse effects, as the amplifier does not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected DC offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces. shows the effect of conducted EMI to the power supplies on the input offset voltage of OPAx202.

The EMIRR IN+ of the OPAx202 is plotted versus frequency, as shown in Figure 44. If available, any dual and quad op-amp device versions have similar EMIRR IN+ performance. The OPAx202 unity-gain bandwidth is 1 MHz. EMIRR performance less than this frequency denotes interfering signals that fall within the op-amp bandwidth.

See the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

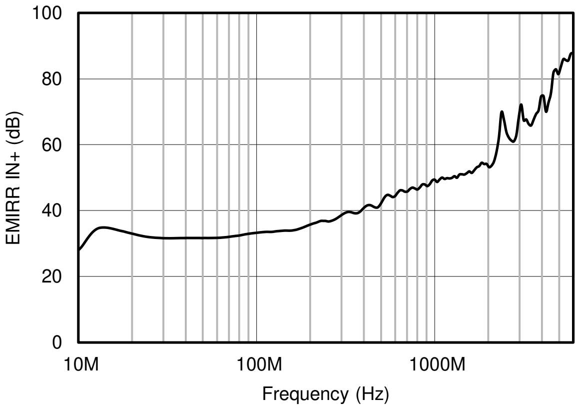


Figure 44. OPAx202 EMIRR IN+

Table 3 lists the EMIRR IN+ values for the OPAx202 at particular frequencies commonly encountered in real-world applications. Table 3 lists applications that may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 3. OPAx202 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	41 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	47 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	54 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	67 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	67 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	81 dB

7.3.8 EMIRR +IN Test Configuration

Figure 45 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input pin using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

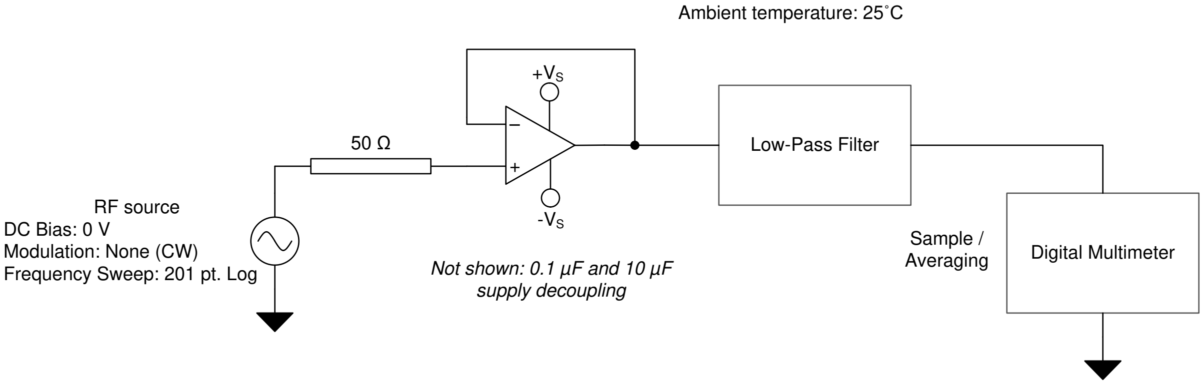


Figure 45. EMIRR +IN Test Configuration

7.4 Device Functional Modes

The OPAx202 have a single functional mode and are operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx202 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA202, OPA2202, and OPA4202 (OPAx202) are unity-gain stable operational amplifiers with low noise, low input bias current, and low input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Designers can use the low output impedance and heavy capacitive load drive abilities to interface to modern, fast-acquisition, precision analog-to-digital converters (ADCs) and buffer precision voltage references and drive power supply decoupling capacitors.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources dominates in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

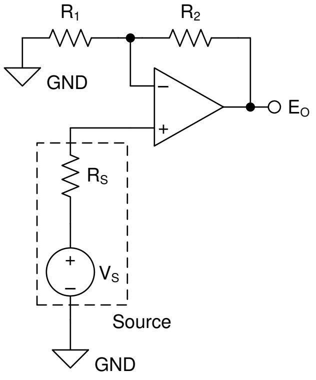
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 42 shows this function. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 46 shows noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. Typically, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx202 means that the current noise contribution is neglected.

The feedback resistor values are typically selected to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

Application Information (continued)

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1+\frac{R_2}{R_1}\right)\cdot\sqrt{(e_S)^2+(e_N)^2+\left(e_{R_1\|R_2}\right)^2+(i_N\cdot R_S)^2+\left(i_N\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]\right)^2}\quad [V_{RMS}]$$

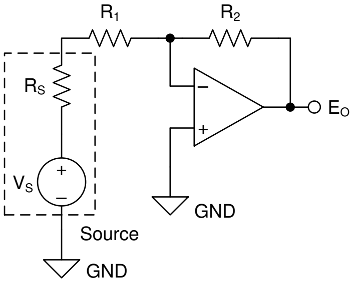
$$(2)\quad e_S=\sqrt{4\cdot k_B\cdot T(K)\cdot R_S}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of R_S

$$(3)\quad e_{R_1\|R_2}=\sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $R_1 \| R_2$

$$(4)\quad k_B=1.38065\cdot 10^{-23}\quad\left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(5)\quad T(K)=237.15+T(°C)\quad [K]$$ Temperature in kelvins

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O=\left(1+\frac{R_2}{R_S+R_1}\right)\cdot\sqrt{(e_N)^2+\left(e_{R_1+R_S\|R_2}\right)^2+\left(i_N\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]\right)^2}\quad [V_{RMS}]$$

$$(7)\quad e_{R_1+R_S\|R_2}=\sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $(R_1 + R_S) \| R_2$

$$(8)\quad k_B=1.38065\cdot 10^{-23}\quad\left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(9)\quad T(K)=237.15+T(°C)\quad [K]$$ Temperature in kelvins

(1) e_N = the voltage noise of the amplifier = 9 nV/√Hz at 1 kHz.
(2) i_N = the current noise of the amplifier = 76 fA/√Hz at 1 kHz.
(3) For additional resources on noise calculations, visit *TI's Precision Labs*.

Figure 46. Noise Calculation in Gain Configurations

8.2 Typical Application

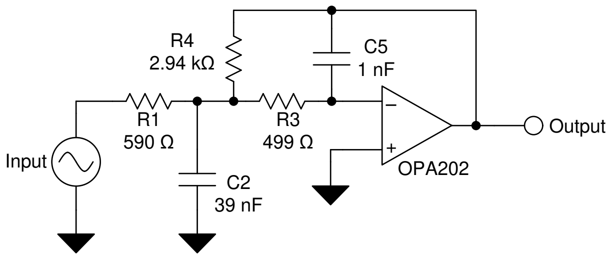


Figure 47. 25-kHz, Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are used in signal processing applications to reduce noise and prevent aliasing. The OPAx202 devices are is designed to construct high-speed, high-precision active filters. Figure 47 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 47. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

Typical Application (continued)

8.2.3 Application Curve

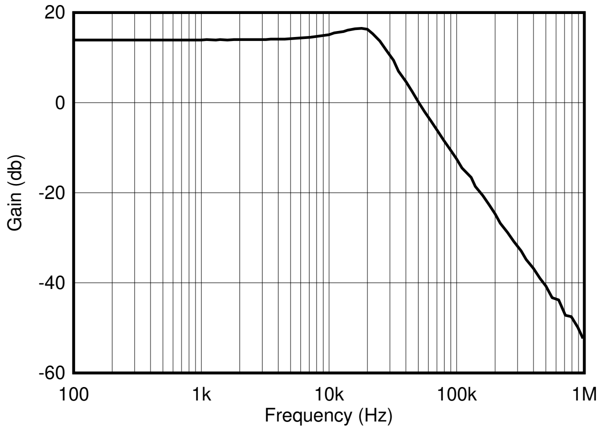


Figure 48. OPAx202 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

9 Power Supply Recommendations

The OPAx202 are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics*.

CAUTION

Supply voltages greater than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *The PCB is a component of op amp design.*
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in Figure 49, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

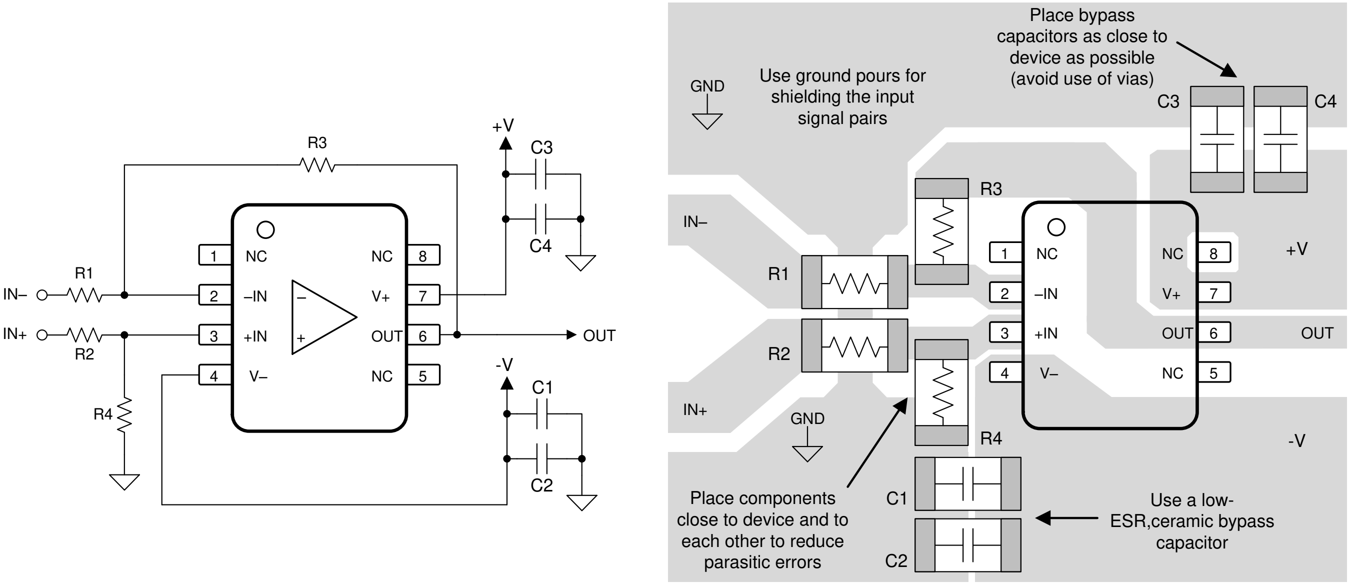


Figure 49. Operational Amplifier Board Layout for Difference Amplifier Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

11.1.1.3 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *The PCB is a component of op amp design*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters*
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers*
- Texas Instruments, *Tuning in Amplifiers*
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes*
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance*
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

11.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA202	Click here	Click here	Click here	Click here	Click here
OPA2202	Click here	Click here	Click here	Click here	Click here
OPA4202	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA202ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 120	OPA202	Samples
OPA202IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 120	1T72	Samples
OPA202IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 120	1T72	Samples
OPA202IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	1T2Q	Samples
OPA202IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	1T2Q	Samples
OPA202IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 120	OPA202	Samples
OPA2202ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OP2202	Samples
OPA2202IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 120	1XDQ	Samples
OPA2202IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 120	1XDQ	Samples
OPA2202IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	OP2202	Samples
OPA4202ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4202	Samples
OPA4202IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4202	Samples
OPA4202IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4202	Samples
OPA4202IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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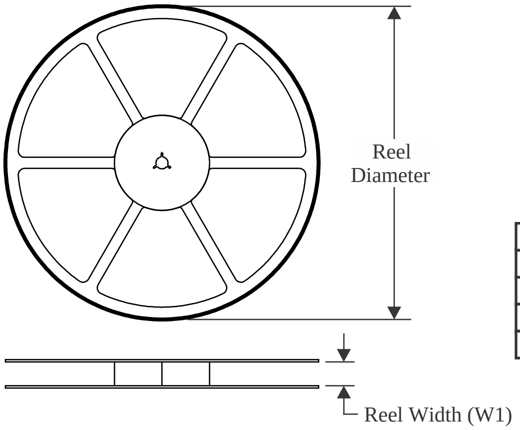
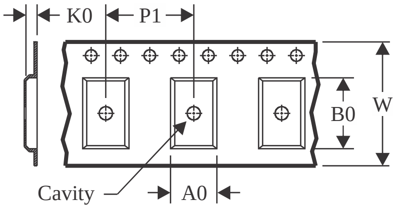
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

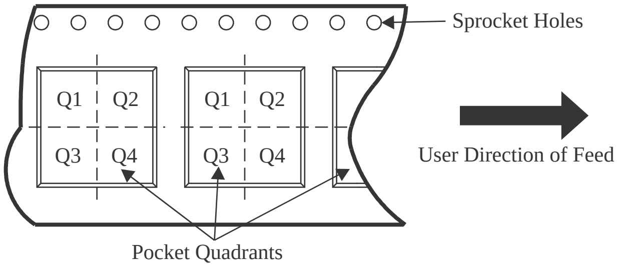


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

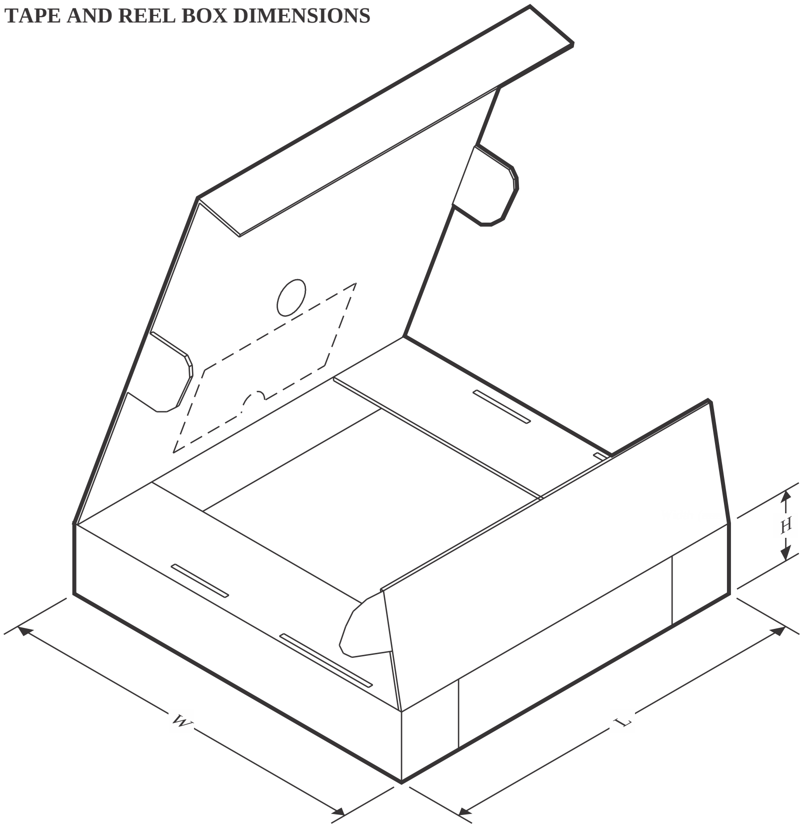
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA202IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA202IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA202IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA202IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA202IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2202IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2202IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2202IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4202IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4202IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

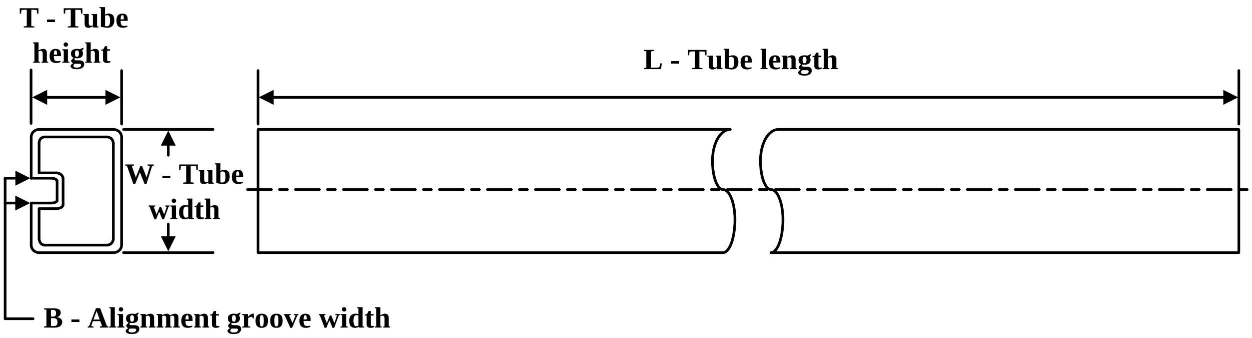
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

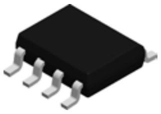
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA202IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA202IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA202IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA202IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA202IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2202IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2202IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2202IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4202IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4202IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA202ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2202ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4202ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4202IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

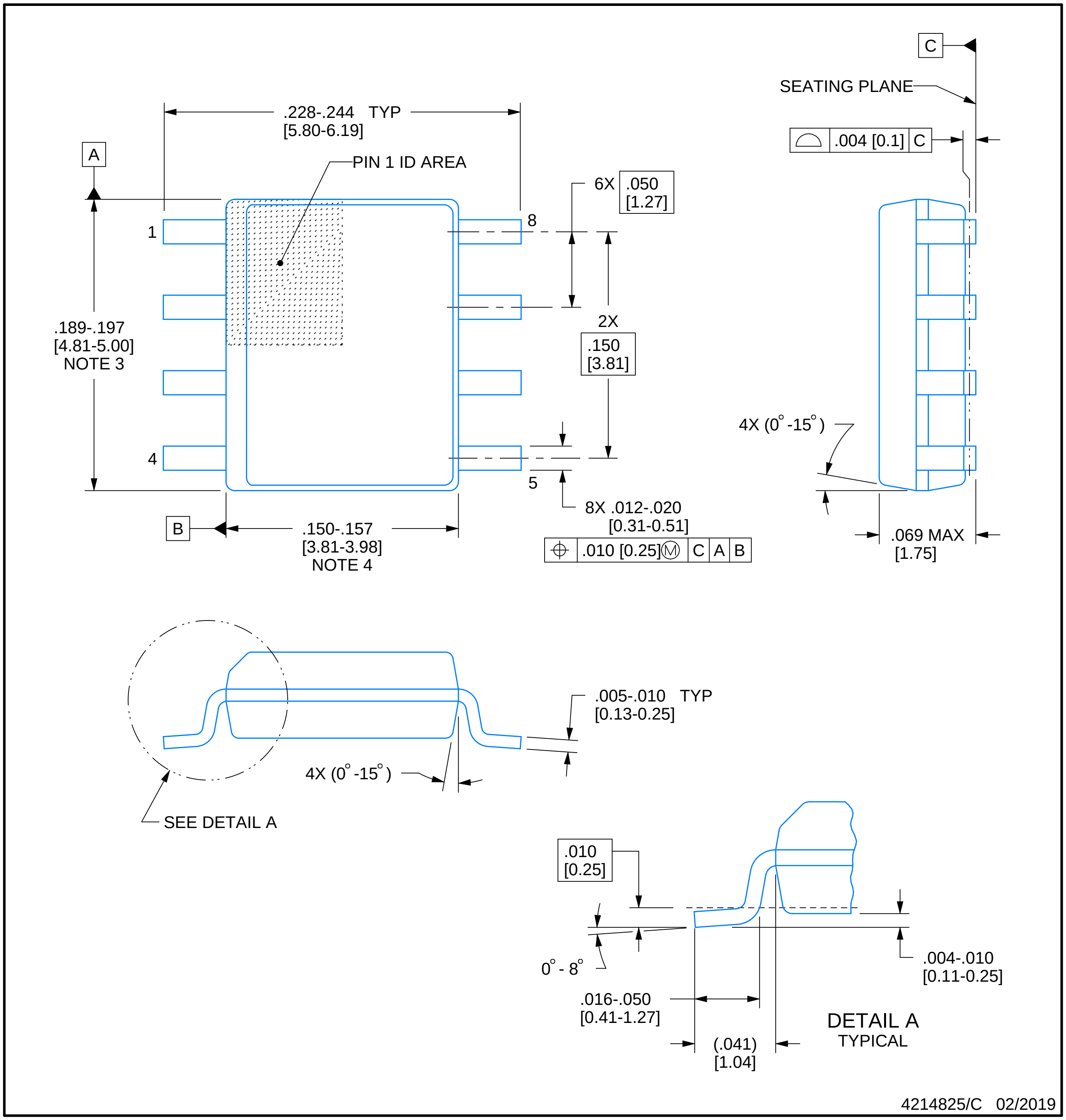


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

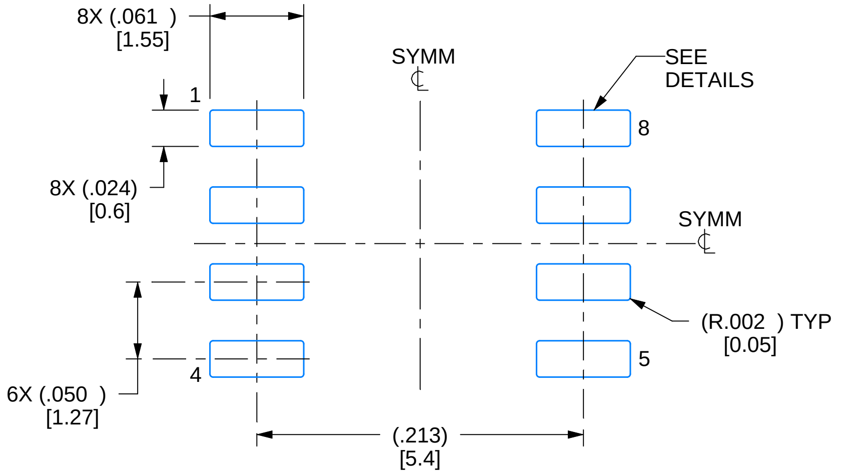
SMALL OUTLINE INTEGRATED CIRCUIT



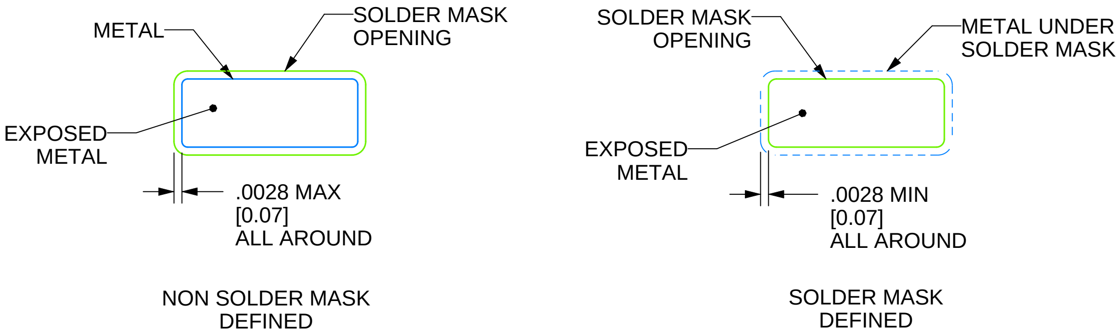
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



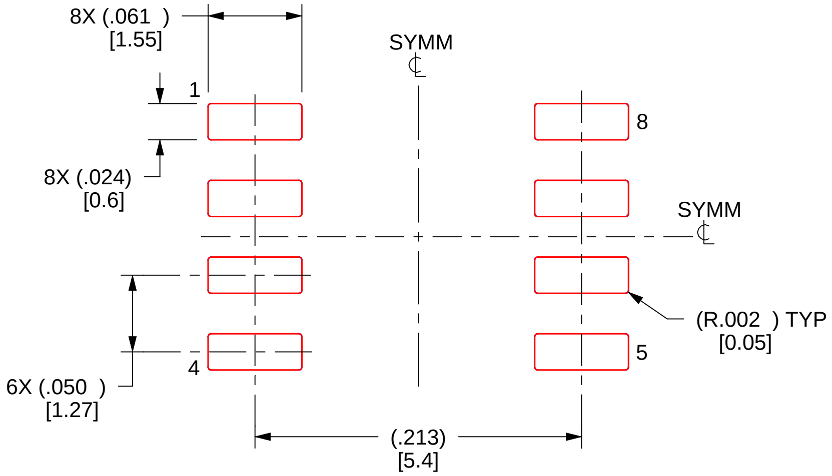
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

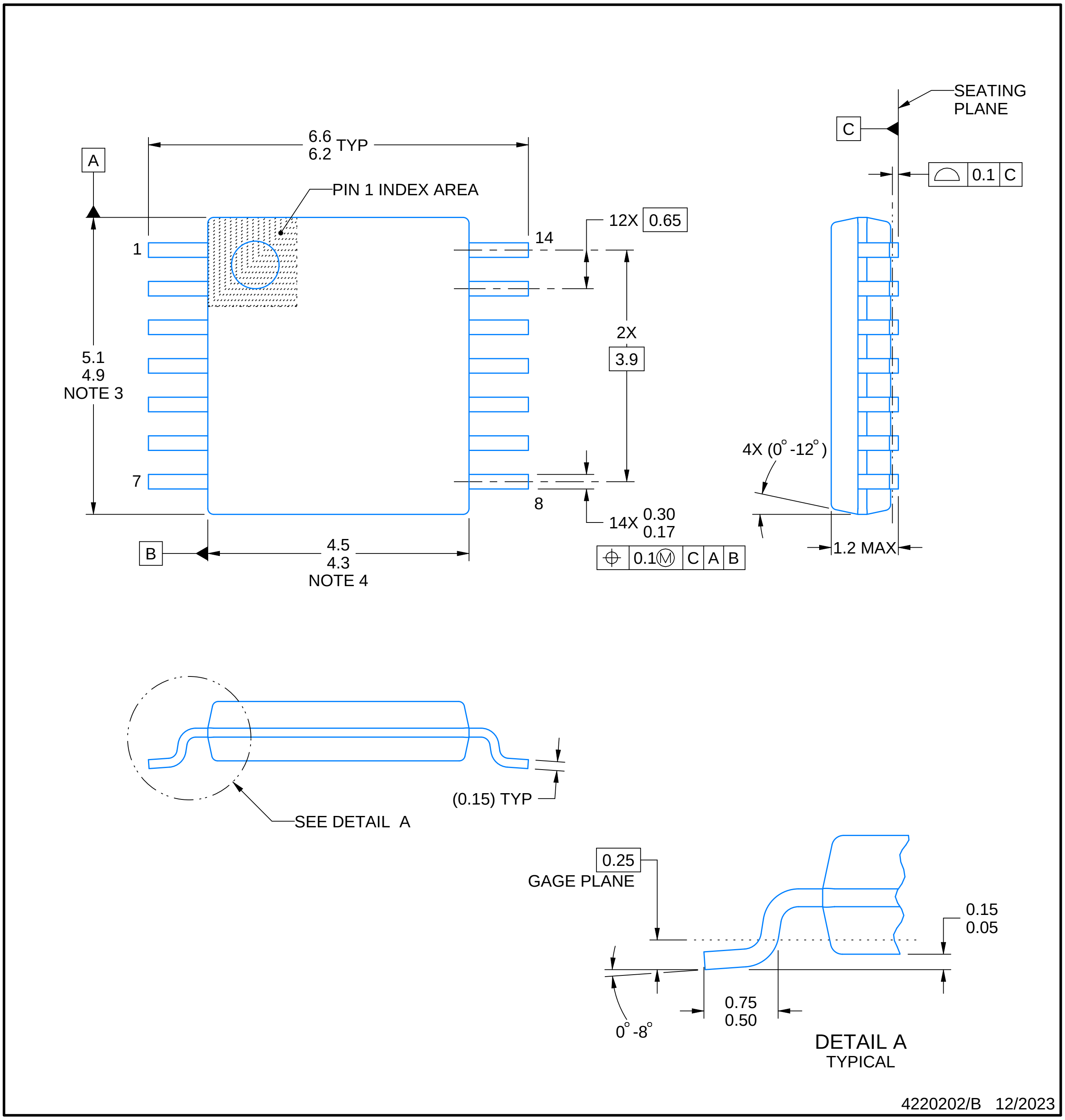
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

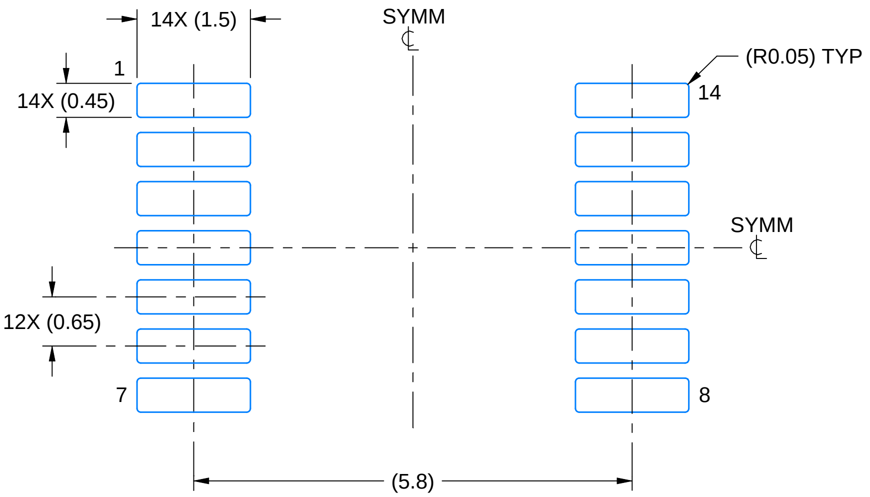
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

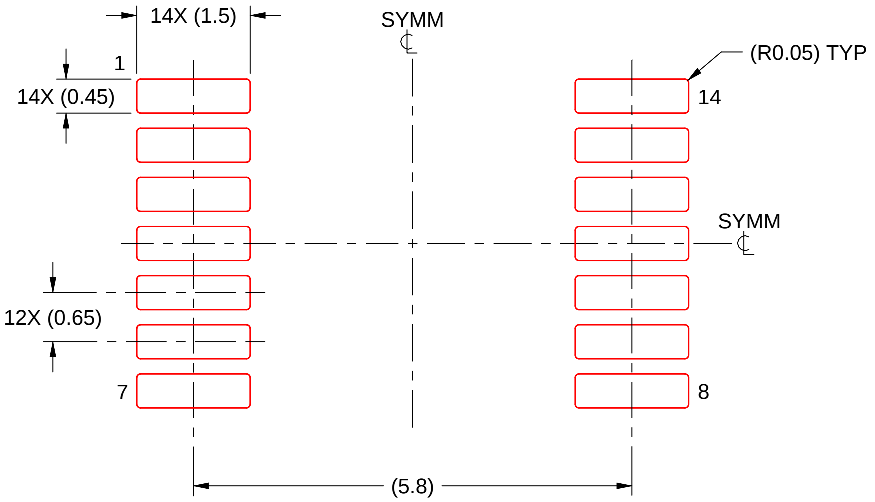
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

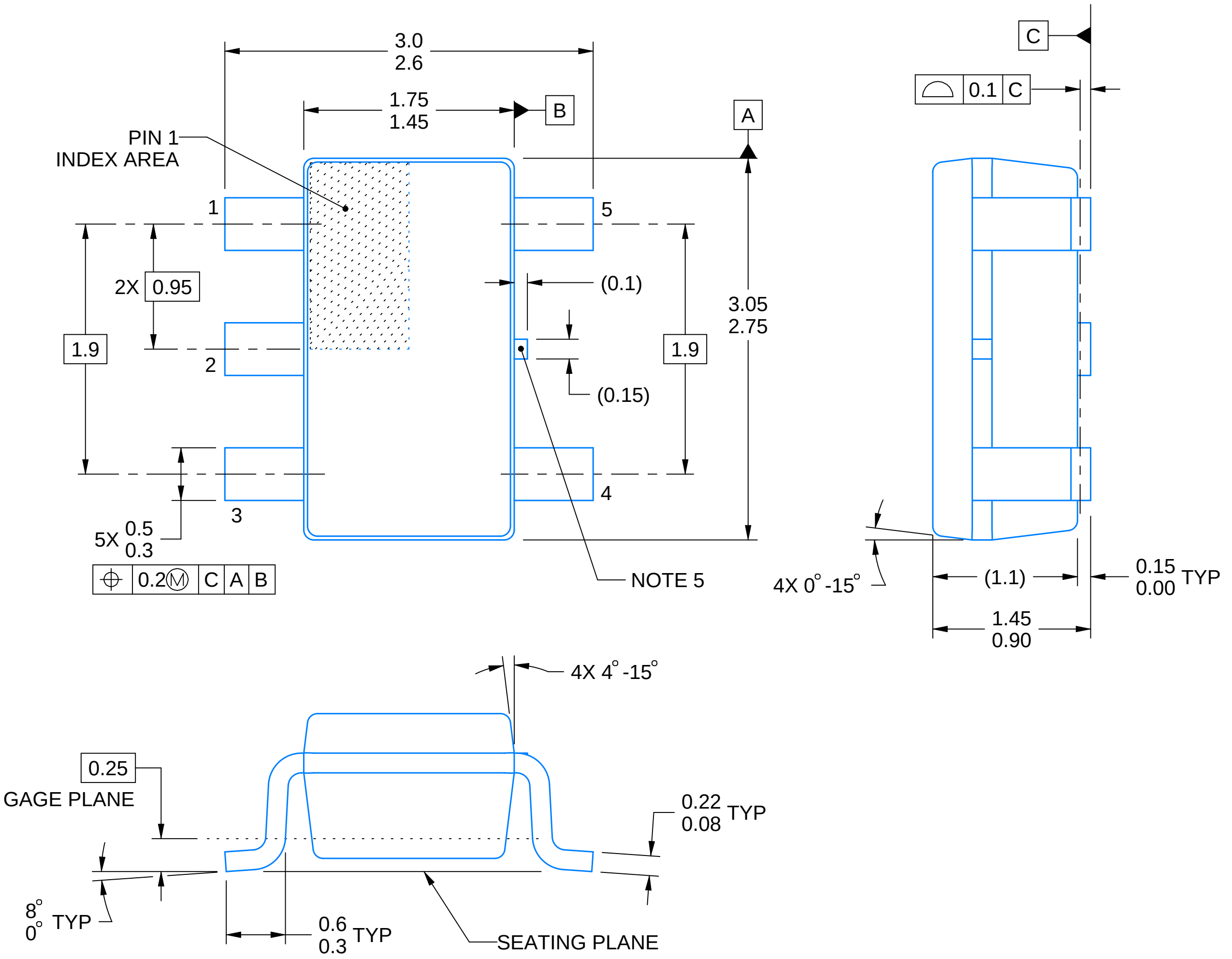
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

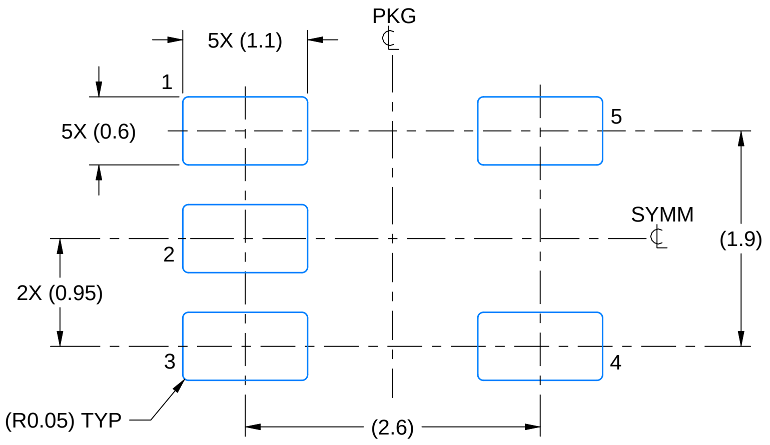
SMALL OUTLINE TRANSISTOR



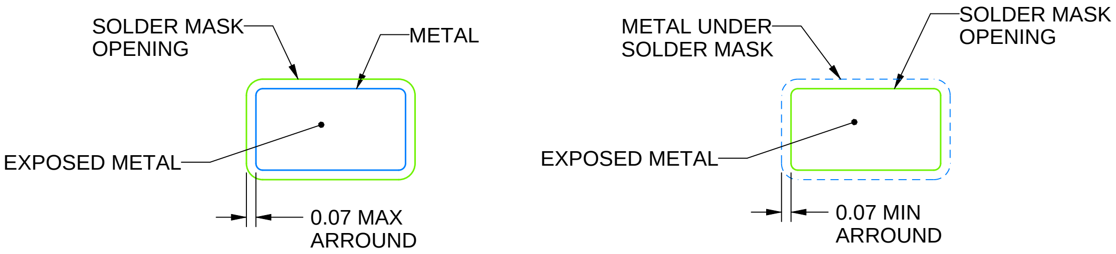
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

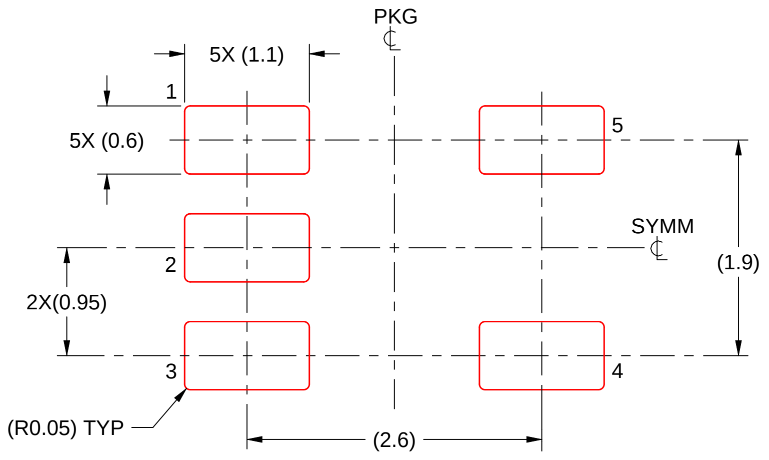
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

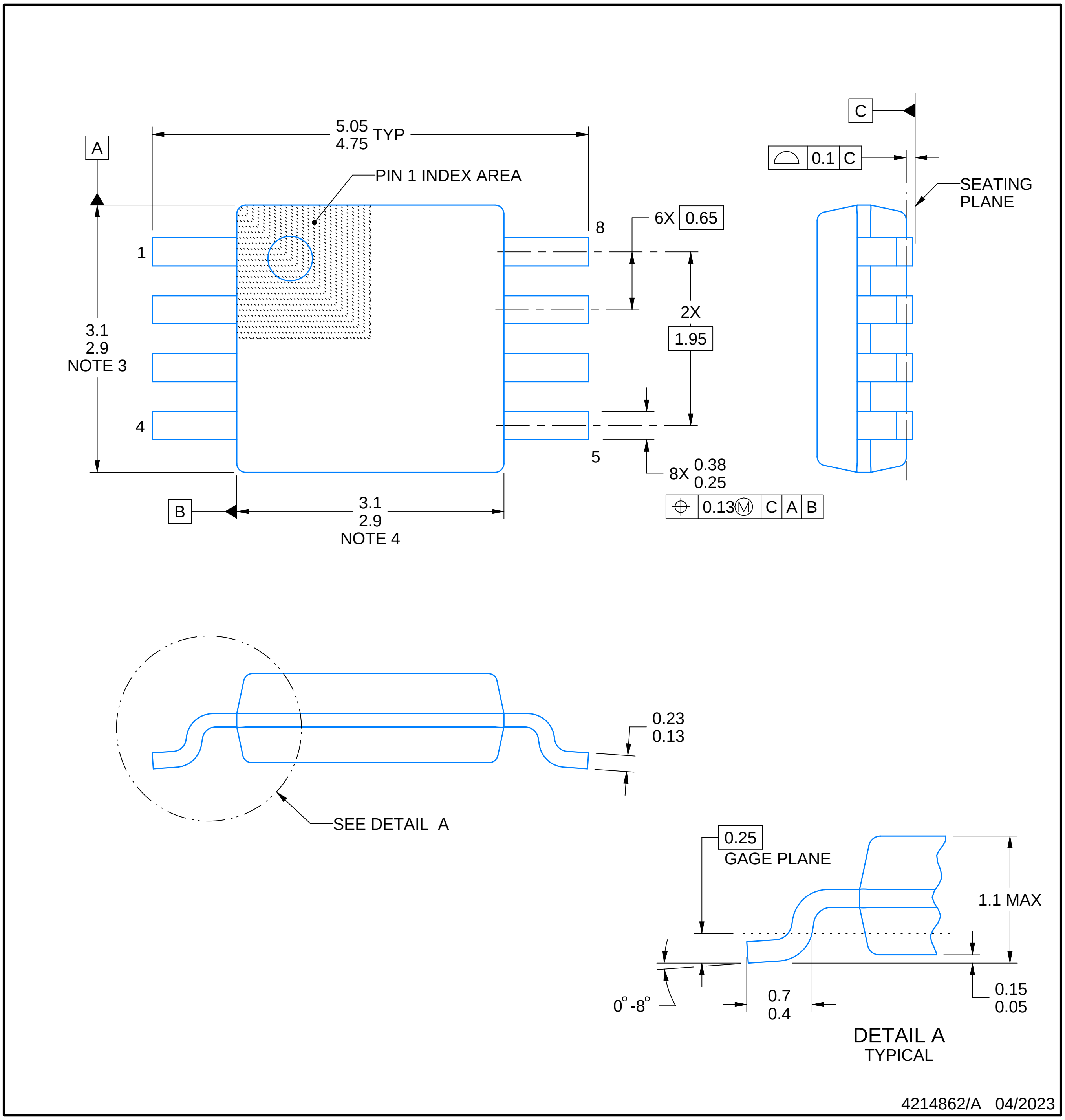


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

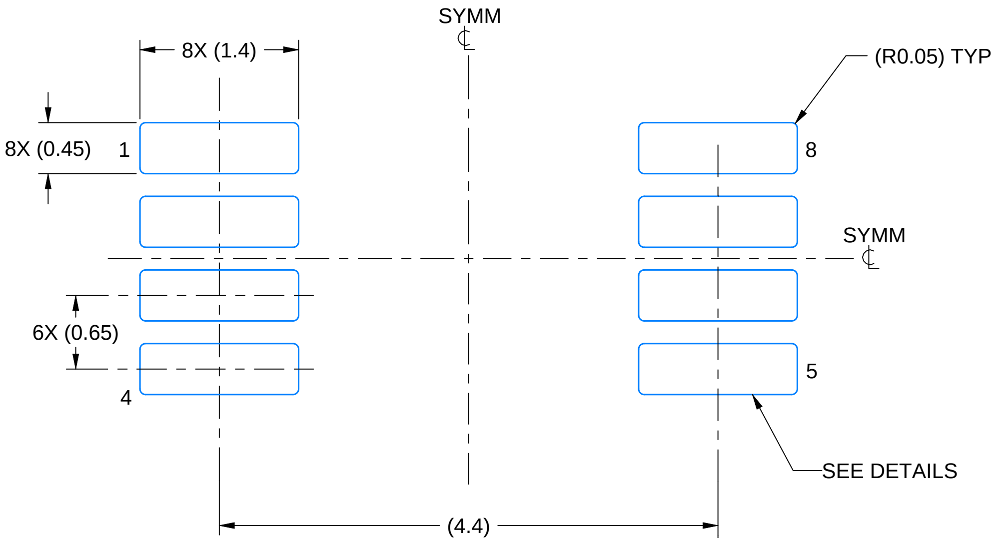
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

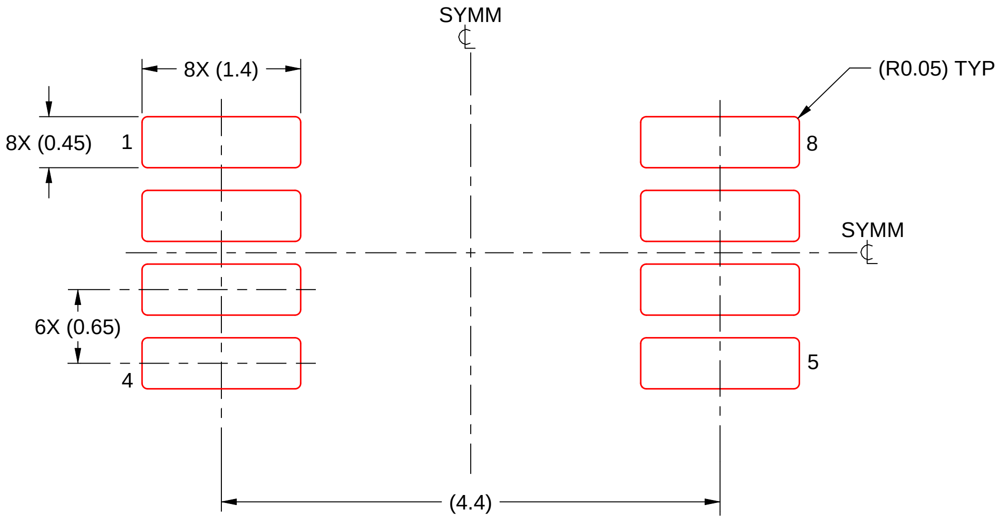
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

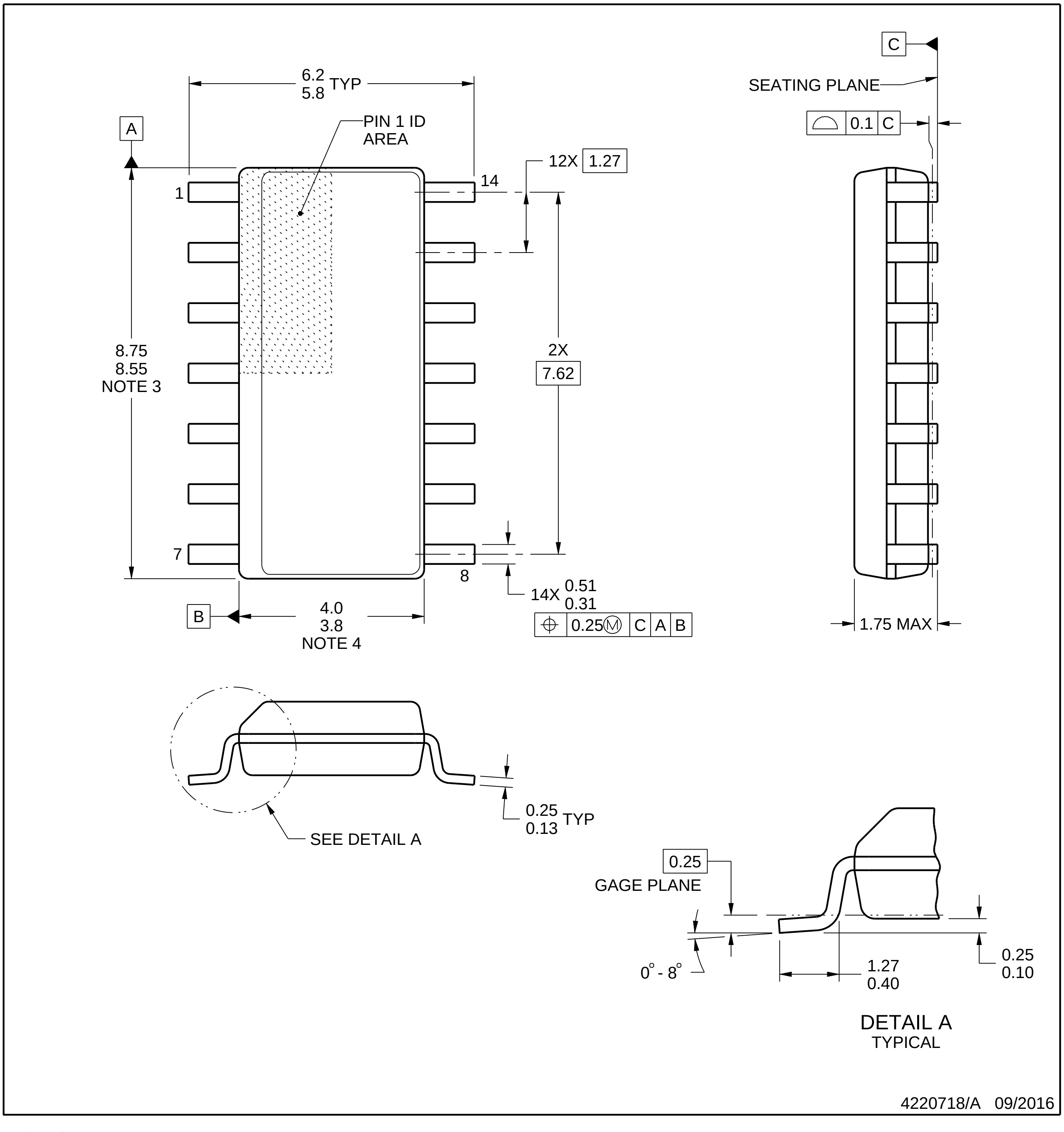
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A

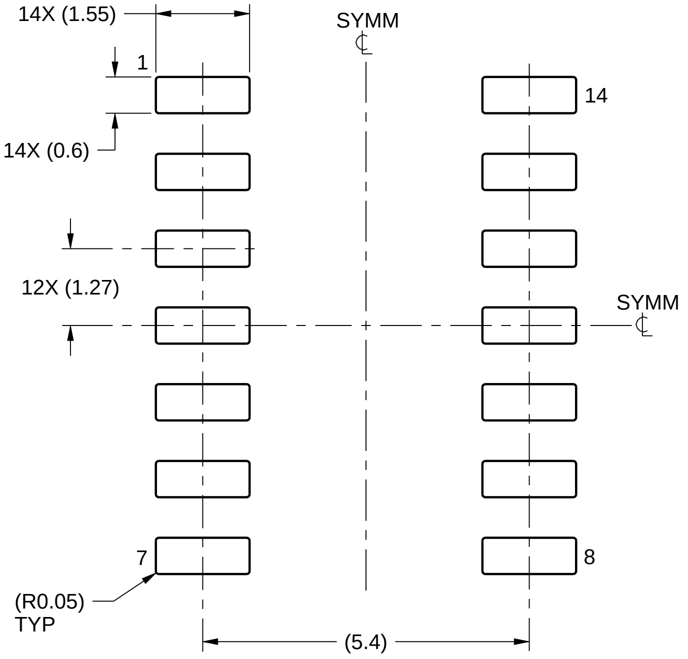
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

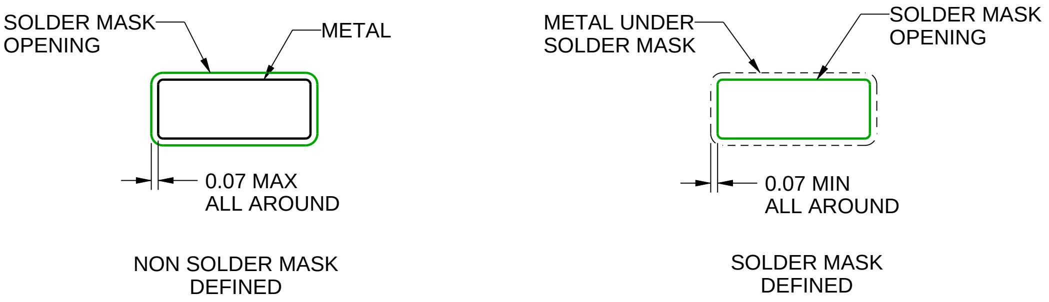


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

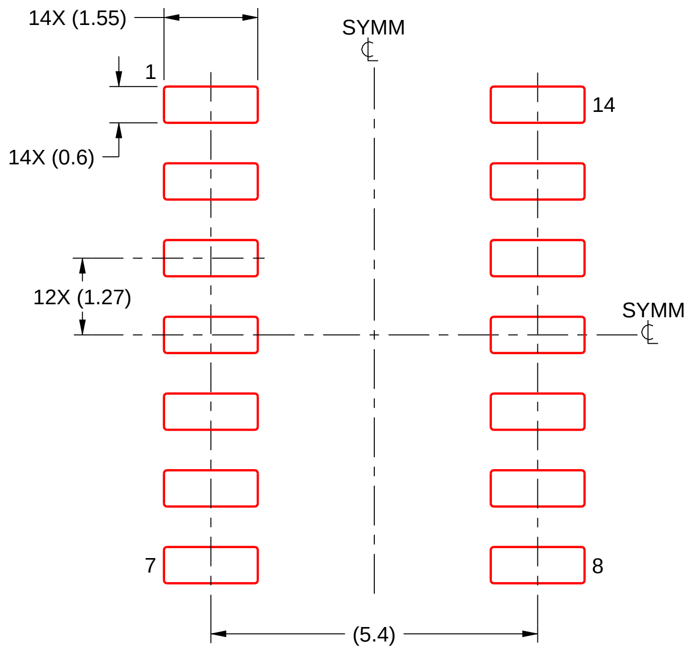


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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