OPA166x Low-Power, Low-Noise-and-Distortion, Bipolar-Input SoundPlus™ Audio Operational Amplifiers

Texas Instruments
Burr-Brown Audio

1 Features

- Low noise: 3.3nV/√Hz at 1kHz
- Low distortion: 0.00006% at 1kHz
- Low quiescent current:
  1.5mA per channel
- Slew rate: 17V/μs
- Wide gain bandwidth: 22MHz (G = +1)
- Unity gain stable
- Rail-to-rail output
- Wide supply range:
  ±1.5V to ±18V or 3V to 36V
- Dual and quad versions available
- Small package sizes:
  Dual: SOIC-8 and VSSOP-8
  Quad: SOIC-14 and TSSOP-14

2 Applications

- USB and firewire audio systems
- Analog and digital mixers
- Portable recording systems
- Audio effects processors
- High-end A/V receivers
- High-end DVD and Blu-Ray™ players
- High-end car audio

3 Description

The dual OPA1662 and quad OPA1664 (OPA166x) series of bipolar-input SoundPlus™ audio operational amplifiers achieve a low 3.3nV/√Hz noise density with an ultra-low distortion of 0.00006% at 1kHz. The OPA166x series of op amps offer rail-to-rail output swing to within 600mV with 2kΩ load, which increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±30mA.

These devices operate over a very wide supply range of ±1.5V to ±18V, or 3V to 36V, on only 1.5mA of supply current per channel. The OPA166x op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

These devices also feature completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

The OPA166x are specified from –40°C to +85°C.

Device Information

PRODUCT	CHANNEL COUNT	PACKAGE(1)
OPA1662	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
OPA1664	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see Section 9.

Table of Contents

4 Pin Configurations

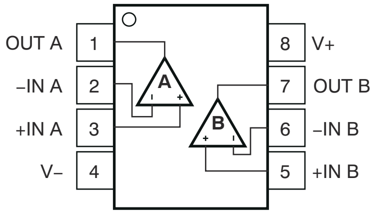


Figure 4-1. OPA1662: D and DGK Packages, SOIC-8 and VSSOP-8 (Top View)

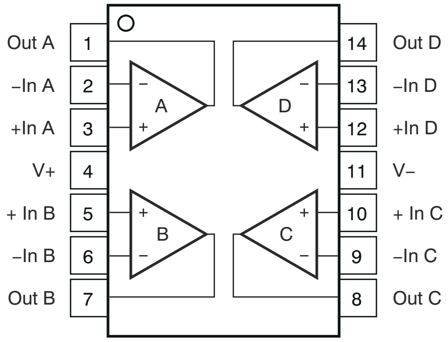


Figure 4-2. OPA1664: D and PW Packages, SOIC-14 and TSSOP-14 (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		40	V
	Input voltage	(V–) – 0.5	(V+) + 0.5	V
	Input current (all pins except power-supply pins)		±10	mA
	Output short-circuit(2)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	
		Machine model (MM)	200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	±1.5		±18	V
T_A	Ambient temperature	–40		85	°C

5.4 Thermal Information: OPA1662

THERMAL METRIC(1)		OPA1662 D (SOIC) 8 PINS	OPA1662 DGK (VSSOP) 8 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156.3	225.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	85.5	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	110.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.8	14.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.3	108.5	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA1664

THERMAL METRIC(1)		OPA1664 D (SOIC) 14 PINS	OPA1664 PW (TSSOP) 14 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.6	125.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	37.0	45.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.9	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.7	5.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.6	56.7	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics: V_S = ±15V

at T_A = 25°C and R_L = 2kΩ, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = +1, f = 1kHz, V_O = $3V_{RMS}$			0.00006		%
					–124		dB
IMD	Intermodulation distortion	G = +1, V_O = $3V_{RMS}$	SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)		0.00004		%
					–128		dB
			DIM 30 (3kHz square wave and 15kHz sine wave)		0.00004		%
					–128		dB
			CCIF twin-tone (19kHz and 20kHz)		0.00004		%
					–128		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = +1			22		MHz
SR	Slew rate	G = –1			17		V/μs
	Full power bandwidth(1)	V_O = $1V_P$			2.7		MHz
	Overload recovery time	G = –10			1		μs
	Channel separation (dual and quad)	f = 1kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20Hz to 20kHz			2.8		μV_{PP}
	Input voltage noise density	f = 1kHz			3.3		$nV/\sqrt{Hz}$
		f = 100Hz			5		
I_n	Input current noise density	f = 1kHz			1		$pA/\sqrt{Hz}$
		f = 100Hz			2		
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±1.5V to ±18V			±0.5	±1.5	mV
		V_S = ±1.5V to ±18V, T_A = –40°C to +85°C(2)			2	8	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5V to ±18V			1	3	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0V			600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0V			±25	±100	nA
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio			106	114		dB
INPUT IMPEDANCE							
	Differential				170 || 2		kΩ || pF
	Common-mode				600 || 2.5		MΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 2kΩ		106	114		dB
OUTPUT							
V_{OUT}	Output voltage	R_L = 2kΩ		(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current				See Typical Characteristics		mA
Z_O	Open-loop output impedance				See Typical Characteristics		Ω
I_{SC}	Short-circuit current(3)				±50		mA
C_{LOAD}	Capacitive load drive				200		pF
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_{OUT} = 0A			1.5	1.8	mA
			T_A = –40°C to +85°C(2)			2	

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

5.7 Electrical Characteristics: V_S = 5V

at T_A = 25°C and R_L = 2kΩ, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = +1, f = 1kHz, V_O = 3V_{RMS}			0.0001		%
					–120		dB
IMD	Intermodulation distortion	G = +1, V_O = 3V_{RMS}	SMPTE/DIN two-tone, 4:1 (60Hz and 7kHz)		0.00004		%
					–128		dB
			DIM 30 (3kHz square wave and 15kHz sine wave)		0.00004		%
					–128		dB
			CCIF twin-tone (19kHz and 20kHz)		0.00004		%
					–128		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = +1			20		MHz
SR	Slew rate	G = –1			13		V/µs
	Full power bandwidth(1)	V_O = 1V_P			2		MHz
	Overload recovery time	G = –10			1		µs
	Channel separation (dual and quad)	f = 1kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20Hz to 20kHz			3.3		$µV_{PP}$
	Input voltage noise density	f = 1kHz			3.3		nV/√Hz
		f = 100Hz			5		
I_n	Input current noise density	f = 1kHz			1		pA/√Hz
		f = 100Hz			2		
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±1.5V to ±18V			±0.5	±1.5	mV
		V_S = ±1.5V to ±18V, T_A = –40°C to +85°C(2)			2	8	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5V to ±18V			1	3	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0V			600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0V			±25	±100	nA
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio			86	100		dB
INPUT IMPEDANCE							
	Differential				170 || 2		kΩ || pF
	Common-mode				600 || 2.5		MΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 2kΩ		90	100		dB
OUTPUT							
V_{OUT}	Output voltage	R_L = 2kΩ		(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current				See Typical Characteristics		mA
Z_O	Open-loop output impedance				See Typical Characteristics		Ω
I_{SC}	Short-circuit current(3)				±40		mA
C_{LOAD}	Capacitive load drive				200		pF
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_{OUT} = 0A			1.4	1.7	mA
			T_A = –40°C to +85°C(2)			2	

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

5.8 Typical Characteristics

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

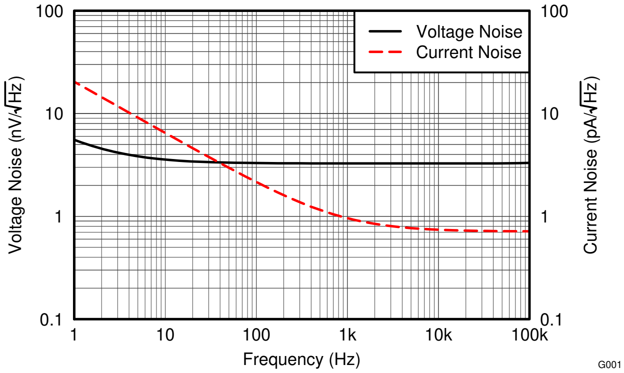


Figure 5-1. Input Voltage Noise Density and Input Current Noise Density vs Frequency

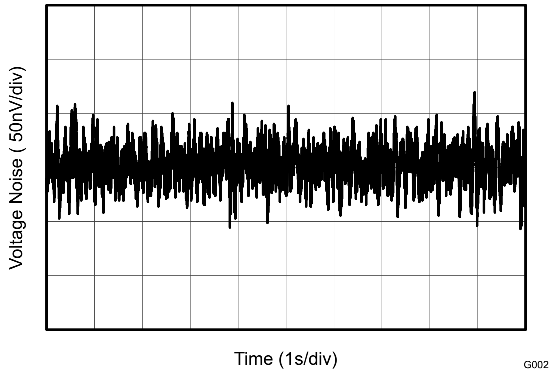


Figure 5-2. 0.1Hz to 10Hz Noise

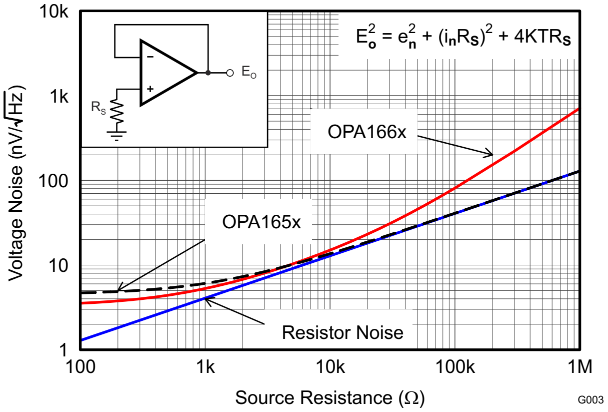


Figure 5-3. Voltage Noise vs Source Resistance

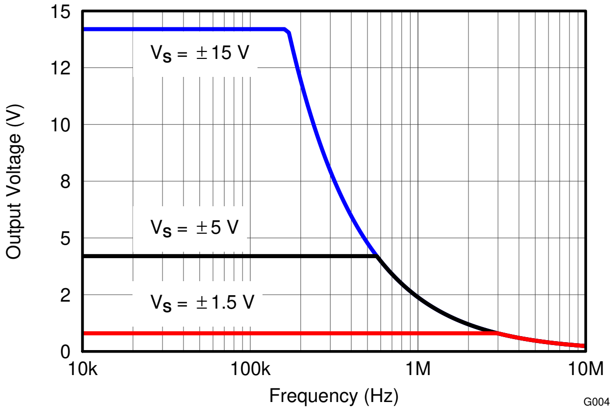


Figure 5-4. Maximum Output Voltage vs Frequency

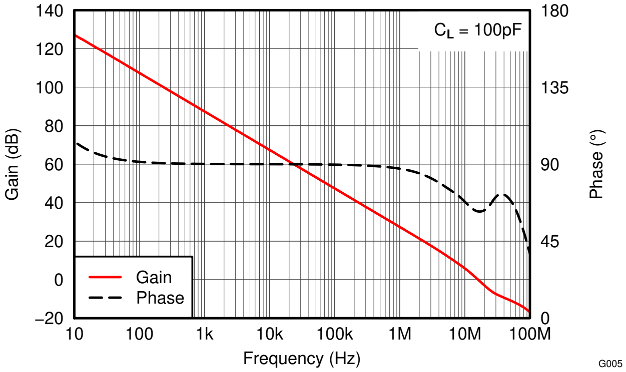


Figure 5-5. Gain and Phase vs Frequency

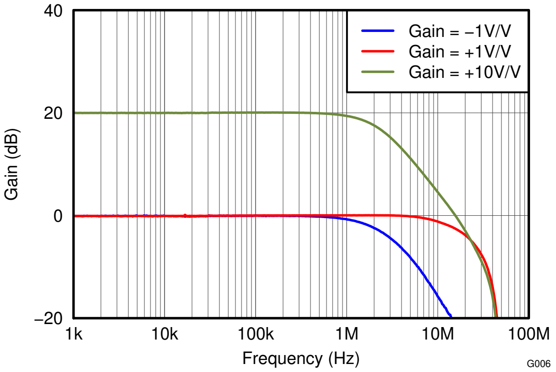


Figure 5-6. Closed-Loop Gain vs Frequency

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

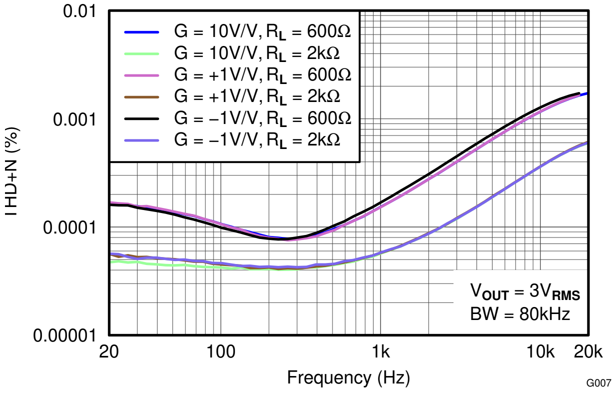


Figure 5-7. THD+N Ratio vs Frequency

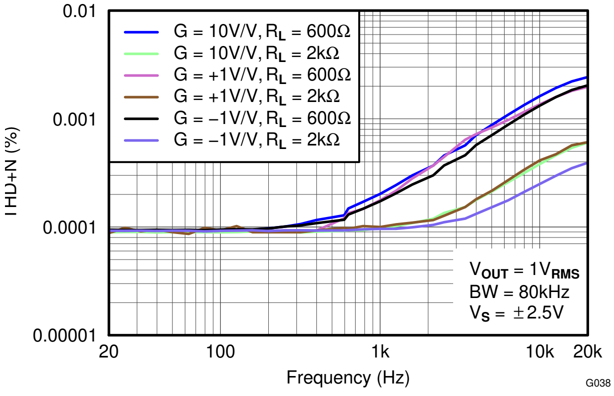


Figure 5-8. THD+N Ratio vs Frequency

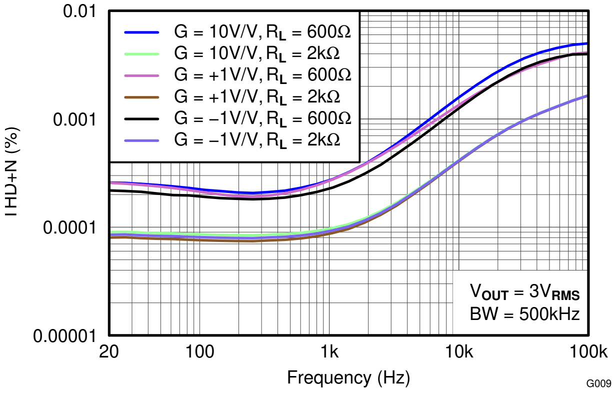


Figure 5-9. THD+N Ratio vs Frequency

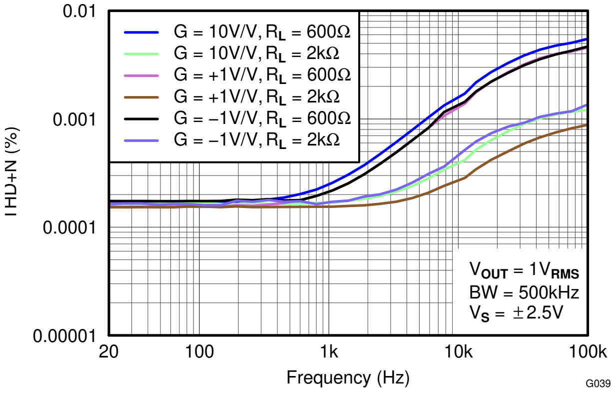


Figure 5-10. THD+N Ratio vs Frequency

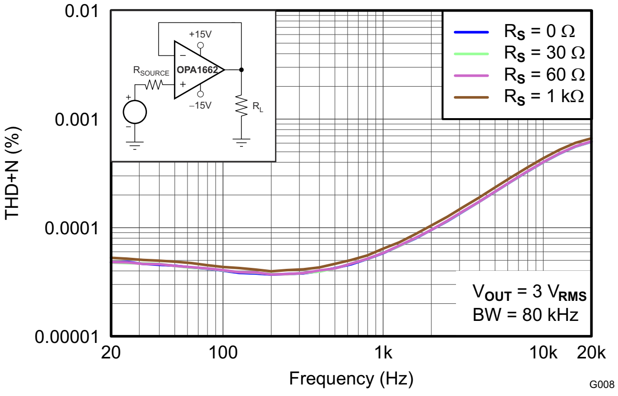


Figure 5-11. THD+N Ratio vs Frequency

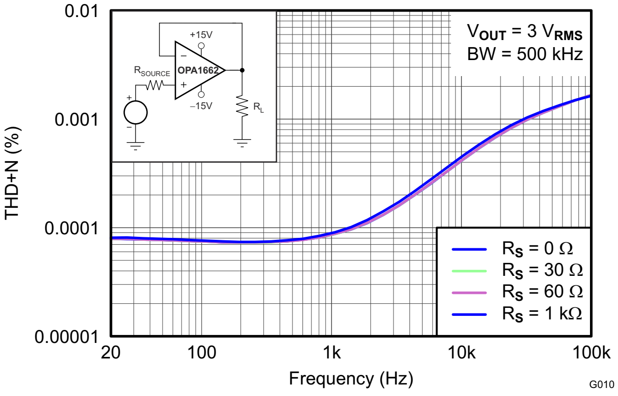


Figure 5-12. THD+N Ratio vs Frequency

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

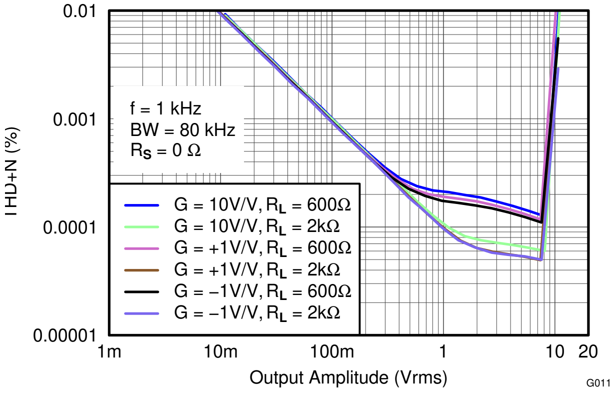


Figure 5-13. THD+N Ratio vs Output Amplitude

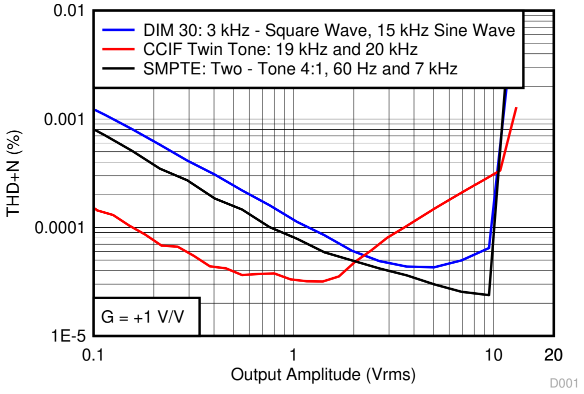


Figure 5-14. Intermodulation Distortion vs Output Amplitude

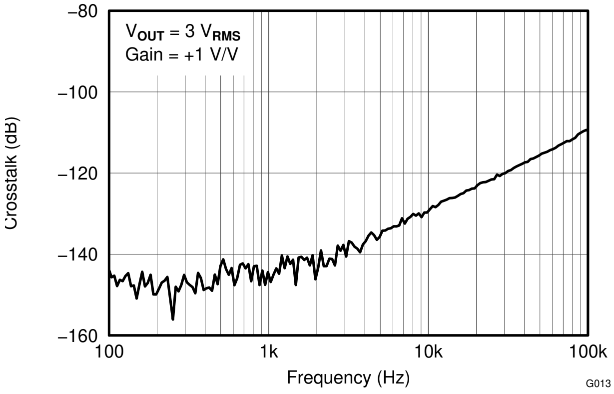


Figure 5-15. Channel Separation vs Frequency

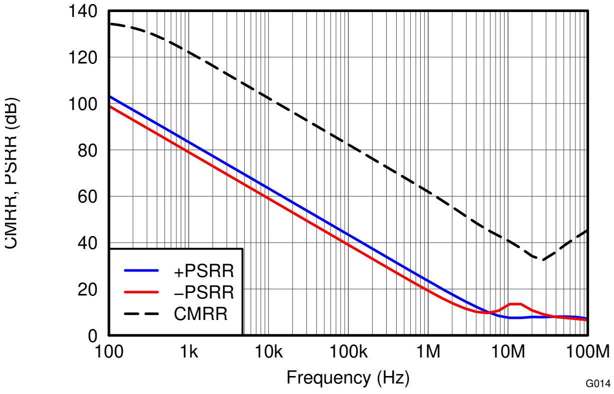


Figure 5-16. CMRR and PSRR vs Frequency (Referred-to-Input)

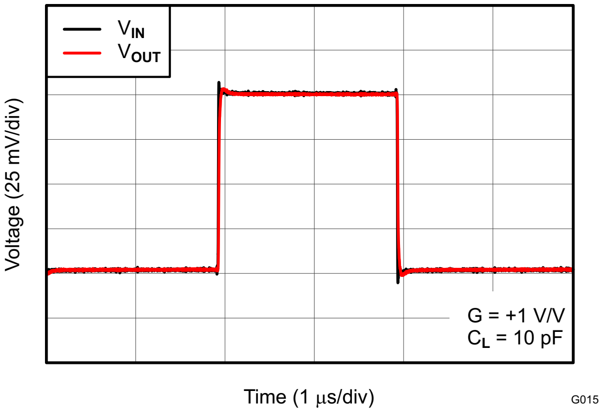


Figure 5-17. Small-Signal Step Response

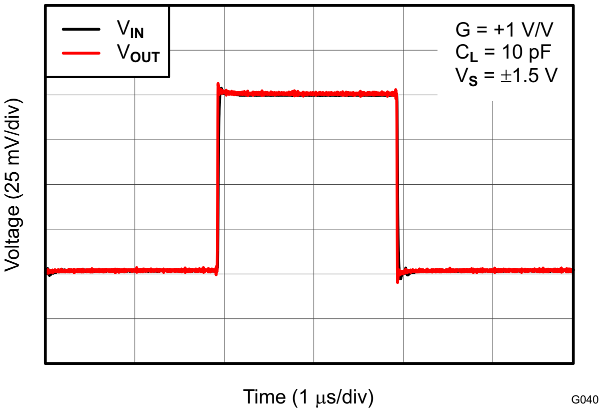


Figure 5-18. Small-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

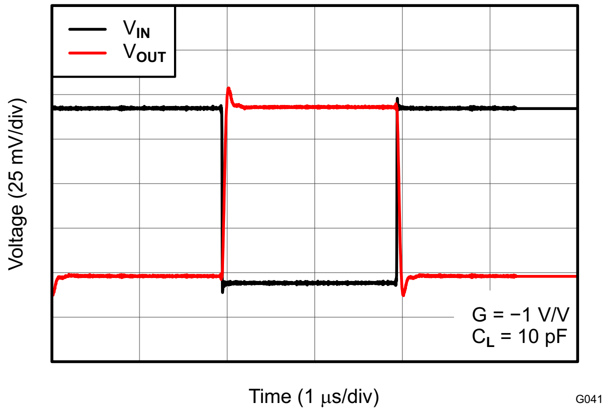


Figure 5-19. Small-Signal Step Response

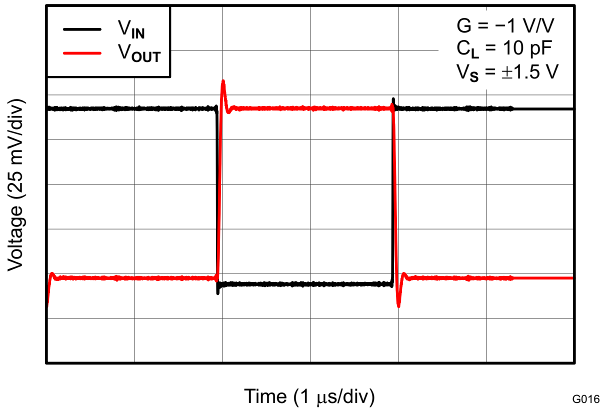


Figure 5-20. Small-Signal Step Response

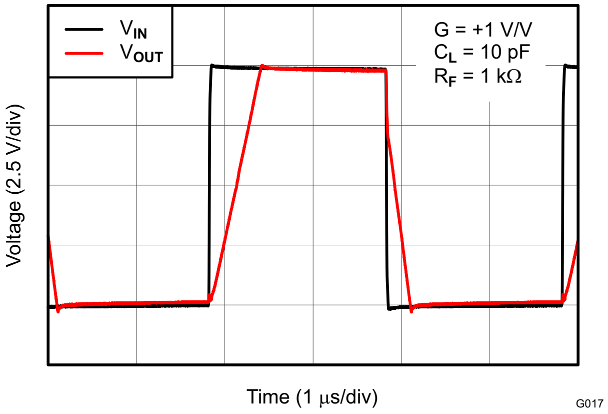


Figure 5-21. Large-Signal Step Response

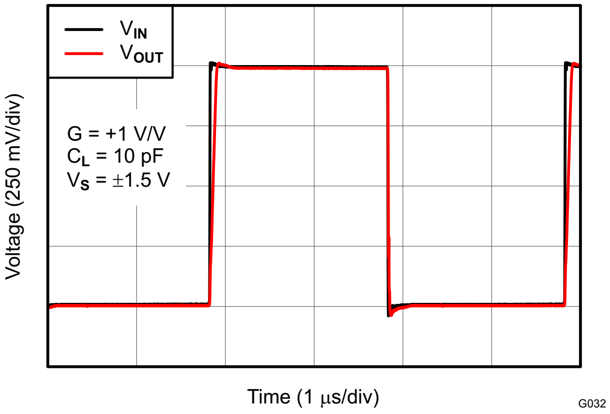


Figure 5-22. Large-Signal Step Response

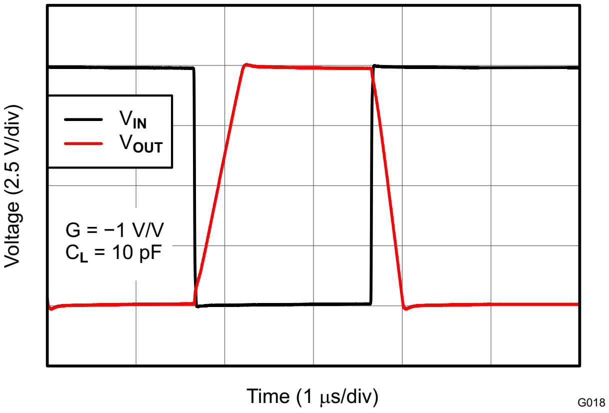


Figure 5-23. Large-Signal Step Response

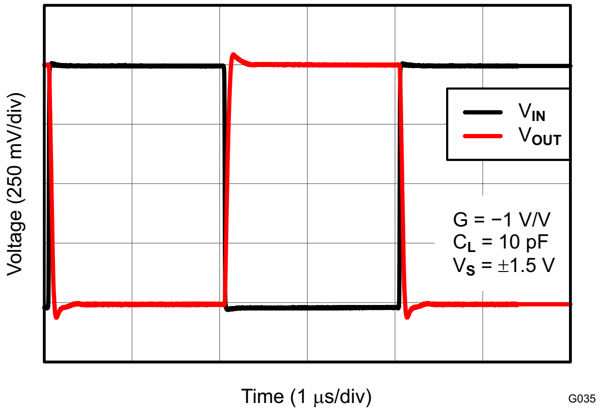


Figure 5-24. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

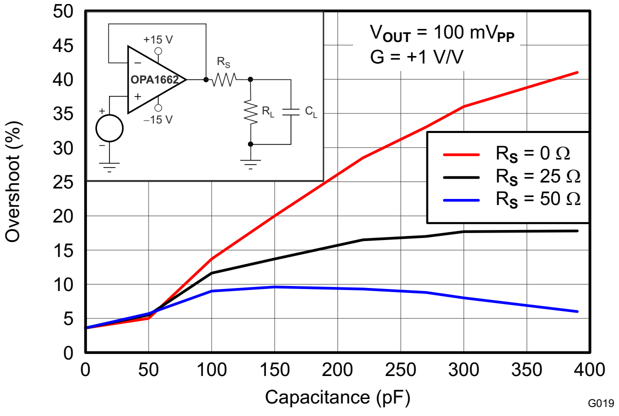


Figure 5-25. Small-Signal Overshoot vs Capacitive Load

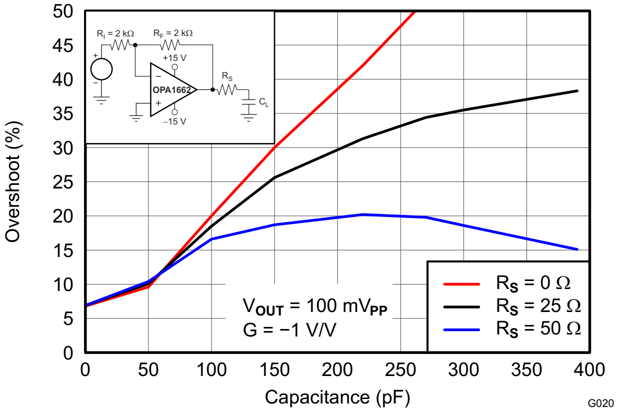


Figure 5-26. Small-Signal Overshoot vs Capacitive Load

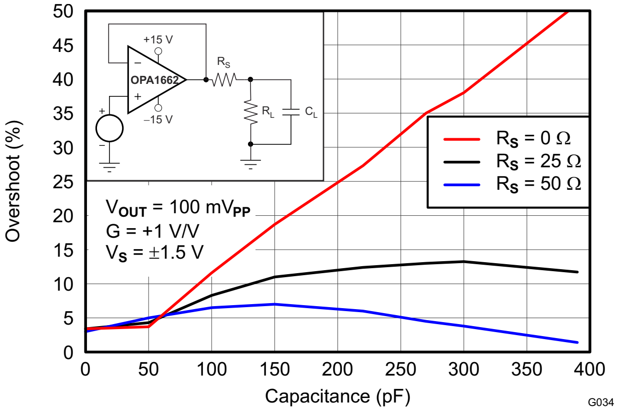


Figure 5-27. Small-Signal Overshoot vs Capacitive Load

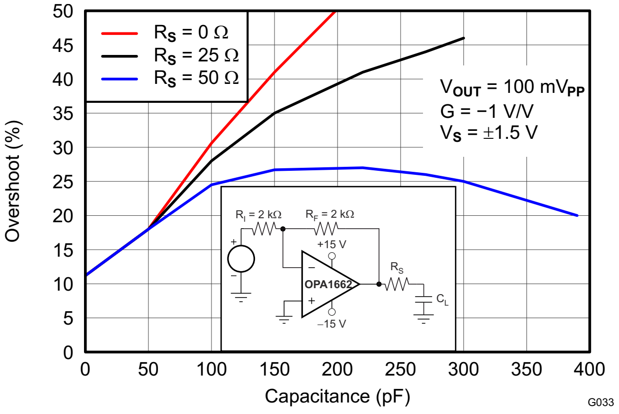


Figure 5-28. Small-Signal Overshoot vs Capacitive Load

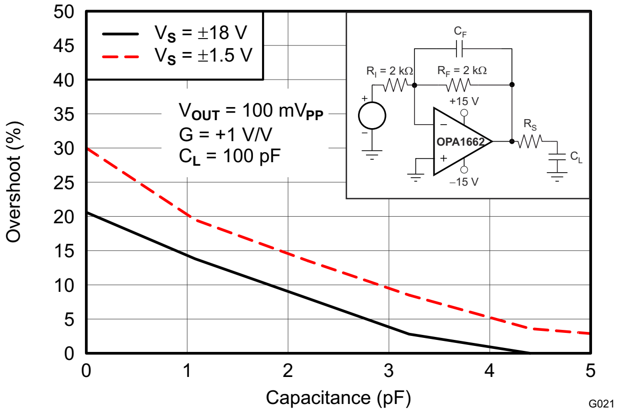


Figure 5-29. Small-Signal Overshoot vs Feedback Capacitor

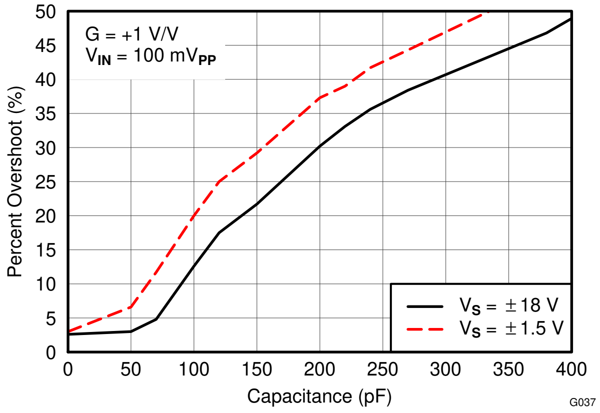


Figure 5-30. Percent Overshoot vs Capacitive Load

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

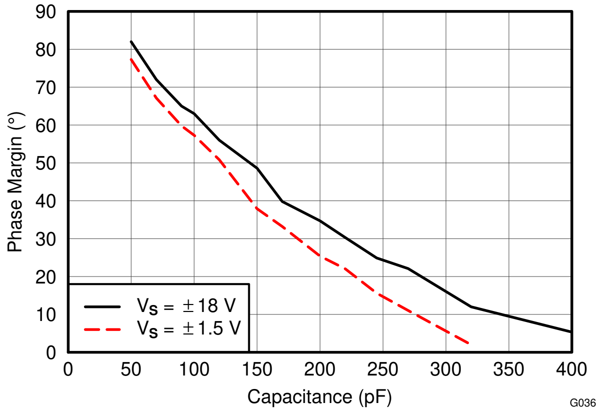


Figure 5-31. Phase Margin vs Capacitive Load

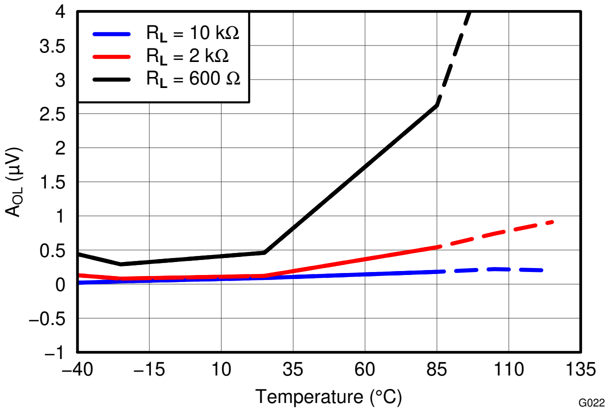


Figure 5-32. Open-Loop Gain vs Temperature

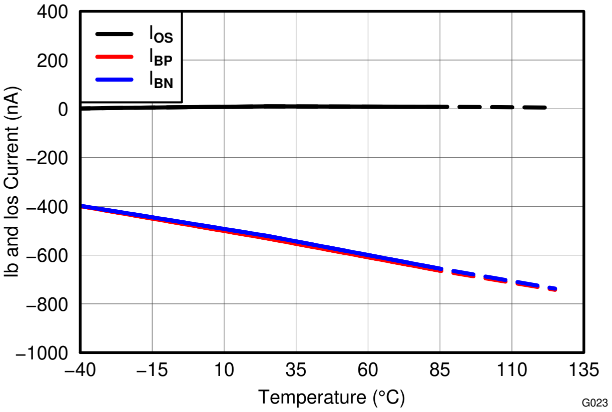


Figure 5-33. I_B and I_{OS} vs Temperature

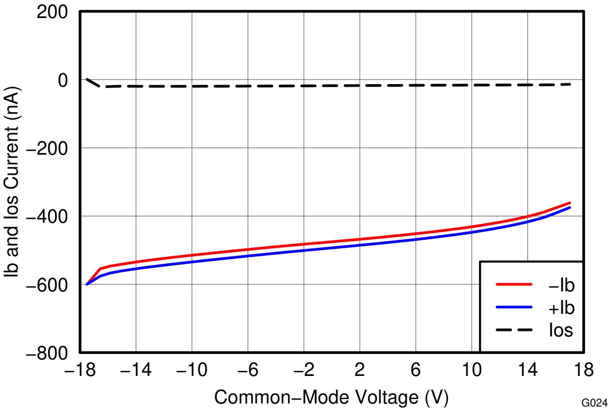


Figure 5-34. I_B and I_{OS} vs Common-Mode Voltage

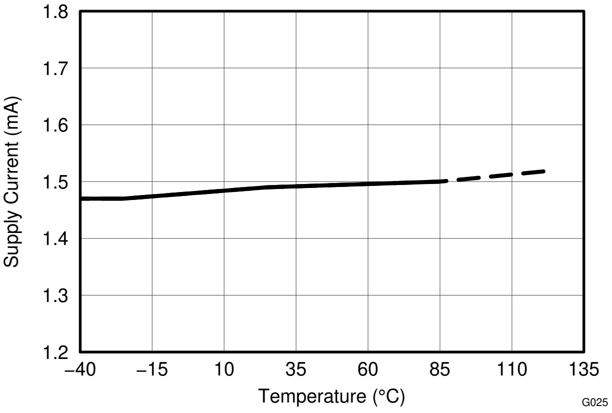


Figure 5-35. Supply Current vs Temperature

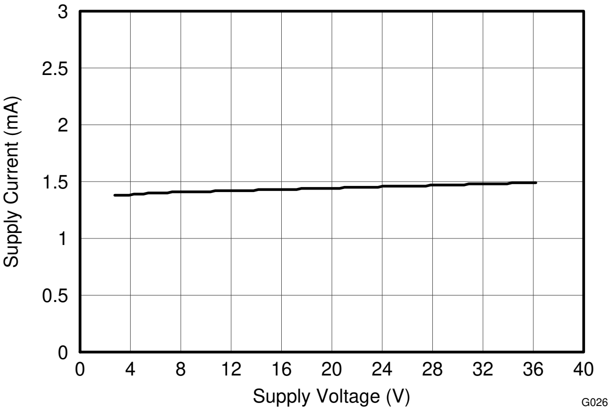


Figure 5-36. Supply Current vs Supply Voltage

5.8 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, and R_L = 2kΩ (unless otherwise noted)

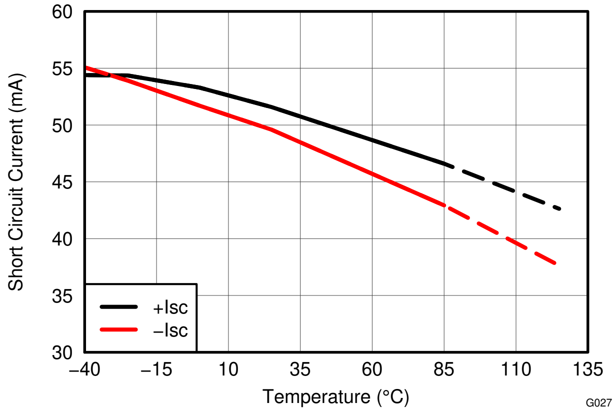


Figure 5-37. Short-Circuit Current vs Temperature

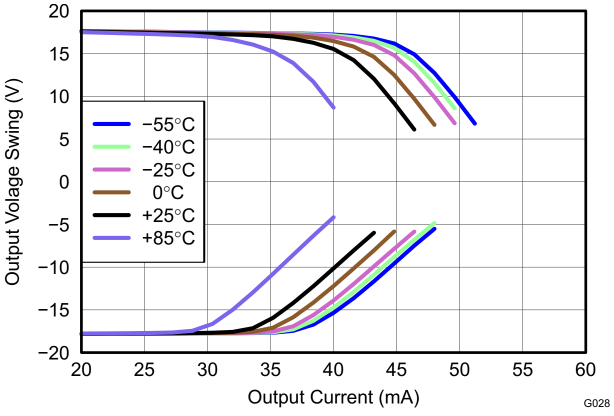


Figure 5-38. Output Voltage vs Output Current

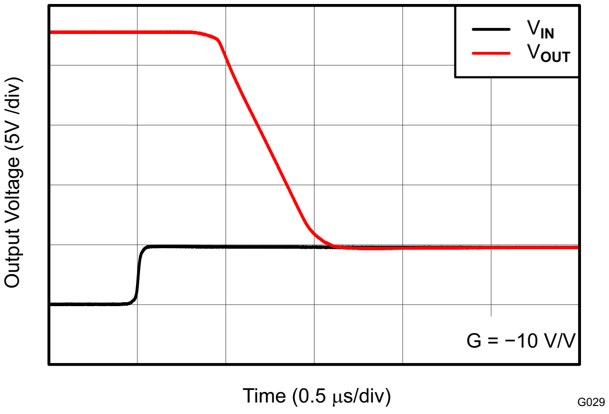


Figure 5-39. Positive Overload Recovery

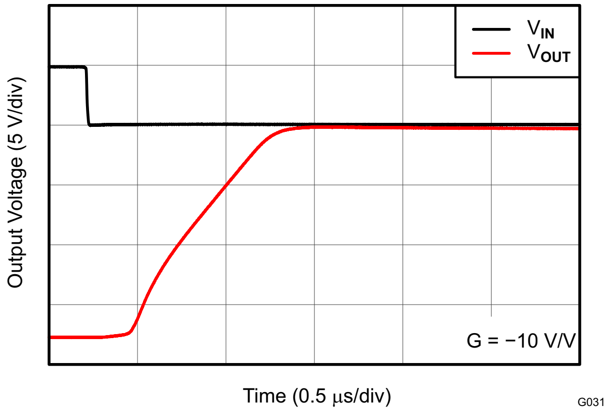


Figure 5-40. Negative Overload Recovery

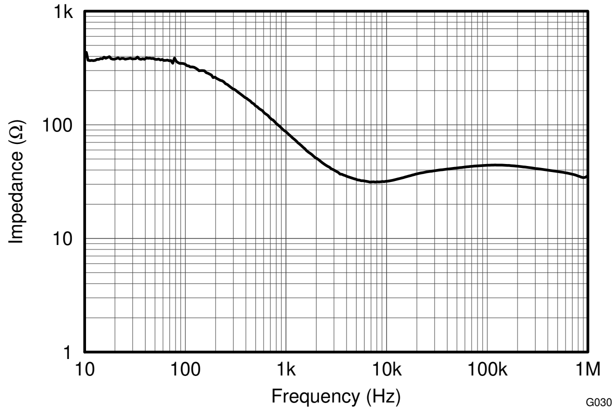


Figure 5-41. Open-Loop Output Impedance vs Frequency

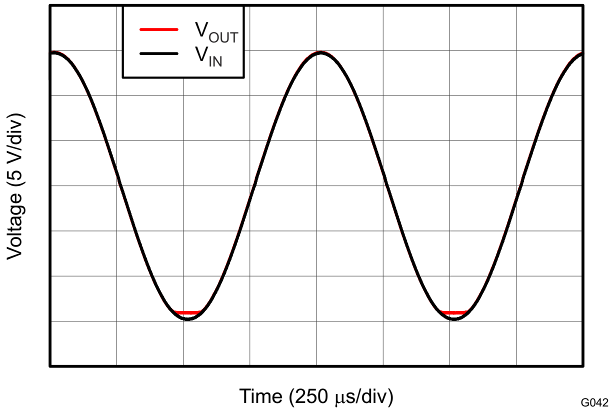


Figure 5-42. No Phase Reversal

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPA166x are unity-gain stable, precision dual and quad op amps with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 6-1 shows a simplified schematic of the OPA166x (one channel shown).

6.1.1 Operating Voltage

The OPA166x series op amps operate from ±1.5V to ±18V supplies while maintaining excellent performance. The OPA166x series can operate with as little as 3V between the supplies and with up to 36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA166x series, power-supply voltages do not need to be equal. For example, set the positive supply to 25V with the negative supply at –5V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are specified over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

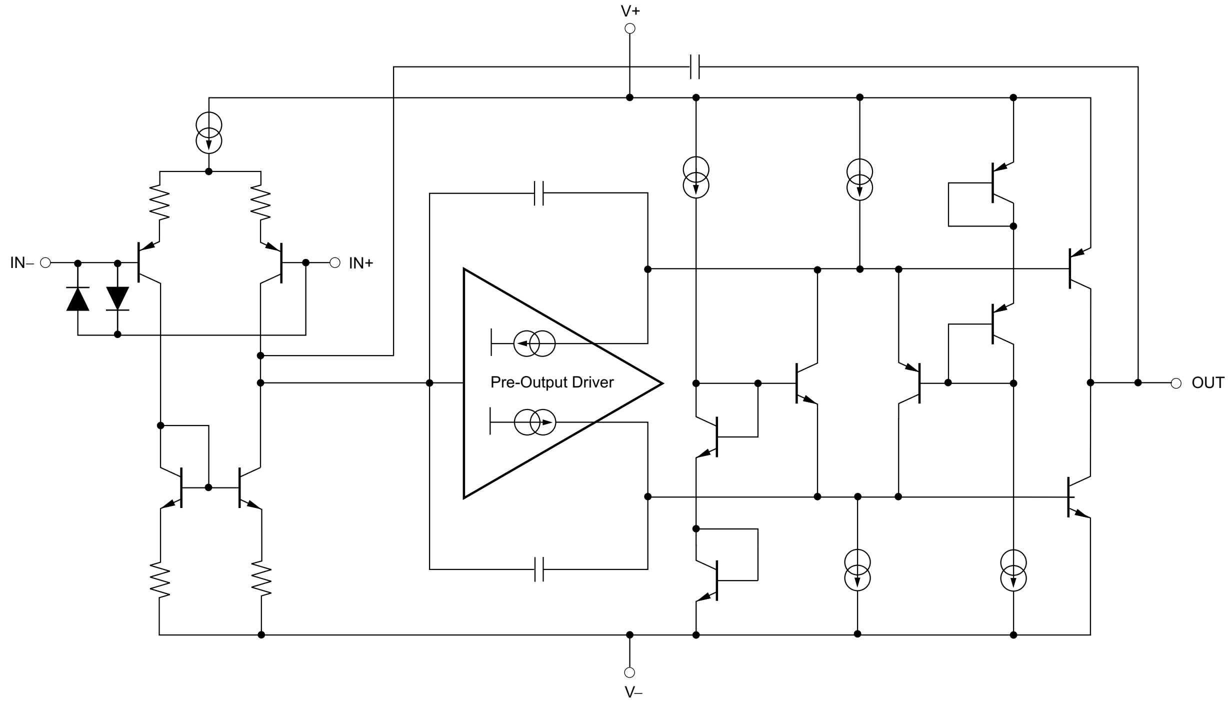


Figure 6-1. OPA166x Simplified Schematic

6.1.2 Input Protection

The input terminals of the OPA166x are protected from excessive differential voltage with back-to-back diodes, as Figure 6-2 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor (R_I), a feedback resistor (R_F), or both, can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA166x and is examined in *Section 6.1.3*. Figure 6-2 shows an example configuration when both current-limiting input and feedback resistors are used.

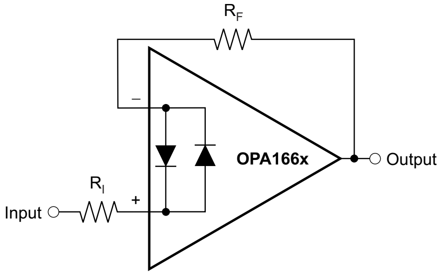


Figure 6-2. Pulsed Operation

6.1.3 Noise Performance

Figure 6-3 shows the total circuit noise for varying source impedance values with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA166x (GBW = 22MHz, G = +1) is shown with total circuit noise calculated. The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA166x series op amps makes them a better choice for low source impedances of less than 1kΩ.

The equation in Figure 6-3 shows the calculation of the total circuit noise, with these parameters:

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = Temperature in kelvins (K)

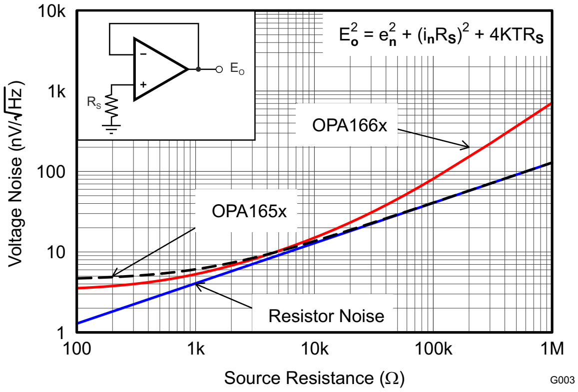


Figure 6-3. Noise Performance of the OPA166x in Unity-Gain Buffer Configuration

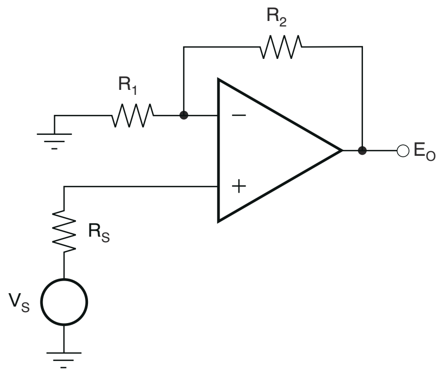
6.1.4 Basic Noise Calculations

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 6-3 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 6-4 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

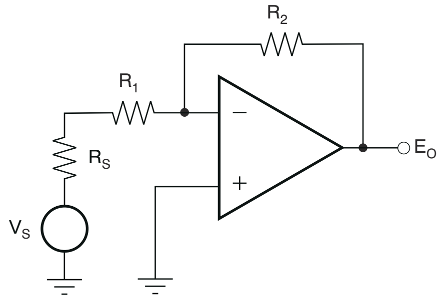
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + \left[\frac{R_2}{R_1}\right]^2 e_1^2 + e_2^2 + \left[1 + \frac{R_2}{R_1}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_1^2 + e_2^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA166x series of op amps at 1kHz, $e_n = 3.3nV/\sqrt{Hz}$.

Figure 6-4. Noise Calculation in Gain Configurations

6.1.5 Total Harmonic Distortion Measurements

The OPA166x series op amps have excellent distortion characteristics. THD + noise is below 0.0006% (G = +1, $V_O = 3V_{RMS}$, BW = 80kHz) throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load (see Figure 5-7 for characteristic performance).

The distortion produced by the OPA166x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 6-5 shows) can be used to extend the measurement capabilities.

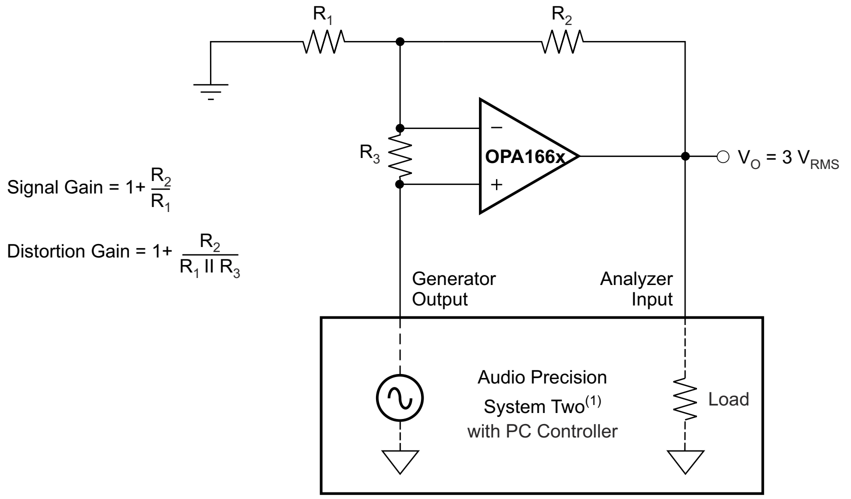
Op amp distortion is considered an internal error source that is referred to the input. Figure 6-5 shows a circuit that causes the op amp distortion to be gained up (refer to the table in Figure 6-5 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 must be kept small to minimize the effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

6.1.6 Capacitive Loads

The dynamic characteristics of the OPA1662 and OPA1664 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 5-25 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

(1) For measurement bandwidth, see Figure 5-7 through Figure 5-12.

Figure 6-5. Distortion Test Circuit

6.1.7 Power Dissipation

The OPA1662 and OPA1664 series op amps are capable of driving 2kΩ loads with a power-supply voltage up to ±18V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA166x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

6.1.8 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is important. Figure 6-6 illustrates the ESD circuits contained in the OPA166x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent the amplifier from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device internal to the OPA166x triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, the ESD cell quickly activates, clamping the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 6-6, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. During this condition, there is a risk that some of the internal ESD protection circuits can be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

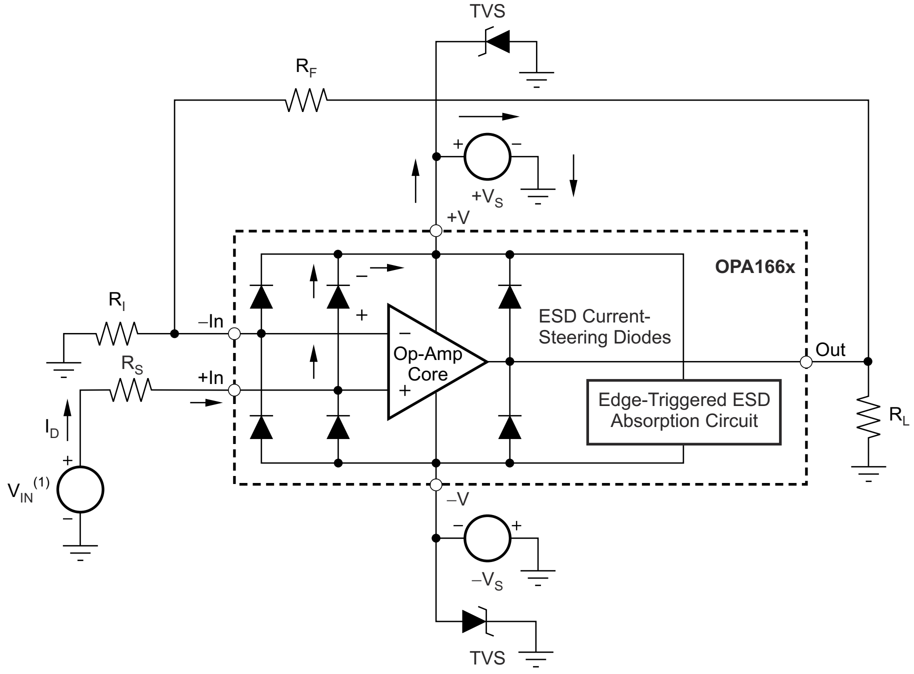
Figure 6-6 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. This also depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes can be added to the supply pins as shown in Figure 6-6.

The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

Figure 6-6. Equivalent Internal ESD Circuitry and the Relation to a Typical Circuit Application (Single Channel Shown)

6.2 Typical Application

Figure 6-7 shows an additional application idea.

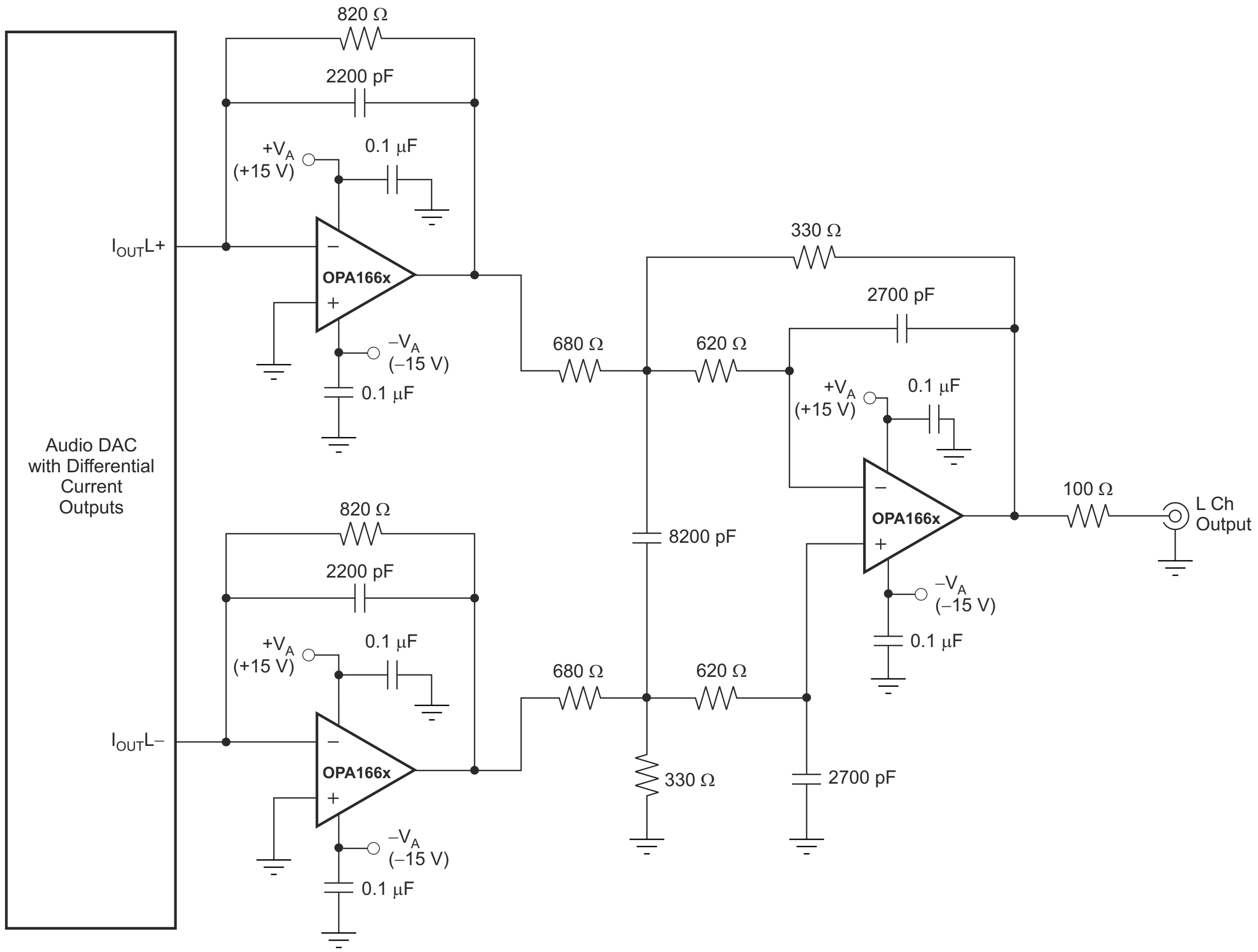


Figure 6-7. Audio DAC I/V Converter and Output Filter

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

Blu-Ray™ is a trademark of Blu-Ray Disc Association.
SoundPlus™ is a trademark of Texas Instruments Incorporated.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2011) to Revision A (December 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added the *Specifications*, *ESD Ratings*, *Recommended Operating Conditions*, *Application and Implementation*, *Typical Application*, *Device and Documentation Support*, *Revision History*, and *Mechanical, Packaging, and Orderable Information* sections...1
- Updated table note 1 in *Absolute Maximum Ratings* 3
- Changed junction temperature from 200°C to 150°C in *Absolute Maximum Ratings* 3

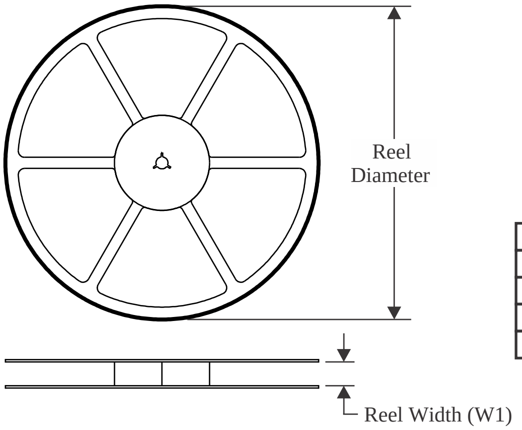
---

9 Mechanical, Packaging, and Orderable Information

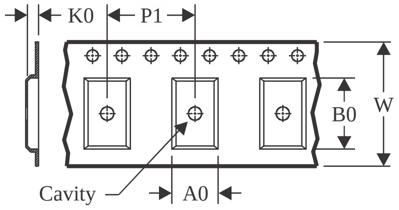
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

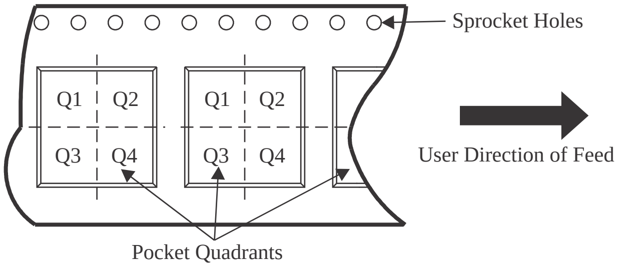


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

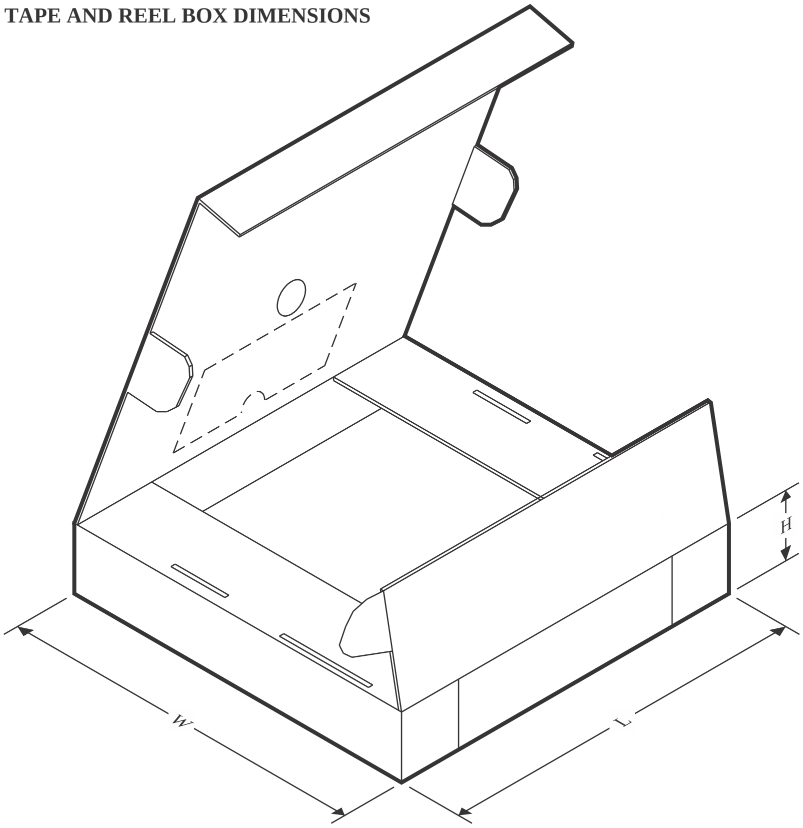
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1662AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1662AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1664AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1664AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

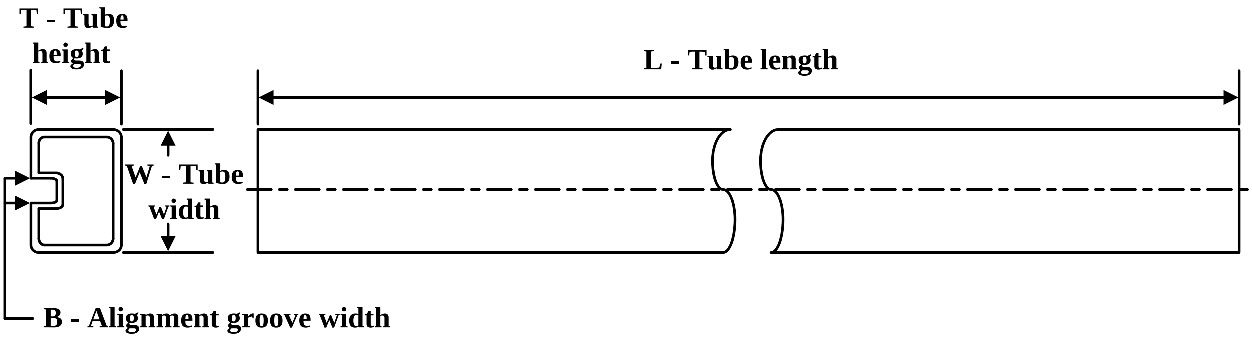
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

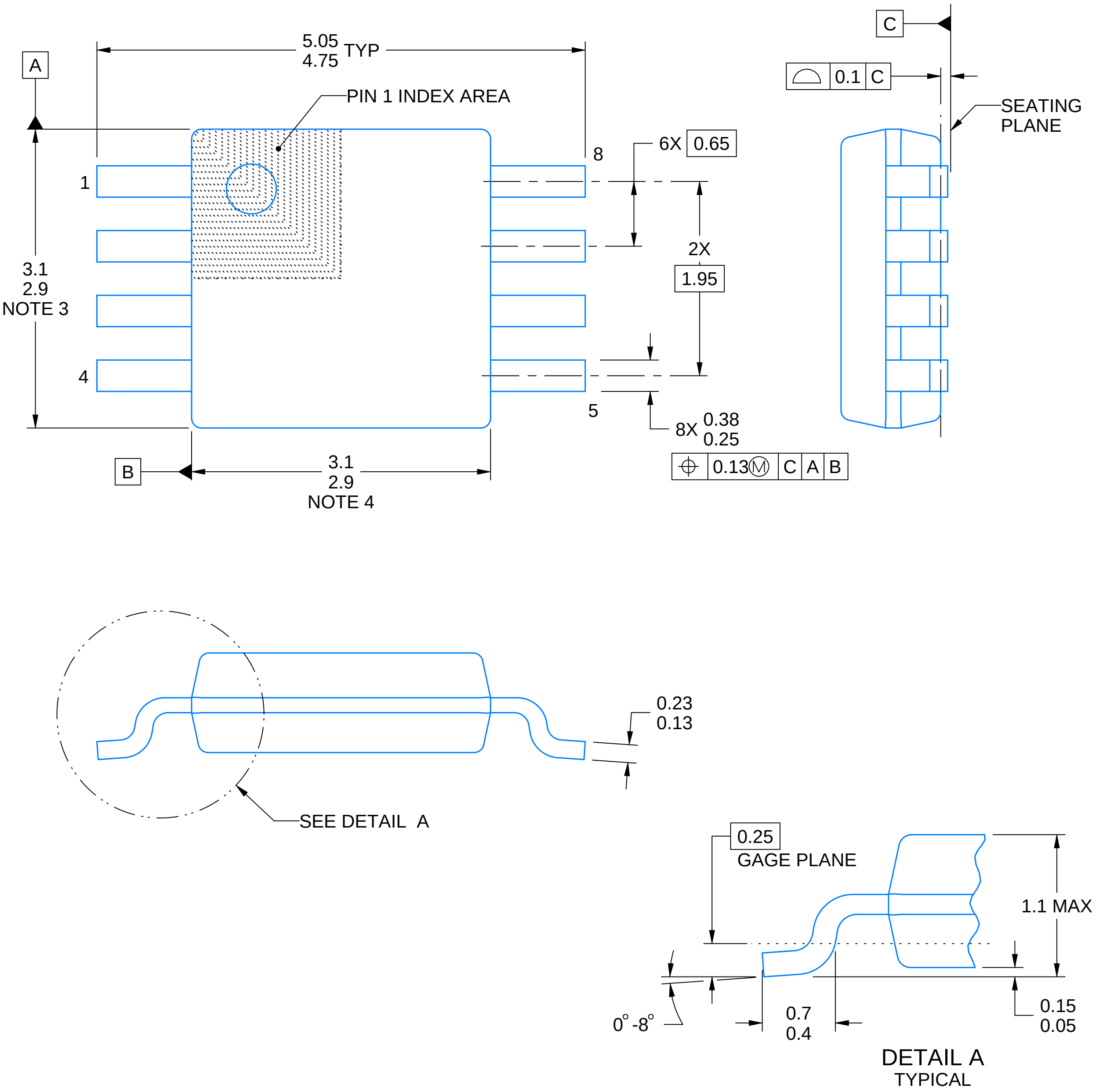
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1662AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA1662AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA1664AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA1664AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

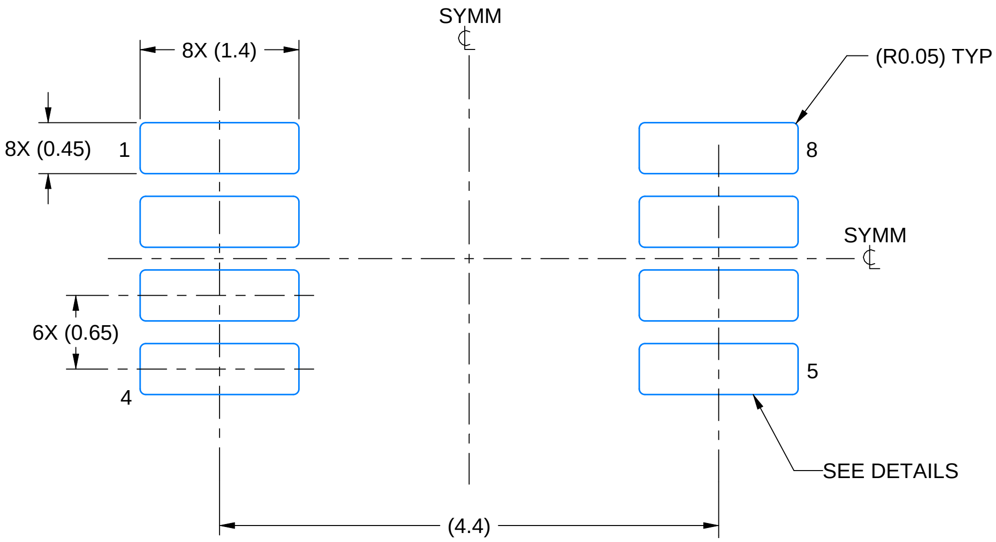
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1662AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA1662AIDGK	DGK	VSSOP	8	80	274	6.55	500	2.88
OPA1664AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA1664AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

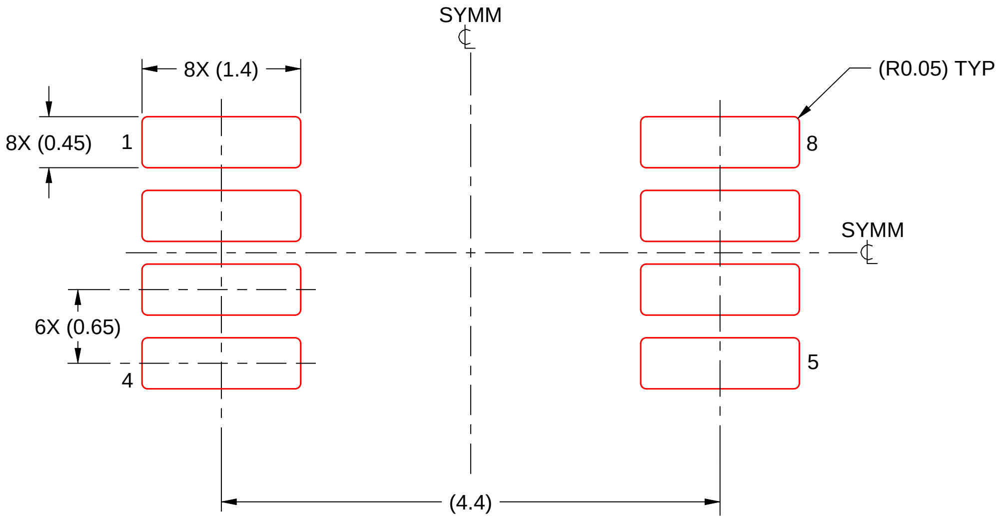
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

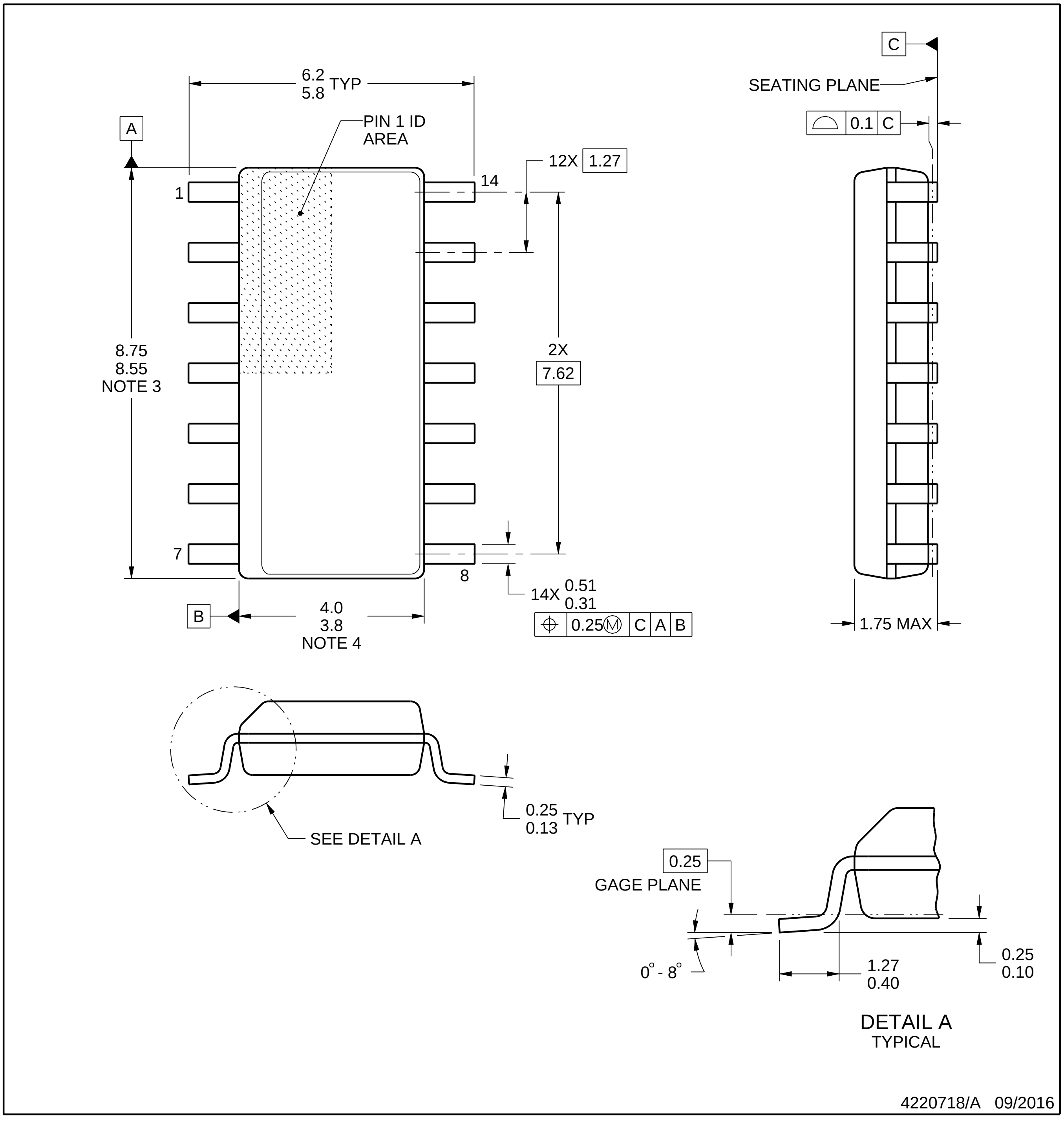
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A

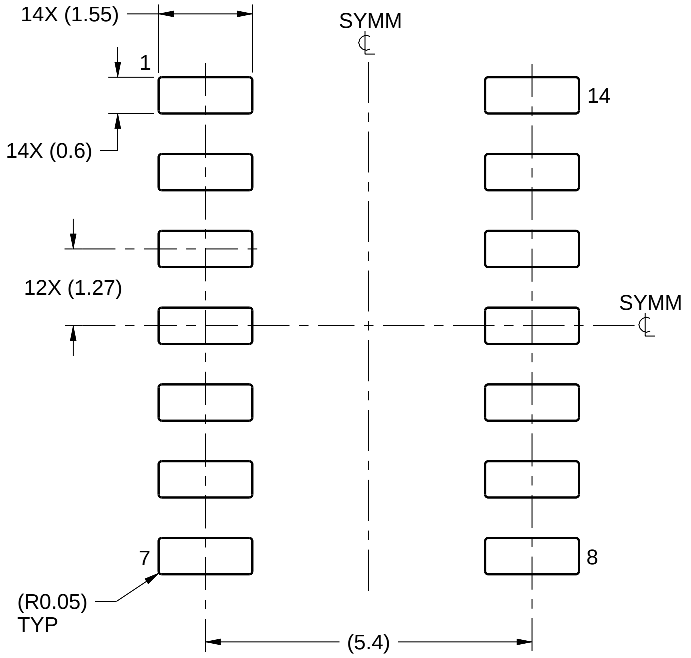
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

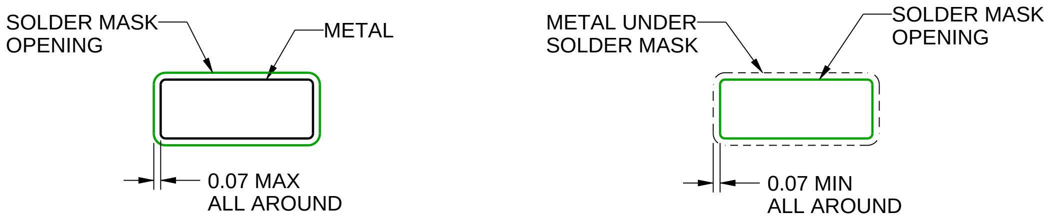


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



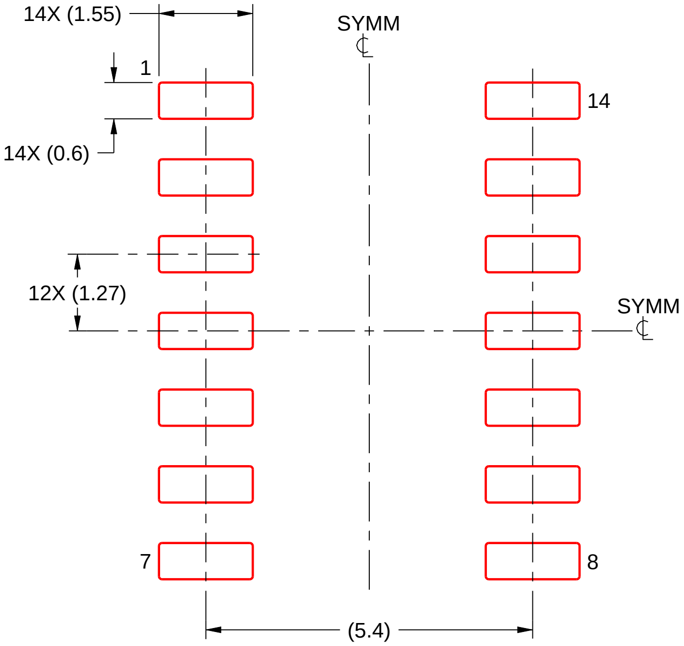
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

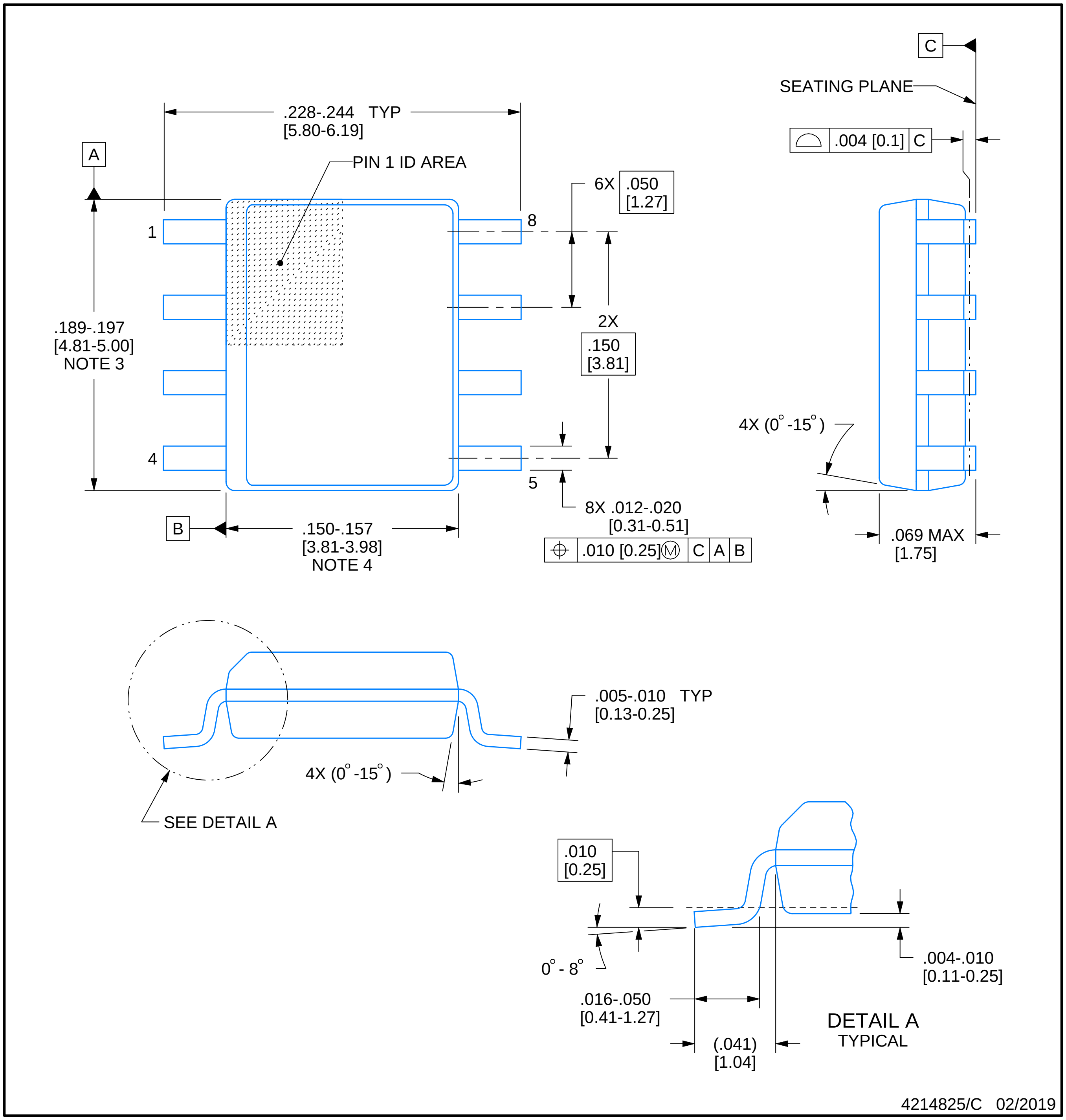
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

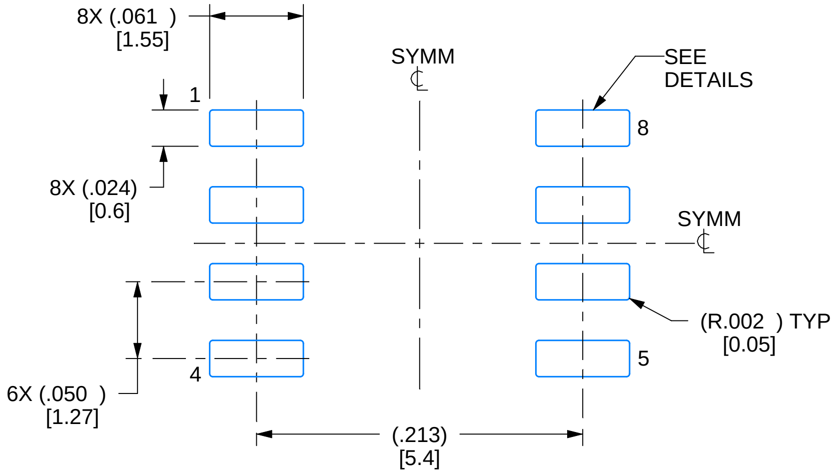
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

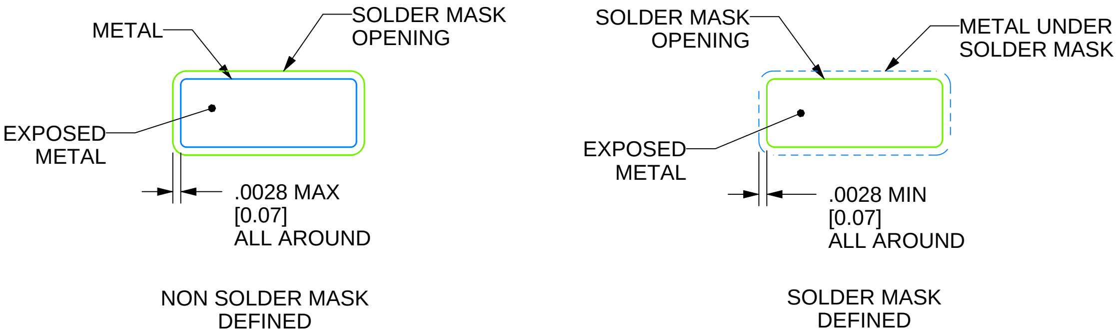


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



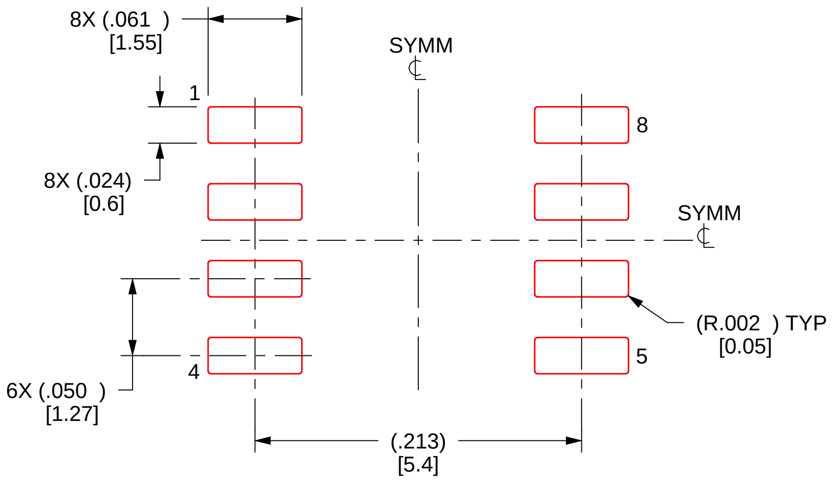
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

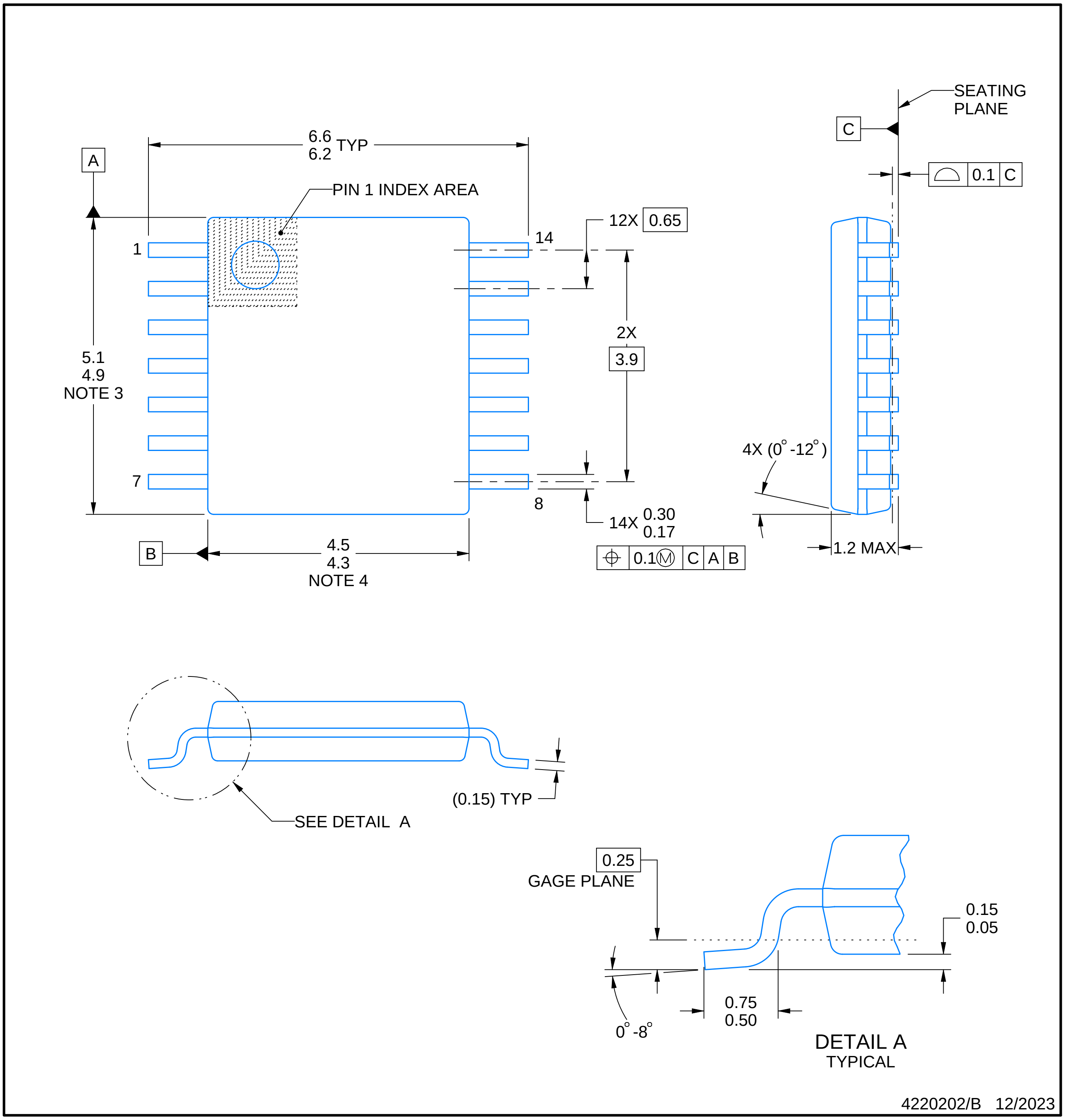
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

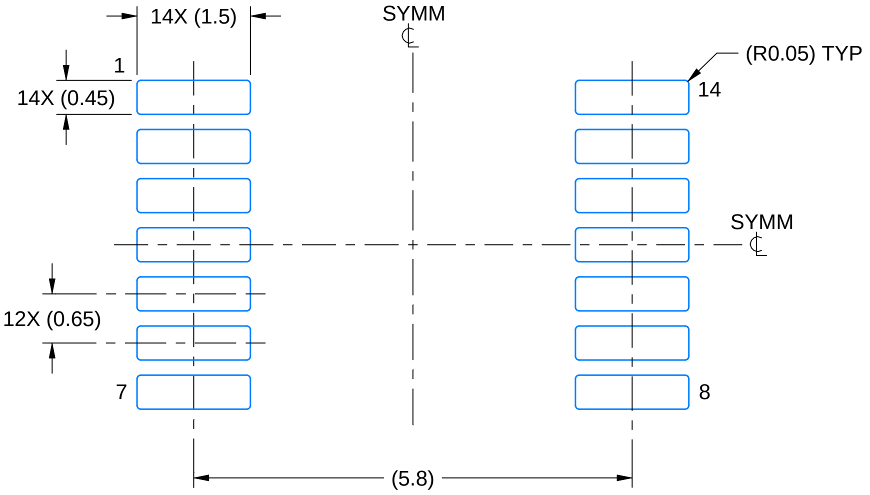
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

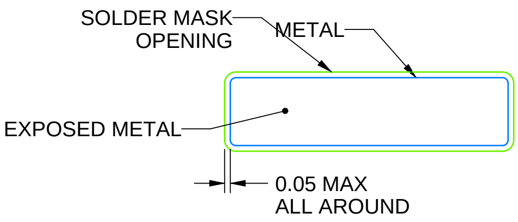


NOTES:

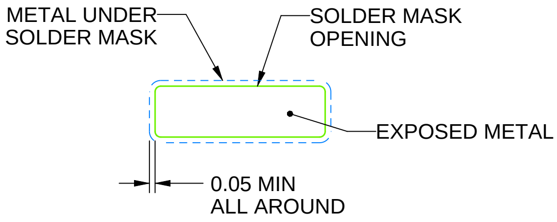
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



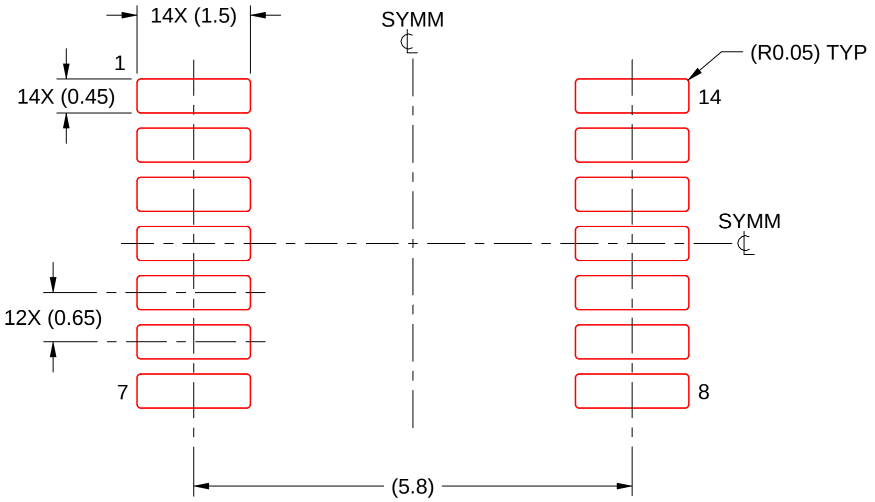
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated