

# LSF0102 2 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Applications

## 1 Features

- Provides bidirectional voltage translation with no direction pin
- Supports up to 100MHz up translation and greater than 100MHz down translation at  $\leq 30\text{pF}$  capacitive load and up To 40MHz up or down translation at 50pF capacitive load
- Allows bidirectional voltage-level translation between
  - 0.95V  $\leftrightarrow$  1.8/2.5/3.3/5V
  - 1.2V  $\leftrightarrow$  1.8/2.5/3.3/5V
  - 1.8V  $\leftrightarrow$  2.5/3.3/5V
  - 2.5V  $\leftrightarrow$  3.3/5V
  - 3.3V  $\leftrightarrow$  5V
- Low standby current
- 5V tolerance I/O port to support TTL
- Low  $R_{ON}$  provides less signal distortion
- High-impedance I/O pins for EN = Low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance >100mA per JESD 17
- $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  operating temperature range

## 2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I<sup>2</sup>C, and other interfaces in telecom infrastructure
- [Enterprise systems](#)
- [Communications equipment](#)
- [Personal electronics](#)
- [Industrial applications](#)

## 3 Description

The LSF family of devices supports bidirectional voltage translation without the need for DIR pin which minimizes system effort (for PMBus, I<sup>2</sup>C, SMBus, and so forth). The LSF family of devices supports up to 100MHz up translation and greater than 100MHz down translation at  $\leq 30\text{pF}$  capacitive load and up to 40MHz up or down translation at 50pF capacitive load which allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

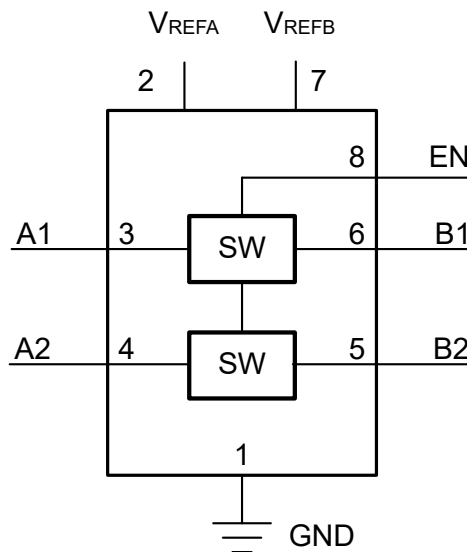
LSF family supports 5V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The LSF family is able to set up different voltage translation levels which makes it very flexible.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
LSF0102	DQE (X2SON, 8)	1.4mm × 1mm
	YZT (DSBGA, 8)	1.98mm × 0.98mm
	DCT (SM8, 8)	2.95mm × 4mm
	DCU (VSSOP, 8)	2mm × 3.1mm
	DDF (SOT-23, 8)	2.9mm × 2.8mm
	DTM (X2SON, 8)	1.35mm × 0.80mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



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## 4 Pin Configuration and Functions

Pinout drawings are not to scale

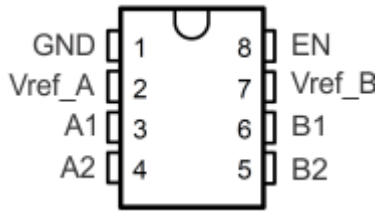


Figure 4-1. LSF0102 DCT, DCU or DDF Package, 8-Pin SM8, VSSOP, or SOT-23 (Top View)

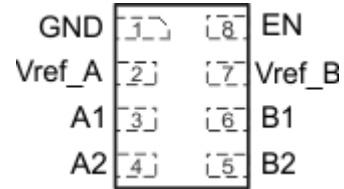


Figure 4-2. LSF0102 DQE Package, 8-Pin X2SON (Transparent Top View)

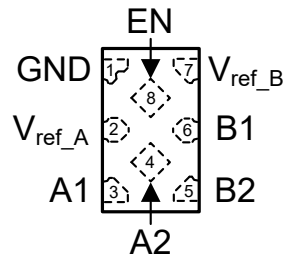
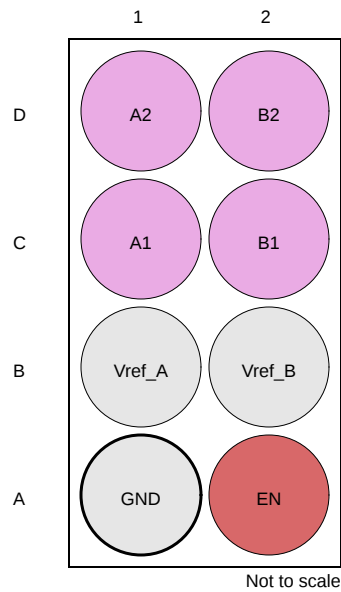


Figure 4-3. LSF0102 DTM Package, 8-Pin X2SON (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
An	3, 4	I/O	Auto-Bidirectional Data port
Bn	6, 5	I/O	
EN	8	I	Enable input; connect to Vref_B and pull-up through a high resistor (200kΩ). See <a href="#">Using the Enable Pin with the LSF Family</a>
GND	1	—	Ground
Vref_A	2	—	Reference supply voltage.
Vref_B	7	—	For proper device biasing, see <a href="#">Section 8</a> and <a href="#">Understanding the Bias Circuit for the LSF Family</a> .

(1) I = input, O = output



**Figure 4-4. LSF0102 YZT Package, 8-Pin DSBGA (Bottom View)**

Legend	
Input	Input or Output
Ground	

**Table 4-2. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
C1	A1	I/O	Auto-Bidirectional Data port
D1	A2	I/O	
C2	B1	I/O	
D2	B2	I/O	
B1	Vref_A	—	Reference supply voltage. For proper device biasing, see <a href="#">Section 8</a> and <a href="#">Understanding the Bias Circuit for the LSF Family</a> .
B2	Vref_B	—	
A2	EN	I	Enable input; connect to Vref_B and pull-up through a high resistor (200kΩ). See <a href="#">Using the Enable Pin with the LSF Family</a>
A1	GND	—	Ground

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_I$	Input voltage <sup>(2)</sup>	-0.5	7	V
$V_{I/O}$	Input/output voltage <sup>(2)</sup>	-0.5	7	V
	Continuous channel current		128	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$T_J$	Junction Temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and input or output negative-voltage ratings may be exceeded if the input and input or output clamp-current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
$V_{ref\_A/B/EN}$	Reference voltage	0	5.5	V
$I_{PASS}$	Pass transistor current		64	mA
$T_A$	Operating free-air temperature	-40	125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LSF0102						UNIT	
	DCU (US8)	DCT (SM8)	DQE (X2SON8)	YZT (DSBGA)	DDF (SOT-23)	DTM (X2SON8)		
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.7	220.0	246.5	125.5	243.3	283.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.9	128.1	149.1	1.0	168.7	184.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	191.3	135.6	100.0	62.7	157.6	187.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	66.3	56.0	17.1	3.4	45.9	25.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	190.1	134.0	99.8	62.7	157.2	186.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	$I_I = -18\text{mA}$ ,	$V_{EN} = 0$			-1.2	V
$I_{IH}$	$V_I = 5\text{V}$	$V_{EN} = 0$			5.0	$\mu\text{A}$
$I_{CC}$	$V_{ref\_B} = V_{EN} = 5.5\text{V}$ , $V_{ref\_A} = 4.5\text{V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND			6		$\mu\text{A}$
$C_{I(ref\_A/B/EN)}$	$V_I = 3\text{V}$ or 0			11		pF
$C_{io(off)}$	$V_O = 3\text{V}$ or 0,	$V_{EN} = 0$		4.0	6.0	pF
$C_{io(on)}$	$V_O = 3\text{V}$ or 0,	$V_{EN} = 3\text{V}$		10.5	12.5	pF
$r_{on}$ <sup>(2)</sup>	$V_I = 0$ ,	$I_O = 64\text{mA}$	$V_{ref\_A} = 3.3\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		8.0	$\Omega$
			$V_{ref\_A} = 1.8\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		9.0	
			$V_{ref\_A} = 1.0\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		10	
	$V_I = 0$ ,	$I_O = 32\text{mA}$	$V_{ref\_A} = 1.8\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		10	$\Omega$
			$V_{ref\_A} = 2.5\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		15	
	$V_I = 1.8\text{V}$ ,	$I_O = 15\text{mA}$	$V_{ref\_A} = 3.3\text{V}$ ; $V_{ref\_B} = V_{EN} = 5\text{V}$		9.0	$\Omega$
	$V_I = 1.0\text{V}$ ,	$I_O = 10\text{mA}$	$V_{ref\_A} = 1.8\text{V}$ ; $V_{ref\_B} = V_{EN} = 3.3\text{V}$		18	$\Omega$
	$V_I = 0\text{V}$ ,	$I_O = 10\text{mA}$	$V_{ref\_A} = 1.0\text{V}$ ; $V_{ref\_B} = V_{EN} = 3.3\text{V}$		20	$\Omega$
$V_I = 0\text{V}$ ,	$I_O = 10\text{mA}$	$V_{ref\_A} = 1.0\text{V}$ ; $V_{ref\_B} = V_{EN} = 1.8\text{V}$		30	$\Omega$	

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

## 5.6 LSF0102 AC Performance (Translating Down) Switching Characteristics, $V_{CCB} = 3.3\text{V}$

over recommended operating free-air temperature range,  $V_{CCB} = 3.3\text{V}$ ,  $V_{CCB} = V_{IH} = V_{ref\_A} + 1$ ,  $V_{IL} = 0$ , and  $V_M = 0.5V_{ref\_A}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{pF}$		$C_L = 30\text{pF}$		$C_L = 15\text{pF}$		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$t_{PLH}$	A or B	B or A	1.1		0.7		0.3		ns
$t_{PHL}$			1.2		0.8		0.4		

## 5.7 LSF0102 AC Performance (Translating Down) Switching Characteristics, $V_{CCB} = 2.5\text{V}$

over recommended operating free-air temperature range,  $V_{CCB} = 2.5\text{V}$ ,  $V_{CCB} = V_{IH} = V_{ref\_A} + 1$ ,  $V_{IL} = 0$ , and  $V_M = 0.5V_{ref\_A}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{pF}$		$C_L = 30\text{pF}$		$C_L = 15\text{pF}$		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$t_{PLH}$	A or B	B or A	1.2		0.8		0.35		ns
$t_{PHL}$			1.3		1		0.5		

## 5.8 LSF0102 AC Performance (Translating Up) Switching Characteristics, $V_{CCB} = 3.3\text{V}$

over recommended operating free-air temperature range,  $V_{CCB} = 3.3\text{V}$ ,  $V_{CCB} = V_T = V_{ref\_A} + 1$ ,  $V_{ref\_A} = V_{IH}$ ,  $V_{IL} = 0$ ,  $V_M = 0.5V_{ref\_A}$  and  $R_L = 300$  (unless otherwise noted) (see [Figure 6-1](#))

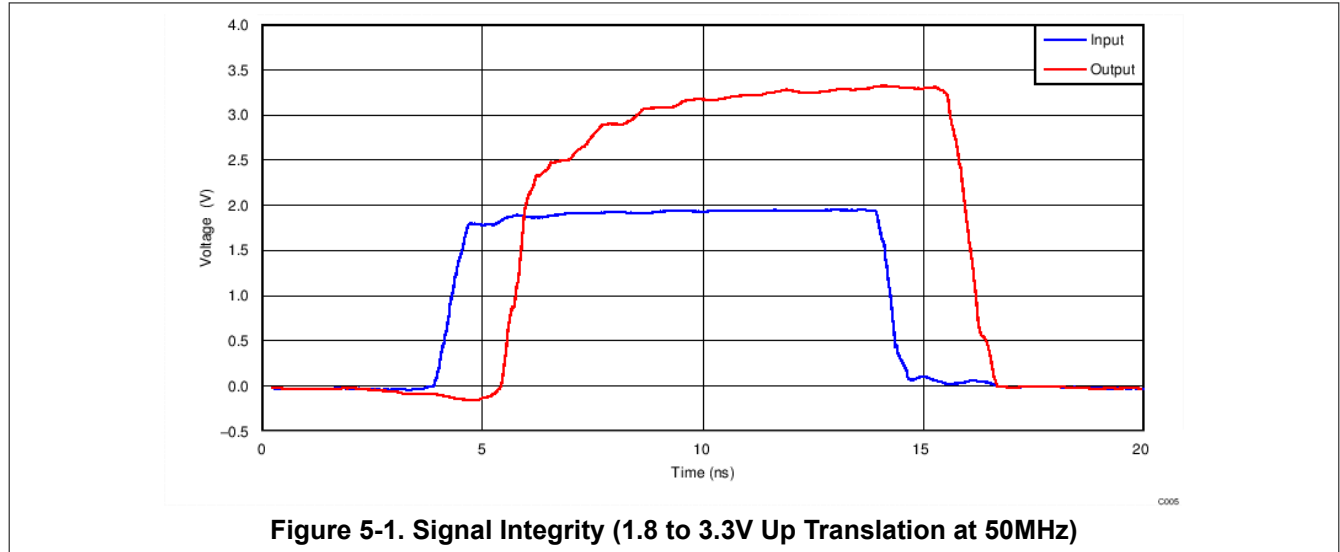
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{pF}$		$C_L = 30\text{pF}$		$C_L = 15\text{pF}$		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$t_{PLH}$	A or B	B or A	1		0.8		0.4		ns
$t_{PHL}$			1		0.9		0.4		

### 5.9 LSF0102 AC Performance (Translating Up) Switching Characteristics, $V_{CCB} = 2.5V$

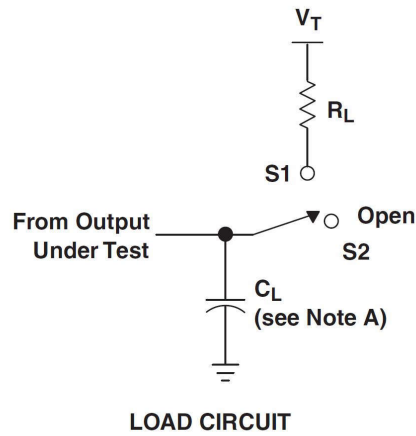
over recommended operating free-air temperature range,  $V_{CCB} = 2.5V$ ,  $V_{CCB} = V_T = V_{ref\_A} + 1$ ,  $V_{ref\_A} = V_{IH}$ ,  $V_{IL} = 0$ ,  $V_M = 0.5V_{ref\_A}$  and  $R_L = 300$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50pF$		$C_L = 30pF$		$C_L = 15pF$		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
$t_{PLH}$	A or B	B or A	1.1		0.9		0.45		ns
$t_{PHL}$			1.3		1.1		0.6		

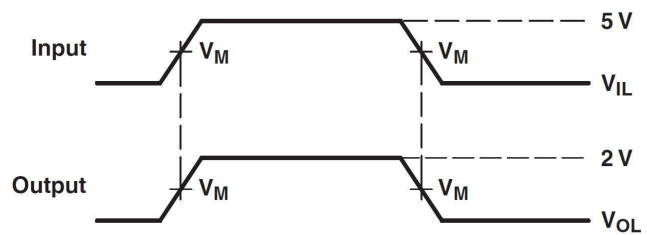
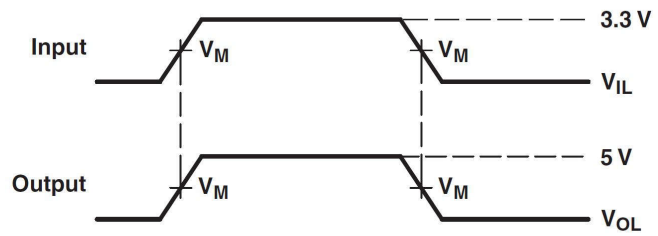
### 5.10 Typical Characteristics



## 6 Parameter Measurement Information



USAGE	SWITCH
Translating up	S1
Translating down	S2



- A.  $C_L$  includes probe and jig capacitance.
- B. Generators that have the following characteristics generate all input pulses:  $PRR \leq 10\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 2\text{ns}$ ,  $t_f \leq 2\text{ns}$ .
- C. The outputs are measured one at a time, with one transition per measurement.

**Figure 6-1. Load Circuit for Outputs**

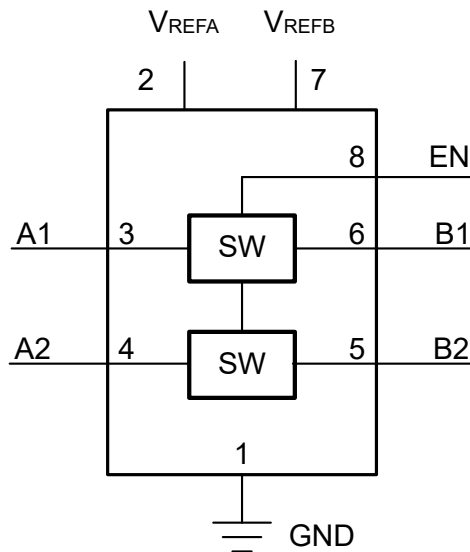


## 7 Detailed Description

### 7.1 Overview

The LSF family can be used in level-translation applications for interfacing devices or systems operating with one another that operate at different interface voltages. The LSF family is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, LSF can achieve 100MHz. The LSF family can also be used in applications where a push-pull driver is connected to the data I/Os. For an overview of device setup and operation, see [The Logic Minute](#) training series on [Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators](#).

### 7.2 Functional Block Diagram



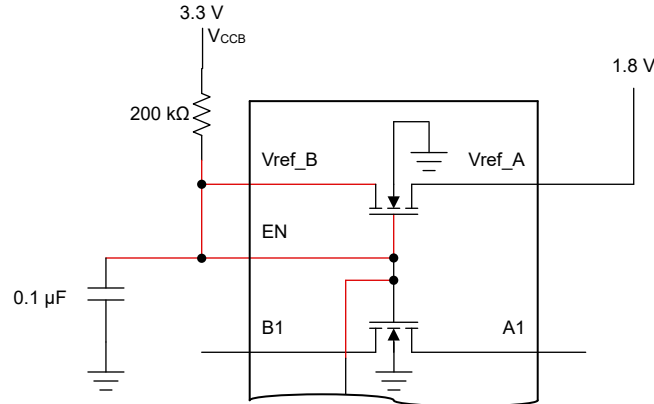
### 7.3 Feature Description

#### 7.3.1 Auto Bidirectional Voltage Translation

The device is an auto bidirectional voltage level translator that is operational from 0.95 to 5.5V on  $V_{ref\_A}$  and 1.8 to 5.5V on  $V_{ref\_B}$ . This allows bidirectional voltage translation between 0.95V and 5.5V without the need for a direction pin in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250- $\Omega$  pullup resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

### 7.3.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to  $V_{ref\_B}$  during operation and both pins must be pulled up to the HIGH side ( $V_{CCB}$ ) through a bias resistor (typically 200k $\Omega$ ). To be in the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the  $V_{ref\_B}$  pin and is recommended to be disabled by an open-drain driver without a pullup resistor. This allows  $V_{ref\_B}$  to regulate the EN input and bias the channels for proper translation. A filter capacitor on  $V_{ref\_B}$  is recommended for a stable supply at the device.



**Figure 7-1. Enable Pin Tied to  $V_{ref\_B}$  Directly and to  $V_{CCB}$  Through a Bias Resistor**

The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation. For additional details on how to use the enable pin, see the [Using the Enable Pin with the LSF Family video](#).

**Table 7-1. Enable Pin Function Table**

INPUT EN <sup>(1)</sup> PIN	Data Port State
Tied directly to $V_{ref\_B}$	An = Bn
L	Hi-Z

(1) EN is controlled by  $V_{ref\_B}$  logic levels.

### 7.4 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low  $R_{ON}$  of the switch allows connections to be made with minimal propagation delay and signal distortion.

Table 7-1 provides a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the [Down Translation with the LSF Family](#) and [Up Translation with the LSF Family](#) videos.

**Table 7-2. Device Functionality**

Signal Direction <sup>(1)</sup>	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at $V_{ref\_A}$ <sup>(2)</sup>
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at $V_{ref\_A}$ and then pulled up to the $V_{PU}$ supply voltage

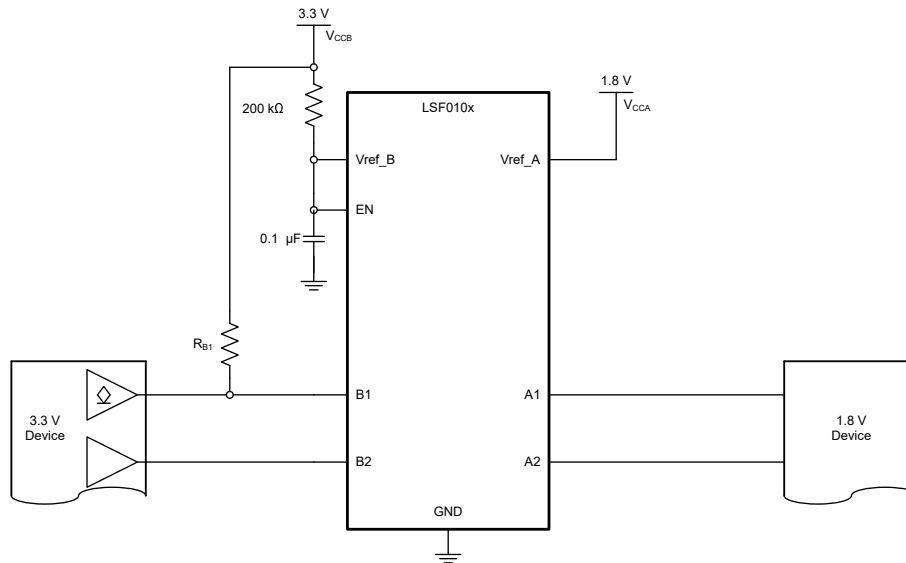
(1) The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.

(2) The A-side can have a pullup to  $V_{ref\_A}$  for additional current drive capability or may also be pulled above  $V_{ref\_A}$  with a pullup resistor. Specifications in the [Recommended Operating Conditions](#) section should always be followed.

## 7.4.1 Up and Down Translation

### 7.4.1.1 Up Translation

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than  $V_{ref\_A}$  by the pull-up resistor that is connected to the pull-up supply voltage ( $V_{PU}$ ). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side, if the low side of the device's output is open drain – or its input has a leakage greater than  $1\mu A$ .



**Figure 7-2. Up Translation Example Schematic with Push-Pull and Open Drain Configuration**

Up translation with the LSF requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. [Equation 1](#) shows the maximum data rate formula and [Equation 2](#) shows the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers. Please see the [Up Translation with the LSF Family](#) video for estimated data rate and sink current calculations based on circuit components.

$$\frac{1}{3 \times 2R_{B1}C_{B1}} = \frac{1}{6R_{B1}C_{B1}} \left( \frac{\text{bits}}{\text{second}} \right) \quad (1)$$

$$I_{OL} \cong \frac{V_{CCA}}{R_{A1}} + \frac{V_{CCB}}{R_{B1}} \quad (A) \quad (2)$$

### 7.4.1.2 Down Translation

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by  $V_{ref\_A}$ . A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than  $1\mu A$ , then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself. For a summary of device operation, refer to [Section 7.4](#). For additional details on the functional operation of the LSF family of devices, see the [Up Translation with the LSF Family](#) and [Down Translation with the LSF Family](#) videos.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The LSF devices can perform voltage translation for open-drain or push-pull interfaces. [Table 8-1](#) provides common interfaces and the corresponding device recommendation from the LSF family which supports the corresponding bit count.

**Table 8-1. Voltage Translator for Common Interfaces**

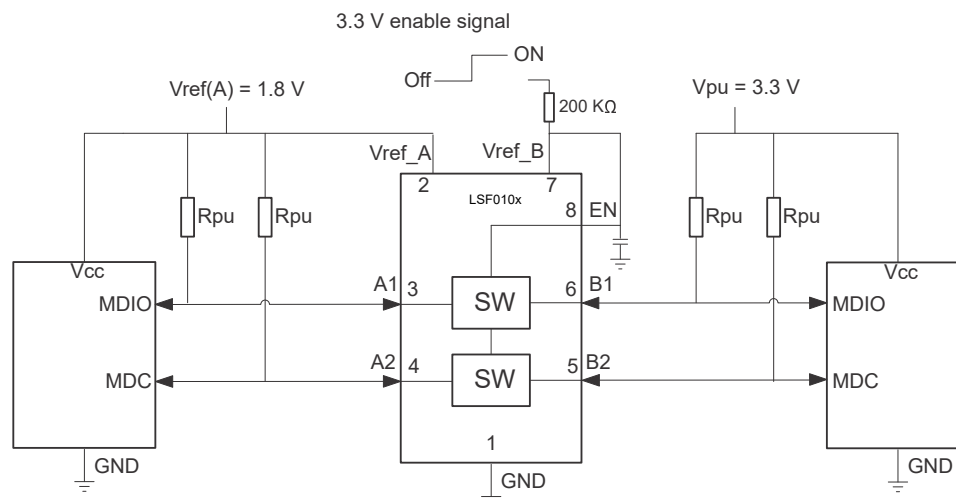
Part Name	Channel Number	Interface
LSF0102	2	GPIO, MDIO, SMBus, PMBus, and I <sup>2</sup> C

Some important reminders regarding the LSF family of devices are as follows:

- LSF devices are switch-based, not buffer-based (for more information, see the TXB family for buffer-based devices).
- Specific data rates cannot be calculated by using  $1/T_{pd}$ .
- $V_{CCB}/V_{CCA}$  are not the same as  $V_{ref\_B}$  or  $V_{ref\_A}$ :  $V_{CCB}$  refers to the B-side supply voltage supplied to the LSF device, while  $V_{ref\_B}$  refers to the voltage at the  $V_{ref\_B}$  pin (pin 7 of Figure 9-1) on the other side of the 200k $\Omega$  resistor.

### 8.2 Typical Applications

#### 8.2.1 Open-Drain Interface (I<sup>2</sup>C, PMBus, SMBus, and GPIO)



**Figure 8-1. Typical Application Circuit for Open-Drain Translation (MDIO Shown as an Example)**

### 8.2.1.1 Design Requirements

#### 8.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

In the previous figure,  $V_{ref\_B}$  is connected through a 200kΩ resistor to a 3.3V power supply and  $V_{ref\_A}$  is set to 1.8V. The A1 and A2 channels have a maximum output voltage equal to  $V_{ref\_A}$  and the B1 and B2 channels have a maximum output voltage equal to  $V_{PU}$ .

The LSF family has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the LSF family of devices are switch-type voltage translators, the power consumption is very low. TI recommends always enabling the LSF family for bidirectional applications (I<sup>2</sup>C, SMBus, PMBus, or MDIO).

**Table 8-2. Application Operating Condition**

PARAMETER	MIN	TYP	MAX	UNIT
$V_{ref\_A}$ <sup>(1)</sup>	0.9		5.5	V
$V_{ref\_B}$	$V_{ref\_A} + 0.8$		5.5	V
$V_{I(EN)}$	$V_{ref\_A} + 0.8$		5.5	V
$V_{PU}$	0		$V_{ref\_B}$	V

(1)  $V_{ref\_A}$  is required to be the lowest voltage level across all inputs and outputs.

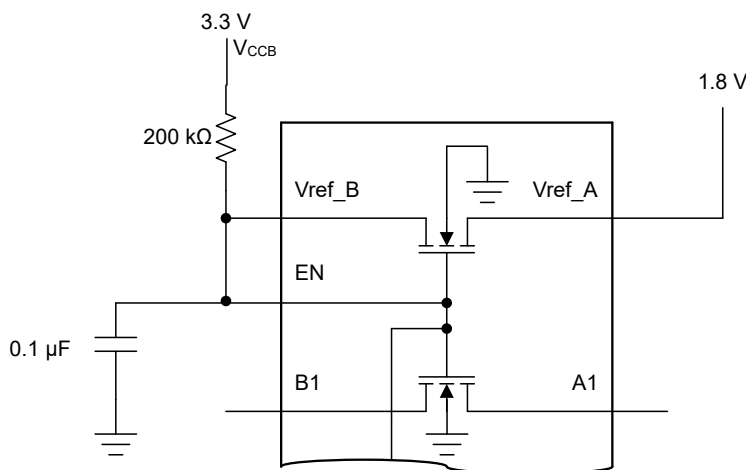
#### Note

The 200kΩ, bias resistor is required to allow  $V_{ref\_B}$  to regulate the EN input and properly bias the device for translation.

#### 8.2.1.1.2 Bias Circuitry

For proper operation,  $V_{CCA}$  must always be at least 0.8V less than  $V_{CCB}$  ( $V_{CCA} + 0.8 \leq V_{CCB}$ ). The 200kΩ bias resistor is required to allow  $V_{ref\_B}$  to regulate the EN input and properly bias the device for translation. A 0.1 μF capacitor is recommended for providing a path from  $V_{ref\_B}$  to ground for high frequency noise.  $V_{ref\_B}$  and  $V_{I(EN)}$  are recommended to be 1.0V higher than  $V_{ref\_A}$  for best signal integrity.

Attempting to drive the EN pin directly with a push-pull output device is a very common design error with the LSF0102 series of devices. It is also very important to note that current does flow into the A-side voltage supply during normal operation. Not all voltage sources can sink current, so be sure that applicable designs can handle this current. For more design details, see the [Understanding the Bias Circuit for the LSF Family](#) video.



**Figure 8-2. Bias Circuitry Inside the LSF010x Device**

## 8.2.1.2 Detailed Design Procedure

### 8.2.1.2.1 Bidirectional Translation

For the bidirectional translation configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to  $V_{ref\_B}$  and both pins must be pulled up to the HIGH side  $V_{CCB}$  through a bias resistor (typically 200k $\Omega$ ). This allows  $V_{ref\_B}$  to regulate the EN input and bias the channels for proper translation. A filter capacitor on  $V_{ref\_B}$  is recommended for a stable supply at the device. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to  $V_{PU}$ ).

#### Note

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW bus contention in either direction. If both outputs are open-drain, no direction control is needed.

### 8.2.1.2.2 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. Doing this causes a voltage drop of 260 mV to 350 mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15mA, the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15mA, calculate the pull-up resistor value using the following equation:

$$R_{pu} = \frac{(V_{pu} - 0.35 V)}{0.015 A} \quad (3)$$

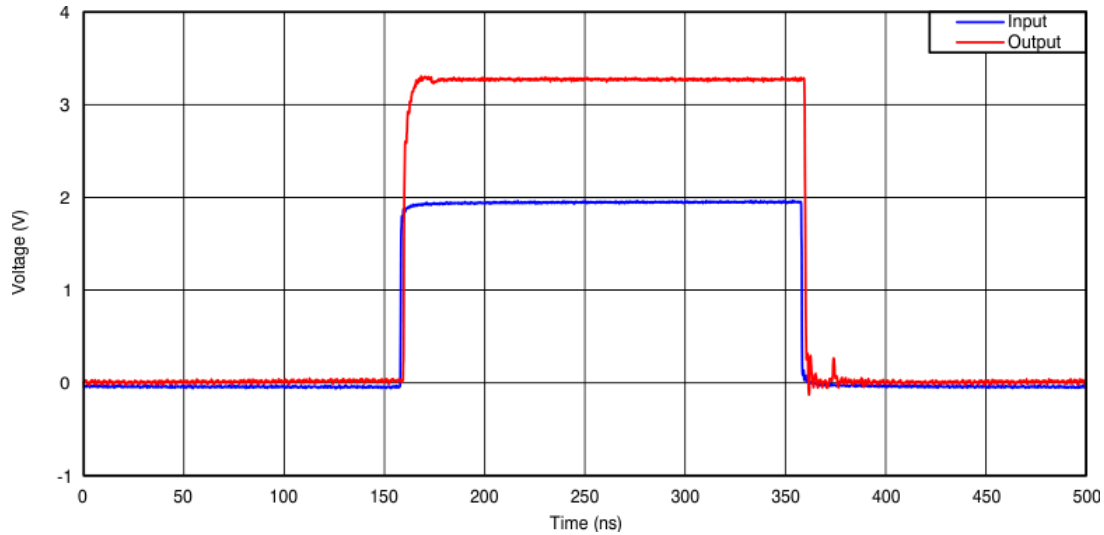
Table 8-3 provides resistor values, reference voltages, and currents at 8mA, 5mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used so that the voltage drop across the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175V, although the 15mA applies only to current flowing through the LSF family device. The device driving the low state at 0.175V must sink current from one or more of the pull-up resistors and maintain  $V_{OL}$ . A decrease in resistance will increase current, and thus result in increased  $V_{OL}$ .

**Table 8-3. Pull-Up Resistor Values**

$V_{PU}$ (1) (2)	8mA		5mA		3mA	
	NOMINAL ( $\Omega$ )	+10% <sup>(3)</sup> ( $\Omega$ )	NOMINAL ( $\Omega$ )	+10% <sup>(3)</sup> ( $\Omega$ )	NOMINAL ( $\Omega$ )	+10% <sup>(3)</sup> ( $\Omega$ )
5V	581	639	930	1023	1550	1705
3.3V	369	406	590	649	983	1082
2.5V	269	296	430	473	717	788
1.8V	181	199	290	319	483	532
1.5V	144	158	230	253	383	422
1.2V	106	117	170	187	283	312

- (1) Calculated for  $V_{OL} = 0.35V$   
(2) Assumes output driver  $V_{OL} = 0.175V$  at stated current  
(3) +10% to compensate for  $V_{DD}$  range and resistor tolerance

### 8.2.1.3 Application Curve



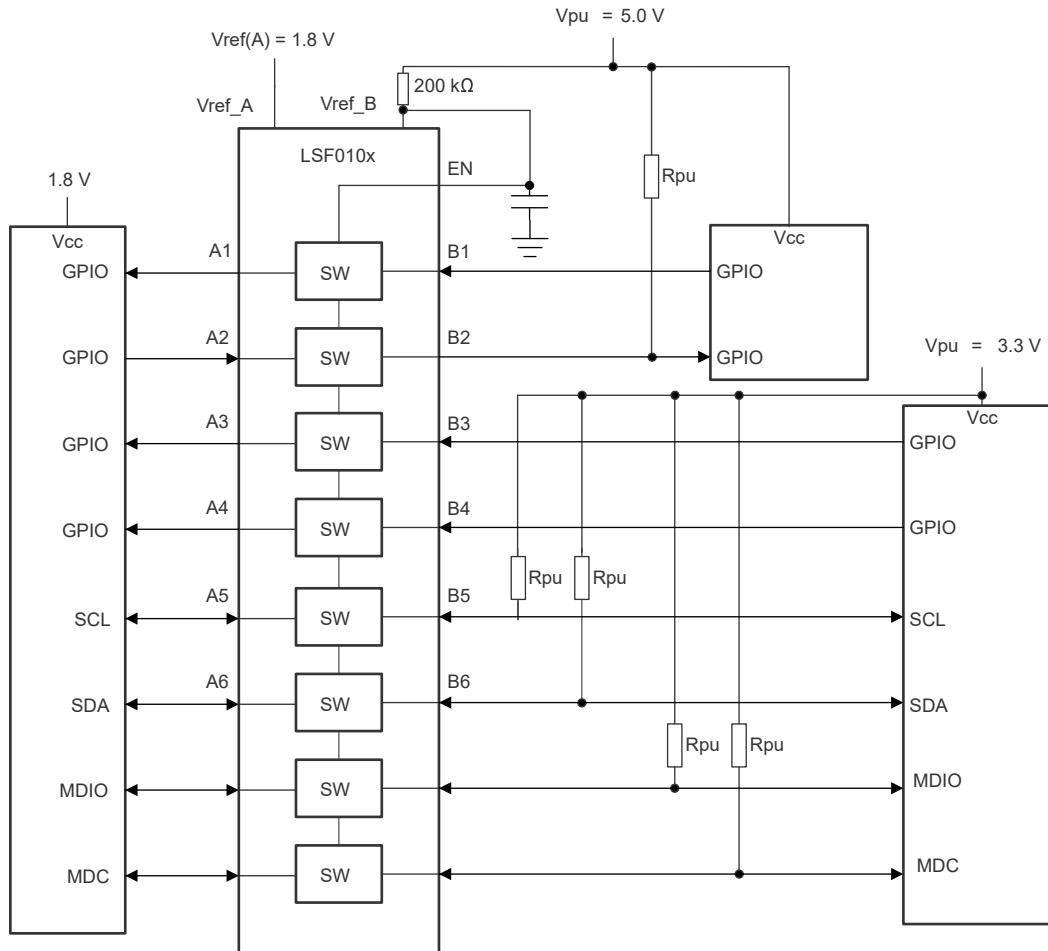
**Figure 8-3. Open Drain Translation (1.8V to 3.3V at 2.5MHz)**

### 8.2.2 Mixed-Mode Voltage Translation

The supply voltage ( $V_{PU}$ ) for each channel can be individually set with a pull-up resistor. [Figure 8-4](#) shows an example of this mixed-mode multi-voltage translation. For additional details on multi-voltage translation, see the [Multi-voltage Translation with the LSF Family](#) video.

With the  $V_{ref\_B}$  pulled up to 5V and  $V_{ref\_A}$  connected to 1.8V, all channels will be clamped to 1.8V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5V to 1.8V):** Channel 1 is an example of this setup. When B1 is 5V, A1 is clamped to 1.8V, and when B1 is LOW, A1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.8V to 5V):** Channel 2 is an example of this setup. When A2 is 1.8V, the switch is high impedance and the B2 channel is pulled up to 5V. When A2 is LOW, B2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3V to 1.8V):** Channels 3 and 4 are examples of this setup. When either B3 or B4 are driven to 3.3V, A3 or A4 are clamped to 1.8V, and when either B3 or B4 are LOW, A3 or A4 are driven LOW through the switch.
- **Open-Drain Bidirectional Translation (3.3V ↔ 1.8V):** Channels 5 through 8 are examples of this setup. These channels are for bidirectional operation for I<sup>2</sup>C and MDIO to translate between 1.8V and 3.3V with open-drain drivers.

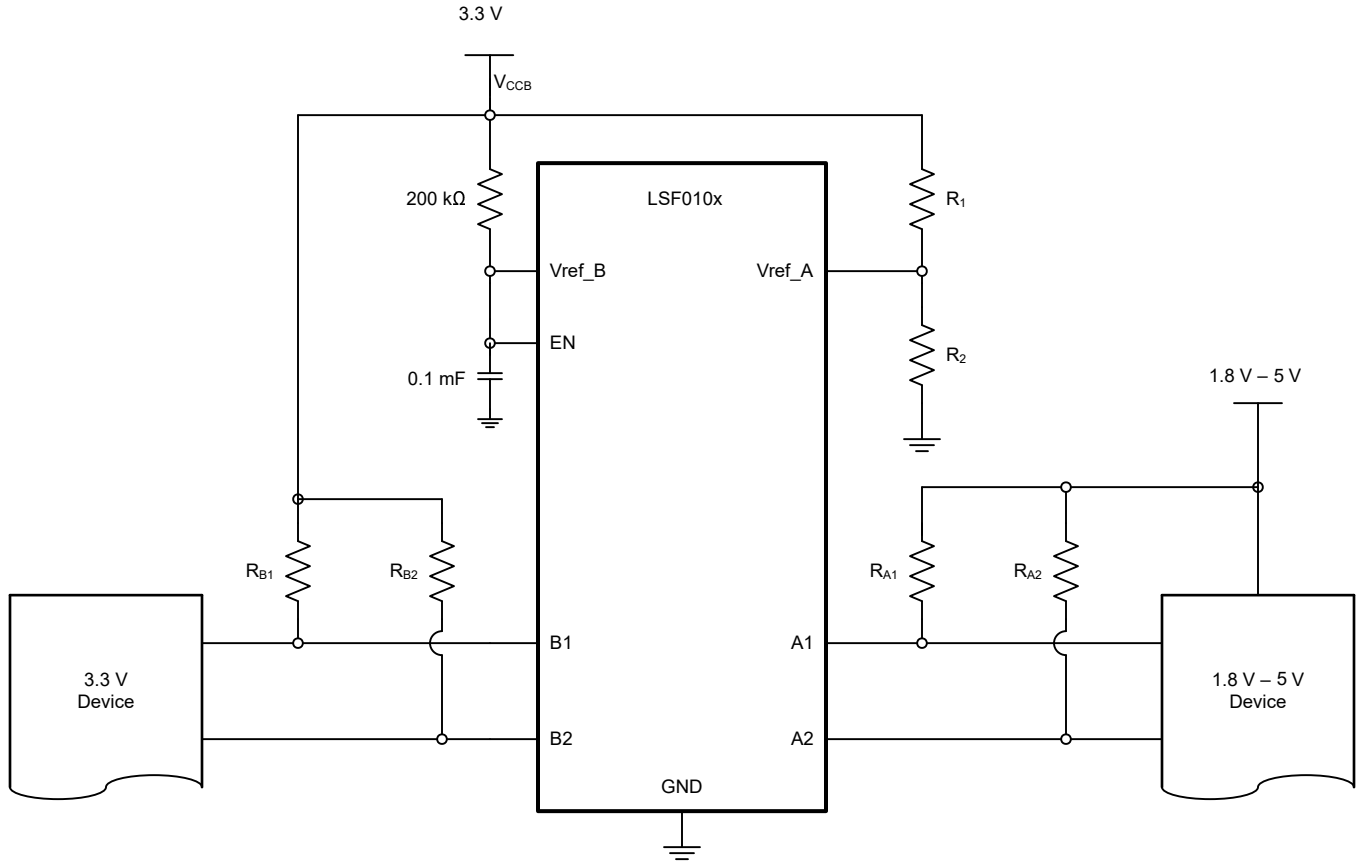


**Figure 8-4. Multi-Voltage Translation with the LSF010x**

### 8.2.3 Single Supply Translation

Sometimes, an external device will have an unknown voltage that could be above or below the desired translation voltage, preventing a normal connection of the LSF. Resistors are added on the A side in place of the second supply in this case – this is an example of when LSF single supply operation is utilized, shown in [Figure 9-5](#). In the following figure, a single 3.3V supply is used to translate between a 3.3V device and a device that can change between 1.8V and 5.0V. R1 and R2 are added in place of the second supply. Note that due to some current coming out of the  $V_{ref\_A}$  pin, this cannot be treated as a simple voltage divider.





**Figure 8-5. Single Supply Translation with 3.3V Supply**

The steps to select the resistor values for R1 and R2 are as follows:

1. Select a value for R1. Typically, 1MΩ is used to reduce current consumption.
2. Plug in values for your system into the following equation. Note that  $V_{ref\_A}$  is the lowest voltage in the system.  $V_{CCB}$  is the primary supply and R1 is the selected value from step 1.

$$R_2 = \frac{200 \left(10^3\right) \times R_1 \times V_{REFA}}{\left(200 \left(10^3\right) + R_1\right) \left(V_{CCB} - V_{REFA}\right) - 0.85 \times R_1} \quad (4)$$

The single supply used must be at least 0.8V larger than the lowest desired translation voltage. The voltage at  $V_{ref\_A}$  must be selected as the lowest voltage to be used in the system. The LSF evaluation module (LSF-EVM) contains unpopulated pads to place R1 and R2 for single supply operation testing. For an example single supply translation schematic and details, see the [Single Supply Translation with the LSF Family](#) video.

### 8.2.4 Voltage Translation for $V_{ref\_B} < V_{ref\_A} + 0.8V$

As described in the *Enable, Disable, and Reference Voltage Guidelines* section, it is generally recommended that  $V_{ref\_B} > V_{ref\_A} + 0.8V$ ; however, the device can still operate in the condition where  $V_{ref\_B} < V_{ref\_A} + 0.8V$  as long as additional considerations are made for the design.

**Typical Operation ( $V_{ref\_B} > V_{ref\_A} + 0.8V$ ):** in this scenario, pullup resistors are not required on the A-side for proper down-translation. When down translating from B to A, the A-side I/O ports will clamp at  $V_{ref\_A}$  to provide proper voltage translation. For further explanation of device operation, see the [Down Translation with the LSF Family](#) video.

**Requirements for  $V_{ref\_B} < V_{ref\_A} + 0.8V$  Operation:** in this scenario, there is not a large enough voltage difference between  $V_{ref\_A}$  and  $V_{ref\_B}$  to ensure that the A side I/O ports will be clamped at  $V_{ref\_A}$ , but rather at a voltage approximately equal to  $V_{ref\_B} - 0.8V$ . For example, if  $V_{ref\_B} = 1.8V$  and  $V_{ref\_A} = 1.2V$ , the A-side I/Os will clamp to a voltage around 1.0V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- $V_{ref\_B}$  must be greater than  $V_{ref\_A}$  during operation ( $V_{ref\_B} > V_{ref\_A}$ )
- Pullup resistors should be populated on A-side I/O ports for the line to be fully pulled up to the desired voltage.

Figure 8-6 shows an example of this setup, where 1.2V ↔ 1.8V translation is achieved with the LSF0102. This type of setup also applies for other voltage nodes such as 1.8V ↔ 2.5V, 1.05V ↔ 1.5V, and others as long as the [Recommended Operating Conditions](#) table is followed.

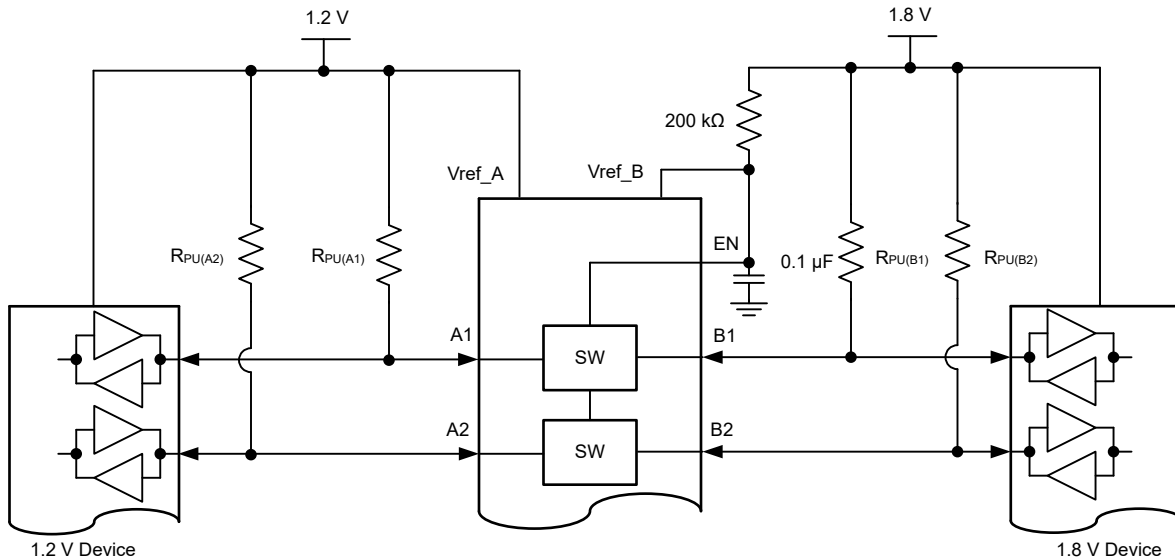


Figure 8-6. 1.2V to 1.8V Level Translation with LSF010x

### 8.3 Power Supply Recommendations

There are no power sequence requirements for the LSF family. [Table 8-4](#) provides recommended operating voltages for all supply and input pins.

Table 8-4. Recommended Operating Voltages

PARAMETER	MIN	TYP	MAX	UNIT
$V_{ref\_A}$ <sup>(1)</sup>	reference voltage (A)	0.9	5.5	V
$V_{ref\_B}$	reference voltage (B)	$V_{ref\_A} + 0.8$	5.5	V
$V_{I(EN)}$	input voltage on EN pin	$V_{ref\_A} + 0.8$	5.5	V
$V_{PU}$	pull-up supply voltage	0	$V_{ref\_B}$	V

(1)  $V_{ref\_A}$  is required to be the lowest voltage level across all inputs and outputs.

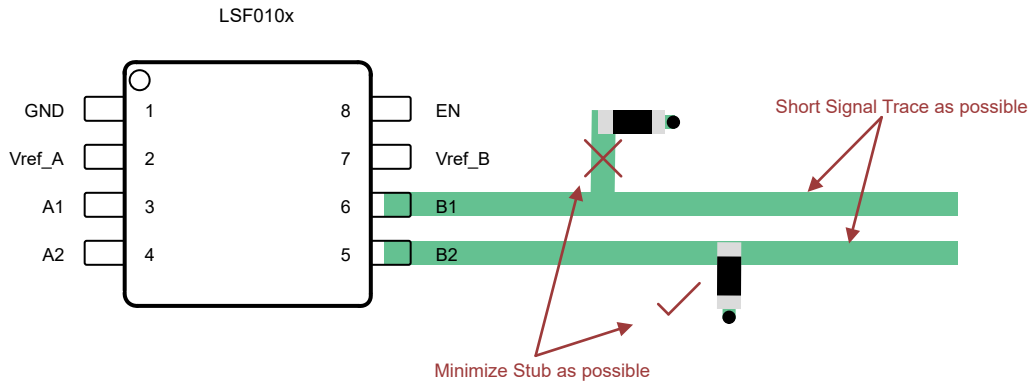
## 8.4 Layout

### 8.4.1 Layout Guidelines

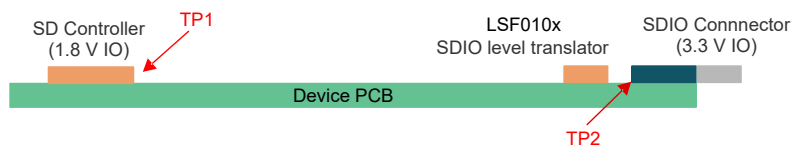
Because the LSF family is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF device close to the high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of the transmitter.

### 8.4.2 Layout Example



**Figure 8-7. Short Trace Layout**



**Figure 8-8. Device Placement**

## 9 Device and Documentation Support

### 9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LSF Translator Family Evaluation Module user's guide](#)
- Texas Instruments, [Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators application note](#)
- Texas Instruments, [Voltage Level Translation with the LSF Family application note](#)
- The Logic Minute Video Training Series on Understanding the LSF Family of Devices:
  - Texas Instruments, [Introduction - Voltage Level Translation with the LSF Family](#)
  - Texas Instruments, [Understanding the Bias Circuit for the LSF Family](#)
  - Texas Instruments, [Using the Enable Pin with the LSF Family](#)
  - Texas Instruments, [Translation Basics with the LSF Family](#)
  - Texas Instruments, [Down Translation with the LSF Family](#)
  - Texas Instruments, [Up Translation with the LSF Family](#)
  - Texas Instruments, [Multi-Voltage Translation with the LSF Family](#)
  - Texas Instruments, [Single Supply Translation with the LSF Family](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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<b>Changes from Revision A (July 2023) to Revision B (April 2024)</b>	<b>Page</b>
• Added the <i>DTM (X2SON, 8)</i> package information throughout the datasheet.....	1
• Added the <i>Up and Down Translation</i> sections.....	11
• Added the <i>Bias Circuitry</i> section.....	13

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<b>Changes from Revision * (April 2023) to Revision A (July 2023)</b>	<b>Page</b>
• Updated the <i>Package Information</i> table format to include package leads.....	1
• Updated the <i>Recommended Operating Conditions</i> table to reflect max of 5.5V.....	5
• Updated the <i>Thermal Information</i> table for DCU and DCT packages.....	5
• Updated the <i>Switching Characteristics Table for Translation Down and Up</i> table .....	6
• Changed <i>pull up resistor</i> to <i>bias resistor</i> in <i>Enable, Disable, and Reference Voltage Guidelines</i> section.....	13

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0102DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(1NT, NG2) (S, Y)	<a href="#">Samples</a>
LSF0102DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(G2, NG2J, NG2P, N G2S) NY	<a href="#">Samples</a>
LSF0102DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	F0102	<a href="#">Samples</a>
LSF0102DQER	ACTIVE	X2SON	DQE	8	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RV	<a href="#">Samples</a>
LSF0102DTMR	ACTIVE	X2SON	DTM	8	12000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K	<a href="#">Samples</a>
LSF0102YZTR	ACTIVE	DSBGA	YZT	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	RV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LSF0102 :**

- Automotive : [LSF0102-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

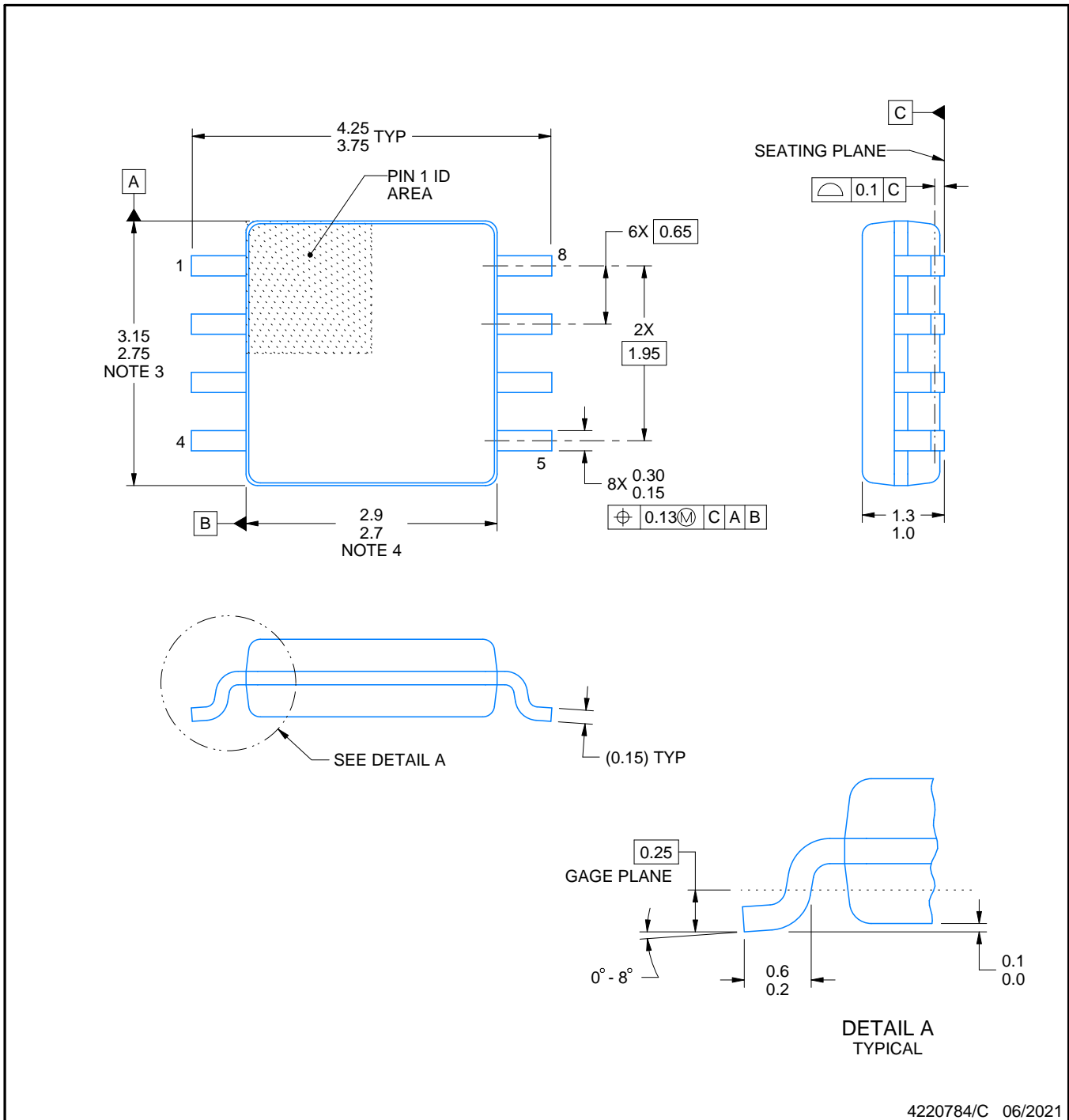
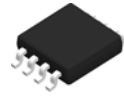
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0102DCTR	SM8	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
LSF0102DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
LSF0102DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3
LSF0102DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
LSF0102YZTR	DSBGA	YZT	8	3000	180.0	8.4	1.02	2.02	0.75	4.0	8.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0102DCTR	SM8	DCT	8	3000	190.0	190.0	30.0
LSF0102DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
LSF0102DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LSF0102DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
LSF0102YZTR	DSBGA	YZT	8	3000	182.0	182.0	20.0



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NOTES:

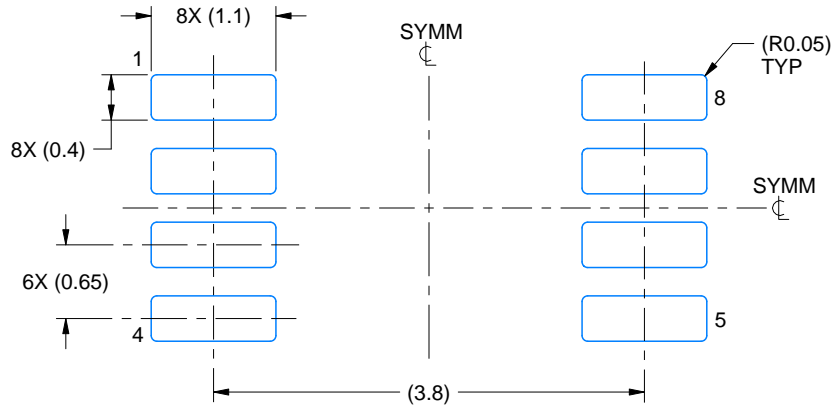
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

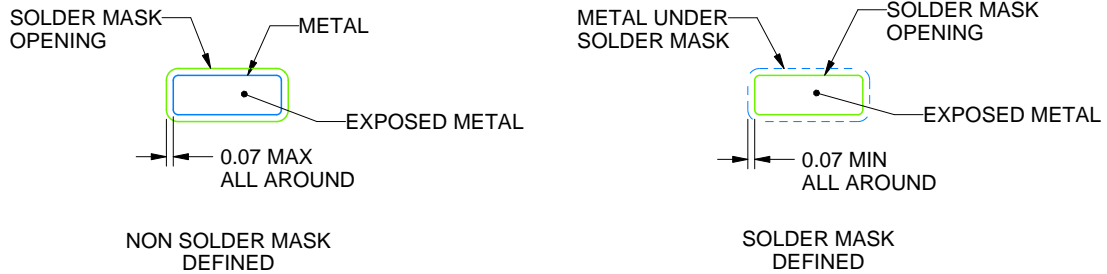
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

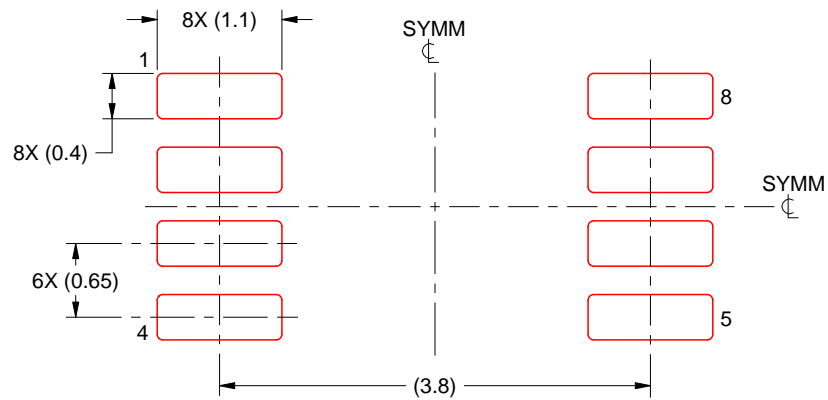
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

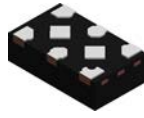


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

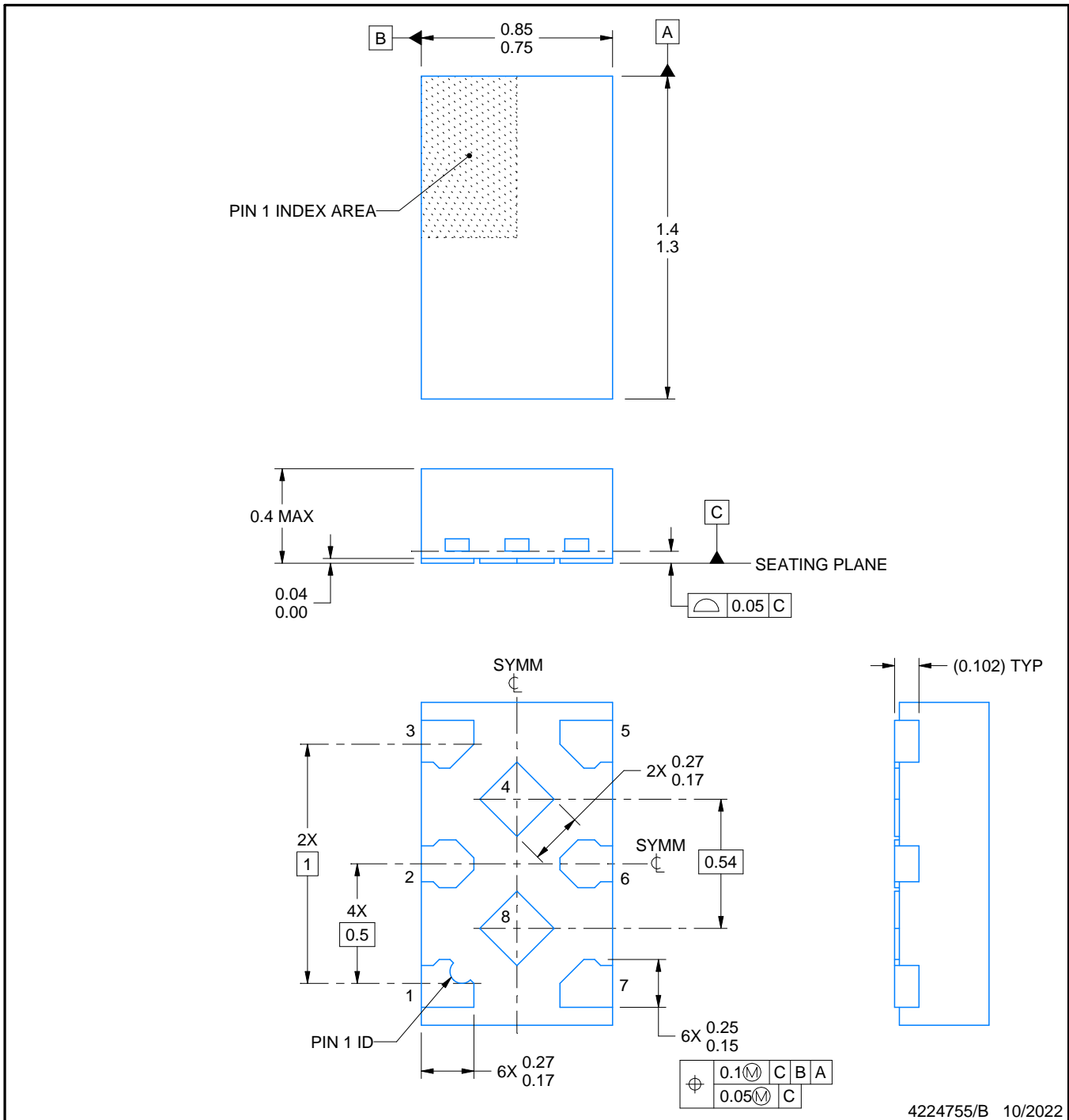


DTM0008A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4224755/B 10/2022

NOTES:

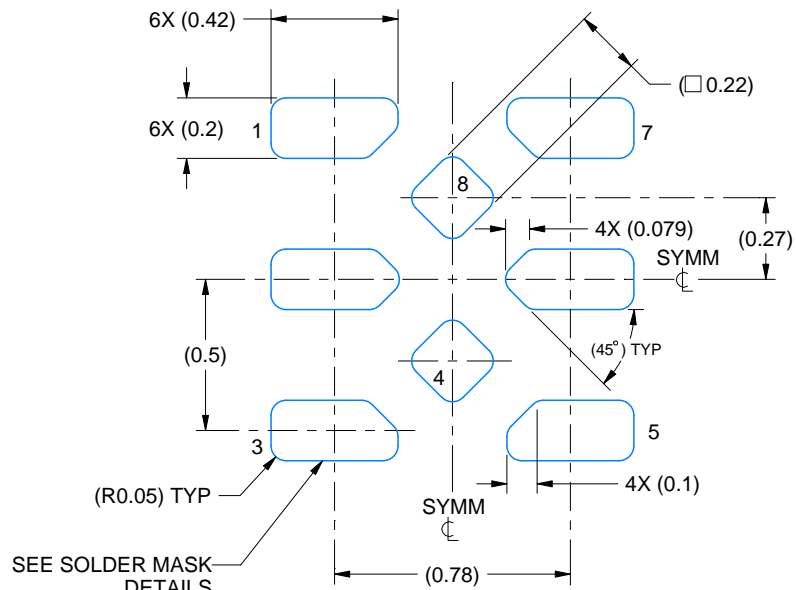
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

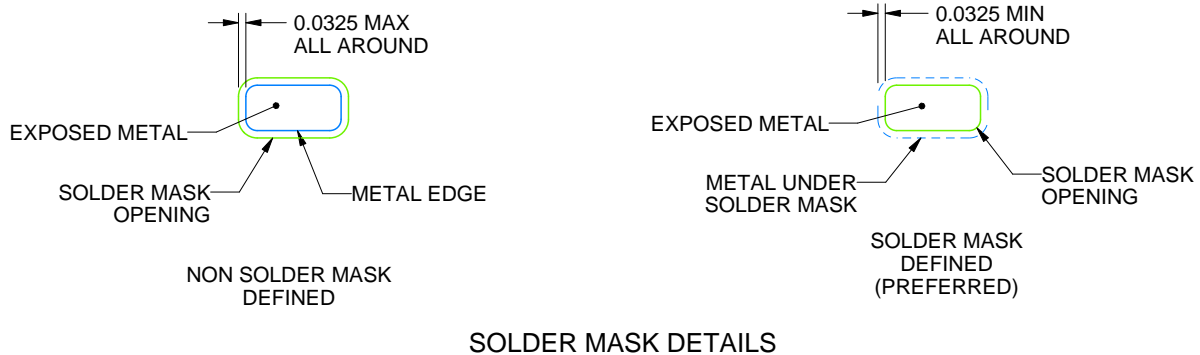
DTM0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4224755/B 10/2022

NOTES: (continued)

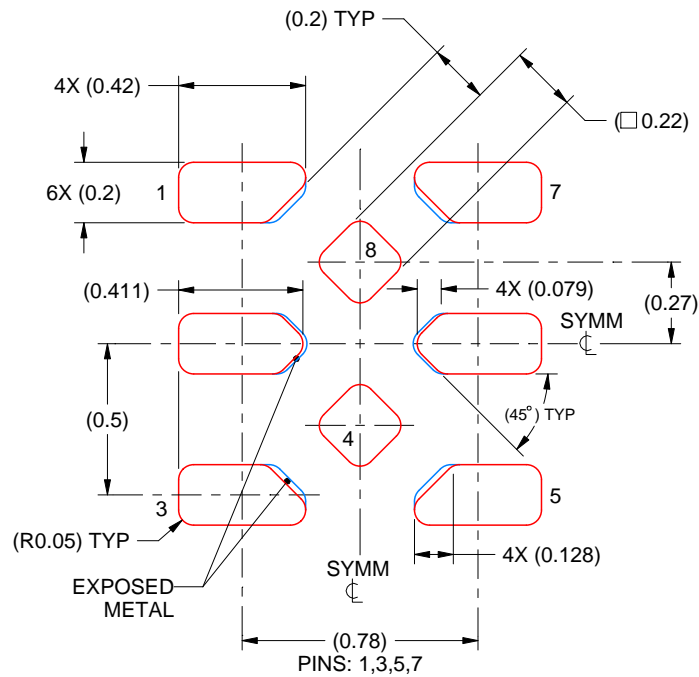
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DTM0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.075 mm THICK STENCIL  
SCALE: 40X

4224755/B 10/2022

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

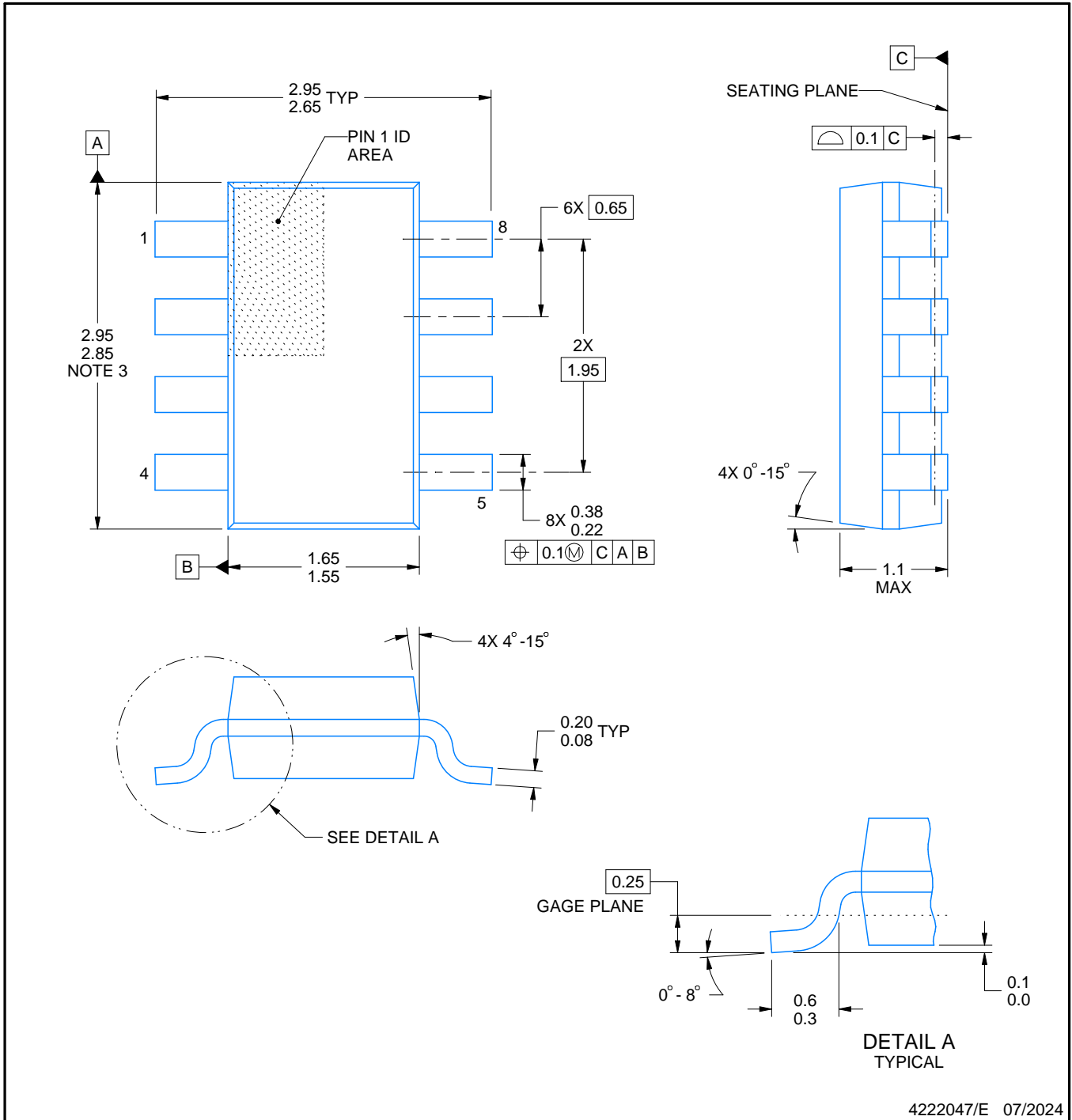
DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

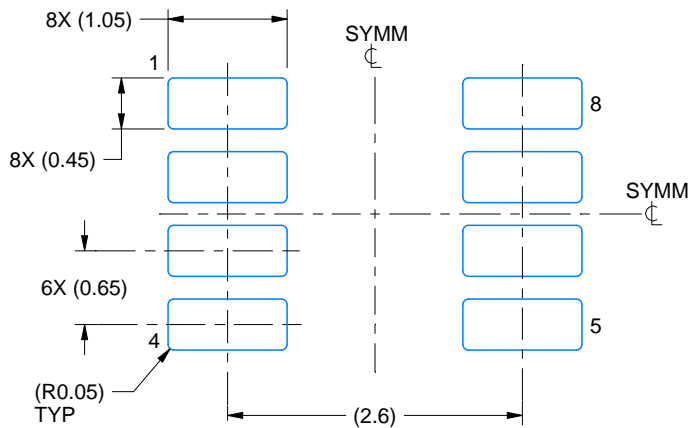


# EXAMPLE BOARD LAYOUT

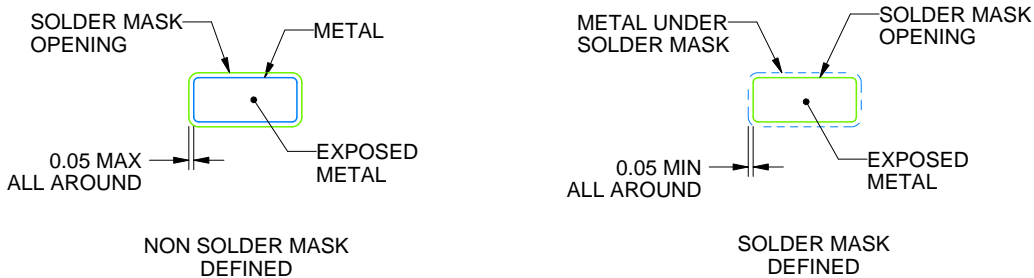
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

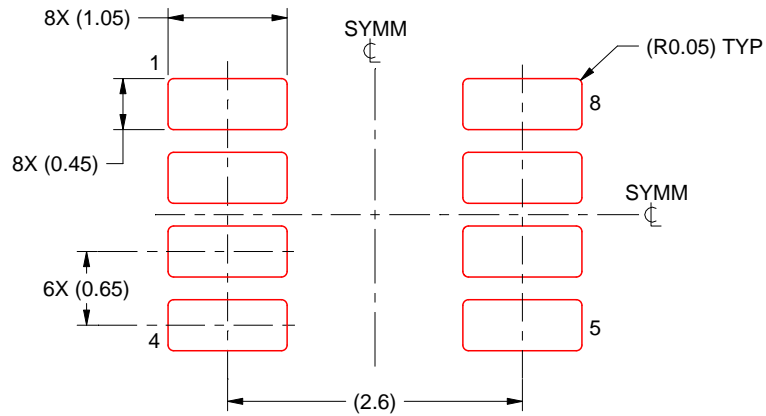
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

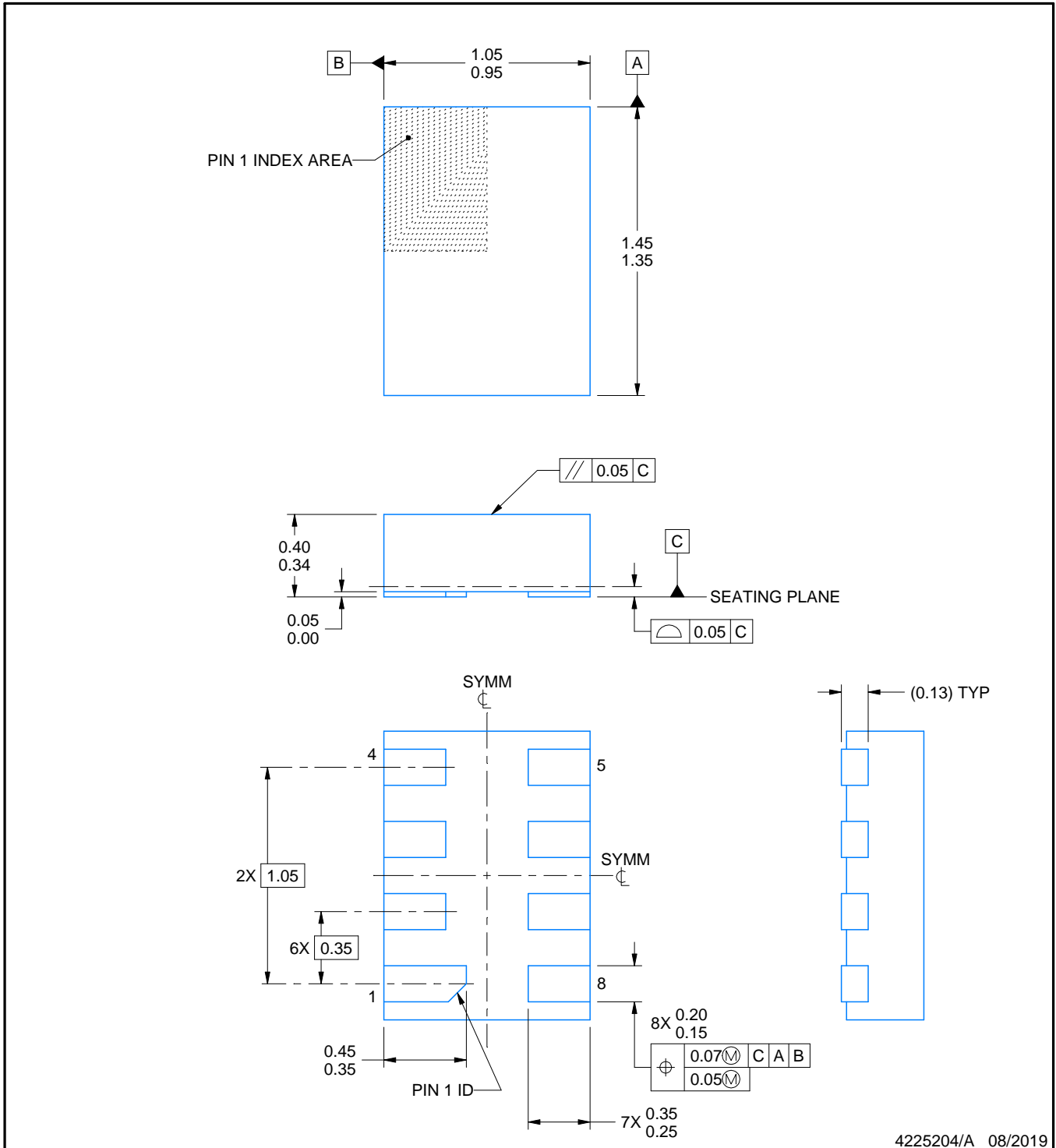
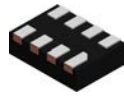


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



4225204/A 08/2019

NOTES:

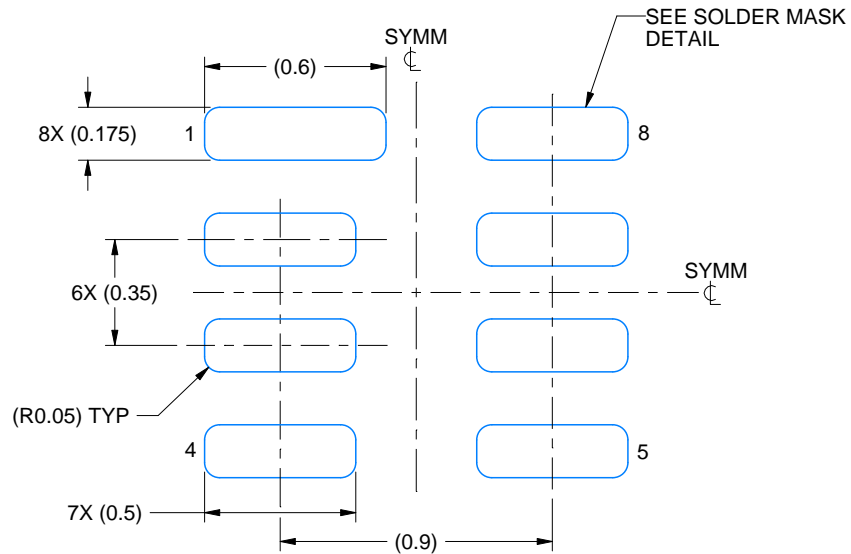
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

# EXAMPLE BOARD LAYOUT

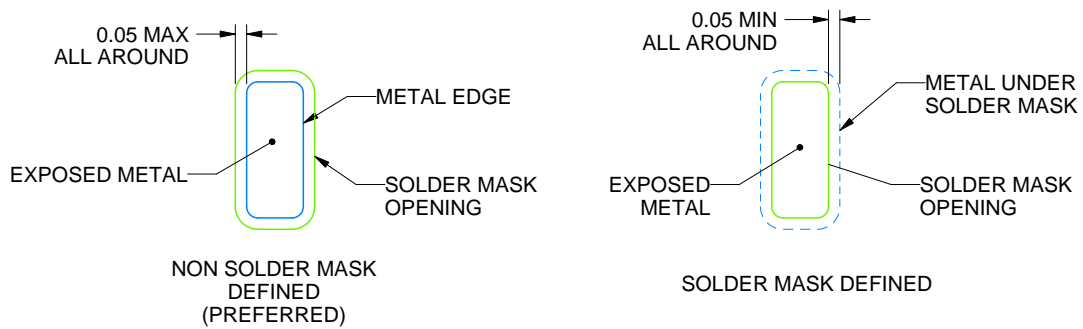
DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 40X



SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

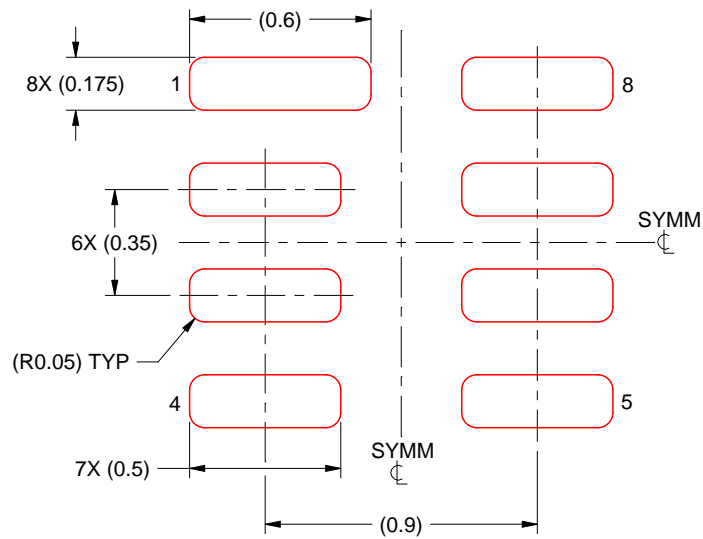
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DQE0008A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 MM THICK STENCIL  
SCALE: 40X

4225204/A 08/2019

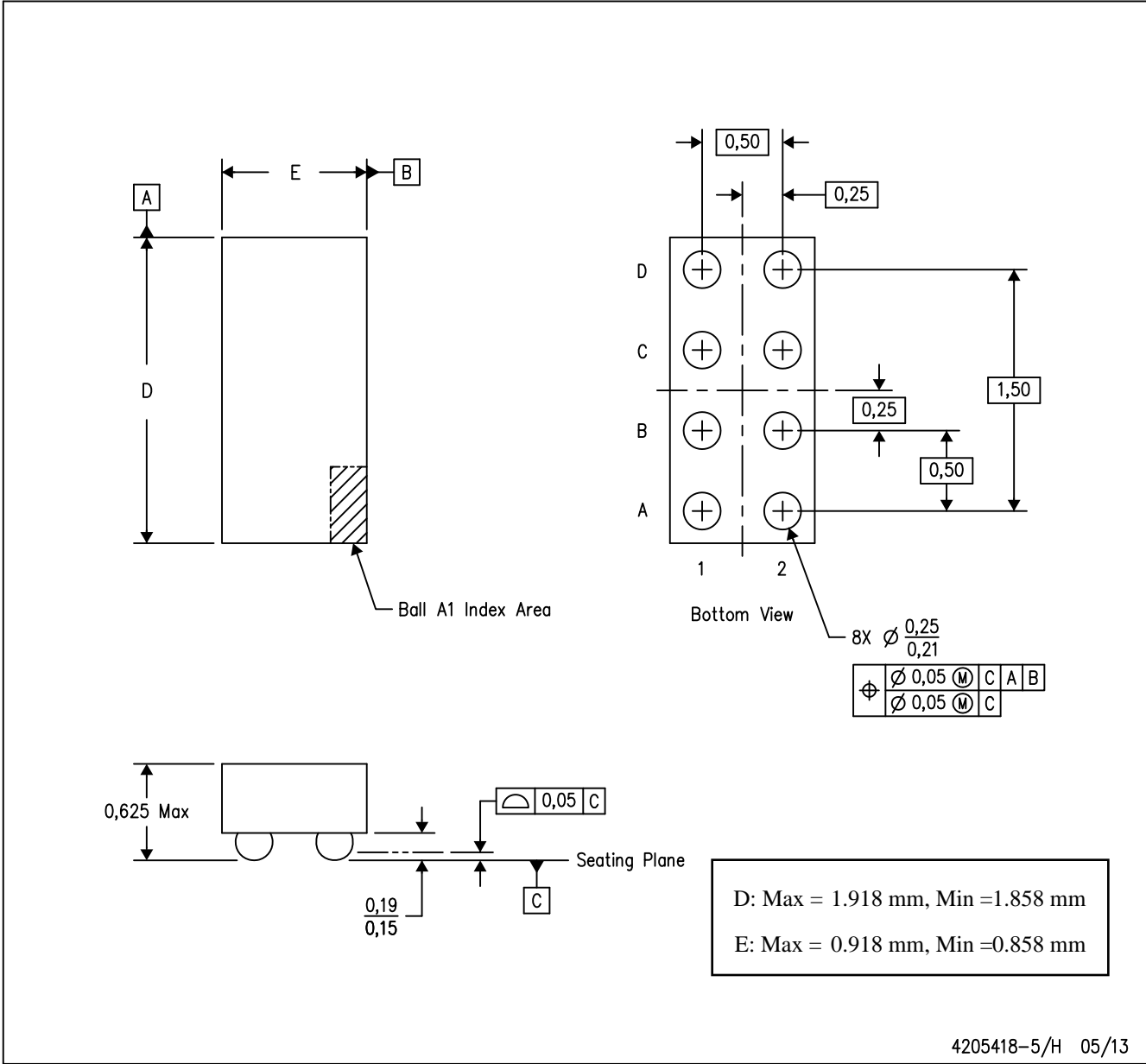
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**MECHANICAL DATA**

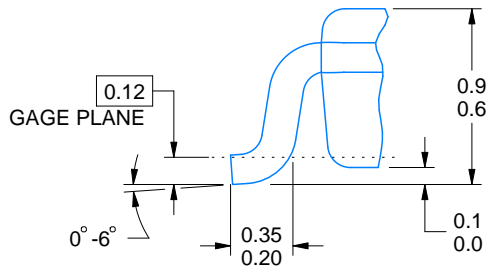
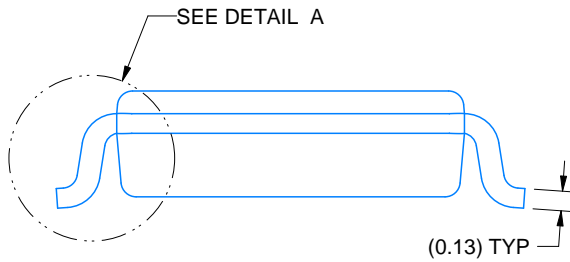
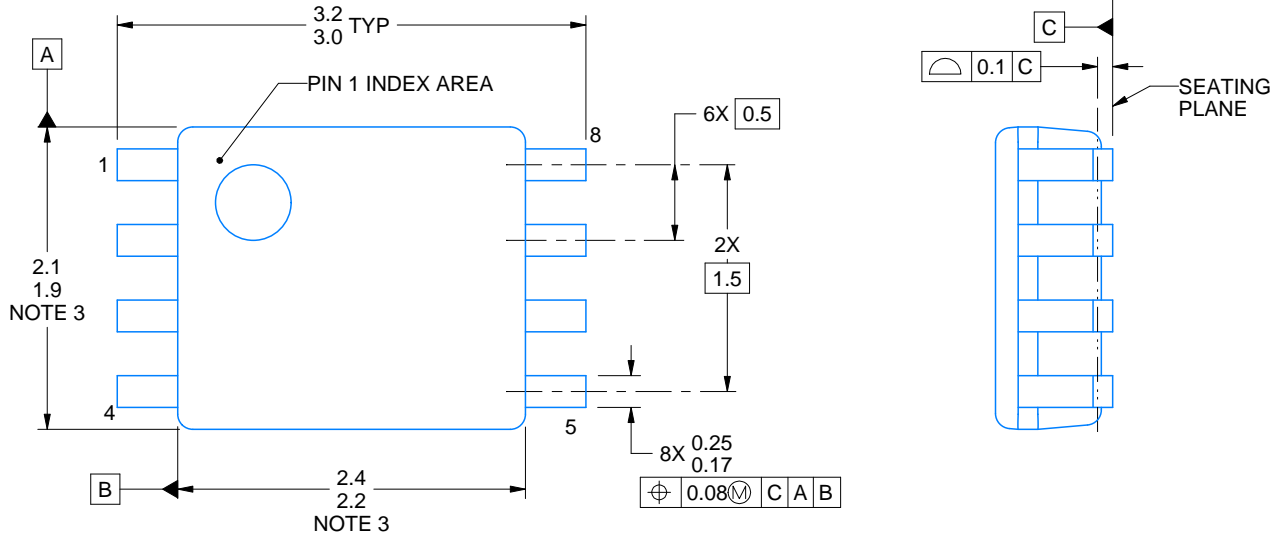
YZT (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



NOTES:

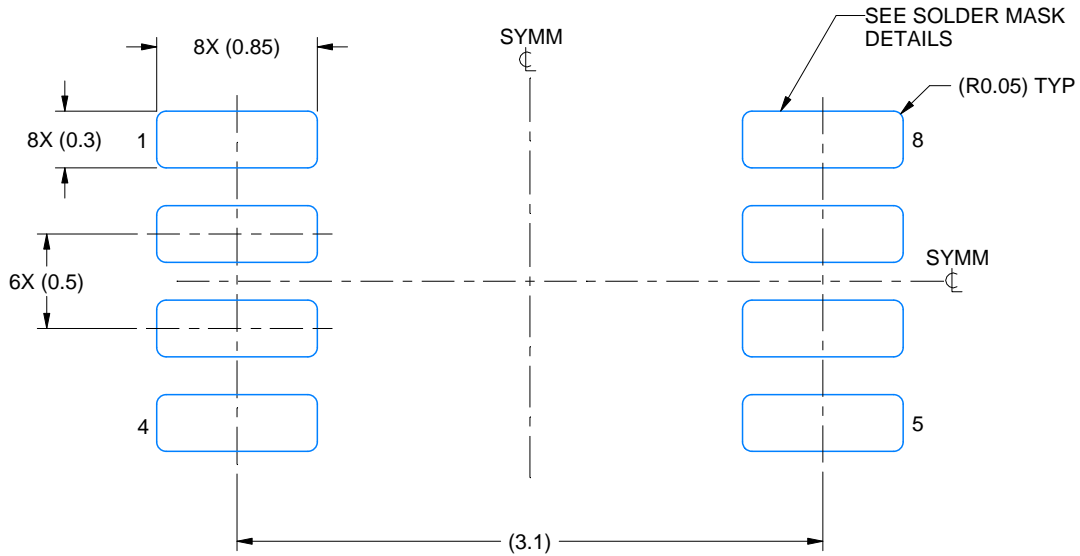
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

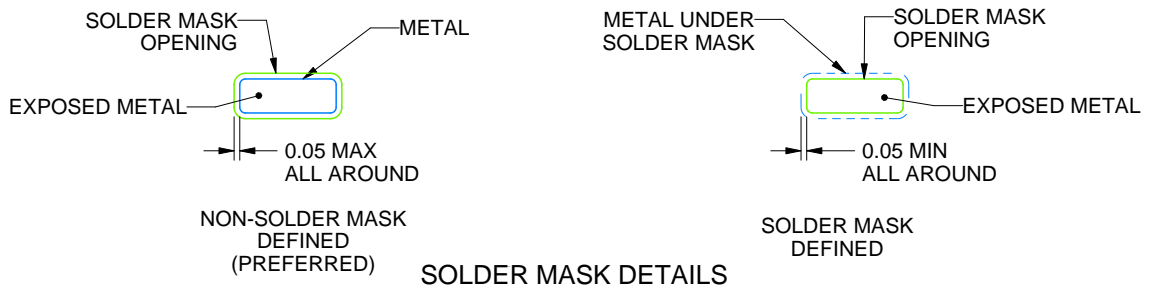
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

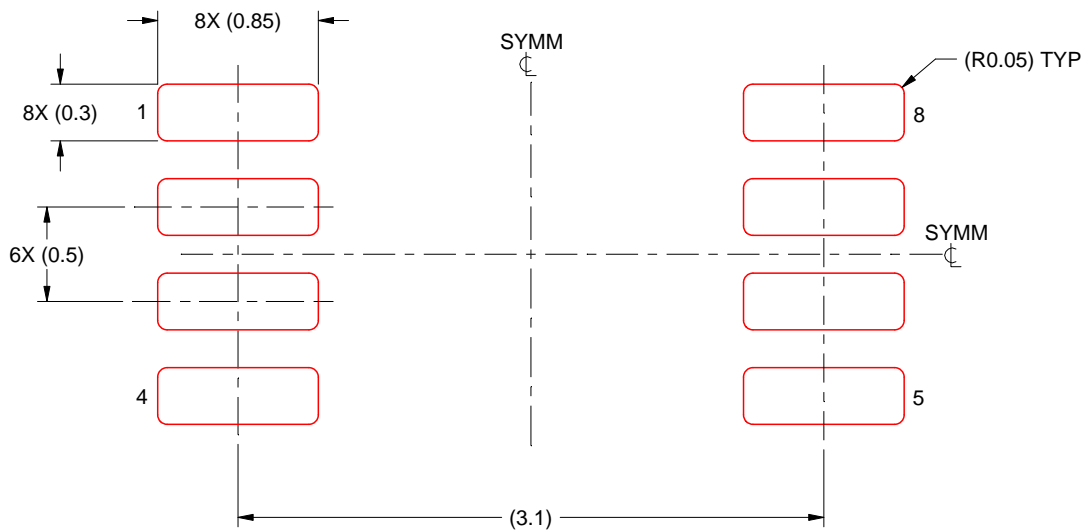


# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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