LMT86 2.2V, SC70/TO-92/TO-92S, Analog Temperature Sensor

1 Features

- LMT86LPG (TO-92S package) has a Fast Thermal Time Constant, 10s Typical (1.2m/s Airflow)
- Very accurate: ±0.4°C typical
- Low 2.2V operation
- Average sensor gain of –10.9mV/°C
- Low 5.4µA quiescent current
- Wide temperature range: –50°C to 150°C
- Output is short-circuit protected
- Push-pull output with ±50µA drive capability
- Footprint compatible with the industry-standard LM20/19 and LM35 temperature sensors
- Cost-effective alternative to thermistors

2 Applications

- Infotainment and cluster
- Powertrain systems
- Smoke and heat detectors
- Drones
- Appliances

3 Description

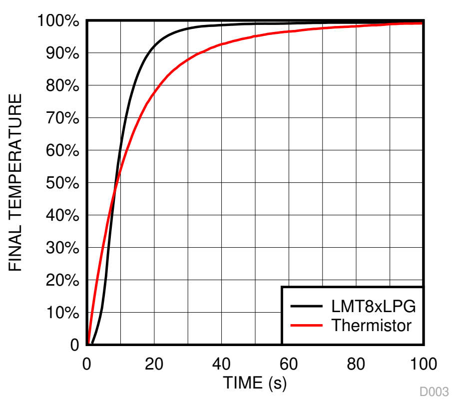
The LMT86 are precision CMOS temperature sensors with ±0.4°C typical accuracy (±2.7°C maximum) and a linear analog output voltage that is inversely proportional to temperature. The 2.2V supply voltage operation, 5.4µA quiescent current, and 0.7ms power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered applications such as drones and sensor nodes. The LMT86LPG through-hole TO-92S package fast thermal time constant supports off-board time-temperature sensitive applications such as smoke and heat detectors. The accuracy over the wide operating range and other features make the LMT86 an excellent alternative to thermistors.

For devices with different average sensor gains and comparable accuracy, refer to *Comparable Alternative Devices* for alternative devices in the LMT8x family.

Device Information(1)

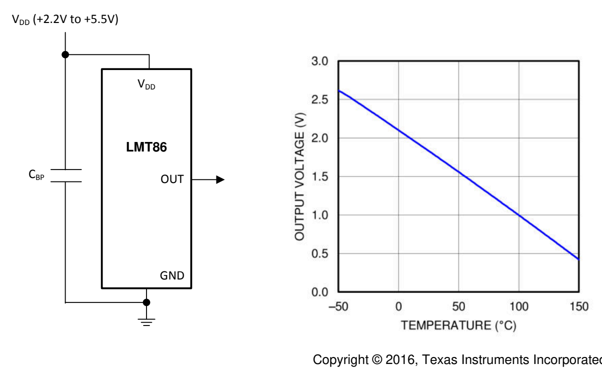
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMT86	SOT (5)	2.00mm × 1.25mm
	TO-92 (3)	4.30mm × 3.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



* Fast thermal response NTC

Thermal Time Constant



Output Voltage vs Temperature

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4 Device Comparison

Table 4-1. Available Device Packages

ORDER NUMBER(1)	PACKAGE	PIN	BODY SIZE (NOM)	MOUNTING TYPE
LMT86DCK	SOT (AKA(2): SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount
LMT86LP	TO-92 (AKA(2): LP)	3	4.30 mm × 3.50 mm	Through-hole; straight leads
LMT86LPG	TO-92S (AKA(2): LPG)	3	4.00 mm × 3.15 mm	Through-hole; straight leads
LMT86LPM	TO-92 (AKA(2): LPM)	3	4.30 mm × 3.50 mm	Through-hole; formed leads
LMT86DCK-Q1	SOT (AKA(2): SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount

(1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.
(2) AKA = Also Known As

Table 4-2. Comparable Alternative Devices

DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
LMT84	–5.5 mV/°C	1.5 V to 5.5 V
LMT85	–8.2 mV/°C	1.8 V to 5.5 V
LMT86	–10.9 mV/°C	2.2 V to 5.5 V
LMT87	–13.6 mV/°C	2.7 V to 5.5 V

5 Pin Configuration and Functions

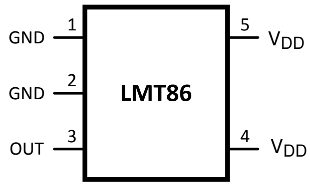
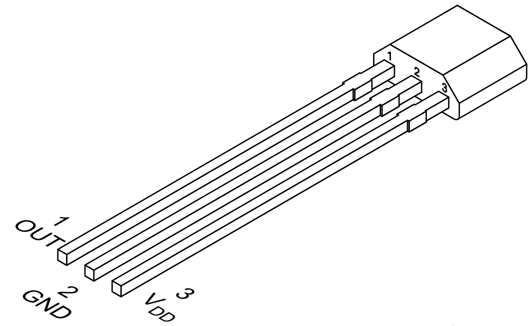
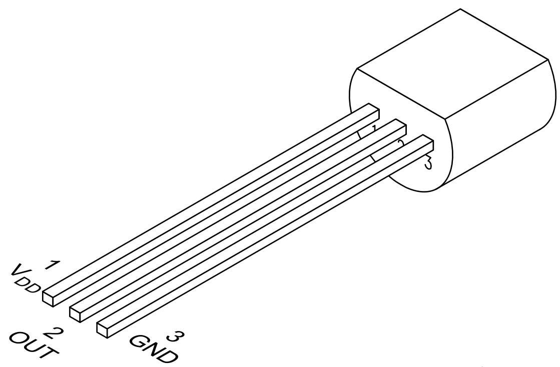


Figure 5-1. 5-Pin SOT (SC70) DCK Package (TOP VIEW)



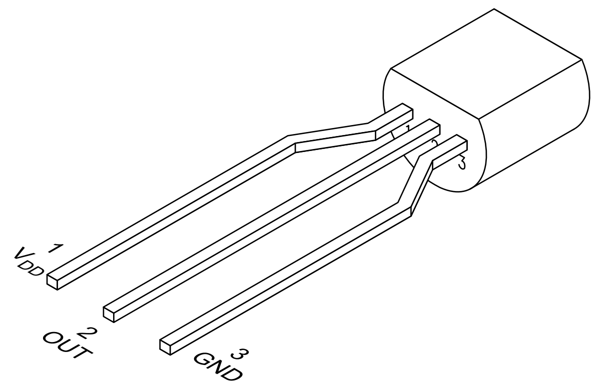
Scale: 4:1

Figure 5-2. LPG Package 3-Pin TO-92S (Top View)



Scale: 4:1

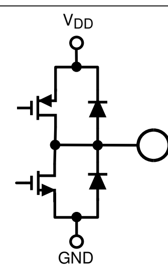
Figure 5-3. LP Package 3-Pin TO-92 (Top View)



Scale: 4:1

Figure 5-4. LPM Package 3-Pin TO-92 (Top View)

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION	
NAME	SOT (SC70)	TO-92	TO-92S		EQUIVALENT CIRCUIT	FUNCTION
GND	1, 2(1)	3	2	Ground	N/A	Power Supply Ground
OUT	3	2	1	Analog Output		Outputs a voltage that is inversely proportional to temperature
V_{DD}	4, 5	1	3	Power	N/A	Positive Supply Voltage

(1) Direct connection to the back side of the die

6 Specifications

6.1 Absolute Maximum Ratings

See (1) (2)

	MIN	MAX	UNIT
Supply voltage	–0.3	6	V
Voltage at output pin	–0.3	(V_{DD} + 0.5)	V
Output current	–7	7	mA
Input current at any pin (3)	–5	5	mA
Maximum junction temperature (T_{JMAX})		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. Reflow temperature profiles are different for lead-free and non-lead-free packages.
(3) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V), the current at that pin should be limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
LMT86LP in TO-92 package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
LMT86DCK in SC70 package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per JESD22-A114(2)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified temperature	$T_{MIN} \le T_A \le T_{MAX}$		°C
	$-50 \le T_A \le 150$		°C
Supply voltage (V_{DD})	2.2	5.5	V

6.4 Thermal Information

THERMAL METRIC(1) (2)		LMT86	LMT86LP	LMT86LPG	UNIT
		DCK (SOT/SC70)	LP/LPM (TO-92)	LPG (TO-92S)	
		5 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3) (4)	275	167	130.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84	90	64.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	146	106.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	35	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	146	106.2	°C/W

(1) For information on self-heating and thermal response time, see section *Mounting and Thermal Conductivity*.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(3) The junction to ambient thermal resistance ($R_{\theta JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(4) Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

6.5 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in Table 7-1.

PARAMETER	CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
Temperature accuracy[3]	40°C to 150°C; V_{DD} = 2.2 V to 5.5 V	–2.7	±0.4	2.7	°C
	0°C to 40°C; V_{DD} = 2.4 V to 5.5 V	–2.7	±0.7	2.7	°C
	0°C to 70°C; V_{DD} = 3.0 V to 5.5 V		±0.3		°C
	–50°C to 0°C; V_{DD} = 3.0 V to 5.5 V	–2.7	±0.7	2.7	°C
	–50°C to 0°C; V_{DD} = 3.6 V to 5.5 V		±0.25		°C

(1) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no dc load.

6.6 Electrical Characteristics

Unless otherwise noted, these specifications apply for +V_{DD} = 2.2 V to 5.5 V. MIN and MAX limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted; typical values apply for $T_A = T_J$ = 25°C.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
	Average sensor gain (output transfer function slope)	–30°C and 90°C used to calculate average sensor gain		–10.9		mV/°C
	Load regulation[3]	Source ≤ 50 µA, (V_{DD} – V_{OUT}) ≥ 200 mV	–1	–0.22		mV
		Sink ≤ 50 µA, V_{OUT} ≥ 200 mV		0.26	1	mV
	Line regulation[4]			200		µV/V
I_S	Supply current	T_A = 30°C to 150°C, (V_{DD} – V_{OUT}) ≥ 100 mV		5.4	8.1	µA
		T_A = –50°C to 150°C, (V_{DD} – V_{OUT}) ≥ 100 mV		5.4	9	µA
C_L	Output load capacitance			1100		pF
	Power-on time[5]	C_L= 0 pF to 1100 pF		0.7	1.9	ms
	Output drive	$T_A = T_J$ = 25°C	–50		50	µA

(1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
(2) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(3) Source currents are flowing out of the LMT86. Sink currents are flowing into the LMT86.
(4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in *Output Voltage Shift*.
(5) Specified by design and characterization.

6.7 Typical Characteristics

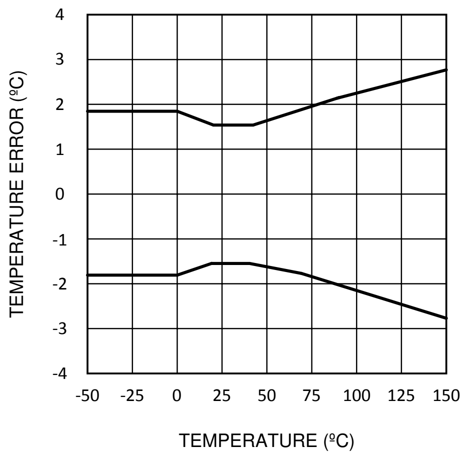


Figure 6-1. Temperature Error vs Temperature

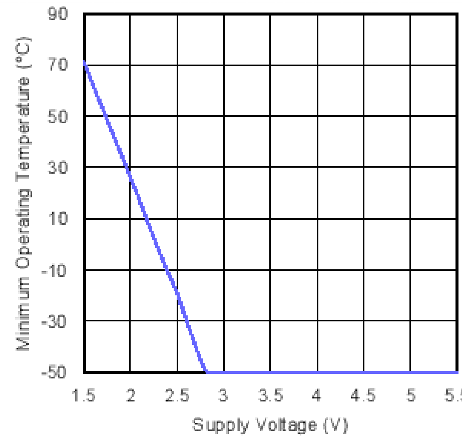


Figure 6-2. Minimum Operating Temperature vs Supply Voltage

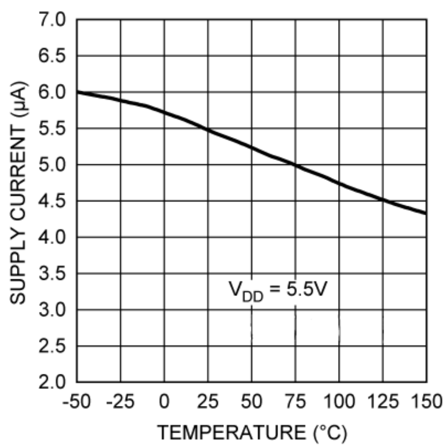


Figure 6-3. Supply Current vs Temperature

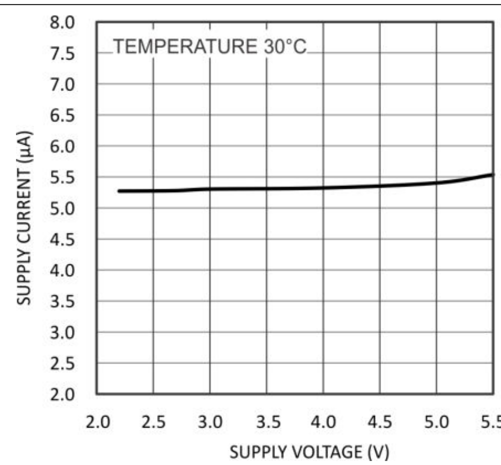


Figure 6-4. Supply Current vs Supply Voltage

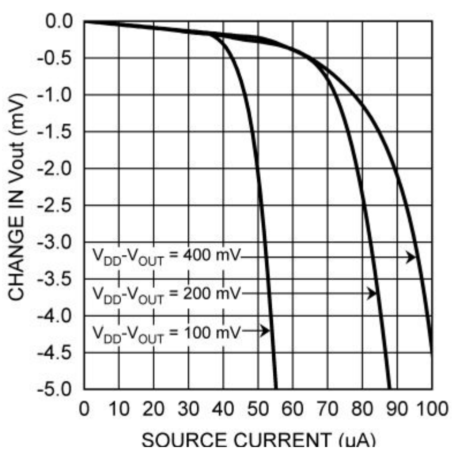


Figure 6-5. Load Regulation, Sourcing Current

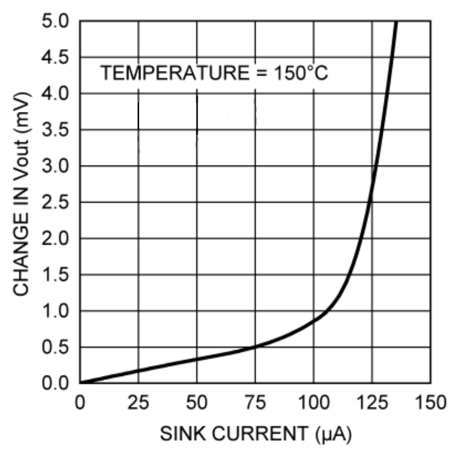


Figure 6-6. Load Regulation, Sinking Current

6.7 Typical Characteristics (continued)

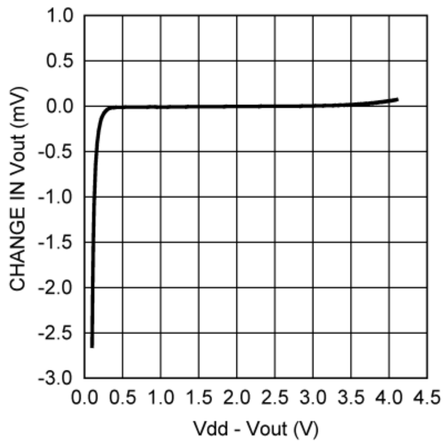


Figure 6-7. Change in V_{OUT} vs Overhead Voltage

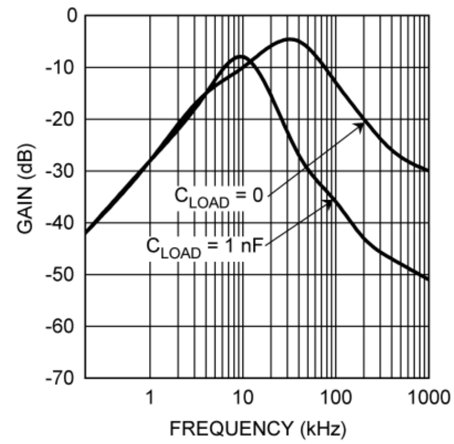


Figure 6-8. Supply-Noise Gain vs Frequency

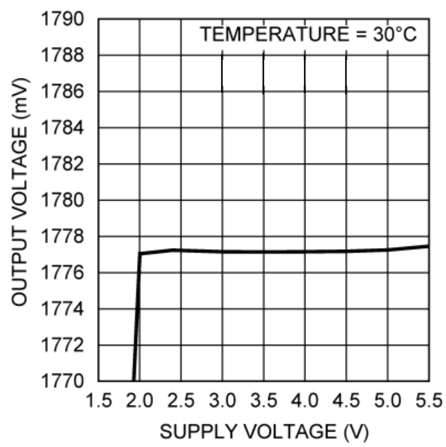


Figure 6-9. Output Voltage vs Supply Voltage

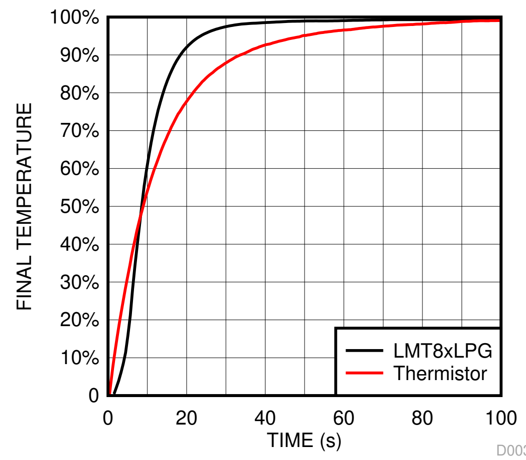


Figure 6-10. LMT86LPG Thermal Response vs Common Leaded Thermistor With 1.2-m/s Airflow

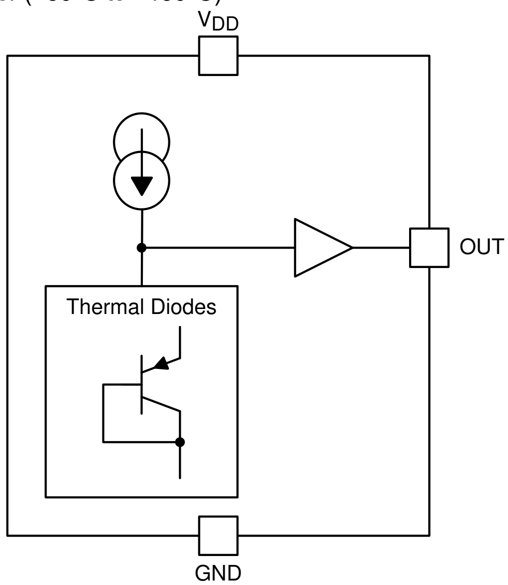
7 Detailed Description

7.1 Overview

The LMT86 is an analog output temperature sensor. The temperature-sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

7.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (−50°C to +150°C)



7.3 Feature Description

7.3.1 LMT86 Transfer Function

Table 7-1 shows the output voltage of the LMT86 across the complete operating temperature range. This table is the reference from which the LMT86 accuracy specifications (listed in the *Accuracy Characteristics* table) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at LMT86 product folder under *Tools and Software Models*.

Table 7-1. LMT86 Transfer Table

TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)
-50	2616	-10	2207	30	1777	70	1335	110	883
-49	2607	-9	2197	31	1766	71	1324	111	872
-48	2598	-8	2186	32	1756	72	1313	112	860
-47	2589	-7	2175	33	1745	73	1301	113	849
-46	2580	-6	2164	34	1734	74	1290	114	837
-45	2571	-5	2154	35	1723	75	1279	115	826
-44	2562	-4	2143	36	1712	76	1268	116	814
-43	2553	-3	2132	37	1701	77	1257	117	803
-42	2543	-2	2122	38	1690	78	1245	118	791
-41	2533	-1	2111	39	1679	79	1234	119	780
-40	2522	0	2100	40	1668	80	1223	120	769
-39	2512	1	2089	41	1657	81	1212	121	757
-38	2501	2	2079	42	1646	82	1201	122	745
-37	2491	3	2068	43	1635	83	1189	123	734
-36	2481	4	2057	44	1624	84	1178	124	722
-35	2470	5	2047	45	1613	85	1167	125	711
-34	2460	6	2036	46	1602	86	1155	126	699

Table 7-1. LMT86 Transfer Table (continued)

TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)	TEMP (°C)	V_{OUT} (mV)
-33	2449	7	2025	47	1591	87	1144	127	688
-32	2439	8	2014	48	1580	88	1133	128	676
-31	2429	9	2004	49	1569	89	1122	129	665
-30	2418	10	1993	50	1558	90	1110	130	653
-29	2408	11	1982	51	1547	91	1099	131	642
-28	2397	12	1971	52	1536	92	1088	132	630
-27	2387	13	1961	53	1525	93	1076	133	618
-26	2376	14	1950	54	1514	94	1065	134	607
-25	2366	15	1939	55	1503	95	1054	135	595
-24	2355	16	1928	56	1492	96	1042	136	584
-23	2345	17	1918	57	1481	97	1031	137	572
-22	2334	18	1907	58	1470	98	1020	138	560
-21	2324	19	1896	59	1459	99	1008	139	549
-20	2313	20	1885	60	1448	100	997	140	537
-19	2302	21	1874	61	1436	101	986	141	525
-18	2292	22	1864	62	1425	102	974	142	514
-17	2281	23	1853	63	1414	103	963	143	502
-16	2271	24	1842	64	1403	104	951	144	490
-15	2260	25	1831	65	1391	105	940	145	479
-14	2250	26	1820	66	1380	106	929	146	467
-13	2239	27	1810	67	1369	107	917	147	455
-12	2228	28	1799	68	1358	108	906	148	443
-11	2218	29	1788	69	1346	109	895	149	432
								150	420

Although the LMT86 is very linear, its response does have a slight umbrella parabolic shape. This shape is very accurately reflected in Table 7-1. The Transfer Table can be calculated by using the parabolic equation (Equation 1).

$$V_{TEMP}(mV) = 1777.3mV - \left[10.888\frac{mV}{°C}(T - 30°C)\right] - \left[0.00347\frac{mV}{°C^2}(T - 30°C)^2\right] \quad (1)$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. Equation 1 can be solved for T resulting in:

$$T = \frac{10.888 - \sqrt{(-10.888)^2 + 4 \times 0.00347 \times (1777.3 - V_{TEMP}(mV))}}{2 \times (-0.00347)} + 30 \quad (2)$$

For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range from the table using the two-point equation (Equation 3):

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1}\right) \times (T - T_1) \quad (3)$$

where

- V is in mV,
- T is in °C,
- T_1 and V_1 are the coordinates of the lowest temperature,
- and T_2 and V_2 are the coordinates of the highest temperature.

For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

$$V - 1885\ \text{mV} = \left(\frac{1558\ \text{mV} - 1885\ \text{mV}}{50^{\circ}\text{C} - 20^{\circ}\text{C}}\right) \times (T - 20^{\circ}\text{C}) \quad (4)$$

$$V - 1885\ \text{mV} = (-10.9\ \text{mV} / ^{\circ}\text{C}) \times (T - 20^{\circ}\text{C}) \quad (5)$$

$$V = (-10.9\ \text{mV} / ^{\circ}\text{C}) \times T + 2103\ \text{mV} \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

7.4 Device Functional Modes

7.4.1 Mounting and Thermal Conductivity

The LMT86 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT86 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT86 will also affect the temperature reading.

Alternatively, the LMT86 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT86 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or V_{DD}, the output from the LMT86 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ($R_{\theta JA}$ or θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use Equation 7 to calculate the rise in the LMT86 die temperature:

$$T_J = T_A + \theta_{JA}\left[(V_{DD} I_S) + (V_{DD} - V_O)\, I_L\right] \quad (7)$$

where

- T_A is the ambient temperature,
- I_S is the supply current,
- $I_L$is the load current on the output,
- and V_O is the output voltage.

For example, in an application where T_A = 30°C, V_{DD} = 5 V, I_S = 5.4 μA, V_O = 1777 mV junction temp 30.014°C self-heating error of 0.014°C. Because the junction temperature of the LMT86 is the actual temperature being measured, take care to minimize the load current that the LMT86 is required to drive. The *Thermal Information* [1] table shows the thermal resistance of the LMT86.

7.4.2 Output Noise Considerations

A push-pull output gives the LMT86 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT86 is ideal for this and other applications which require strong source or sink current.

The LMT86 supply-noise gain (the ratio of the AC signal on V_{OUT} to the AC signal on V_{DD}) was measured during bench tests. Figure 6-8 shows the typical attenuation found in the *Typical Characteristics* section. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT86.

[1] For information on self-heating and thermal response time, see section *Mounting and Thermal Conductivity*.

7.4.3 Capacitive Loads

The LMT86 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, Figure 7-1 shows how the LMT86 can drive a capacitive load less than or equal to 1100 pF. For capacitive loads greater than 1100 pF, Figure 7-2 shows how a series resistor may be required on the output.

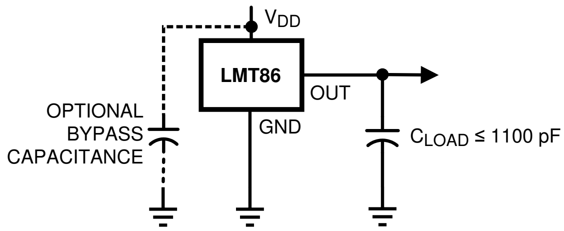


Figure 7-1. LMT86 No Decoupling Required for Capacitive Loads Less Than 1100 pF

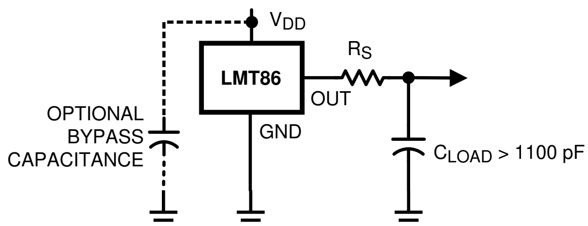


Figure 7-2. LMT86 With Series Resistor for Capacitive Loading Greater Than 1100 pF

Table 7-2. Recommended Series Resistor Values

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	800 Ω

7.4.4 Output Voltage Shift

The LMT86 device is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT}. The shift typically occurs when $V_{DD} – V_{OUT} = 1$ V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT}. Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic. The accuracy specifications in the *Accuracy Characteristics* table already include this possible shift.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMT86 features make it suitable for many general temperature-sensing applications. It can operate down to 2.2-V supply with 5.4-μA power consumption, making it ideal for battery-powered devices. Package options like the through-hole TO-92 package allow the LMT86 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application.

8.2 Typical Applications

8.2.1 Connection to an ADC

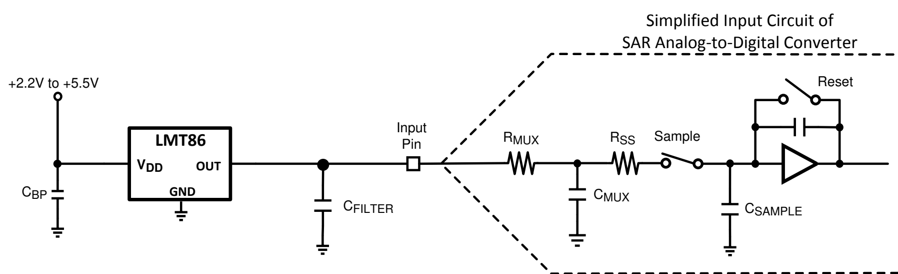


Figure 8-1. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

8.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT86 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor, C_{FILTER}.

8.2.1.2 Detailed Design Procedure

The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

8.2.1.3 Application Curve

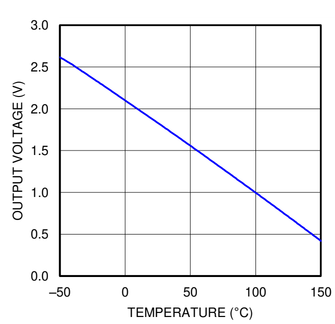


Figure 8-2. Analog Output Transfer Function

8.2.2 Conserving Power Dissipation With Shutdown

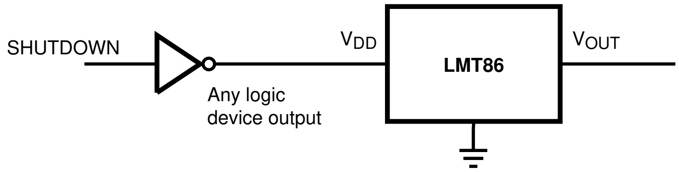


Figure 8-3. Conserving Power Dissipation With Shutdown

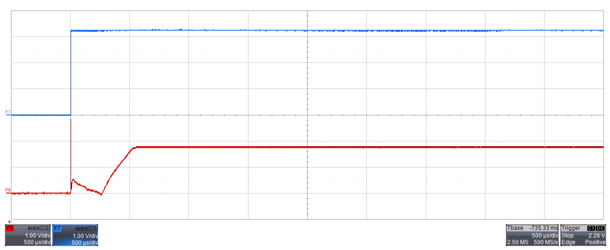
8.2.2.1 Design Requirements

Because the power consumption of the LMT86 is less than 9 µA, it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a microcontroller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

8.2.2.2 Detailed Design Procedure

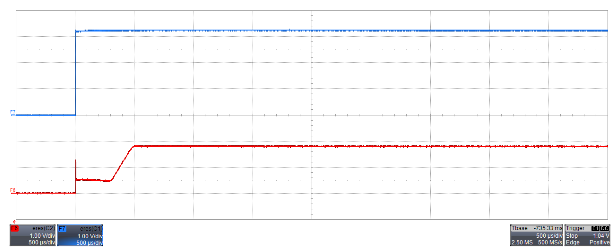
Simply connect the V_{DD} pin of the LMT86 directly to the logic shutdown signal from a microcontroller.

8.2.2.3 Application Curves



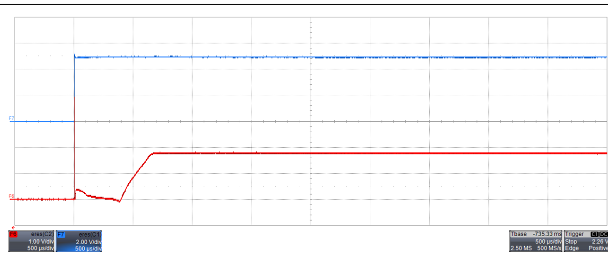
Time: 500 µs/div; Top Trace: V_{DD} 1 V/div; Bottom Trace: OUT 1 V/div

Figure 8-4. Output Turnon Response Time Without a Capacitive Load and V_{DD} = 3.3 V



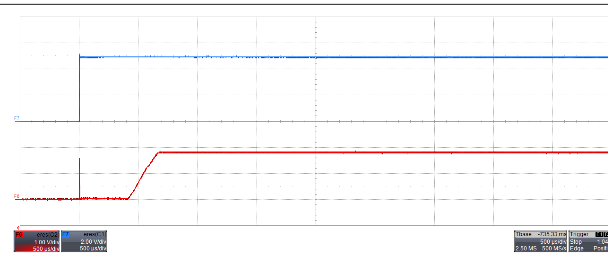
Time: 500 µs/div; Top Trace: V_{DD} 1 V/div; Bottom Trace: OUT 1 V/div

Figure 8-5. Output Turnon Response Time With a 1.1-nF Capacitive Load and V_{DD} = 3.3 V



Time: 500 µs/div; Top Trace: V_{DD} 2 V/div; Bottom Trace: OUT 1 V/div

Figure 8-6. Output Turnon Response Time Without a Capacitive Load and V_{DD} = 5 V



Time: 500 µs/div; Top Trace: V_{DD} 2 V/div; Bottom Trace: OUT 1 V/div

Figure 8-7. Output Turnon Response Time With 1.1-nF Capacitive Load and V_{DD} = 5 V

9 Power Supply Recommendations

The low supply current and supply range (2.2 V to 5.5 V) of the LMT86 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems, it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT86.

10 Layout

10.1 Layout Guidelines

The LMT86 The LMT86 is extremely simple to layout. If a power-supply bypass capacitor is used, it should be connected as shown in the *Layout Example*.

10.2 Layout Example

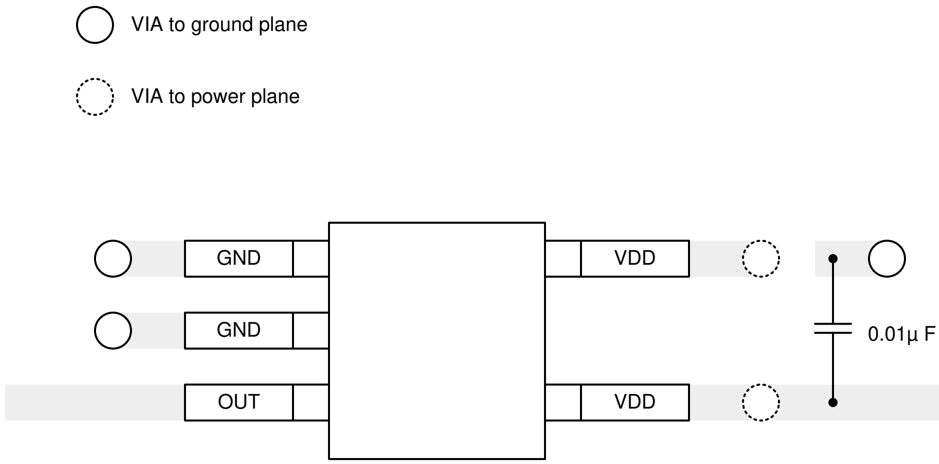


Figure 10-1. SC70 Package Recommended Layout

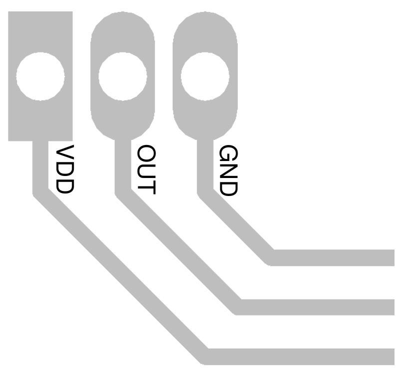


Figure 10-2. TO-92 LP Package Recommended Layout

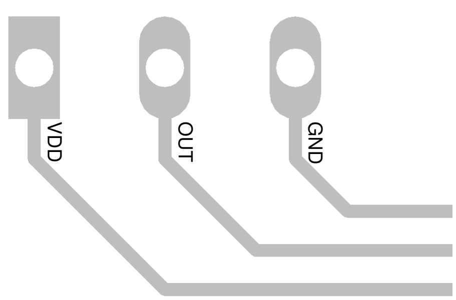


Figure 10-3. TO-92 LPM Package Recommended Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2017) to Revision F (May 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................ 1

Changes from Revision D (June 2017) to Revision E (October 2017) — **Page**

- Moved the automotive device to a standalone data sheet (SNIS201) 1
- Changed TO-92 GND pin number from: 1 to: 3 3
- Changed TO-92 V_{DD} pin number from: 3 to: 1 3

Changes from Revision C (October 2015) to Revision D (June 2017) — **Page**

- Updated data sheet text to the latest documentation and translations standards....................1
- Added AEC-Q100 automotive qualification bullets to *Features* 1
- Added Time Constant graph....................1
- Removed disk drivers, games, wireless transceivers, and cell phones from *Applications* 1
- Added LPG (TO-92S) package....................3
- Added Figure 6-10 to *Typical Characteristics* 6

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMT86DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-50 to 150	BSA	Samples
LMT86DCKT	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-50 to 150	BSA	
LMT86LP	ACTIVE	TO-92	LP	3	1800	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT86	Samples
LMT86LPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT86	Samples
LMT86LPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT86	Samples
LMT86LPM	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT86	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMT86 :

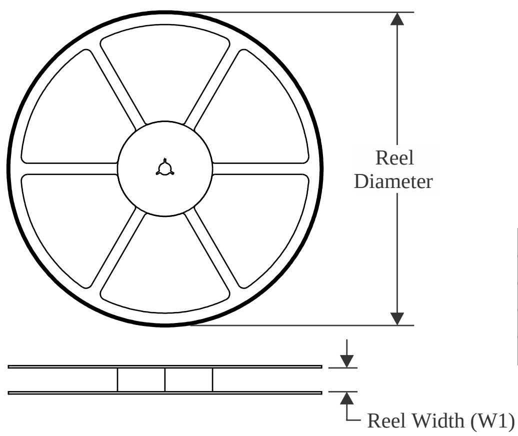
- Automotive : LMT86-Q1

NOTE: Qualified Version Definitions:

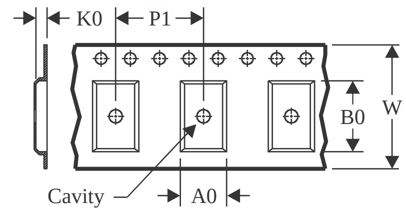
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

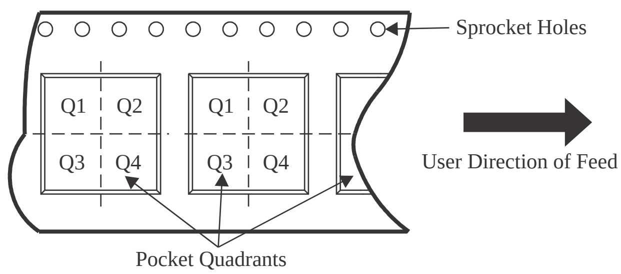


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

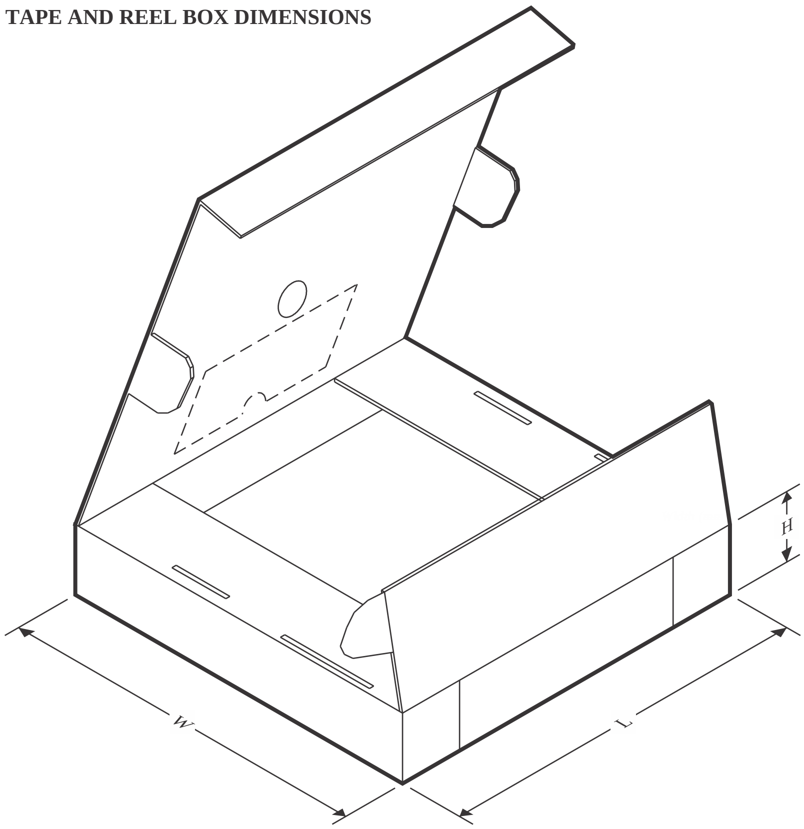
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

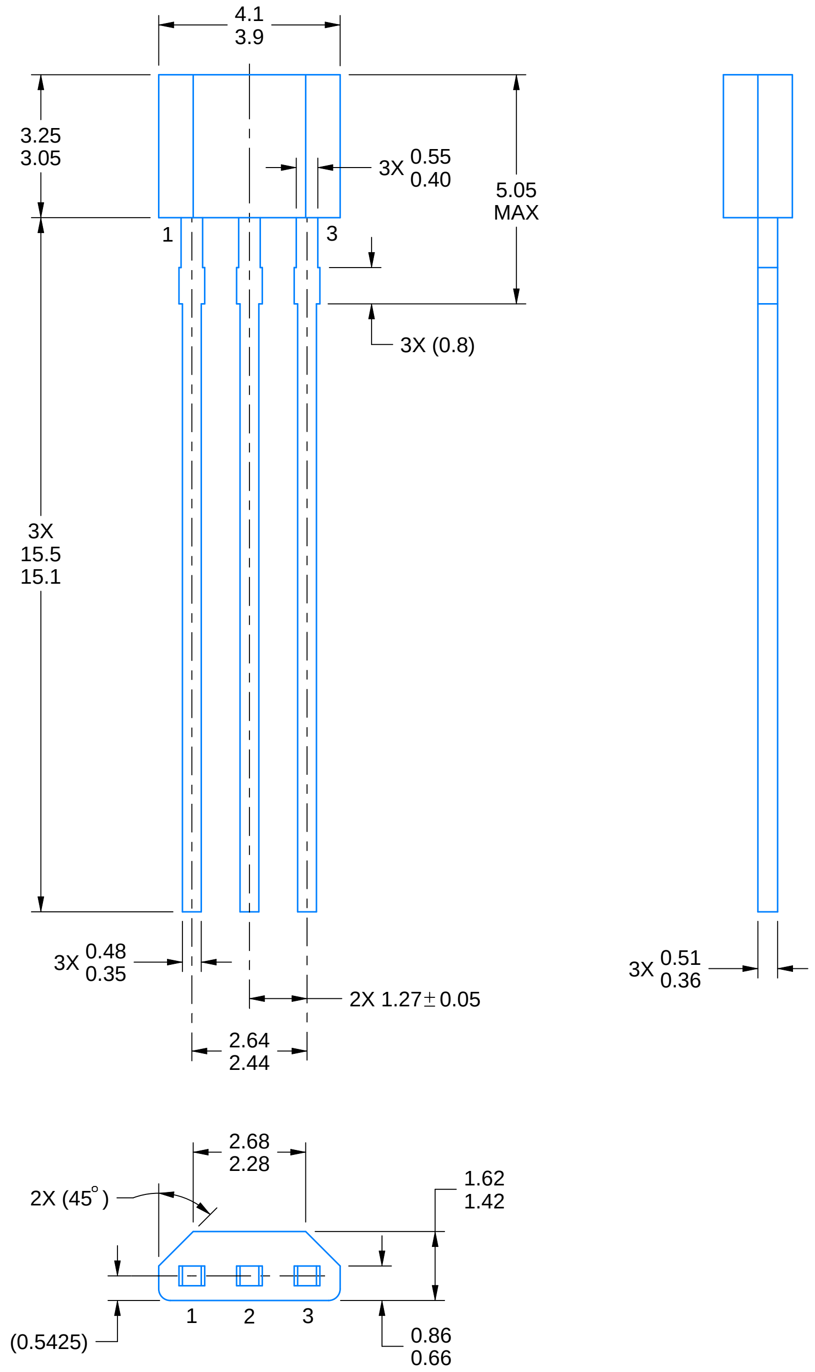
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT86DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

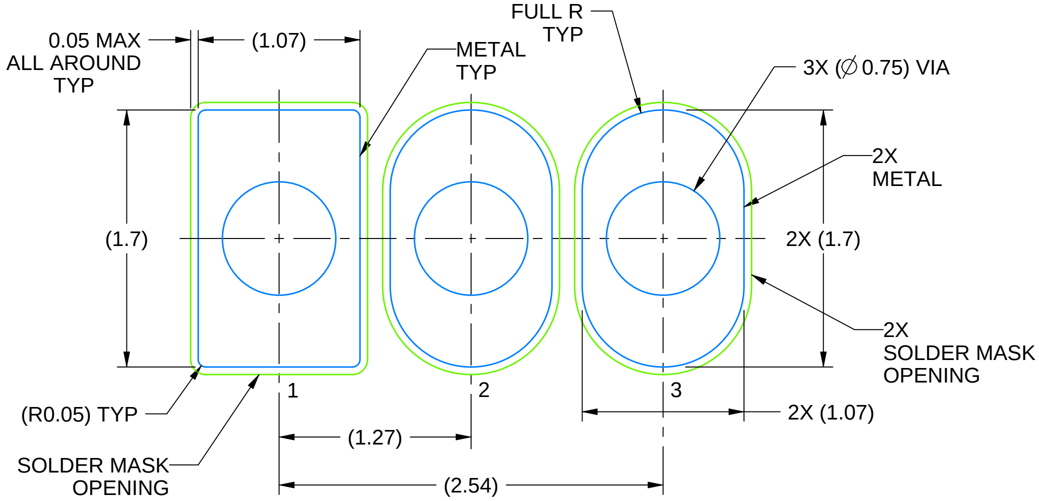
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT86DCKR	SC70	DCK	5	3000	208.0	191.0	35.0



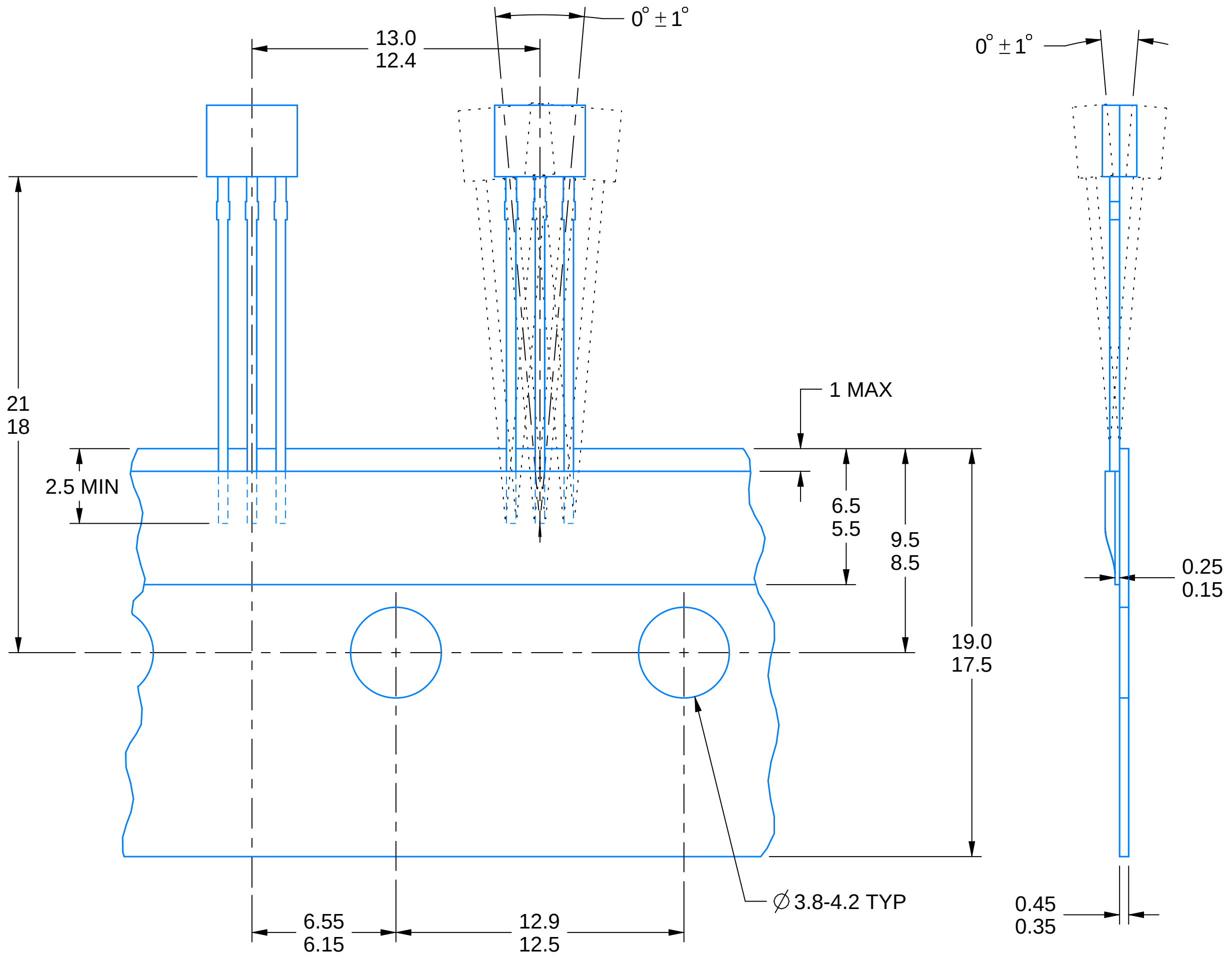
4221343/C 01/2018

NOTES:

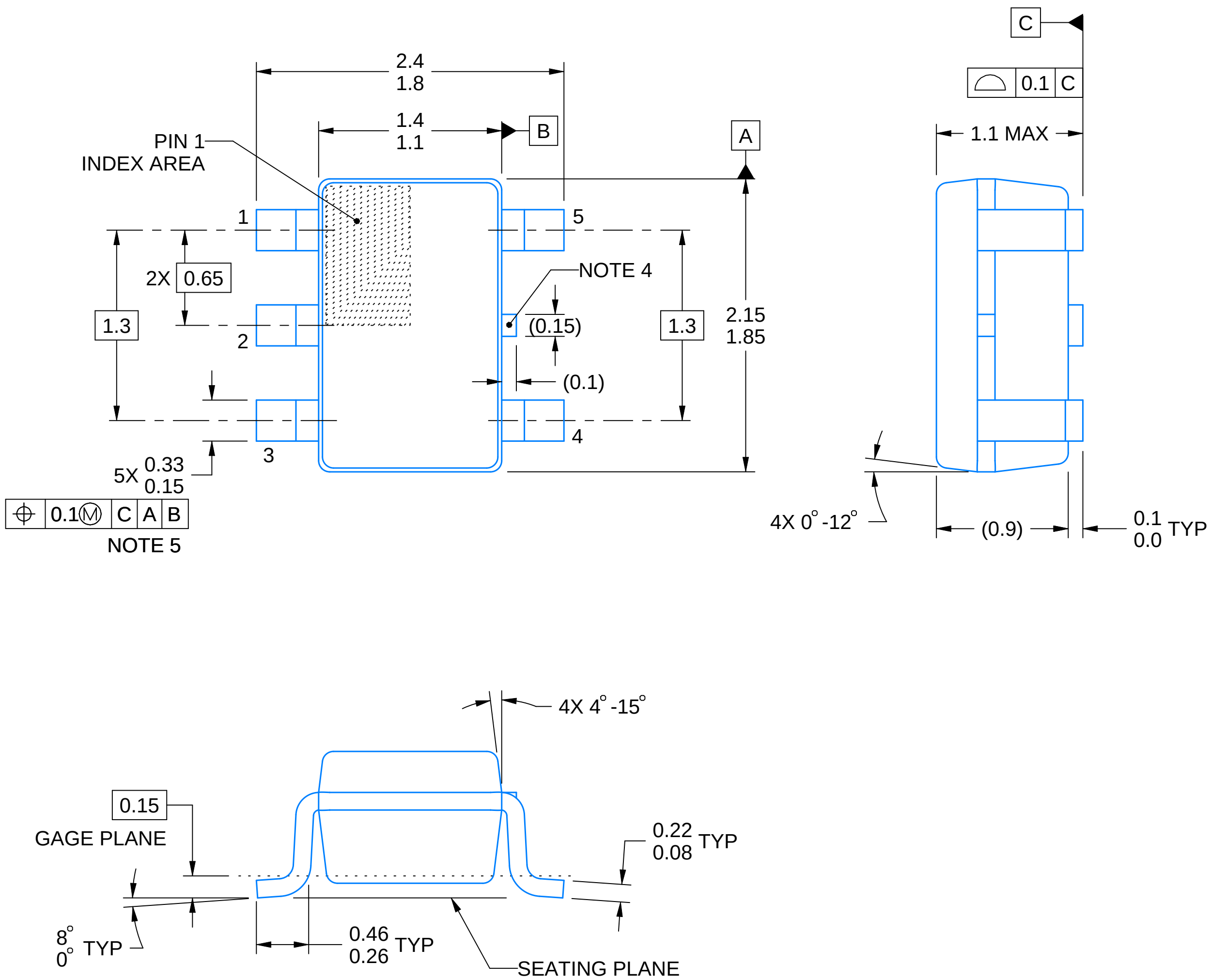
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X



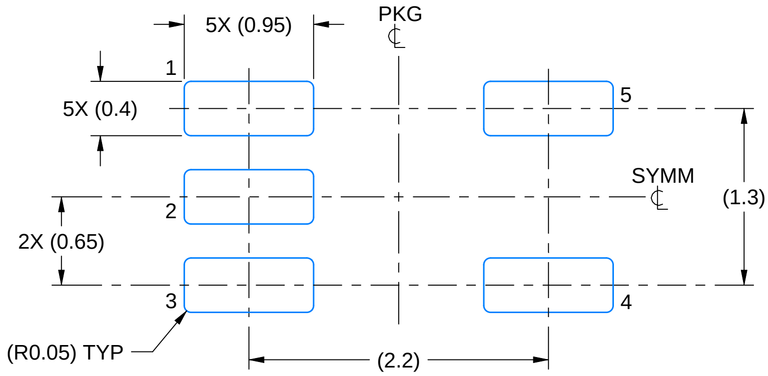
4221343/C 01/2018



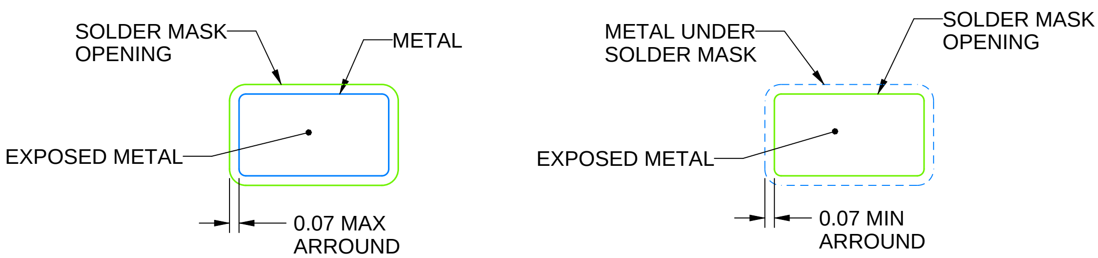
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

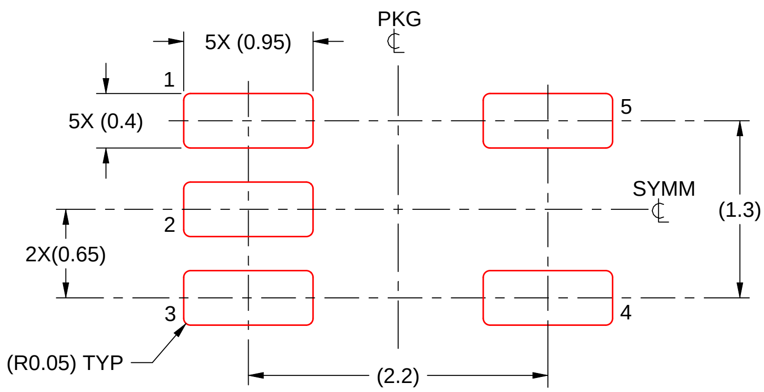


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

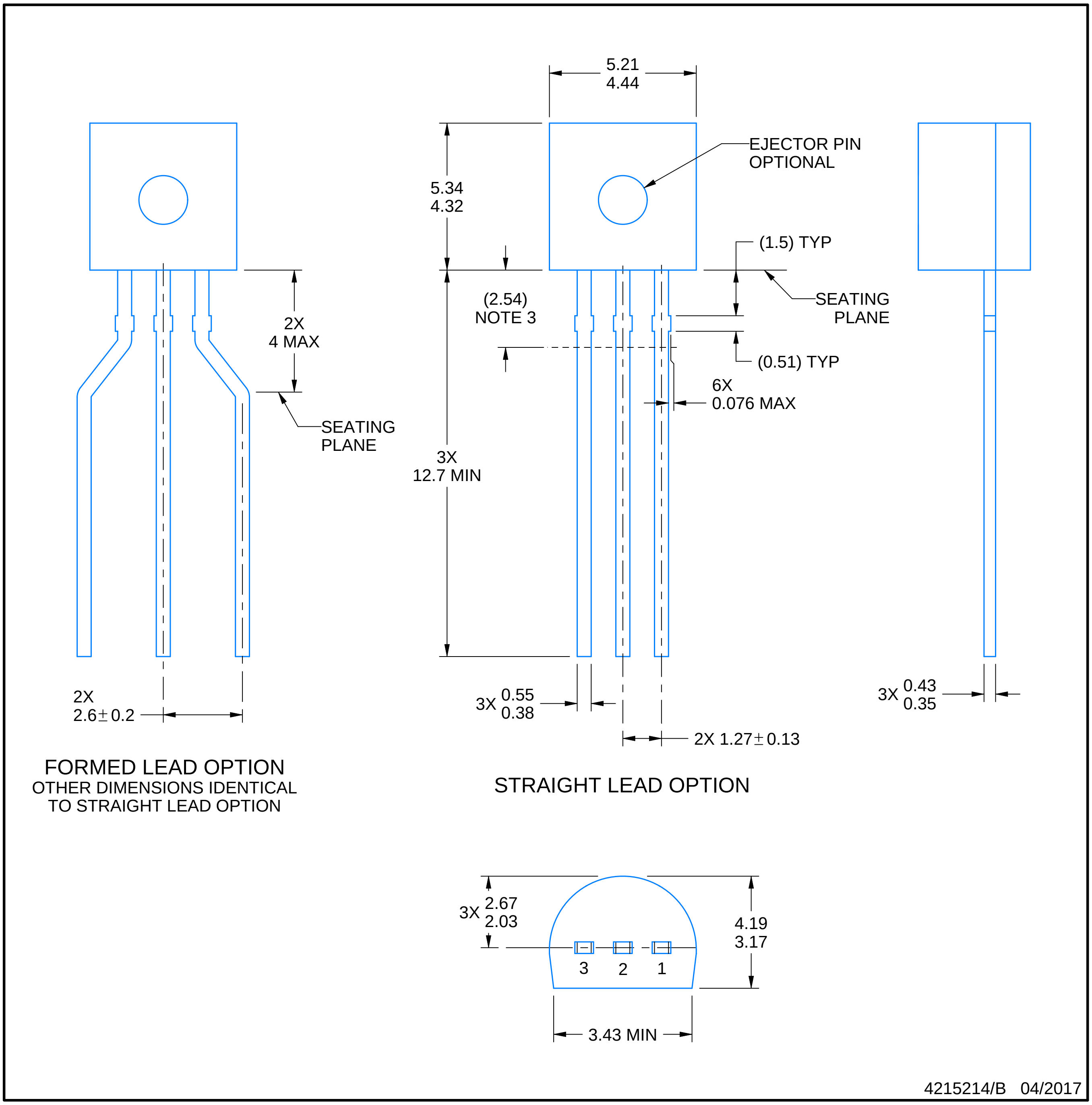
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

LP 3

TO-92 - 5.34 mm max height

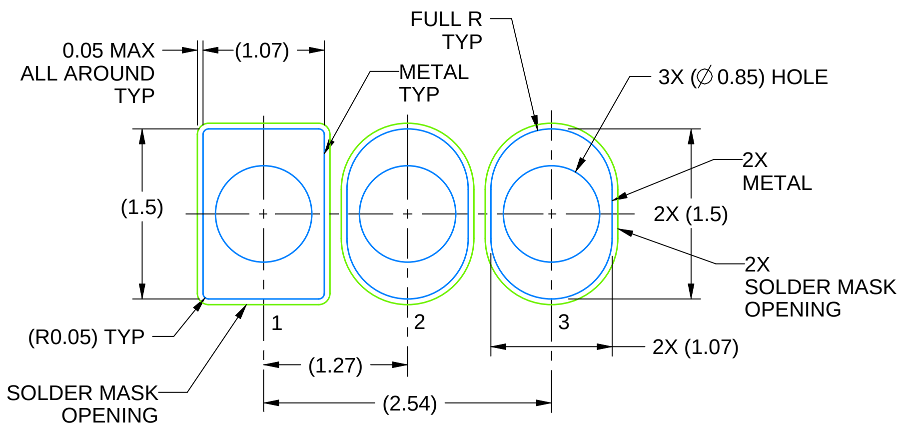
TRANSISTOR OUTLINE

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

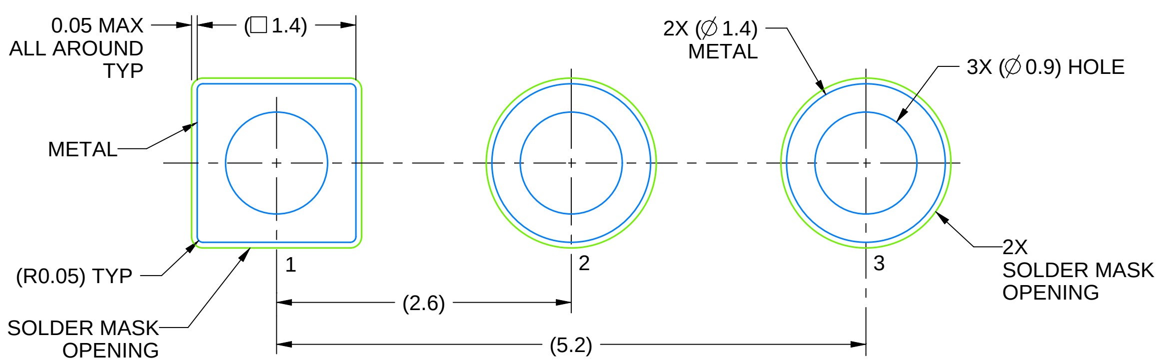


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

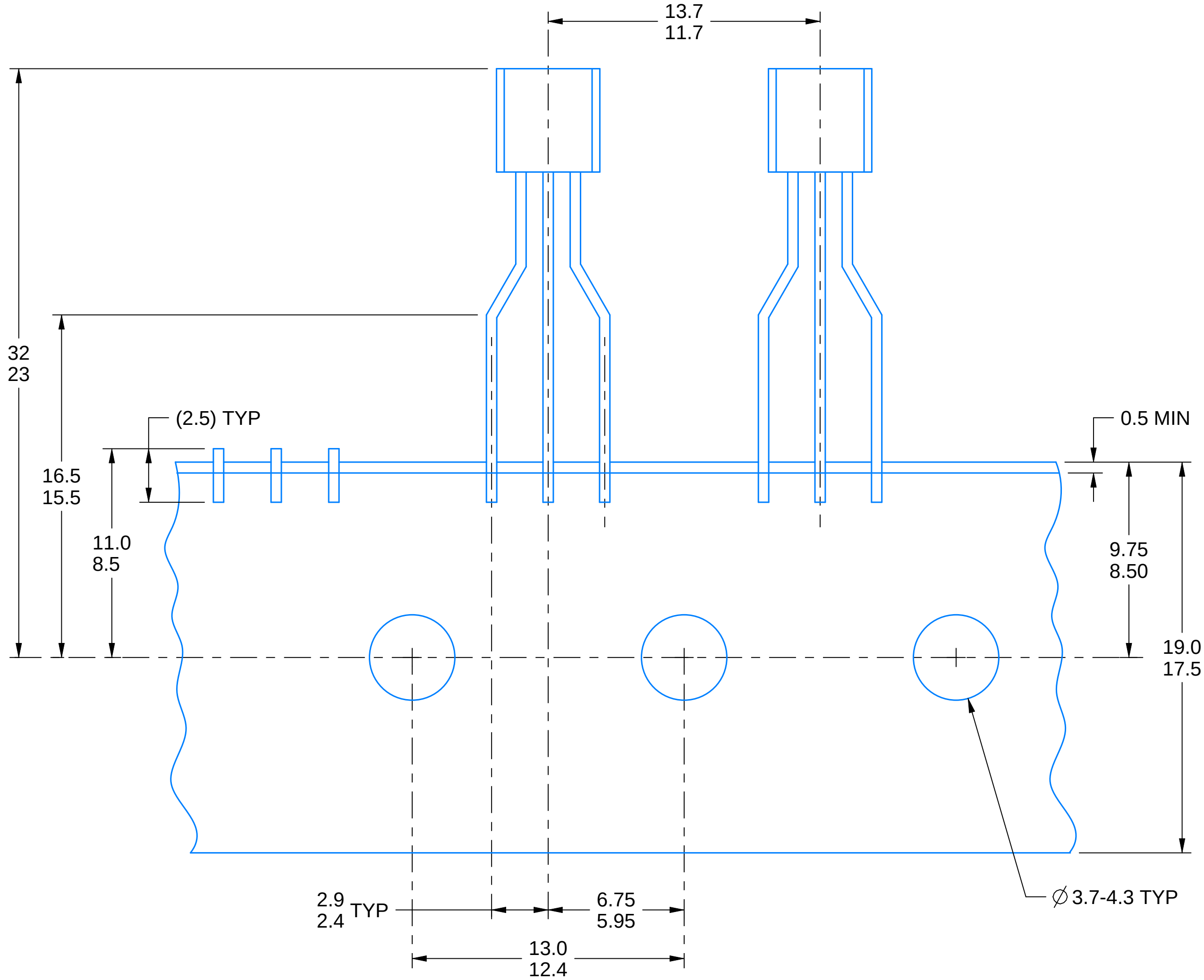


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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