

LM5125-Q1, Wide-VIN, Dual-Phase, Automotive, Boost Controller With V_{OUT} Tracking

1 Features

- AEC-Q100 qualified for automotive applications
 - Temperature grade 1: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- **Functional Safety-Capable**
 - **Documentation available to aid functional safety system design**
- Input voltage 4.5V to 42V
 - Minimum 2.5V for $V_{BIAS} \geq 4.5\text{V}$ or $V_{OUT} \geq 6\text{V}$
- Output Voltage 6V to 60V
 - 2% accuracy, internal feedback resistors
 - Bypass operation for $V_I > V_{OUT}$
 - Dynamic output voltage tracking
 - Digital PWM tracking (DTRK)
 - Analog tracking (ATRK)
 - Overvoltage protection (64V, 50V, 35V, 28.5V)
- Low shutdown I_Q of 2 μA typ. (5 μA maximum)
- Low operating I_Q of 1.4mA typ. (2mA maximum)
- Stacking with interleaved multiphase operation
 - Up to 4-phases without external clock
- Switching frequency from 100kHz to 2.2MHz
 - Synchronization to external clock (SYNCIN)
 - Dynamically selectable switching modes (FPWM, diode emulation)
 - Spread spectrum (DRSS)
- Selectable dead time (18ns to 200ns)
- Current sense resistor or DCR sensing
- Average inductor current monitor
- Average input current limit
 - Programmable current limit
 - Selectable delay time
- Power-good indicator
- Programmable V_I undervoltage lockout (UVLO)
- Lead-less VQFN-32 package with wettable flanks

2 Applications

- **High-end audio power supply**
- Voltage stabilizer module
- Start-stop application

3 Description

The LM5125-Q1 is a stackable, multiphase, synchronous, boost controller. The device provides a regulated output voltage for lower or equal input voltage also supporting V_I to V_{OUT} bypass mode to save power. Two devices can be stacked with or without external clock.

V_{OUT} can be dynamically programmed using the digital or analog ATRK/DTRK function. V_I can be as low as 2.5V after start-up as the internal VCC supply is automatically switched from V_{BIAS} to V_{OUT} for $V_{BIAS} < 4.5\text{V}$. The fixed switching frequency is set between 100kHz and 2.2MHz through a resistor on the RT pin or the SYNCIN clock. The switching modes, FPWM, or diode emulation can be changed during operation.

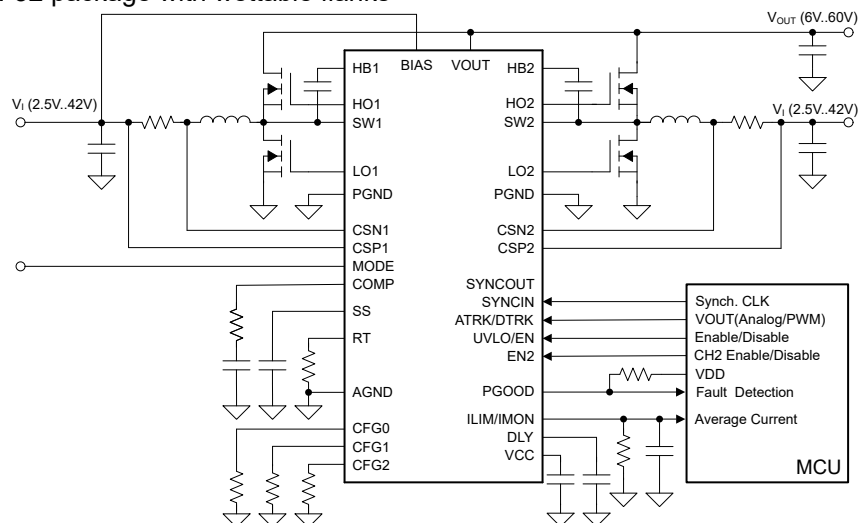
The implemented protections peak current limit, average input current limit, average inductor current monitor, over and undervoltage protection, or the thermal shutdown protect the device and the application.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LM5125-Q1	RHB (VQFN, 32)	5mm × 5mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

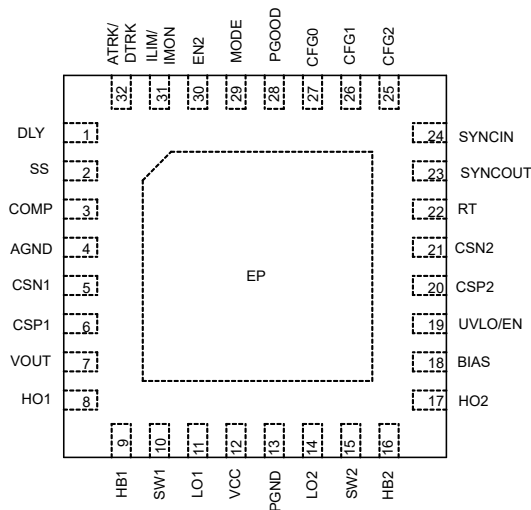


Figure 4-1. LM5125-Q1 RHB Package, VQFN 32 Pin (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DLY	1	O	Average input current limit delay setting pin. A capacitor from DLY to AGND sets the delay from when V_{IMON} reaches 1V until the average input current limit is enabled.
SS	2	O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
COMP	3	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
AGND	4	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
CSN1	5	I	Current sense amplifier input of phase 1. The pin operates as the negative input pin.
CSP1	6	I	Current sense amplifier input of phase 1. The pin operates as the positive input pin. Input to the internal undervoltage lockout for the input voltage.
VOUT	7	I	Output voltage sensing pin. An internal feedback resistor voltage divider is connected from the pin to AGND. Connect a 0.1µF local VOUT capacitor from the pin to ground.
HO1	8	O	High-side gate driver output for phase 1. Connect directly to the gate of the high-side N-channel MOSFET through a short, low inductance path.
HB1	9	P	High-side driver supply for bootstrap gate drive for phase 1. Boot diode is internally connected from VCC to the pin. Connect a 0.1µF capacitor between the pin and SW1.
SW1	10	P	Switching node connection for phase 1. Connect directly to the source of the phase 1 high-side N-channel MOSFET.
LO1	11	O	Low-side gate driver output for phase 1. Connect directly to the gate of the low-side N-channel MOSFET through a short, low inductance path.
VCC	12	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET drivers. Connect a 10µF capacitor between the pin and PGND.
PGND	13	G	Power ground connection pin for low-side gate drivers and VCC bias supply.
LO2	14	O	Low-side gate driver output for phase 2. Connect directly to the gate of the low-side N-channel MOSFET through a short, low inductance path.
SW2	15	P	Switching node connection for phase 2. Connect directly to the source of the phase 2 high-side N-channel MOSFET.
HB2	16	P	High-side driver supply for bootstrap gate drive for phase 2. Boot diode is internally connected from VCC to the pin. Connect a 0.1µF capacitor between the pin and SW2.

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
HO2	17	O	High-side gate driver output for phase 2. Connect directly to the gate of the high-side N-channel MOSFET through a short, low inductance path.
BIAS	18	P	Supply voltage input to the VCC regulator. Connect a 1µF local BIAS capacitor from the pin to ground.
UVLO/EN	19	I	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. If greater than $V_{UVLO-RISING}$, phase 1 is enabled.
CSP2	20	I	Current sense amplifier input of phase 2. The pin operates as the positive input pin.
CSN2	21	I	Current sense amplifier input of phase 2. The pin operates as the negative input pin.
RT	22	O	Switching frequency setting pin. The switching frequency is programmed by a single resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
SYNCOUT	23	O	Clock output pin. SYNCOUT provides a phase shifted clock output, set by the CFG2.pin. SYNCOUT pin can be left floating when not used.
SYNCIN	24	I	External clock synchronization pin. Input for an external clock that overrides the free-running internal oscillator. Connect the SYNCIN pin to ground when not used.
CFG2	25	I/O	Device configuration pin. Sets if the device is configured as single, primary or secondary device using the internal or external clock and the Overvoltage Protection Level.
CFG1	26	I	Device configuration pin. Sets the overvoltage protection level, spread spectrum mode, PGOOD configuration and 120% peak current limit latch off.
CFG0	27	I	Device configuration pin. Sets the dead time and enables the 20µA ATRK current.
PGOOD	28	O	Power-good indicator with open-drain output stage. The pin is pulled low when the output voltage is less than the undervoltage threshold or great than the overvoltage threshold based on the CFG1-pin setting. The pin is also pulled low indicating faults (see Power-Good Indicator (PGOOD-pin)). The pin can be left floating if not used.
MODE	29	I	Operation mode selection pin selecting DEM or FPWM.
EN2	30	I	Enable pin for phase 2.
ILIM/IMON	31	O	Input current monitor and average input current limit setting pin. Sources a current proportional to phase 1 and phase 2 differential current sense voltage. A resistor is connected from this pin to AGND.
ATRK/DTRK	32	I	Output regulation target programming pin. The output voltage regulation target can be programmed by connecting the pin through a resistor to AGND, or by controlling the pin voltage directly with a voltage in the recommended operating range of the pin from 0.2V to 2.0V. A digital PWM signal between 8% to 80% duty cycle sets the output voltage regulation in the recommended operating range.
EP	-	G	Exposed pad of the package. The Exposed pad must be connected to AGND and soldered to a large ground plane to reduce thermal resistance.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)⁽¹⁾

		MIN	MAX	UNIT
Input ⁽²⁾	BIAS to AGND	-0.3	50	V
	UVLO/EN to AGND	-0.3	BIAS + 0.3	
	CSPx to AGND	-0.3	50	
	CSPx to CSNx	-0.3	0.3	
	VOOUT to AGND	-0.3	65	
	HBx to AGND	-0.3	71	
	HBx to SWx	-0.3	5.8 ⁽³⁾	
	SWx to AGND	-0.3	65	
	SWx to AGND (100ns)	-5		
	CFG1, CFG2, SYNCIN, ATRK/DTRK, DLY, MODE, EN2, CFG0 to AGND	-0.3	5.5	
	RT to AGND	-0.3	2.5	
	PGND to AGND	-0.3	0.3	
	Output ⁽²⁾	VCC to AGND	-0.3	
HOx to SWx (50ns)		-1		
LOx to AGND (50ns)		-1		
PGOOD, SYNCOUT, SS, COMP, ILIM/IMON to AGND		-0.3	5.5	
Operating junction temperature, T _J ⁽⁴⁾		-40	150	°C
Storage temperature, T _{STG}		-55	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) It is not allowed to apply an external voltage directly to CFG0, CFG1, CFG2, COMP, SS, RT, LOx, HOx pins.
- (3) Operating lifetime is derated when the pin voltage is greater than 5.5V.
- (4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins		±750

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _I	Boost Controller Input Voltage (when BIAS ≥ 4.5V or V _{OUT} ≥ 6V)	2.5		42	V
V _{OUT}	Boost Controller Output Voltage	6		60	V
V _{BIAS}	BIAS Input Voltage	4.5		42	V
V _{UVLO/EN}	UVLO/EN Input Voltage	0		42	V
V _{EN2}	EN2 Input Voltage	0		5.25	V
V _{MODE}	MODE Input Voltage	0		5.25	V
V _{CSP1} , V _{CSN1} , V _{CSP2} , V _{CSN2}	Current Sense Input Voltage	2.5		42	V
V _{ATRK}	ATRK Input Voltage	0.2		2	V
V _{DTRK}	DTRK Input Voltage	0		5.25	V
V _{DLY}	DLY Voltage	0		5.25	V
V _{PGOOD}	PGOOD Voltage	0		5.25	V
V _{ILIM/IMON}	ILIM/IMON Voltage	0		5.25	V
V _{SYNCIN}	Synchronization Pulse Input Voltage	0		5.25	V
f _{SW}	Switching Frequency Range	100		2200 ⁽²⁾	kHz
f _{SYNCIN}	Synchronization Pulse Frequency Range	100		2200 ⁽²⁾	kHz
f _{DTRK}	DTRK Frequency Range	100		2200	kHz
T _J	Operating Junction Temperature	-40		150 ⁽³⁾	°C

- (1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*
- (2) Maximum switching frequency is programmed by R_{RT}. The device supports up to 2200kHz switching.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM5125-Q1	UNIT
		RHB(VQFN)	
		32 PINS	
R _{qJA}	Junction-to-ambient thermal resistance	33.9	°C/W
R _{qJC(top)}	Junction-to-case (top) thermal resistance	24.8	°C/W
R _{qJB}	Junction-to-board thermal resistance	14.1	°C/W
γ _{JT}	Junction-to-top characterization parameter	0.4	°C/W
γ _{JB}	Junction-to-board characterization parameter	14.0	°C/W
R _{qJC(bot)}	Junction-to-case (bottom) thermal resistance	4.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = -40°C to 150°C. Unless otherwise stated, V_I = V_{BIAS} = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (BIAS, VCC, VOUT)					
I _{SD}	V _I current in shutdown state (BIAS connected to V _I). Current into BIAS, CSP1, CSN1, CSP2, CSN2, SW1, SW2.	V _{EN/UVLO} = 0V, V _{OUT} = 12V, T _J = -40°C to 125°C	2	5	μA
I _{SD_BIAS}	BIAS-pin current in shutdown state	V _{EN/UVLO} = 0V, V _{OUT} = 12V, T _J = -40°C to 125°C	2	5	μA

5.5 Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40^\circ\text{C}$ to 150°C . Unless otherwise stated, $V_I = V_{\text{BIAS}} = 12\text{V}$, $V_{\text{OUT}} = 24\text{V}$, $R_T = 14\text{k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{SD_VOUT}}$	VOUT-pin current in shutdown state	$V_{\text{EN/UVLO}} = 0\text{V}$, $V_{\text{OUT}} = 12\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		0.001	0.5	μA
$I_{\text{Q_BIAS_FPWM}}$	BIAS-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching, RT and IMON current is excluded)	1-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 0\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{ATRK}} = 0.667\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1	1.5	mA
		2-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 2\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{ATRK}} = 0.667\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1.4	2	mA
$I_{\text{Q_BIAS_DEM}}$	BIAS-pin quiescent current in active state, DEM-Mode, internal clock (not-switching, RT and IMON current is excluded)	1-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 0\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{ATRK}} = 0.667\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1	1.5	mA
		2-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 2\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{ATRK}} = 0.667\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1.6	2	mA
$I_{\text{Q_VOUT_FPWM}}$	VOUT-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching)	2-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 2\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{ATRK}} = 0.667\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		250	300	μA
$I_{\text{Q_BIAS_BYP}}$	BIAS-pin current in bypass state (RT and IMON current is excluded)	1-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 0\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{OUT}} = 12\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1	1.5	mA
	BIAS-pin current in bypass state (RT and IMON current is excluded)	2-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 2\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{OUT}} = 12\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C		1.5	2.0	mA
$I_{\text{Q_VOUT_BYP}}$	VOUT-pin current in bypass state	2-phase, $V_{\text{EN/UVLO}} = 2.0\text{V}$, $V_{\text{EN2}} = 2\text{V}$, $V_{\text{CFG2}} = 0\text{V}$, $V_{\text{OUT}} = 12\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C , no resistor between HO and SW.		280	330	μA
I_{BIAS}	BIAS-pin bias current	$V_{\text{BIAS}} = 12\text{V}$, $I_{\text{VCC}} = 200\text{mA}$		200	210	mA
I_{VOUT}	VOUT-pin bias current when VCC is supplied by VOUT	$V_{\text{BIAS}} = 3.3\text{V}$, $I_{\text{VCC}} = 200\text{mA}$		200	210	mA
VCC REGULATOR (VCC)						
$V_{\text{BIAS-RISING}}$	Threshold to switch VCC supply from VOUT-pin to BIAS-pin	V_{BIAS} rising	4.25	4.35	4.45	V
$V_{\text{BIAS-FALLING}}$	Threshold to switch VCC supply from BIAS-pin to VOUT-pin	V_{BIAS} falling	4.1	4.2	4.3	V
$V_{\text{BIAS-HYS}}$	VCC supply threshold hysteresis		100	150		mV
$V_{\text{VCC-REG1}}$	VCC regulation	No load	4.75	5	5.25	V
$V_{\text{VCC-REG2}}$	VCC regulation during dropout	$V_{\text{BIAS}} = 4.5\text{V}$, $I_{\text{VCC}} = 110\text{mA}$	4	4.3		V
$V_{\text{VCC-UVLO-RISING}}$	VCC UVLO threshold	VCC rising	3.4	3.5	3.6	V
$V_{\text{VCC-UVLO-FALLING}}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V
$V_{\text{VCC-UVLO-HYS}}$	VCC UVLO threshold hysteresis	VCC falling		215		mV
$I_{\text{VCC-CL}}$	VCC sourcing current limit	$V_{\text{VCC}} = 4\text{V}$	200			mA
ENABLE (EN/UVLO)						
$V_{\text{EN-RISING}}$	Enable threshold	EN rising	0.50	0.55	0.6	V
$V_{\text{EN-FALLING}}$	Enable threshold	EN falling	0.40	0.45	0.50	V
$V_{\text{EN-HYS}}$	Enable hysteresis	EN falling		100		mV
R_{EN}	EN pulldown resistance	$V_{\text{EN}} = 0.2\text{V}$	30	37	50	k Ω
$V_{\text{UVLO-RISING}}$	UVLO threshold	UVLO rising	1.05	1.1	1.15	V

5.5 Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40^\circ\text{C}$ to 150°C . Unless otherwise stated, $V_I = V_{\text{BIAS}} = 12\text{V}$, $V_{\text{OUT}} = 24\text{V}$, $R_T = 14\text{k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{UVLO-FALLING}}$	UVLO threshold	UVLO falling	1.025	1.075	1.125	V
$V_{\text{UVLO-HYS}}$	UVLO hysteresis	UVLO falling		25		mV
$I_{\text{UVLO-HYS}}$	UVLO pulldown hysteresis current	$V_{\text{UVLO}} = 0.7\text{V}$	9	10	11	μA
$I_{\text{UVLO/EN}}$	UVLO/EN-pin bias current	$V_{\text{UVLO/EN}} = 0.3\text{V}$, pull-down resistor = active.		8	11	μA
		$V_{\text{UVLO/EN}} = 0.7\text{V}$, 10 μA current = active.	9	10	11	μA
		$V_{\text{UVLO/EN}} = 3.3\text{V}$			1	μA
CH2 ENABLE (EN2)						
$V_{\text{EN2_H}}$	Enable 2 high level input voltage	EN2 rising	1.19		5.25	V
$V_{\text{EN2_L}}$	Enable 2 low level input voltage	EN2 falling	-0.3		0.41	V
I_{EN2}	Enable 2 bias current	EN1 = EN2 = 3.3V		0.01	1	μA
CONFIGURATION (CFG0, CFG1, CFG2)						
R_{CFGx_1}	Level 1 resistance			0	0.1	k Ω
R_{CFGx_2}	Level 2 resistance		0.48	0.51	0.54	k Ω
R_{CFGx_3}	Level 3 resistance		1	1.15	1.3	k Ω
R_{CFGx_4}	Level 4 resistance		1.81	1.9	2.00	k Ω
R_{CFGx_5}	Level 5 resistance		2.57	2.7	2.84	k Ω
R_{CFGx_6}	Level 6 resistance		3.61	3.8	3.99	k Ω
R_{CFGx_7}	Level 7 resistance		4.85	5.1	5.36	k Ω
R_{CFGx_8}	Level 8 resistance		6.18	6.5	6.83	k Ω
R_{CFGx_9}	Level 9 resistance		7.89	8.3	8.72	k Ω
$R_{\text{CFGx}_{10}}$	Level 10 resistance		9.98	10.5	11.03	k Ω
$R_{\text{CFGx}_{11}}$	Level 11 resistance		12.64	13.3	13.97	k Ω
$R_{\text{CFGx}_{12}}$	Level 12 resistance		15.39	16.2	17.01	k Ω
$R_{\text{CFGx}_{13}}$	Level 13 resistance		19.48	20.5	21.53	k Ω
$R_{\text{CFGx}_{14}}$	Level 14 resistance		23.66	24.9	26.15	k Ω
$R_{\text{CFGx}_{15}}$	Level 15 resistance		28.60	30.1	31.61	k Ω
$R_{\text{CFGx}_{16}}$	Level 16 resistance		34.68	36.5	38.33	k Ω
SWITCHING FREQUENCY						
V_{RT}	RT regulation		0.7	0.75	0.8	V
f_{SW1}	Switching frequency	$R_T = 316\text{k}\Omega$	85	100	115	kHz
f_{SW2}	Switching frequency	$R_T = 14\text{k}\Omega$	1980	2200	2420	kHz
$t_{\text{ON-MIN}}$	Minimum controllable on-time	$R_T = 14\text{k}\Omega$	14	20	50	ns
$t_{\text{OFF-MIN}}$	Minimum forced off-time	$R_T = 14\text{k}\Omega$	60	80	100	ns
D_{MAX1}	Maximum duty cycle limit	$R_T = 316\text{k}\Omega$	98.9%	99.2%	99.5%	
D_{MAX2}	Maximum duty cycle limit	$R_T = 14\text{k}\Omega$	75%	82%	89%	
SYNCHRONIZATION (SYNCIN)						
	SYNCIN frequency activity detection threshold	Spread Spectrum = off	0		50	kHz
	SYNCIN activity detection cycles			3		cycles
f_{SYNC}	Syncing frequency range from RT set frequency during synchronization	single device	Frequency synchronized to ext. clock min. = 100kHz, max. = 2200kHz		-50%	50%
		dual device			-25%	25%
$V_{\text{SYNCIN_H}}$	SYNCIN high level input voltage	SYNCIN rising	1.19		5.25	V

5.5 Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40^\circ\text{C}$ to 150°C . Unless otherwise stated, $V_I = V_{\text{BIAS}} = 12\text{V}$, $V_{\text{OUT}} = 24\text{V}$, $R_T = 14\text{k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{SYNCIN_L}}$	SYNCIN low level input voltage	SYNCIN falling	-0.3		0.41	V
I_{SYNCIN}	SYNCIN bias current	SYNCIN = 3.3V		0.01	1	μA
	Minimum SYNCIN pullup / pulldown pulse width		135			ns
VOUT PROGRAMMING (ATRK/DTRK)						
$V_{\text{OUT_REG}}$	V_{OUT} regulation with ATRK voltage	ATRK = 0.2V	5.88	6	6.12	V
		ATRK = 0.4V	11.82	12	12.18	V
		ATRK = 0.8V	23.64	24	24.36	V
		ATRK = 1.6V	47.28	48	48.72	V
		ATRK = 2V	59.10	60	60.90	V
G_{DTRK}	Conversion ratio of DTRK duty cycle to V_{ATRK}	$f_{\text{DTRK}} = 100\text{kHz}, 2200\text{kHz}$		25		mV / %
	DTRK duty cycle range		8%		80%	
V_{ATRK}	ATRK voltage for given DTRK duty cycle	$f_{\text{DTRK}} = 100\text{kHz}, \text{DC} = 8\%$	0.196	0.2	0.204	V
		$f_{\text{DTRK}} = 100\text{kHz}, \text{DC} = 40\%$	0.99	1	1.01	V
		$f_{\text{DTRK}} = 100\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V
		$f_{\text{DTRK}} = 440\text{kHz}, \text{DC} = 8\%$	0.196	0.2	0.204	V
		$f_{\text{DTRK}} = 440\text{kHz}, \text{DC} = 40\%$	0.99	1	1.01	V
		$f_{\text{DTRK}} = 440\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V
		$f_{\text{DTRK}} = 2200\text{kHz}, \text{DC} = 8\%$	0.19	0.2	0.21	V
		$f_{\text{DTRK}} = 2200\text{kHz}, \text{DC} = 40\%$	0.98	1	1.02	V
	$f_{\text{DTRK}} = 2200\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V	
$V_{\text{DTRK_H}}$	DTRK high level input voltage	DTRK rising	1.19		5.25	V
$V_{\text{DTRK_L}}$	DTRK low level input voltage	DTRK falling	-0.3		0.41	V
I_{ATRK}	Source current when activated through CFG0		19.8	20	20.2	μA
$I_{\text{ATRK/DTRK}}$	ATRK/DTRK-pin bias current	20 μA current is disabled, $V_{\text{ATRK/DTRK}} = 2\text{V}$		0.01	1	μA
	Minimum DTRK pullup / pulldown pulse width		25			ns
SOFT START (SS)						
I_{SS}	Soft-start current		42.5	50	57.5	μA
$V_{\text{SS-DONE}}$	Soft-start done threshold		2.15	2.2	2.25	V
R_{SS}	SS pulldown switch R_{DSON}			30	70	Ω
$V_{\text{SS-DIS}}$	SS discharge detection threshold		20	45	70	mV
CURRENT SENSE (CSPx, CSNx)						
A_{CS}	Current sense amplifier gain	$V_{\text{CSP}} = 2.5\text{V}$		10		V/V
V_{CLTH}	Positive peak current limit threshold	Referenced to CS input	54	60	66	mV
V_{NCLTH}	Negative peak current limit threshold	Referenced to CS input, FPWM mode	-33	-30	-27	mV
V_{ICL}	Input current limit	Referenced to CS input	65	72	80	mV
	Peak current limit trip delay			50		ns
V_{ZCD}	ZCD threshold (CSPx – CSNx)	CS input falling, $f_{\text{SW}} = 100\text{kHz}$, DEM	0	1	2	mV
$V_{\text{ZCD_BYP}}$	ZCD threshold for phase 1 in bypass mode (CSP1 – CSN1)		-4	-2.5	-1.5	mV
	ZCD threshold for phase 2 in bypass mode (CSP2 – CSN2)		-4	-2.5	-1.5	mV

5.5 Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40^\circ\text{C}$ to 150°C . Unless otherwise stated, $V_I = V_{\text{BIAS}} = 12\text{V}$, $V_{\text{OUT}} = 24\text{V}$, $R_T = 14\text{k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{SLOPE}	Peak slope compensation amplitude	Referenced to CS input, $f_{\text{SW}} = 100\text{kHz}$	40	48	55	mV	
I_{CSNx}	CSNx current	Device in Standby state, $V_I = V_{\text{BIAS}} = V_{\text{OUT}} = 12\text{V}$			1.2	μA	
I_{CSPx}	CSPx current			150	170	μA	
$\Delta I_{\text{ph1_ph2}}$	Peak Inductor Current unbalance (Phase 1 to Phase 2)	$V_{\text{CL}} = 60\text{mV}$	-10%	0	10%		
CURRENT MONITOR / LIMITER WITH DELAY (IMON/ILIM)							
G_{IMON}	Transconductance Gain		0.283	0.333	0.383	$\mu\text{A}/\text{mV}$	
I_{OFFSET}	Offset current		3	4	5	μA	
V_{ILIM}	ILIM regulation target		0.93	1	1.07	V	
$V_{\text{ILIM_th}}$	ILIM activation threshold			1		V	
$V_{\text{ILIM_reset}}$	DLY reset threshold	ILIM falling, referenced to V_{ILIM}	87%	90%	93%		
I_{DLY}	DLY sourcing/sinking current			5		μA	
$V_{\text{DLY_peak_rise}}$		V_{DLY} rising		2.6		V	
$V_{\text{DLY_peak_fall}}$		V_{DLY} falling		2.4		V	
$V_{\text{DLY_valley}}$				0.2		V	
OPERATION MODES							
$V_{\text{MODE_H}}$	MODE-pin high level	FPWM		1.19	5.25	V	
$V_{\text{MODE_L}}$	MODE-pin low level	DEM		-0.3	0.41	V	
I_{MODE}	MODE-pin bias current	MODE = 3.3V		0.01	1	μA	
OVER / UNDER VOLTAGE MONITOR							
$V_{\text{OVP-H}}$	Overvoltage threshold	V_{OUT} rising (referenced to error amplifier reference)	108%	110%	112%		
$V_{\text{OVP-L}}$	Overvoltage threshold	V_{OUT} falling (referenced to error amplifier reference)	101%	103%	105%		
$V_{\text{OVP_max-H}}$	Overvoltage threshold	64V	V_{OUT} rising (referenced to error amplifier reference)	63	64	65	V
		50V		49	50	51	V
		35V		34	35	36	V
		28.5V		27	28.5	30	V
$V_{\text{OVP_max-L}}$	Overvoltage threshold	64V	V_{OUT} falling (referenced to error amplifier reference)	62	63	64	V
		50V		48	49	50	V
		35V		33	34	35	V
		28.5V		26	27.5	29	V
$V_{\text{UVP-H}}$	Undervoltage threshold	V_{OUT} rising (referenced to error amplifier reference)	91%	93%	95%		
$V_{\text{UVP-L}}$	Undervoltage threshold	V_{OUT} falling (referenced to error amplifier reference)	88%	90%	92%		
PGOOD							
R_{PGOOD}	PGOOD pulldown switch $R_{\text{DS(on)}}$	1mA sinking		90	180	Ω	
	Minimum BIAS for valid PGOOD		2			V	
MOSFET DRIVER (HBx, HOx, SWx, LOx)							
	High-state on resistance (HO driver)	100mA sinking, HB – SW = 5V		1.1	2	Ω	
	Low-state on resistance (HO driver)	100mA sourcing, HB – SW = 5V		0.6	1.2	Ω	
	High-state on resistance (LO driver)	100mA sinking, VCC = 5V		1.1	2	Ω	
	Low-state on resistance (LO driver)	100mA sourcing, VCC = 5V		0.7	1.4	Ω	

5.5 Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40^\circ\text{C}$ to 150°C . Unless otherwise stated, $V_I = V_{\text{BIAS}} = 12\text{V}$, $V_{\text{OUT}} = 24\text{V}$, $R_T = 14\text{k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{HB-UVLO}}$	HB-SW UVLO threshold	HB-SW rising	2.85	3.05	3.25	V
$V_{\text{HB-UVLO}}$	HB-SW UVLO threshold	HB-SW falling	2.6	2.8	3	V
$V_{\text{HB-HYS}}$	HB-SW UVLO threshold hysteresis			250		mV
$I_{\text{HB-SLEEP}}$	HB quiescent current in bypass	HB-SW = 5V		8	15	μA
t_{DHL}	HO off to LO on deadtime	CFG0 setting =		18		ns
t_{DLH}	LO off to HO on deadtime			18		ns
I_{CP}	HB charge pump current available at HBx-pin	BIAS = 4.5V, VOUT = 6V	55	75	100	μA
DEAD TIME CONTROL						
DT1	Dead time setting 1			18		ns
DT2	Dead time setting 2			30		ns
DT3	Dead time setting 3			50		ns
DT4	Dead time setting 4			75		ns
DT5	Dead time setting 5			100		ns
DT6	Dead time setting 6			125		ns
DT7	Dead time setting 7			150		ns
DT8	Dead time setting 8			200		ns
THERMAL SHUTDOWN (TSD)						
$T_{\text{TSD-RISING}}$	Thermal shutdown threshold	Temperature rising		175		$^\circ\text{C}$
$T_{\text{TSD-HYS}}$	Thermal shutdown hysteresis			15		$^\circ\text{C}$
TIMINGS						
STANDBY _{timer}	STANDBY timer		130	150	170	μs

5.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES					
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H		1	μs

6 Detailed Description

6.1 Overview

The LM5125-Q1 is a wide input range dual phase boost controller. The device provides a regulated output voltage if the input voltage is equal or lower than the adjusted output voltage. The resistor-to-digital (R2D) interface offers the user a simple and robust selection of all the device functionality.

The operation modes DEM (Diode Emulation Mode) and FPWM (Forced Pulse Width Modulation) are on-the-fly pin-selectable during operation. The peak current mode control operates with fixed switching frequency set by the RT-pin. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

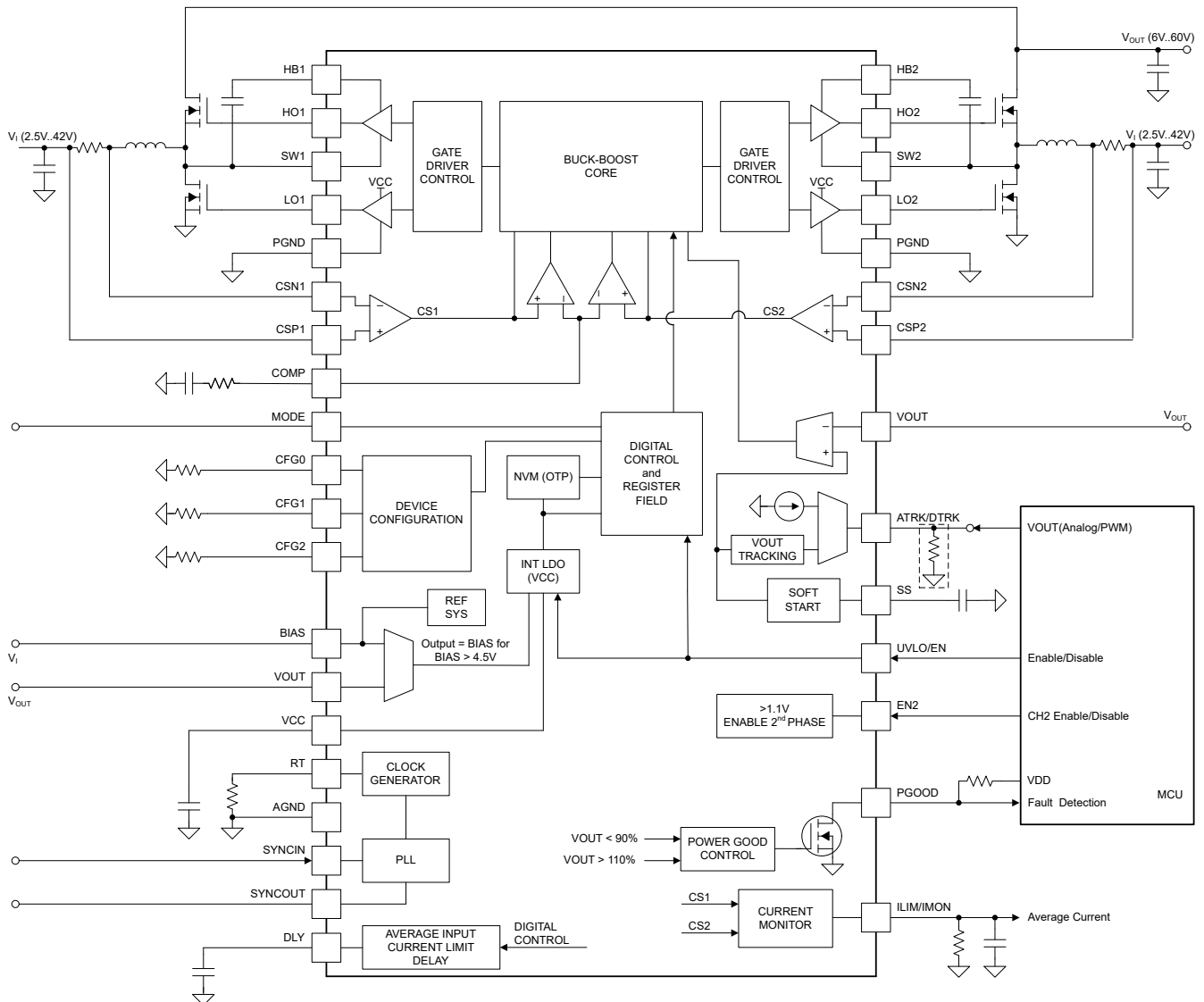
The integrated average current monitor can help monitor or limit input current. The output voltage can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). The adjustment is either possible by changing the analog reference voltage of the ATRK/DTRK-pin or the adjustment can be done directly with a PWM input signal on the ATRK/DTRK pin.

The internal wide input LDOs provide a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltages selection, the power losses are kept at a minimum. The separate BIAS-pin can be connected to the input, output, or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The LM5125-Q1 integrates a full bridge N-channel MOSFET driver. The gate driver circuit has a high driving capability to make sure of high efficiency targets over the wide range of the supported application. The gate driver features an integrated high voltage low dropout bootstrap diode. The internal bootstrap circuit has a protection against an overvoltage that can be injected by negative spikes and an undervoltage lockout protection to avoid a linear operation of the external power FET. An integrated charge pump make sure of 100% duty cycle operation in BYPASS mode.

The devices built-in protection features provide a safe operation under different fault conditions. There is a V_I undervoltage lockout protection to avoid brownout situations. Because the input UVLO threshold and hysteresis can be configured through an external feedback divider, the brownout is avoided under the different designs. The device has an output overvoltage protection. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition of the internal VCC regulators. All output-related fault events are monitored and indicated at the open-drain PGOOD-pin of the device.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Device Configuration (CFG0-pin, CFG1-pin, CFG2-pin)

The CFG0-pin defines the dead time and the ATRK/DTRK-pin 20µA current. The levels shown in [Table 6-1](#) are selected by the specified resistors in the [Specifications](#) section. When V_{OUT} is programmed by the resistor, the 20µA ATRK-pin current must be on, for voltage tracking must be off.

Table 6-1. CFG0-pin Settings

Level	Dead Time [ns]	20µA ATRK Current
1	18	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	18	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

The CFG1-pin setting defines the V_{OUT} overvoltage protection level, Clock Dithering, the 120% input current limit protection (I_{CL_latch}) operation, and the power-good pin behavior.

OVP, Spread Spectrum, Peak Current Limit Latch, Power-Good Pin Behavior:

OVP bit 0: OVP bit 0 and 1 set the V_{OUT} overvoltage protection level. [00] = 64V, [01] = 50V, [10] = 35V or [11] = 28.5V.

Clock Dithering: Enables dual random spread spectrum (DRSS) clock dithering or disables clock dithering.

I_{CL_latch} : When I_{CL_latch} is enabled and the peak current limit is exceeded by 20% the device goes to the [Shutdown State](#) (turns off and is latched). If I_{CL_latch} is disabled the device stays active and tries to limit the inductor current at peak current limit.

PGOOD_{OVP_enable}: When PGOOD_{OVP_enable} is enabled the PGOOD-pin is pulled low for V_{OUT} above OVP (Overvoltage Protection) or below the UV (Undervoltage) threshold. If PGOOD_{OVP_enable} is disabled the PGOOD-pin is only pulled low when V_{OUT} is below UV (Undervoltage) threshold.

Table 6-2. CFG1-pin Settings

Level	OVP Bit 0	Clock Dithering Mode	I_{CL_latch}	PGOOD _{OVP_enable}
1	0	enabled (DRSS)	disabled	disabled
2	1	enabled (DRSS)	disabled	disabled
3	0	enabled (DRSS)	disabled	enabled
4	1	enabled (DRSS)	disabled	enabled
5	0	enabled (DRSS)	enabled	disabled
6	1	enabled (DRSS)	enabled	disabled

Table 6-2. CFG1-pin Settings (continued)

Level	OVP Bit 0	Clock Dithering Mode	I _{CL_latch}	PGOOD _{OVP_enable}
7	0	enabled (DRSS)	enabled	enabled
8	1	enabled (DRSS)	enabled	enabled
9	0	disabled	disabled	disabled
10	1	disabled	disabled	disabled
11	0	disabled	disabled	enabled
12	1	disabled	disabled	enabled
13	0	disabled	enabled	disabled
14	1	disabled	enabled	disabled
15	0	disabled	enabled	enabled
16	1	disabled	enabled	enabled

Table 6-3. Overvoltage Protection Level Selection

OVP Level	OVP Bit 1	OVP Bit 0
64V	0	0
50V	0	1
35V	1	0
28.5V	1	1

The CFG2-pin defines the V_{OUT} overvoltage protection level, if the device uses the internal clock generator or an external clock applied at the SYNCIN-pin. The CFG2-pin configures as well if the device is a single device or part of a dual device configuration, the SYNCIN and SYNCOUT-pin is enabled, disabled accordingly. During clock synchronization, the clock dither function is disabled.

OVP, internal / external clock, Single / Dualchip:

OVP bit 1: OVP bit 0 and 1 set the V_{OUT} overvoltage protection level. [00] = 64V, [01] = 50V, [10] = 35V or [11] = 28.5V.

Single: Internal clock: Device is used standalone using the internal oscillator.

Single ext. clock: Device is used standalone using an external clock signal applied at SYNCIN or the internal oscillator when no clock is applied..

Primary: Device is used as primary device acting as a controller in a dual device configuration using the internal oscillator. The phase shift of the 2nd phase is either optimized for 3-phase (240° shift to 1st phase) or 4-phase (180° shift to 1st phase) operation.

Primary ext. clock: Device is used as primary device acting as a controller in a dual device configuration using an external clock signal applied at SYNCIN-pin. The phase shift is either optimized for 3-phase (240° shift to 1st phase) or 4-phase (180° shift to 1st phase) operation.

Secondary: Device is used as secondary device syncing the clock to the SYNCIN-pin signal.

Device 2nd Phase Phase Shift, SYNCIN, SYNCOUT, Clock Dithering:

Phase Shift of the Device 2nd Phase: Phase shift for the 2nd phase of the single, primary or secondary device as configured in the Single / Dualchip column.

SYNCIN: Defines if the clock syncing function at the SYNCIN-pin is active (on) or disabled (off). The device is only syncing to an external clock applied to the SYNCIN-pin when SYNCIN is active.

Clock Dithering: In case the internal oscillator is used the clock dithering is set according to the CFG1-pin setting Clock Dithering Mode. When an external clock is used the clock dithering function is disabled ignoring the CFG1-pin setting.

Table 6-4. CFG2-pin Settings

Level	OVP Bit 1	Single / Dualchip	Phase Shift of the Device 2 nd Phase	SYNCIN	SYNCOU	SYNCOU Phase Shift	Clock Dithering
1	0	Single	180°	off	off	off	CFG1-pin
2	1						
3	0						
4	1	Single ext. clock	180°	on	off	off	disabled
5	0						
6	1						
7	0	Primary 3-phase	240°	off	on	120°	CFG1-pin
8	1						
9	0	Primary 4-phase	180°	off	on	90°	CFG1-pin
10	1						
11	0	Primary ext. clock 3-phase	240°	on	on	120°	disabled
12	1						
13	0	Primary ext. clock 4-phase	180°	on	on	90°	disabled
14	1						
15	0	Secondary	180°	on	off	off	disabled
16	1						

6.3.2 Switching Frequency and Synchronization (SYNCIN)

The switching frequency of 100kHz to 2.2MHz is set by the RT resistor connected between the RT-pin and AGND. The RT resistor must be selected between 12kΩ and 350kΩ according to Equation 2. If configured to use an external clock the device can synchronize the switching frequency to an external clock applied at the SYNCIN-pin. For single device configuration within ±50% of the set frequency by the RT-pin, when dual device is used within ±25%. The internal clock is synchronized at the rising edge of the external clock signal applied at the SYNCIN-pin. The CFG1-pin Spread Spectrum setting is ignored during frequency synchronization and clock dithering is disabled.

The device always starts with the internal clock and starts synchronizing to an applied external clock during the START PHASE 1 and 2 and the ACTIVE state (see Functional State Diagram). The device synchronizes to the external clock as soon as the clock is applied and switches back to the internal clock in case the external clock stops.

$$F_{SW} = \frac{1}{R_{RT} \times s + 31.5 \text{ G}\Omega + 18 \text{ ns}} \quad (1)$$

$$R_{RT} = \left(\frac{1}{F_{SW}} - 18 \text{ ns} \right) \times 31.5 \frac{\text{G}\Omega}{\text{s}} \quad (2)$$

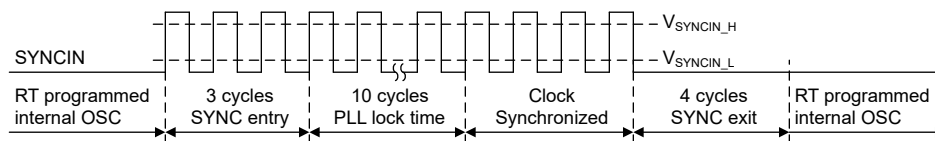


Figure 6-1. Clock Synchronization

6.3.3 Dual Random Spread Spectrum (DRSS)

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function can be enabled by the CFG1-pin. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When the device is configured to use an external clock applied at the SYNCIN-pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

In dual device configuration DRSS is damped in the 2nd device for switching frequencies < 220kHz.

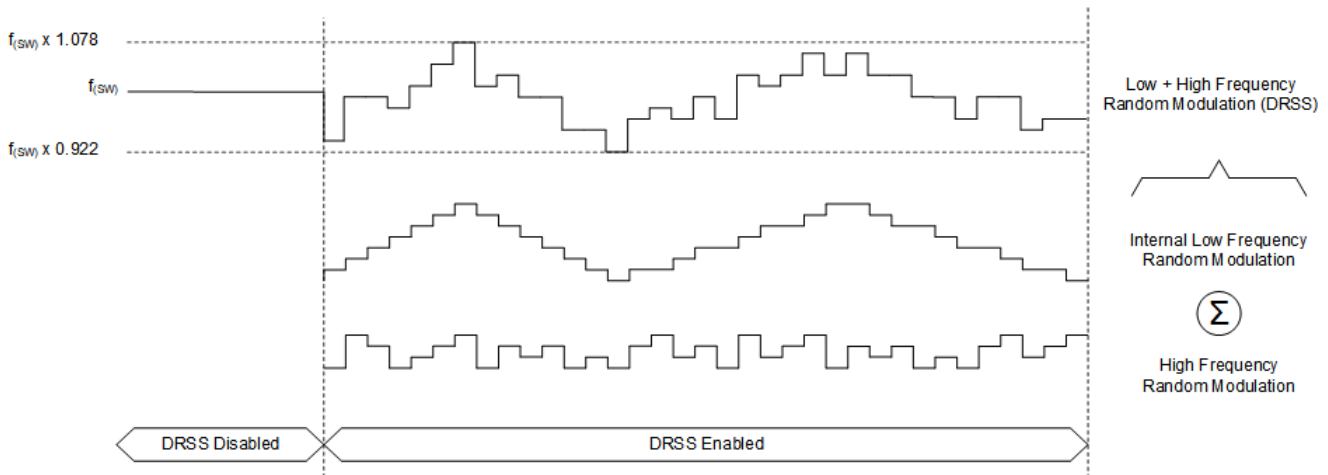


Figure 6-2. Dual Random Spread Spectrum

6.3.4 Operation Modes (BYPASS, DEM, FPWM)

The device supports bypass mode, forced PWM (FPWM) and diode emulation mode (DEM) operation. The mode can be changed on the fly and is set by the MODE-pin. Bypass mode is automatically activated for $V_{OUT} < V_I$. In dual-device stacked operation both devices must use the same mode.

The device operation mode is set to DEM for $V_{MODE} < 0.4V$ and to FPWM for $V_{MODE} > 1.2V$.

Table 6-5. Mode-pin Settings

Operation Mode	MODE-pin
DEM	$V_{MODE} < 0.4V$
FPWM	$V_{MODE} > 1.2V$

Details about the different operation modes are described in table [Operation Modes](#).

Table 6-6. Operation Modes

Operation Mode	Description
BYPASS	V_I is connected to V_{OUT} (no regulation) while current flow from V_{OUT} to V_I is prevented for DEM selection and limited to V_{NCLTH} for FPWM selection.
DEM	Current flow from V_{OUT} to V_I is prevented. The SW-pin voltage is monitored during the high-side on time and the high-side switch is turned off when the voltage falls below the zero current detection threshold V_{ZCD} . This improves light load efficiency.
FPWM	Converter keeps switching also for light load with fixed frequency in continuous conduction mode (CCM) for best light load transient response.

The device enters and exits Bypass mode when the conditions in table [Bypass Mode Entry, Exit](#) are met.

Table 6-7. Bypass Mode Entry, Exit

Operation Mode	Bypass	Conditions
DEM / FPWM	Entry	$V_{OUT} < V_I - 100\text{mV}$ and $V_{COMP} < V_{COMP-MIN} + 100\text{mV}$
DEM	Exit	$V_{COMP} > V_{COMP-MIN} + 100\text{mV}$ $((V_{CSP1} - V_{CSN1}) < V_{ZCD_BYP} \parallel (V_{CSP2} - V_{CSN2}) < V_{ZCD_BYP})$
FPWM	Exit	$V_{COMP} > V_{COMP-MIN} + 100\text{mV}$ $((V_{CSP1} - V_{CSN1}) < V_{NCLTH} \parallel (V_{CSP2} - V_{CSN2}) < V_{NCLTH})$

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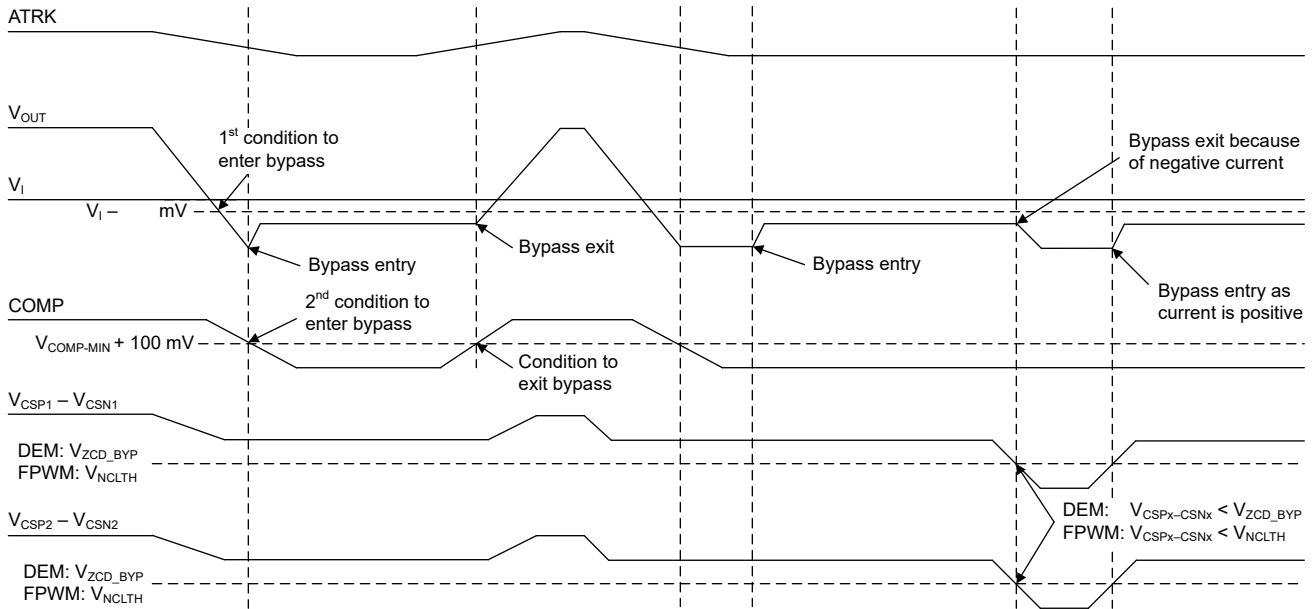


Figure 6-3. Bypass Mode Entry, Exit

6.3.5 Dual- and Multi-phase Operation

The 2nd phase is enabled, disabled by the EN2-pin and can be enabled, disabled during operation as well. The 2nd phase is 180° phase shifted towards phase 1 for lowest input and output ripple. In dual phase operation both phases work in FPWM operation and support up to 2.2MHz switching frequency.

For stacked device configuration the phase shift between the phases is set by the CFG2-pin (see [CFG2-pin settings](#)). The CFG2-pin is read out during boot up and the setting is latched. The primary device switching frequency can be synced to an external clock applied at the SYNCIN-pin (see [Switching Frequency and Synchronization \(SYNCIN\)](#)). The primary device communicates the operation mode via the SYNCOUT-pin to the secondary device.

Pin	Primary SYNCIN = on	Secondary
SYNCIN	High: internal oscillator Pulse: PLL sync Low: internal oscillator	High: bypass mode Pulse: operation as defined by MODE-pin Low: stop switching
SYNCOUT	High: communicate bypass mode to secondary device Pulse: communicate operation as defined by MODE-pin to secondary device Low: communicate stop switching to secondary device.	

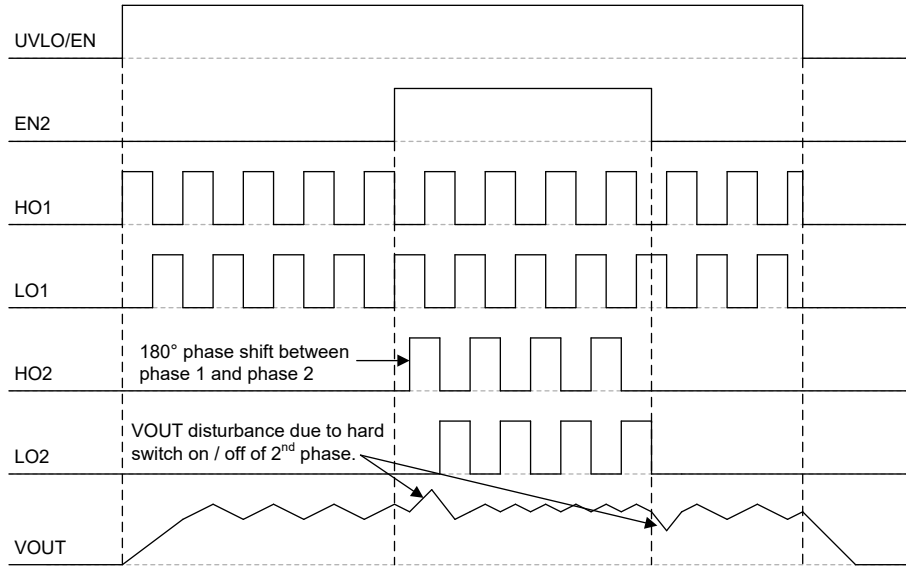


Figure 6-4. Single Device Dual-phase Operation

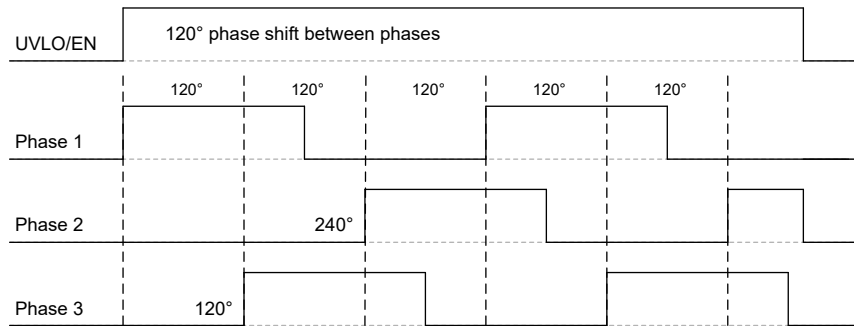


Figure 6-5. 2 Devices 3-phase Operation

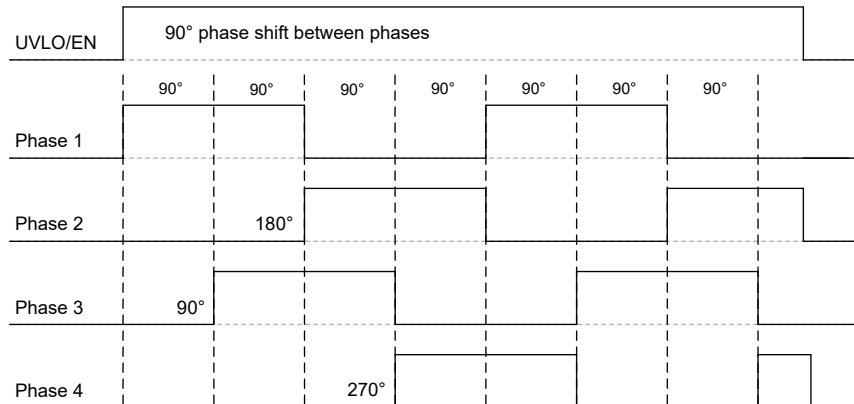


Figure 6-6. 2 Devices 4-phase Operation

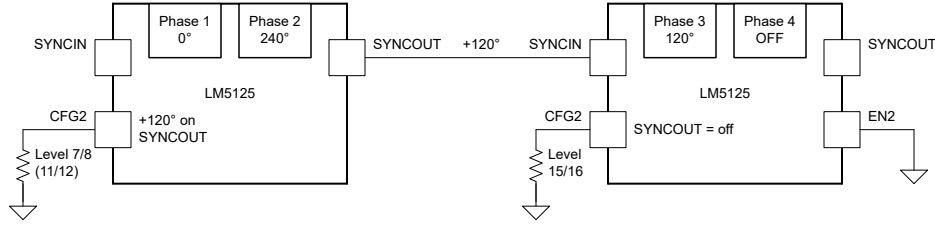


Figure 6-7. 3-Phase Configuration

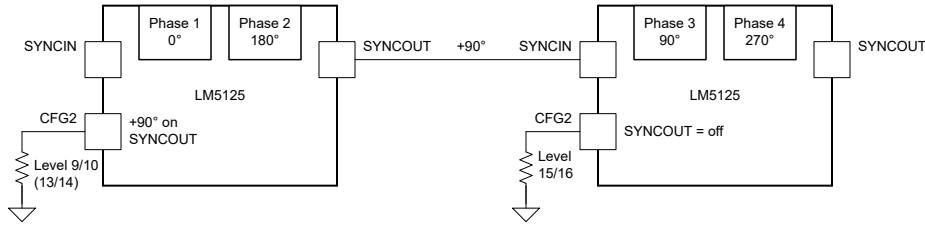


Figure 6-8. 4-Phase Configuration

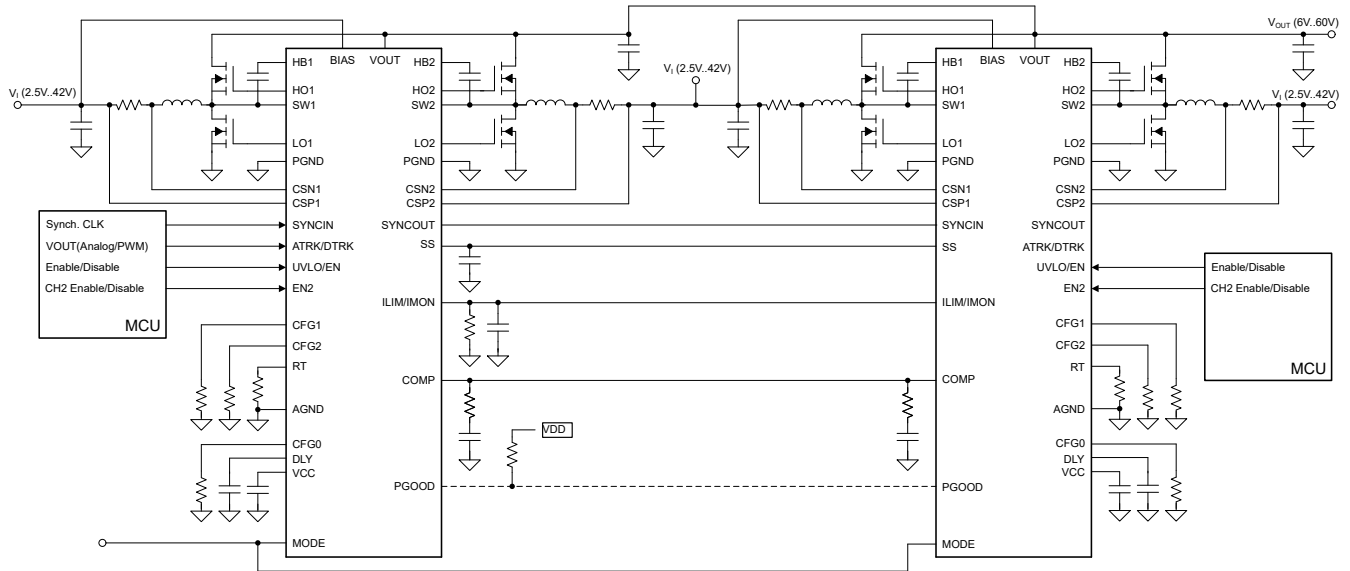


Figure 6-9. Typical Application 4-phase Operation

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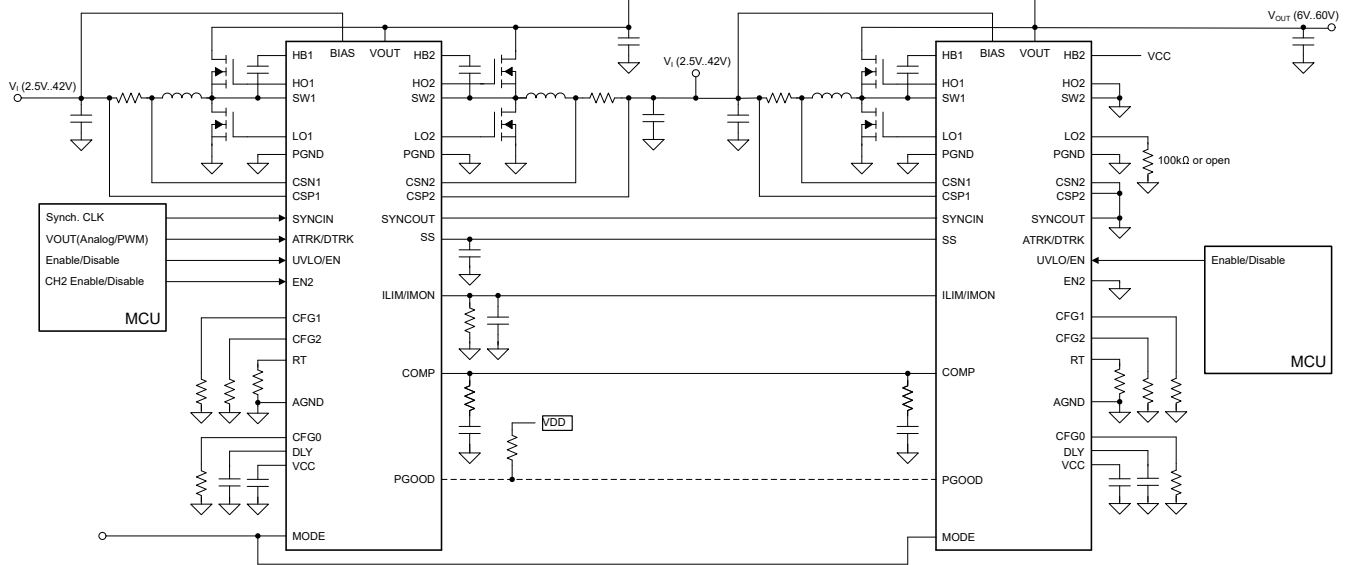


Figure 6-10. Typical Application 3-phase Operation

6.3.6 BIAS (BIAS-pin)

The gate drivers are powered by an internal 5V VCC regulator. The VCC regulator is sourced from the BIAS-pin for $V_{BIAS} > V_{BIAS-RISING}$ or the VOUT-pin for $V_{BIAS} < V_{BIAS-FALLING}$. The BIAS-pin must be connected to a voltage $\geq 2.5V$ (that is, V_I or 5V) as the reference system is permanently supplied by the BIAS-pin and can shut down for voltages $< 2V$.

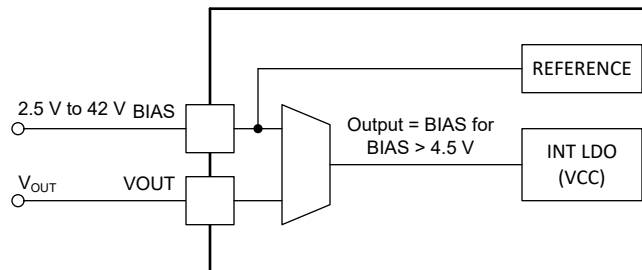


Figure 6-11. On the Fly BIAS Supply Selection

6.3.7 Soft Start (SS-pin)

At start-up during the START PHASE 1 and 2 state (see FSM) the device regulates the error amplifiers reference to the SS-pin voltage or the ATRK/DTRK-pin voltage, whichever is lower. This action results in a gradual rise of the output voltage V_{OUT} . During soft-start the device forces diode emulation mode (DEM) until the soft-start done signal is generated.

The external soft-start capacitor is first discharged to the V_{SS-DIS} voltage, then charged by the I_{SS} current and the soft-start done signal is generated when $V_{SS-DONE}$ is reached. In boost topology the soft-start time (t_{SS}) varies with the input supply voltage as V_{OUT} is equal to V_I at start-up.

$$t_{SS} = V_{ATRK} \times \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_I}{V_{OUT}}\right) \quad (3)$$

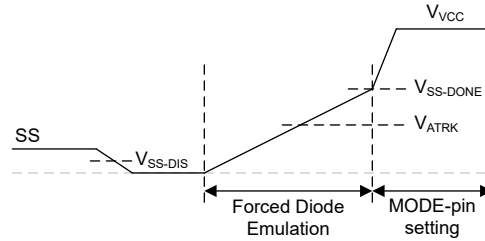


Figure 6-12. Soft Start

6.3.8 V_{OUT} Programming (V_{OUT} , $ATRK$, $DTRK$)

The output voltage V_{OUT} is sensed at the V_{OUT} -pin. V_{OUT} can be programmed between 6V and 60V by connecting a 10k Ω to 100k Ω resistor to the $ATRK/DTRK$ -pin, applying a voltage between 0.2V and 2V or a digital signal between 8% and 80% duty cycle. At start-up during the STANDBY state (Functional State Diagram), the programming method analog signal or digital signal is detected. At the transition to the START PHASE 1 and 2 state the programming method is latched and cannot be changed during operation. $ATRK$ supports up to 10kHz signals, however, the $ATRK$ -pin voltage must be changed slow enough that V_{OUT} can follow. The device tries to regulate V_{OUT} as well for $ATRK < 0.2V$ or $> 2V$, but performance is not endured. For V_{OUT} programming by resistor the 20uA current must be enabled by CFG0 and is sourced through the $ATRK$ -pin, which generates the $ATRK$ voltage via the external resistor. For analog tracking ($ATRK$) or digital tracking ($DTRK$), TI recommends to disable the 20uA current.

Equation for programming V_{OUT} by resistor:

$$R_{ATRK} = \frac{V_{OUT}}{6V} \times 10 \text{ k}\Omega \quad (4)$$

Equation for programming V_{OUT} by voltage ($ATRK$):

$$V_{OUT} = V_{ATRK} \times 30 \quad (5)$$

Equation for programming V_{OUT} by digital signal ($DTRK$):

$$V_{OUT} = 0.75 \frac{V}{\%} \times \text{Duty Cycle} \quad (6)$$

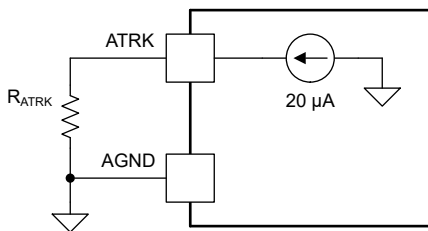


Figure 6-13. V_{OUT} Programming by Resistor

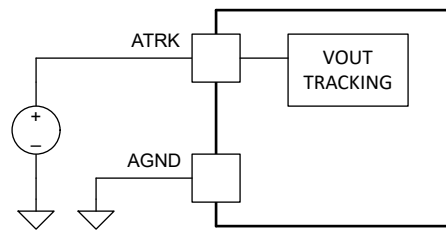


Figure 6-14. V_{OUT} Tracking by Analog Voltage

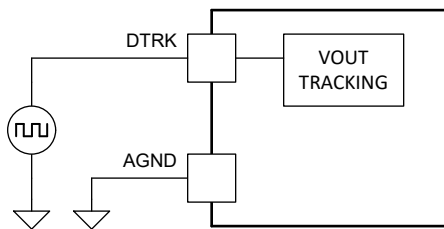


Figure 6-15. V_{OUT} Tracking by Digital Signal

6.3.9 Protections

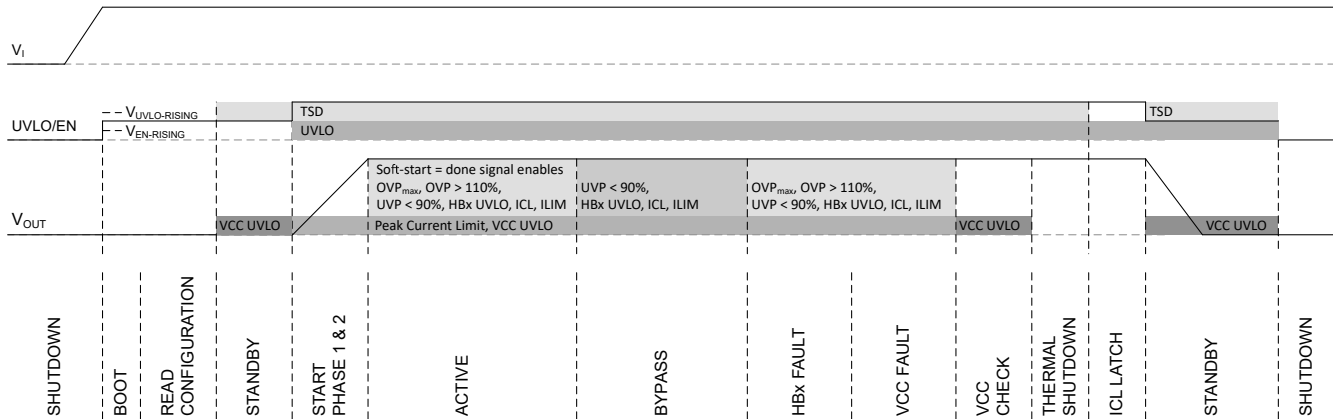


Figure 6-16. Protections

6.3.10 V_{OUT} Overvoltage Protection (OVP)

The Overvoltage Protection (OVP) monitors the V_{OUT} -pin using two thresholds. The programmable threshold V_{OVP_max-H} limiting V_{OUT} to 64V, 50V, 35V or 28.5V, and the V_{OVP-H} threshold limiting the programmed V_{OUT} to 110%. In BYPASS state the 110% $OVP-H$ detection is disabled.

When V_{OUT} rises above the V_{OVP_max-H} or the V_{OVP-H} threshold (not active during Bypass), the low-side driver is turned off and the high-side driver is turned on. Current flow from V_I to V_{OUT} is monitored through CSP1 - CSN1 and when phase 2 is active also through CSP2 - CSN2 allowing current flow from V_I to V_{OUT} . The high-side driver is turned off when the current from V_I to V_{OUT} is zero or negative preventing current flow from V_{OUT} to V_I . When V_{OUT} falls below the V_{OVP_max-L} or V_{OVP-L} threshold the device continues normal operation.

6.3.11 Thermal Shutdown (TSD)

An internal thermal shutdown (TSD) protects the device by disabling the MOSFET drivers and VCC regulator if the junction temperature (T_J) exceeds the $T_{TSD-RISING}$ threshold. After the junction temperature (T_J) is reduced by the $T_{TSD-HYS}$ hysteresis, the device continues operation according to the [Functional State Diagram](#).

6.3.12 Power-Good Indicator (PGOOD-pin)

The device provides a power-good indicator (PGOOD) to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor can be externally connected. The PGOOD switch opens when the V_{OUT} pin voltage is higher than the V_{UVP-H} threshold. PGOOD is pulled low under the following conditions:

- The V_{OUT} -pin voltage is below the V_{OUT} falling undervoltage threshold V_{UVP-L} .
- The V_{OUT} -pin voltage is above the V_{OUT} rising overvoltage threshold V_{OVP-H} or V_{OVP_max-H} and the $PGOOD_{OVP_enable}$ function is enabled (see [CFG1-pin Settings](#)).
- The device is in SHUTDOWN state and V_{BIAS} is greater than approximately 1.7V (see [Functional State Diagram](#)).
- The EN/UVLO-pin voltage is falling below the undervoltage lockout threshold voltage $V_{UVLO-FALLING}$.
- The VCC regulator voltage VCC falls below the undervoltage lockout threshold $V_{VCC-UVLO-FALLING}$.
- Thermal Shutdown is triggered (see [Functional State Diagram](#)).
- The HBx-pin voltage is below the V_{HBx} falling $V_{HB-UVLO}$ threshold and boot refresh enters the 512 cycles hiccup mode off time (see [MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection \(LOx, HOx, HBx-pin\)](#)). PGOOD is only pulled low during the Hiccup off-time.
- The switch peak current limit is exceeded by 20% and the I_{CL_latch} function is enabled (see [CFG1-pin Settings](#)).
- An OTP memory fault occurred (CRC fault).

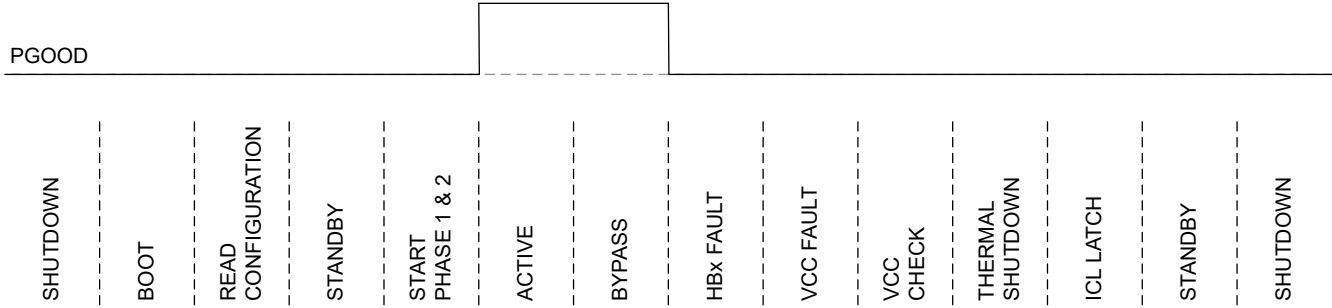


Figure 6-17. PGOOD Status for All Device States

6.3.13 Current Sensing, Peak Current Limit, and Slope Compensation (CSP1, CSP2, CSN1, CSN2)

The current sense amplifier has a gain of 10 (ACS) and an internal slope compensation ramp is added to prevent subharmonic oscillation at high duty cycles. The slope of the compensation ramp must be greater than at least half of the sensed inductor current falling slope fulfilling.

$$\frac{V_{OUT} - V_I}{2 \times L} \times R_S \times Margin < V_{SLOPE} \times f_{SW} \quad (7)$$

6.3.14 Current Sense Programming (CSP1, CSP2, CSN1, CSN2)

The peak current limit for each phase is set by the sense resistors R_{SNS1} and R_{SNS2} . The positive peak current limit for phase 1 is active when CSP1 – CSN1 reaches the threshold V_{CLTH} (typical 60mV), for phase 2 CSP2 – CSN2. The negative peak current limit is active when V_{NCLTH} (typical -30mV) is reached. R_1, R_2, R_4, R_5 are 0Ω and R_3, R_6 are open.

$$R_{SNS} = \frac{I_{peak_lim}}{V_{CLTH}} \quad (8)$$

The peak limit can be programmed by adding the resistors R_1, R_2, R_3, R_4, R_5 and R_6 . Resistor R_1 and R_2 must have the same value as well as resistor R_4 and R_5 . The resistors must be < 1Ω because the CSx Amplifiers are supplied by the CSPx pins. R_3 and R_6 must be between 1Ω and 20Ω.

$$I_{peak_lim_ph1} = \left(\frac{R_1 + R_2}{R_3} + 1 \right) \times \frac{V_{CLTH}}{R_{SNS1}} \quad (9)$$

$$I_{peak_lim_ph2} = \left(\frac{R_4 + R_5}{R_6} + 1 \right) \times \frac{V_{CLTH}}{R_{SNS2}} \quad (10)$$

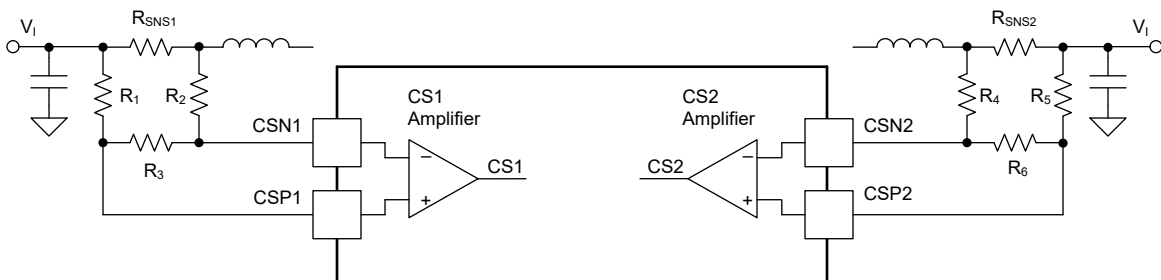


Figure 6-18. Peak Limit Programming through Additional Resistors

6.3.15 Input Current Limit and Monitoring (ILIM, IMON, DLY)

The average input current can be monitored at the IMON-pin. Phase 1 and phase 2 input current is summed up generating a source current at the IMON pin, which is converted to a voltage by the resistor R_{IMON} . The

resulting voltage V_{IMON} is calculated according to Equation 12, the required resistor R_{IMON} according to Equation 11. V_{IMON} can regulate up to 3V and is self protecting not reaching the absolute maximum value.

$$R_{IMON} = \frac{V_{IMON}}{(R_{CS1} + R_{CS2}) \times I_{IN} \times G_{IMON} + 2 \times I_{OFFSET}} \quad (11)$$

$$V_{IMON} = ((R_{CS1} + R_{CS2}) \times I_{IN} \times G_{IMON} + 2 \times I_{OFFSET}) \times R_{IMON} \quad (12)$$

R_{CS1} and R_{CS2} are the respective phase sense resistors. I_{IN} the input current, G_{IMON} the transconductance gain and I_{OFFSET} the offset current given in the electrical characteristics table.

The average input current can be limited by choosing an appropriate resistor connected to the ILIM-pin. V_{OUT} is then regulated down until the set average input current limit is reached. The DLY-pin capacitor C_{DLY} adds an additional delay time t_{DLY} to activate and deactivate the average input current limit (see Average Current Limit). When the ILIM-pin voltage reaches the threshold V_{ILIM} (typical 1V) the source current I_{DLY} is activated charging up the DLY-pin capacitor C_{DLY} . The DLY-pin voltage V_{DLY} rises until $V_{DLY_peak_rise}$ is reached, which activates the average input current limit. The ILIM-pin voltage is regulated to V_{ILIM} and the input current is regulated down to the average input current limit set by R_{ILIM} resulting in a V_{OUT} drop. To exit the average current limit regulation the output load has to decrease, which causes V_{OUT} to rise and V_{ILIM} to fall below V_{ILIM_reset} (typical 0.9V). V_{ILIM_reset} activates the sink current I_{DLY} , which discharges the DLY-pin capacitor C_{DLY} . When V_{DLY} reaches $V_{DLY_peak_fall}$ the average input current limit is deactivated and the DLY-pin is discharged to V_{DLY_valley} . The required resistor R_{ILIM} is calculated according to Equation 13.

$$R_{ILIM} = \frac{1V}{(R_{CS1} + R_{CS2}) \times I_{IN_LIM} \times G_{IMON} + 2 \times I_{OFFSET}} \quad (13)$$

$$t_{DLY} = \frac{2.6 \times C_{DLY}}{5 \times 10^{-6}} \quad (14)$$

$$C_{DLY} = t_{DLY} \times \frac{5 \times 10^{-6}}{2.6} \quad (15)$$

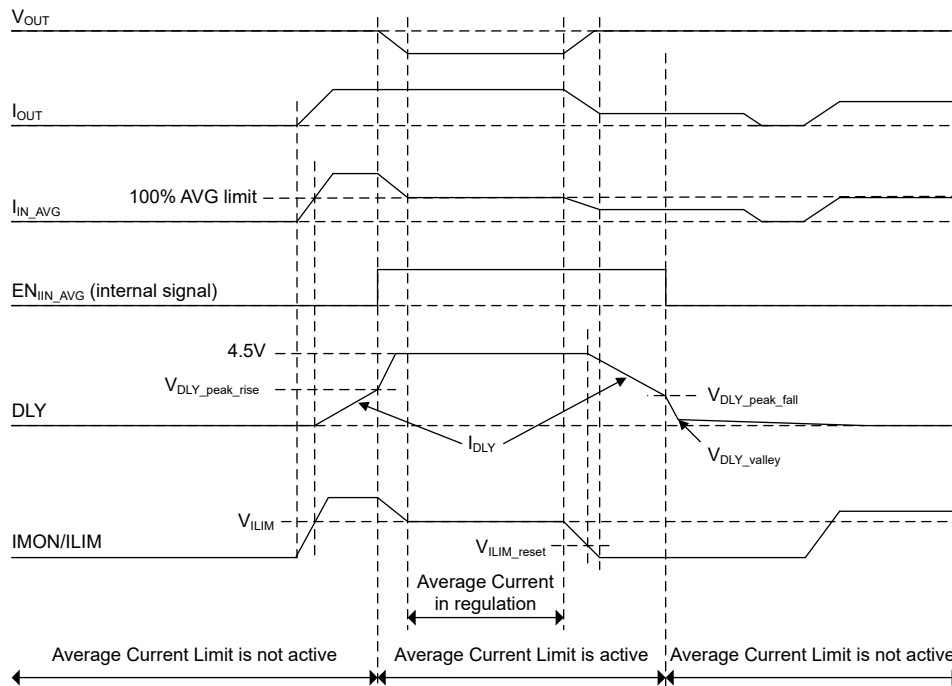


Figure 6-19. Average Current Limit

6.3.16 Signal Deglitch Overview

The following image shows the signal deglitching. For all signals, the rising and falling edge is deglitched with the same deglitch time.

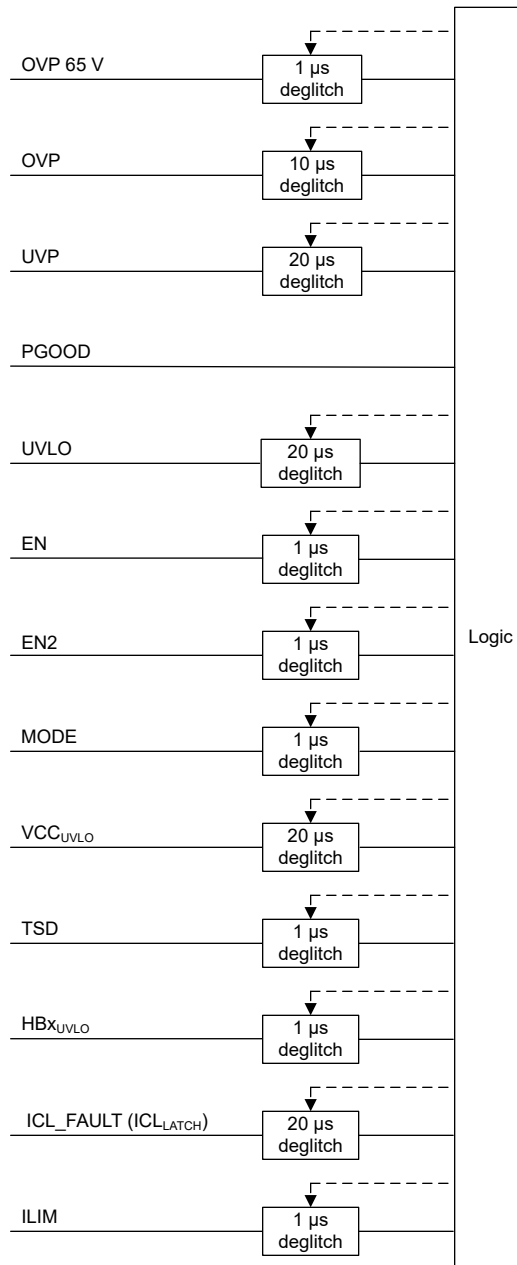


Figure 6-20. Signal Deglitching

6.3.17 MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LOx, HOx, HBx-pin)

The device integrates N-channel logic MOSFET drivers. The LOx driver is powered by VCC and the HOx driver is powered by HBx. When the SWx-pin voltage is approximately 0V by turning on the low-side MOSFET, the capacitor C_{HBx} is charged from VCC through the internal boot diode. The recommended value of C_{HBx} is 0.1 μ F. During shutdown, the gate drivers outputs are high impedance.

The LOx and HOx outputs are controlled with an adaptive dead-time methodology, which makes sure that both outputs are not turned on at the same time to prevent shoot through. When the device turns on LOx the adaptive

dead-time logic turns off HOx and waits for the HOx-SWx voltage to drop below typically 1.5V, then LOx is turned on after a small dead-time delay t_{DHL} . Also the HOx driver turn-on is delayed until the LOx-PGND voltage has discharged below typically 1.5V. HOx is then turned on after a small dead-time delay t_{DLH} .

If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter can not start up properly and can be stuck at the maximum duty cycle in a high-power dissipation state. This condition can be avoided by selecting a lower threshold MOSFET or by turning on the device when the BIAS-pin voltage is sufficient. During bypass operation the minimum HOx-SWx voltage is 3.75V.

The hiccup mode fault protection is triggered by HBx-UVLO. If the HBx-SWx voltage is less than the HBx UVLO threshold ($V_{HB-UVLO}$), LOx turns on by force for 75ns to replenish the boost capacitor. The device allows up to four consecutive replenish switching. After the maximum four consecutive boot replenish switching, the device skips switching for 12 cycles. If the device fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching, the device stops switching and enters 512 cycles of hiccup mode off-time. During the hiccup mode off-time PGOOD = low and the SS-pin is grounded.

If required the slew rate of the switching node voltage can be adjusted by adding a gate resistor in parallel with pulldown PNP transistor. The resistor can decrease the effective dead-time.

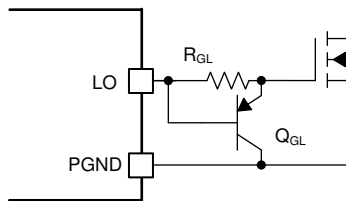


Figure 6-21. Slew Rate Control

6.4 Device Functional Modes

The different operation modes are shown in the Functional State Diagram (FSM).

- (1) : Does not include BOOT, READ CONFIGURATION, THERMAL SHUTDOWN, VCC CHECK, and ICL LATCH state.
 (2) : Phase 2 is ON for EN2 = high and OFF for EN2 = low. When enabled after STANDBY a 150 us biasing time is added before the 2nd phase starts switching.
 (3) : GND for V_{BIAS} > 1.7 V, HIZ for V_{BIAS} < 1.7 V.
 (4) : ATRK/DTRK function (analog, digital) is detected during STANDBY state and latched at the transition to the START PHASE 1 & 2 state.

|| : logic OR
 & : logic AND
 ! : logic NOT
 TSD : Thermal Shutdown
 ①②③ : Priority

THERMAL SHUTDOWN	
Phase 1 & 2	= OFF
VCC	= OFF
CFGx	= OFF
PGOOD	= GND
STANDBY _{timer}	= RESET

VCC CHECK	
Phase 1 & 2	= OFF
VCC	= ON
CFGx	= OFF
PGOOD	= GND

VCC FAULT	
Phase 1	= ON
Phase 2	= ON/OFF ⁽²⁾
VCC	= ON
PGOOD	= GND
Operation Mode	= no switching
STANDBY _{timer}	= ON

HBx FAULT	
Phase 1	= ON
Phase 2	= ON/OFF ⁽²⁾
VCC	= ON
PGOOD	= GND
Operation Mode	= no switching
HBx FAULT timer	= start

BYPASS	
Phase 1	= ON
Phase 2	= ON/OFF ⁽²⁾
VCC	= ON
PGOOD	= HIZ
Operation Mode	= BYPASS

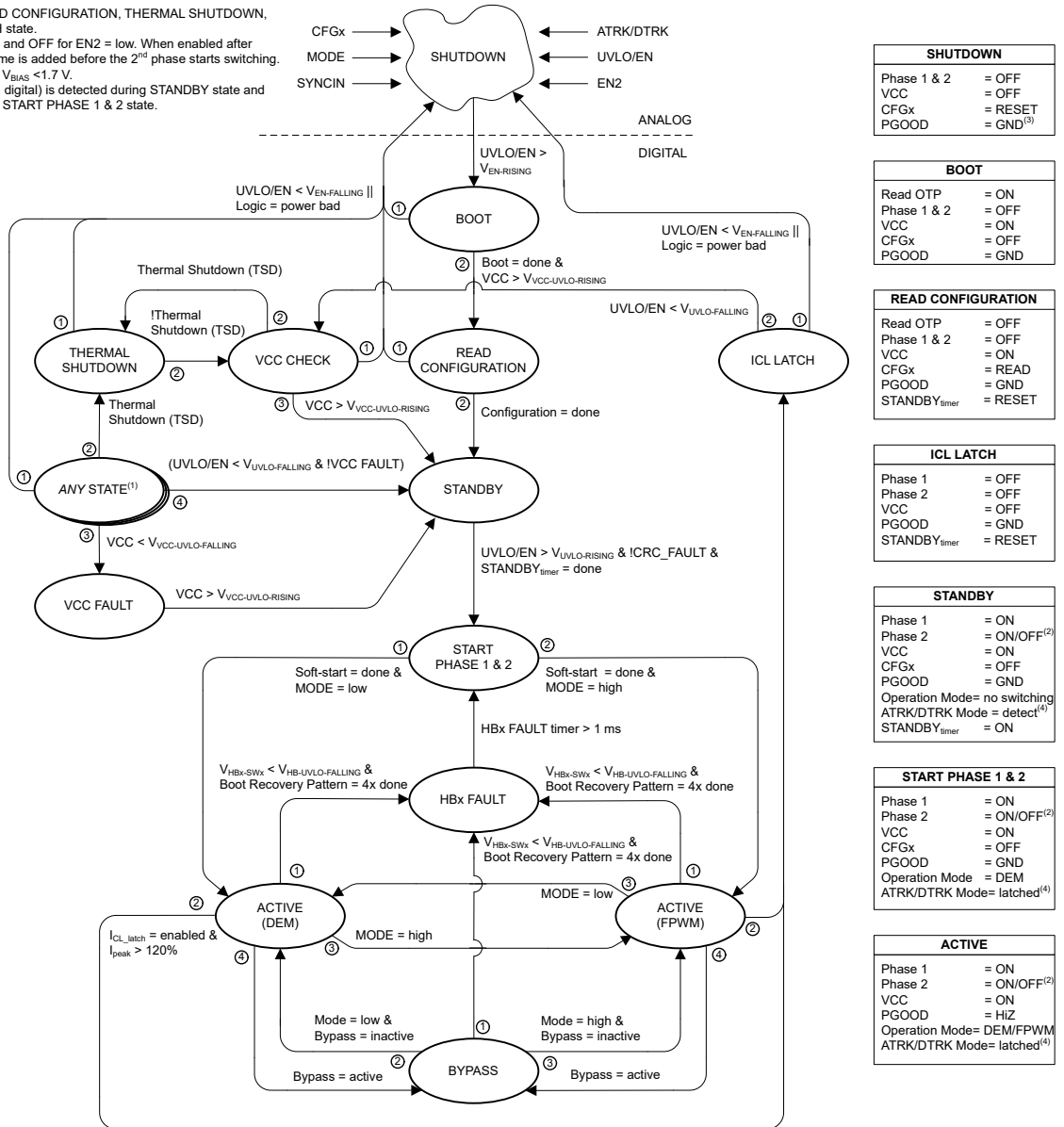


Figure 6-22. Functional State Diagram

6.4.1 Shutdown State

The device shuts down for UVLO/EN pin = low consuming 2µA from BIAS pin and 0.1µA from the VOUT pin. In shutdown, COMP, SS, and PGOOD are grounded. The VCC regulator is disabled.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device integrates several optional features to meet system design requirements, including input UVLO, programmable soft-start time, clock synchronization, spread spectrum, Average input current regulation, inductor current monitoring, 5V compatible BIAS pin for enhanced thermal capability, cold crank support, synchronization, dynamic output voltage tracking and programmable dead time.

7.1.1 Feedback Compensation

The open-loop response of a boost regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator including a power stage transfer function with an embedded current loop can be simplified as one pole, one zero, and one right-half-plane zero (RHPZ) system.

Modulator transfer function is defined as follows:

$$\frac{\hat{v}_{out}}{\hat{v}_{comp}} = A_M \times \frac{\left(1 + \frac{s}{\omega_{Z_ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{P_LF}}} \quad (16)$$

where

- Modulator DC gain, $A_M = \frac{R_{out} \times D'}{2 \times A_{cs} \times R_{cs_eq}}$
- Load pole, $\omega_{P_LF} = \frac{2}{R_{out} \times C_{out}}$
- ESR zero, $\omega_{Z_ESR} = \frac{1}{R_{ESR} \times C_{out}}$
- RHPZ, $\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m_eq}}$
- The equivalent load resistance, $R_{out} = \frac{V_{out}^2}{P_{out_total}}$
- The equivalent inductance, $L_{m_eq} = \frac{L_m}{N_p}$
- The equivalent current sense resistor, $R_{cs_eq} = \frac{R_{cs}}{N_p}$
- N_p is the number of the phases.

If the equivalent series resistance (ESR) of C_{out} (R_{ESR}) is small enough and the RHPZ frequency is far away from the target crossover frequency, the modulator transfer function can be further simplified to a one pole system and the voltage loop can be closed with only two loop compensation components, R_{COMP} and C_{COMP} , leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

As shown in [Figure 7-1](#), a g_m amplifier is utilized as the output voltage error amplifier. The feedback transfer function includes the feedback resistor divider gain and loop compensation of the error amplifier. R_{COMP} , C_{COMP} , and C_{HF} configure the error amplifier gain and phase characteristics, create a pole at origin, a low frequency zero and a high frequency pole.

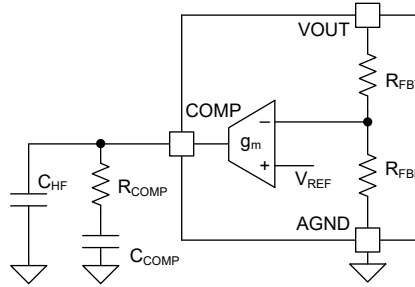


Figure 7-1. Type II g_m Amplifier Compensation

Feedback transfer function is defined as follows:

$$-\frac{\hat{v}_{\text{comp}}}{\hat{v}_{\text{out}}} = \frac{A_{VM} \times \omega_{Z_EA}}{s} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{1 + \frac{s}{\omega_{P_EA}}} \quad (17)$$

where

- The middle-band voltage gain, $A_{VM} = K_{FB} \times g_m \times R_{COMP}$
- The feedback resistor divider gain $K_{FB} = \frac{R_{FBB}}{R_{FBT} + R_{FBB}}$. $K_{FB} = \frac{1}{30}$ for the internal feedback resistor divider.
- Low frequency zero, $\omega_{Z_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$
- High frequency pole, $\omega_{P_EA} \approx \frac{1}{R_{COMP} \times C_{HF}}$

The pole at the origin minimizes the output steady state error. Place the low frequency zero to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost can be achieved at the crossover frequency. Place the high frequency pole beyond the crossover frequency because the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is usually limited to one fifth of the RHPZ frequency.

For higher crossover frequency, R_{COMP} can be increased, while proportionally decreasing C_{COMP} . Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP} , results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

7.2 Typical Application

7.2.1 Application

A typical application example is a dual-phase boost converter as shown in [Figure 7-2](#). This converter is designed for Class-H audio amplifier. The output voltage is adjustable up to 45V. The peak power is 1kVA with an input average current limit of 26A.

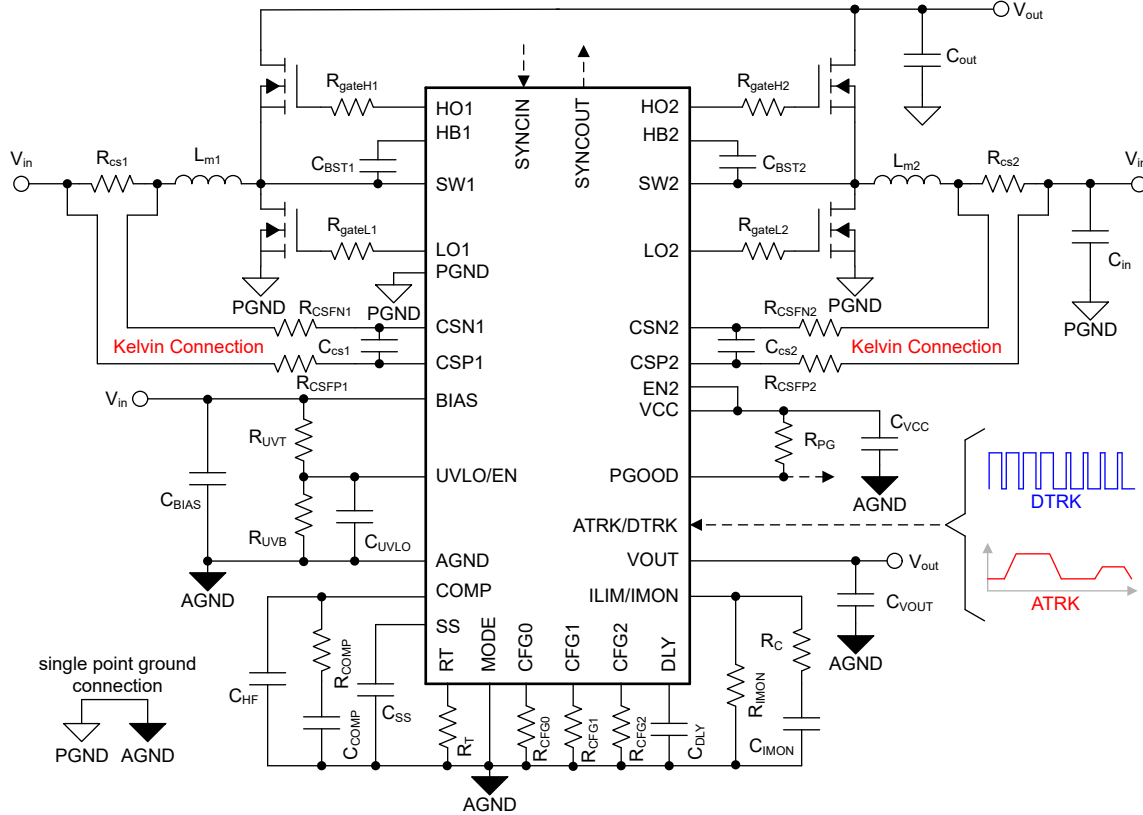


Figure 7-2. Schematic of Dual-phase Boost Converter

7.2.2 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Minimum input voltage, V_{in_min}	9V
Typical input voltage, V_{in_typ}	14.4V
Maximum input voltage, V_{in_max}	18V
Minimum output voltage, V_{out_min}	8V
Maximum output voltage, V_{out_max}	45V
Maximum output power at maximum output voltage and typical input voltage, P_{out_total}	1000W
Rated output power, P_{rated_total}	300W
Maximum delay at twice rated output power and typical input voltage, t_{delay}	100ms
Estimated efficiency, η	95%

7.2.3 Detailed Design Procedure

7.2.3.1 Determine the Total Phase Number

Interleaved operation offers many advantages in high current applications such as higher efficiency, lower component stresses and reduced input and output ripple. For dual phase interleaved operation, the output power path is split reducing the input current in each phase by one-half. Ripple currents in the input and output capacitors are reduced significantly since each channel operates 180 degrees out of phase from the other. As shown in Figure 7-3, the input current ripple is reduced significantly.

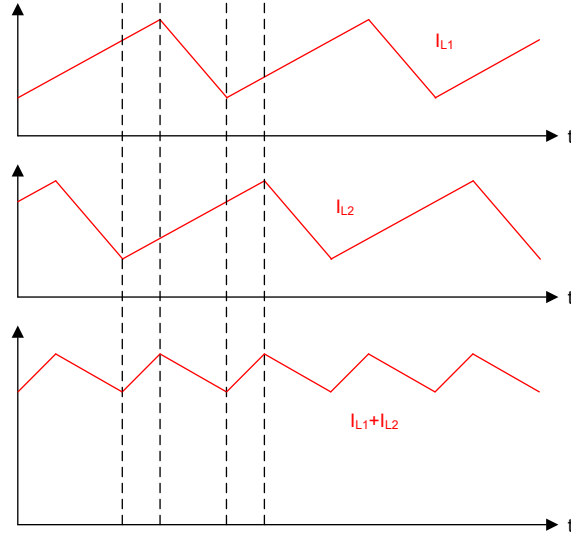


Figure 7-3. Input Current Ripple Reduced With Dual Phase Interleaving

Here 2 phase is selected for the design:

$$N_p = 2 \quad (18)$$

The total power P_{out_total} is shared among phases, the power of each phase can be found as:

$$P_{out} = \frac{P_{out_total}}{N_p} = 500W \quad (19)$$

7.2.3.2 Determining the Duty Cycle

In CCM, The duty cycle is defined as:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad (20)$$

$$D' = 1 - D \quad (21)$$

In this application, the maximum duty cycle can be found as:

$$D_{max} = \frac{V_{out_max} - V_{in_min}}{V_{out_max}} = 0.8 \quad (22)$$

7.2.3.3 Timing Resistor R_T

Generally, higher switching frequency (f_{sw}) leads to smaller size and higher losses. Operation around 400kHz is a reasonable compromise considering size, efficiency and EMI. The value of R_T for 400kHz switching frequency is calculated as follows:

$$R_T = \left(\frac{1}{f_{sw}} - 18ns \right) \times 31.5 \frac{\Omega}{ns} = 78.2k\Omega \quad (23)$$

A standard value of 78.7k Ω is chosen for R_T .

7.2.3.4 Inductor Selection L_m

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the RHPZ frequency of the control loop.

- The inductor current ripple ratio is selected to balance the winding loss and core loss of the inductor. As the ripple current increases the core loss increases and the copper loss decreases.

- The falling slope of the inductor current must be small enough to prevent sub-harmonic oscillation. A larger inductance value results in a smaller falling slope of the inductor current.
- The RHPZ must be placed at high frequency, allowing a higher crossover frequency of the control loop. As the inductance value decrease the RHPZ frequency increases.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle, that is:

$$V_{\text{slope}} \times f_{\text{sw}} > \frac{V_{\text{out_max}} - V_{\text{in_min}}}{2 \times L_m} \times R_{\text{cs}} \quad (24)$$

where

- V_{slope} is a 48mV peak (at 100% duty cycle) slope compensation ramp at the input of the current sense amplifier.

The lower limit of the inductance can be found as:

$$L_m > \frac{V_{\text{out_max}} - V_{\text{in_min}}}{2 \times V_{\text{slope}} \times f_{\text{sw}}} \times R_{\text{cs}} \quad (25)$$

R_{cs} is estimated to = 1.5mΩ, so the following can be found

$$L_m > 1.4\mu\text{H} \quad (26)$$

The RHPZ frequency can be found as:

$$\omega_{\text{RHPZ}} = \frac{R_{\text{out}} \times D^2}{L_{m_eq}} \quad (27)$$

The crossover frequency must be lower than 1/5 of RHPZ frequency:

$$f_c < \frac{1}{5} \times \frac{\omega_{\text{RHPZ}}}{2\pi} \quad (28)$$

Assume a crossover frequency of 1kHz is desired, the upper limit of the inductance can be found as:

$$L_m < 5.2\mu\text{H} \quad (29)$$

The inductor ripple current is typically set between 30% and 70% of the full load current, known as a good compromise between core loss and winding loss of the inductor.

Per phase input current can be calculated as:

$$I_{\text{in_vinmax}} = \frac{P_{\text{out}}}{\eta \times V_{\text{in_max}}} = 29.2\text{A} \quad (30)$$

In continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33%. The input voltage that result in a maximum ripple ratio can be found as:

$$V_{\text{in_RRmax}} = V_{\text{out_max}} \times (1 - 0.33) = 30\text{V} \quad (31)$$

Thus, the maximum input voltage $V_{\text{in_max}}$ must be used to calculate the maximum ripple ratio.

For this example, a ripple ratio of 0.3, 30% of the input current was chosen. Knowing the switching frequency and the typical output voltage, the inductor value can be calculated as follows:

$$L_m = \frac{V_{\text{in_max}}}{I_{\text{in}} \times \text{RR}} \times \frac{1}{f_{\text{sw}}} \times \left(1 - \frac{V_{\text{in_max}}}{V_{\text{out_max}}}\right) = \frac{18\text{V}}{29.2\text{A} \times 0.3} \times \frac{1}{400\text{kHz}} \times 0.6 = 3.1\mu\text{H} \quad (32)$$

The closest standard value of 3.3μH was chosen for L_m .

The inductor ripple current at typical input voltage can be calculated as:

$$I_{pp} = \frac{V_{in_typ}}{L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in_typ}}{V_{out}}\right) = 7.4A \quad (33)$$

If a ferrite core inductor is selected, make sure the inductor does not saturate at peak current limit. The inductance of a ferrite core inductor is almost constant until saturation. Ferrite core has low core loss with a big size.

For powder core inductor, the inductance decreases slowly with increased DC current. This action leads to higher ripple current at high inductor current. For this example, the inductance drops to 70% at peak current limit compared to 0A. The current ripple at peak current limit can be found as:

$$I_{pp_bias} = \frac{V_{in_typ}}{0.7 \times L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in_typ}}{V_{out}}\right) = 10.6A \quad (34)$$

7.2.3.5 Current Sense Resistor R_{CS}

The maximum per phase average input current at typical input voltage and maximum output voltage can be calculated as:

$$I_{in_vintyp} = \frac{P_{out}}{\eta \times V_{in_typ}} = 36.5A \quad (35)$$

The peak current can be calculated as:

$$I_{pk_vintyp} = I_{in_vintyp} + \frac{I_{pp_bias}}{2} = 36.5A + \frac{10.6A}{2} = 41.8A \quad (36)$$

The current sense resistor can be found as:

$$R_{CS} = \frac{V_{CLTH}}{I_{pk_vintyp}} = \frac{60mV}{41.8A} = 1.43m\Omega \quad (37)$$

A standard value of 1.5mΩ is chosen for R_{CS} .

7.2.3.6 Current Sense Filter R_{CSFP} , R_{CSFN} , C_{CS}

The current sense filters are suggested. 100pF of C_{CS} and 1Ω of R_{CSFP} , R_{CSFN} are normal recommendations. C_{CS} must be placed physically as close to the device.

Route CSPx and CSNx traces together with Kelvin connections to the current sense resistors.

Increase C_{CS} and R_{CSFN} to increase the RC time constant. Increasing R_{CSFP} can bring significant current sensing error.

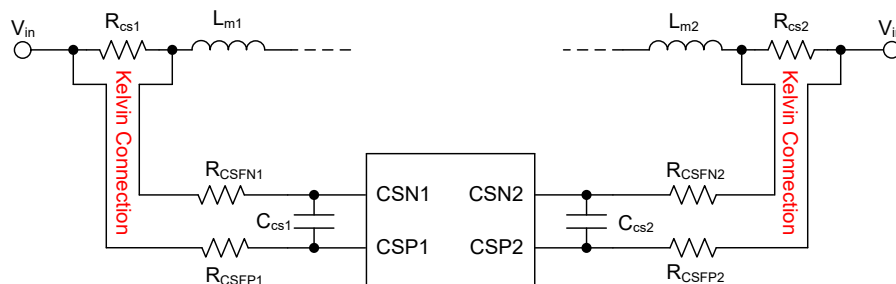


Figure 7-4. Current Sense Filter

7.2.3.7 Low-Side Power Switch Q_L

Select a logic level N-channel MOSFET that 5V VCC is sufficient to completely enhance the MOSFET. Also, note the minimum HOx-SWx voltage is 3.75V during bypass operation. Make sure the MOSFET is turned on at this voltage.

Selection of the power MOSFET devices by breaking down the losses is one way to compare the relative efficiencies of different devices. Losses in the low-side MOSFET device can be separated into conduction loss and switching loss.

Low-side conduction loss is approximately calculated as follows:

$$P_{COND_LS} = D \times I_{in}^2 \times R_{DS(on)} \times 1.3 \quad (38)$$

Where, the factor of 1.3 accounts for the increase in the MOSFET on-resistance due to heating. Alternatively, the factor of 1.3 can be eliminated and the high temperature on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs temperature curves in the MOSFET datasheet.

Switching loss occurs during the brief transition period as the low-side MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET device. The low-side switching loss is approximately calculated as follows:

$$P_{SW_LS} = 0.5 \times V_{out} \times I_{in} \times (t_R + t_F) \times f_{sw} \quad (39)$$

t_R and t_F are the rise and fall times of the low-side MOSFET. The rise and fall times are usually mentioned in the MOSFET data sheet or can be empirically observed with an oscilloscope.

Reverse recovery of the high-side MOSFET increases the fall time and turn on current of the low-side MOSFET resulting in higher turn on loss.

An additional Schottky diode can be placed in parallel with the low-side MOSFET, with short connections to the source and drain in order to minimize negative voltage spikes at the SW node.

7.2.3.8 High-Side Power Switch Q_H and Additional Parallel Schottky Diode

Losses in the high-side MOSFET device can be separated into conduction loss, dead-time loss, and reverse recovery loss. Switching loss is calculated for the low-side MOSFET device only. Switching loss in the high-side MOSFET device is negligible because the body diode of the high-side MOSFET device turns on before and after the high-side MOSFET device switches.

High-side conduction loss is approximately calculated as follows:

$$P_{COND_HS} = D' \times I_{in}^2 \times R_{DS(on)} \times 1.3 \quad (40)$$

Dead-time loss is approximately calculated as follows:

$$P_{DT_HS} = V_D \times I_{in} \times (t_{DLH} + t_{DHL}) \times f_{sw} \quad (41)$$

where

- V_D is the forward voltage drop of the high-side MOSFET body diode.
- t_{DLH} is the deadtime between low side switch turn-off and high side switch turn-on.
- t_{DHL} is the deadtime between high side switch turn-off and low side switch turn-on.

Reverse recovery characteristics of the high-side MOSFET switch strongly affect efficiency, especially when the output voltage is high. Small reverse recovery charge helps to increase the efficiency while also minimizes switching noise.

Reverse recovery loss is approximately calculated as follows:

$$P_{RR_HS} = V_{out} \times Q_{RR} \times f_{sw} \quad (42)$$

where

- Q_{RR} is the reverse recovery charge of the high-side MOSFET body diode.

An additional Schottky diode can be placed in parallel with the high-side switch to improve efficiency. Usually, the power rating of this parallel Schottky diode can be less than the high-side switch because the diode conducts only during dead-times. The power rating of the parallel diode must be high enough to handle inrush current at startup, any load exists before switching, hiccup mode operation, and so forth.

7.2.3.9 Snubber Components

A resistor-capacitor snubber network across the high-side N-channel MOSFET device reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and can couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50Ω. Increasing the value of the snubber capacitor results in more damping, but this action also results higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber can not be necessary with an optimized layout.

7.2.3.10 V_{out} Programming

For fixed output voltage, V_{OUT} can be programmed by connecting a resistor to ATRK/DTRK and turn on precise internal 20μA current source.

$$R_{ATRK} = \frac{V_{out_max}}{6V} \times 10k\Omega = 75k\Omega \quad (43)$$

For class-H audio application, V_{out} can be adjusted to optimize the efficiency. Analog tracking or digital tracking can be applied with ATRK/DTRK.

For analog tracking, apply a voltage to ATRK/DTRK to program V_{out} . The voltage can be found as:

$$V_{\text{ATRK_max}} = \frac{V_{\text{out_max}}}{30} = 1.5\text{V} \quad (44)$$

$$V_{\text{ATRK_min}} = \frac{V_{\text{out_min}}}{30} = 0.4\text{V} \quad (45)$$

The output voltage can also be programmed by digital PWM signal (DTRK). The duty cycle D_{TRK} can be found as:

$$D_{\text{TRK}} = \frac{V_{\text{out_max}}}{0.75\text{V}} \times 100\% = 60\% \quad (46)$$

$$D_{\text{TRK_min}} = \frac{V_{\text{out_min}}}{0.75\text{V}} \times 100\% = 16\% \quad (47)$$

Make sure the DTRK frequency is between 100kHz and 2200kHz.

A two stage RC filter with offset can be utilized to convert a digital PWM signal to analog voltage as shown in [Figure 7-5](#).

The two stage RC filter is used to filter the PWM signal into a smooth analog voltage. The two stage RC filter is selected considering voltage ripple and rise time on ATRK/DTRK.

Pullup resistor (R_{PU}) and pulldown resistor (R_{PD}) are utilized to add an offset voltage to ATRK/DTRK so that 100% PWM duty cycle sets the output voltage to $V_{\text{out_max}}$ and 0% PWM duty cycle sets the output voltage to $V_{\text{out_min}}$.

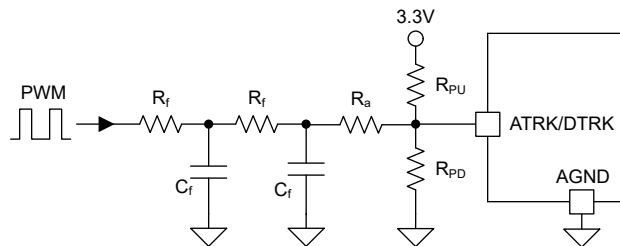


Figure 7-5. Two Stage RC Filter to ATRK/DTRK

In this application, 400kHz PWM frequency is used. $R_f=4.99\text{k}\Omega$, $C_f=47\text{nF}$ are selected for the filter. $R_a=1.5\text{k}\Omega$, $R_{\text{PU}}=51\text{k}\Omega$, $R_{\text{PD}}=7.87\text{k}\Omega$ are selected to create a proper offset voltage.

The voltage ripple and rise time of ATRK/DTRK can be observed in [Figure 7-6](#) and [Figure 7-7](#). The voltage ripple at ATRK/DTRK is $9.2\mu\text{V}$, which is pretty low. And rise time of around 1ms is also good for the audio system.

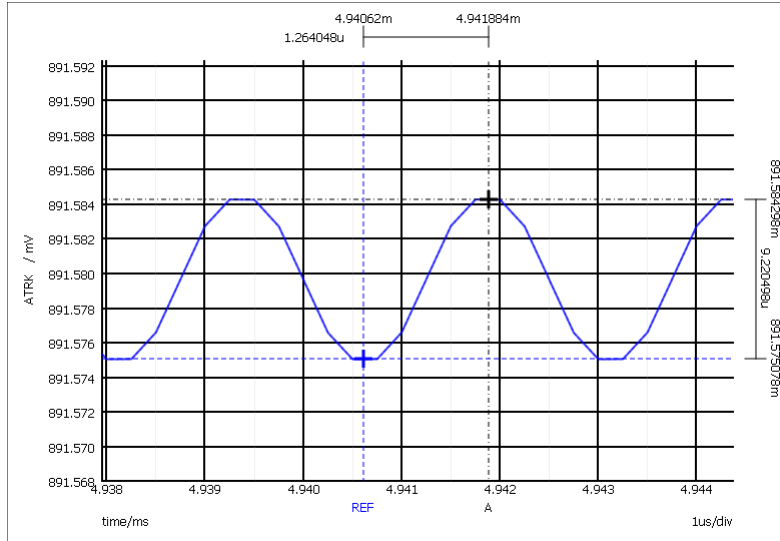


Figure 7-6. Voltage Ripple of ATRK/DTRK

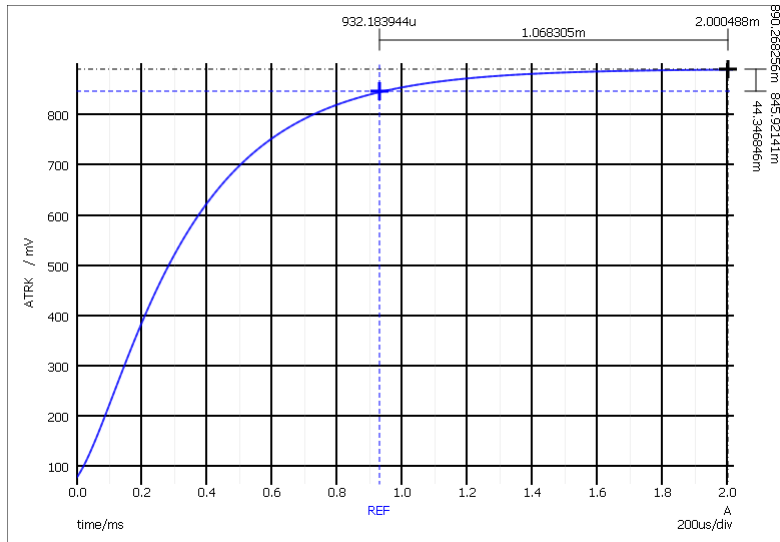


Figure 7-7. Rise Time of ATRK/DTRK

7.2.3.11 Input Current Limit (ILIM/IMON)

In audio applications, the transient power can be high. For this application, 1000W is selected as peak output power. But the average power is typically much lower than the peak power. 300W is selected as average power. With proper ILIM/IMON setting, the average input current can be limited to less than 300W while allowing 1000W peak for 100ms. When the average current loop is triggered, V_{OUT} drops till the input and output power is balanced.

The per phase input current at average output power and typical input voltage can be found as:

$$I_{avg} = \frac{P_{avg_total}}{2 \times \eta \times V_{in_typ}} = 11.0A \quad (48)$$

13A is selected as the average input current limit.

$$I_{lim} = 13A \quad (49)$$

The current out of ILIM/IMON at can be found as:

$$I_{MON_lim} = 2 \times (R_{cs} \times I_{lim} \times G_{IMON} + I_{OFFSET}) = 2 \times (1.5m\Omega \times 13A \times 0.333mA/V + 4\mu A) = 21\mu A \quad (50)$$

R_{ILIM} can be calculated as:

$$R_{IMON} = \frac{V_{ILIM}}{I_{MON}} = \frac{1V}{21\mu A} = 47.6k\Omega \quad (51)$$

A standard value of 47.5kΩ is chosen for R_{IMON} .

As shown in [Figure 7-8](#), C_{IMON} and R_c can be used to create a proper delay before the average current loop is triggered.

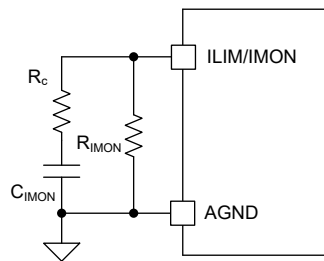


Figure 7-8. ILIM/IMON Pin Configuration

In this application, 100ms delay at twice rated power is required.

At zero load, current out of ILIM/IMON can be found as:

$$I_{MON_0A} = 2 \times I_{OFFSET} = 8\mu A \quad (52)$$

The ILIM/IMON voltage at zero load can be calculated as:

$$V_{IMON_0A} = R_{IMON} \times I_{MON_0A} = 0.38V \quad (53)$$

At twice rated power, current out of ILIM/IMON can be found as:

$$I_{MON_tr} = 2 \times (R_{cs} \times 2 \times I_{lim} \times G_{IMON} + I_{OFFSET}) = 2 \times (1.5m\Omega \times 26A \times 0.333mA/V + 4\mu A) = 34\mu A \quad (54)$$

C_{IMON} can be determined by:

$$C_{IMON} = \frac{t_{delay}}{R_{IMON} \times \ln\left(\frac{R_{IMON} \times I_{MON_tr} - V_{IMON_0A}}{R_{IMON} \times I_{MON_tr} - V_{ILIM}}\right)} = 3.0\mu F \quad (55)$$

A standard value of 3.3μF is chosen for C_{IMON} .

R_c can be determined by:

$$R_c = \frac{1}{20\pi \times C_{IMON}} = 4.8k \quad (56)$$

A standard value of 4.99kΩ is chosen for R_c .

7.2.3.12 UVLO Divider

The desired start-up voltage and the hysteresis are set by the voltage divider R_{UVT} , R_{UVB} . For this design, the start-up voltage (V_{in_on}) is set to 8.5V which is 0.5V below V_{in_min} . UVLO hysteresis voltage is set to 1V. This action results UVLO shutdown voltage (V_{in_off}) of 7.5V. The values of R_{UVT} , R_{UVB} are calculated as follows:

$$R_{UVT} = \frac{V_{in_on} - \frac{V_{UVLO_RISING}}{V_{UVLO_FALLING}} \times V_{in_off}}{I_{UVLO_HYS}} = \frac{8.5V - \frac{1.1V}{1.075V} \times 7.5V}{10\mu A} = 82.6k\Omega \quad (57)$$

A standard value of 82.5kΩ is chosen for R_{UVT} .

$$R_{UVB} = \frac{V_{UVLO_FALLING} \times R_{UVT}}{V_{in_off} - V_{UVLO_FALLING}} = \frac{1.075V \times 82.5k\Omega}{7.5V - 1.075V} = 13.8k\Omega \quad (58)$$

A standard value of 13.8kΩ is chosen for R_{UVB} .

A 100nF UVLO capacitor (C_{UVLO}) is selected in case V_{in} drops below V_{in_off} momentarily during the start-up or during a severe load transient at the low input voltage.

7.2.3.13 Soft Start

The soft-start time at maximum output voltage is the longest. The soft-start capacitor can be found for 6ms soft-start time:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ATRk_max}} \left(\frac{V_{out_max}}{V_{out_max} - V_{in_typ}} \right) = \frac{50\mu A \times 6ms}{1.5V} \left(\frac{45V}{45V - 14.4V} \right) = 0.29\mu F \quad (59)$$

A standard value of 0.33μF is chosen for C_{SS} .

7.2.3.14 CFG Settings

CFG0 is chosen based on deadtime and turn on or turnoff ATRK/DTRK pin 20μA current source referring to [Table 6-1](#).

Here, 50ns deadtime and turning on 20μA current source are selected. Level 3 (1.3kΩ) is selected for CFG0.

CFG1 is selected considering OVP, DRSS, peak current limit latch and PGOOD OVP enable.

Here, 50V OVP (OVP bit 0), DRSS off, I_{CL_latch} disabled, PGOOD OVP disabled are selected. Level 10 (10.5kΩ) is selected for CFG1.

CFG2 is selected considering OVP, interleaving phase angle, SYNCIN, and clock dithering referring to [Table 6-4](#).

Here, 50V OVP (OVP bit 1), 180° interleaving phase angle, SYNCIN disabled, DRSS set according to CFG1 are selected. Level 1 (0Ω) is selected for CFG1.

7.2.3.15 Output Capacitor C_{out}

The output capacitors smooth the output voltage ripple and provide a source of charge during load transient conditions.

Ripple current rating of output capacitor must be carefully selected. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement can be dramatically reduced by placing high-quality ceramic capacitors earlier than the bulk aluminum capacitors close to the power switches.

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors.

The single phase boost output RMS ripple current can be expressed as:

$$I_{1p_rms} \approx I_{out} \times \sqrt{\frac{D}{1-D}} \quad (60)$$

The output RMS current is reduced with interleaving as shown in [Figure 7-10](#). Dual phase interleaved boost output RMS ripple current can be expressed as:

$$I_{out_2p_rms} \approx \begin{cases} \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{D \times (1-2D)}{D'}}, & D < 0.5 \\ \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{2D-1}{D'}}, & D \geq 0.5 \end{cases} \quad (61)$$

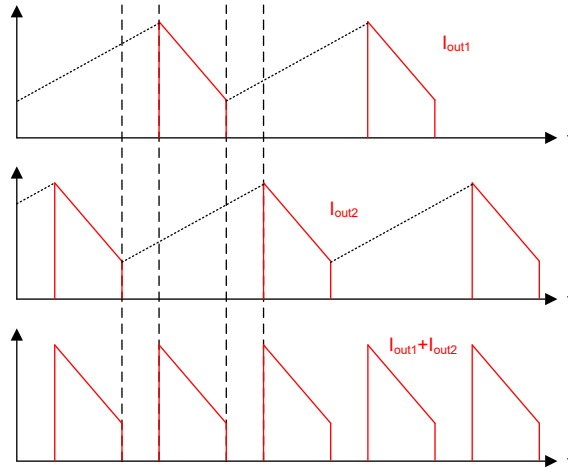


Figure 7-9. Normalized Output Capacitor RMS Ripple Current

Decoupling capacitors are critical for minimized voltage spike of the MOSFETs. This is also important from EMI view. Quite a few 0603/100nF ceramic capacitors are placed close to the MOSFETs following "vertical loop" concept. Refer to [Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout application brief](#) for more details.

A few 10μF ceramic capacitors are also necessary to reduce the output voltage ripple and split the output ripple current.

Typically, aluminum capacitors are required for high capacitance. In this example, four 150μF aluminum capacitors are selected.

The output transient response is closely related to the bandwidth of the loop gain and the output capacitance. According to [How to Determine Bandwidth from the Transient-response Measurement technical article](#), the overshoot or undershoot V_p can be estimated as:

$$V_p = \frac{\Delta I_{tran}}{2\pi \times f_c \times C_{out}} \quad (62)$$

where ΔI_{tran} is the transient load current step.

Please be aware that [Equation 62](#) is valid only if the converter is always operating in CCM or FPWM during load step. If the converter enters DCM or pulsing skip mode at light load, the overshoot is worse.

Due to the inherent path from input to output, unlimited inrush current can flow when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising must be controlled by a hot-swap or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side MOSFET.

7.2.3.16 Input Capacitor C_{in}

Input capacitors are always required to provide a stable input voltage. The input capacitors must be able to handle the inductor ripple current.

The single phase boost input RMS ripple current can be expressed as:

$$I_{in_1p_rms} = \frac{I_{pp}}{\sqrt{12}} \quad (63)$$

The input RMS current is reduced with interleaving as shown in [Figure 7-10](#). Dual phase interleaved boost input RMS ripple current can be expressed as:

$$I_{in_2p_rms} = \begin{cases} \frac{I_{pp}}{\sqrt{12}} \times \frac{1-2D}{D}, & D < 0.5 \\ \frac{I_{pp}}{\sqrt{12}} \times \frac{2D-1}{D}, & D \geq 0.5 \end{cases} \quad (64)$$

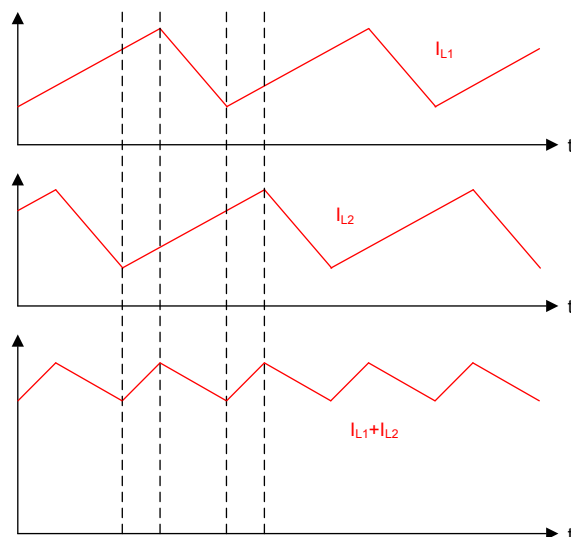


Figure 7-10. Normalized Output Capacitor RMS Ripple Current

The input capacitor is also an important part of the input filter. Higher capacitance and ESR help damping the input filter better. Aluminum electrolytic capacitor is a good choice for input capacitor with high capacitance and ESR. Refer to [Input Filter Design for Switching Power Supplies application note](#) for more details.

7.2.3.17 Bootstrap Capacitor

The bootstrap capacitor between the HBx and SWx pin supplies the gate current to charge the high-side MOSFET device gate during each cycle's turn-on and also supplies recovery charge for the bootstrap diode. These current peaks can be several amperes. The recommended value of the bootstrap capacitor is 0.1μF. C_{BST} must be a good-quality, low-ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. The minimum value for the bootstrap capacitor is calculated as follows:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \quad (65)$$

where

- Q_G is the high-side MOSFET gate charge at VCC = 5V
- ΔV_{BST} is the tolerable voltage droop on C_{BST}, which is typically less than 5% of VCC or 0.15V, conservatively

In this example, the value of the bootstrap capacitors (C_{BST}) are 0.1μF.

7.2.3.18 VCC Capacitor C_{VCC}

The primary purpose of the VCC capacitor is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The value of C_{VCC} must be at least 10 times greater than the value of C_{BST} and must be a good-quality, low-ESR, ceramic capacitor. Place C_{VCC} close to the pins of the device to minimize potentially damaging voltage transients caused by trace inductance.

A value of 10µF was selected for this design example.

7.2.3.19 BIAS Capacitor

The C_{BIAS} capacitor must be a high-quality, ceramic capacitor and placed physically close to the device.

A value of 1µF is selected for this design example.

7.2.3.20 VOUT Capacitor

The C_{OUT} capacitor must be a high-quality, ceramic capacitor and placed physically close to the device.

A value of 0.1µF is selected for this design example.

7.2.3.21 Loop Compensation

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the following four steps:

1. Select crossover frequency, f_c. Select the cross over frequency (f_c) at one fifth of the RHPZ frequency or one tenth of the switching frequency whichever is lower. RHPZ at minimum input voltage and maximum output voltage must be considered.

$$\frac{f_{sw}}{10} = 40\text{kHz} \quad (66)$$

$$\frac{f_{RHPZ}}{5} = \frac{R_{out} \times D^2}{5 \times 2\pi \times L_{m_eq}} = 1.6\text{kHz} \quad (67)$$

Crossover frequency f_c=1.5kHz is selected .

2. Determine required R_{COMP}

Knowing f_c, R_{COMP} is calculated as follows:

$$R_{COMP} = \frac{2\pi \times f_c \times C_{out} \times A_{cs} \times R_{cs_eq}}{D' \times K_{FB} \times g_m} = \frac{2\pi \times 1.6\text{kHz} \times 600\mu\text{F} \times 10 \times 0.75\text{m}\Omega}{0.2 \times \frac{1}{30} \times 1 \frac{\text{mA}}{\text{V}}} = 6.78\text{k}\Omega \quad (68)$$

A standard value of 6.8kΩ is selected for R_{COMP}

3. Determine C_{COMP}

Place ω_{Z_EA} at the load pole frequency ω_{P_LF} to cancel load pole. Knowing R_{COMP}, C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{R_{COMP} \times \omega_{P_LF}} = \frac{1}{6.8\text{k}\Omega \times \frac{2}{2.025\Omega \times 600\mu\text{F}}} = 89\text{nF} \quad (69)$$

A standard value of 100nF is selected for C_{COMP}

4. Determine C_{HF}.

Place ω_{HF} at ω_{RHPZ} or ω_{Z_ESR} zero whichever is lower. Knowing R_{COMP}, RHPZ and ESR zero, C_{HF} is calculated as follows:

$$C_{HF} = \frac{1}{R_{COMP} \times \omega_{HF}} = \frac{1}{6.8\text{k}\Omega \times 49\text{kHz}} = 3\text{nF} \quad (70)$$

A standard value of 3.3nF is selected for C_{HF}.

7.2.4 Application Curves

7.2.4.1 Efficiency

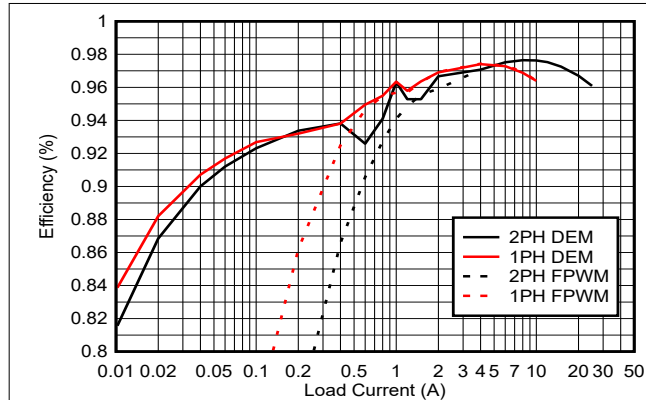


Figure 7-11. Efficiency vs Output Current, $V_{in} = 14.4V$, $V_{out} = 24V$

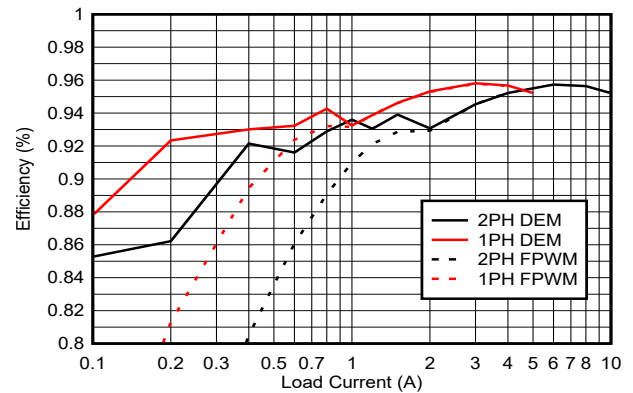


Figure 7-12. Efficiency vs Output Current, $V_{in} = 14.4V$, $V_{out} = 45V$

7.2.4.2 Steady State Waveforms

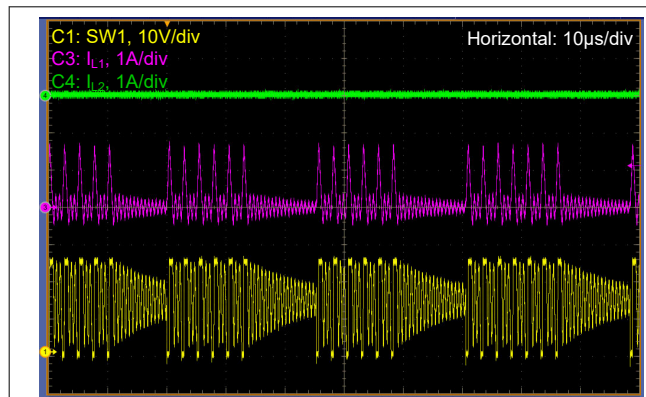


Figure 7-13. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 0.1A$

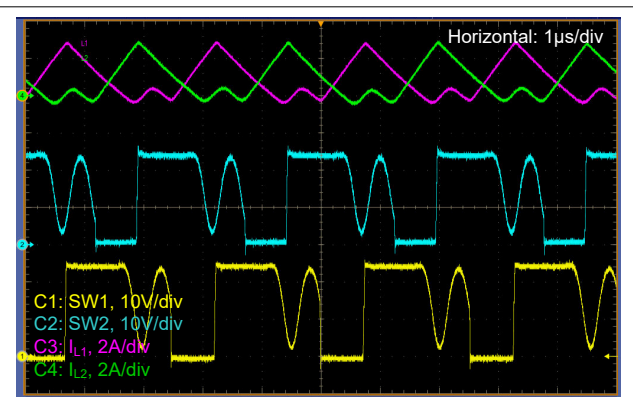


Figure 7-14. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 1A$

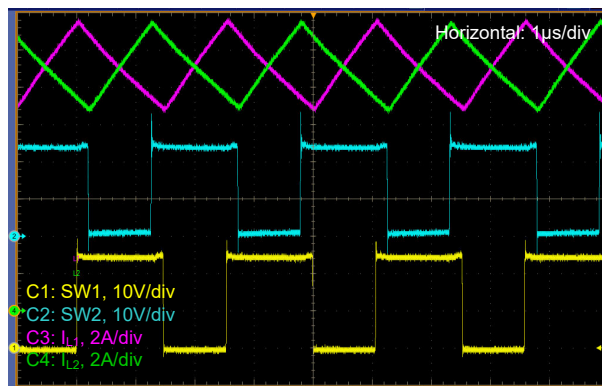


Figure 7-15. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 15A$

7.2.4.3 Step Load Response

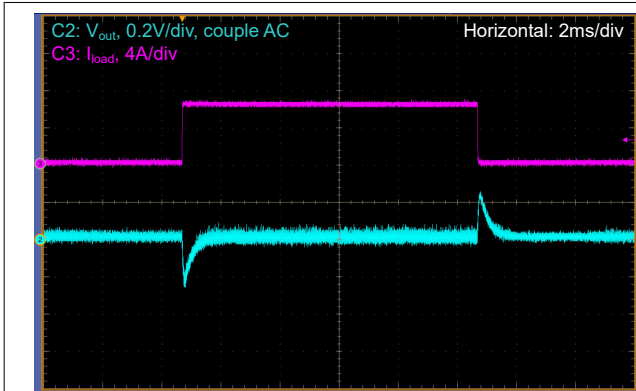


Figure 7-16. Load Transient, $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$ to $6.25A$ at $1A/\mu s$

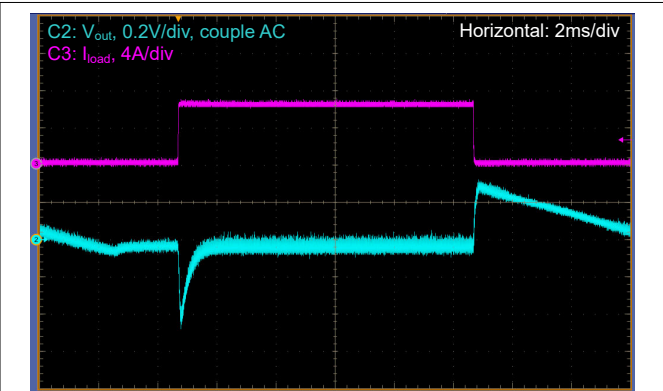


Figure 7-17. Load Transient, $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 0A$ to $6.25A$ at $1A/\mu s$

7.2.4.4 Sync Operation

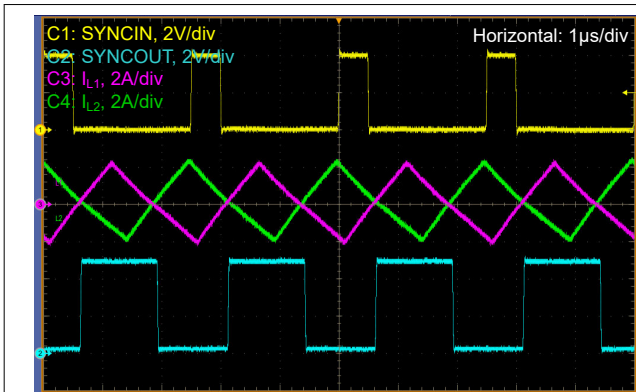


Figure 7-18. $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$, CFG2 = Level 13

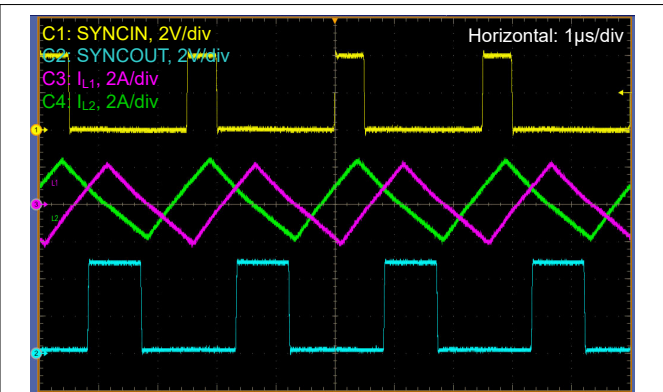
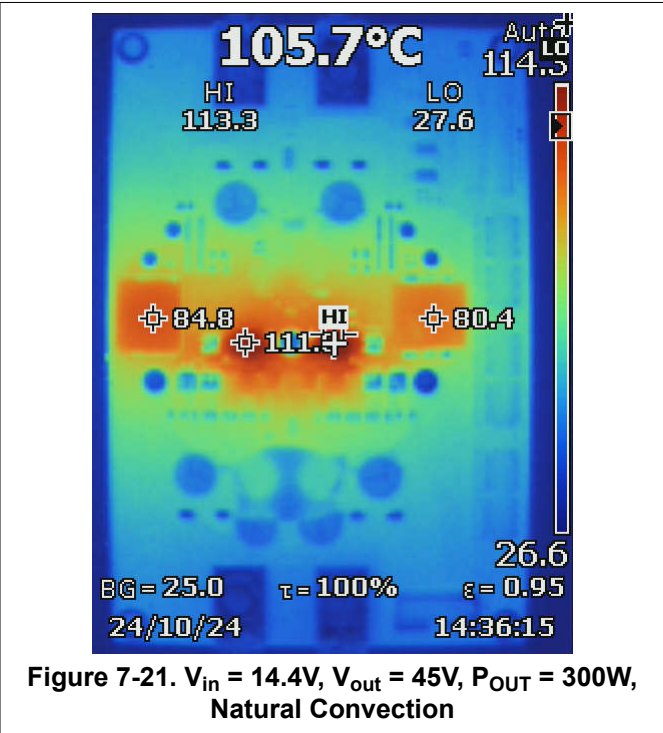
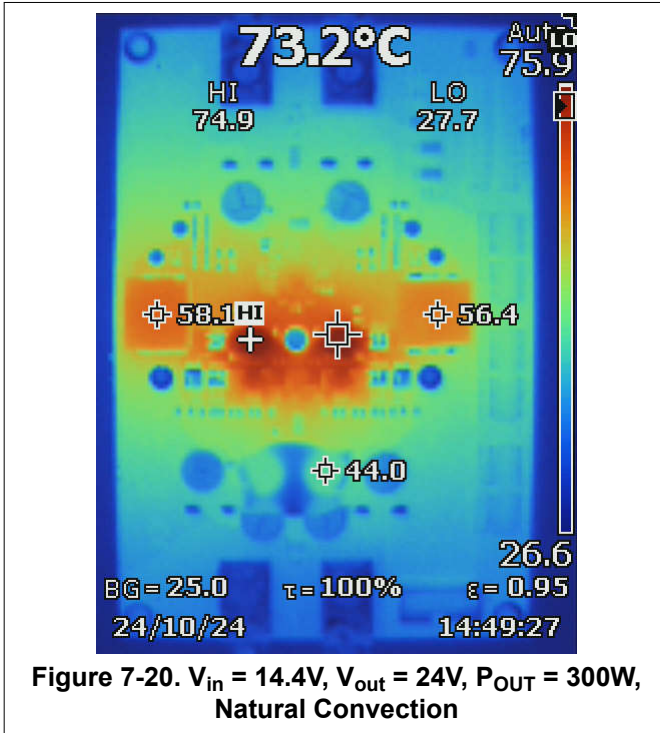


Figure 7-19. $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$, CFG2 = Level 11

ADVANCE INFORMATION

7.2.4.5 Thermal Performance



7.3 Power Supply Recommendations

The LM5125-Q1 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use [Equation 71](#) to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{71}$$

where

- η the efficiency.

One way to get a value for the efficiency is the data from the efficiency graphs in [Efficiency](#) in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at V_I each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Unless carefully designed, the EMI input filter can lead to instability as well as some of the previously mentioned affects.

7.4 Layout

7.4.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. Poor PCB design can cause among others converter instability, load regulation problems, noise or EMI issues. Thermal relieved connections in the power path, for VCC or the bootstrap capacitor, must not be used as thermal relieved connections add significant inductance.

- Place the VCC, BIAS, HB1 and HB2 capacitors close to the corresponding device pins and connect them with short and wide traces to minimize inductance, as the capacitors carry high peak currents.
- Place CSN1, CSP1, CSN2, and CSP2 filter resistors and capacitors close to the corresponding device pins to minimize noise coupling between the filter and the device. Route the traces to the sense resistors R_{CS1} and R_{CS2} , which are placed close to the inductor, as differential pair and surrounded by ground to avoid noise coupling. Use Kelvin connections to the sense resistors.
- Place the compensation network R_{COMP} and C_{COMP} as well as the frequency setting resistor R_{RT} close to the corresponding device pins and connect them with short traces to avoid noise coupling. Connect the analog ground pin AGND to these components.
- Place the ATRK resistor R_{ATRK} (when used) close to the ATRK pin and connect to AGND.
- Note the layout of following components is not so critical:
 - Soft-start capacitor C_{SS}
 - DLY capacitor C_{DLY}
 - ILIM/IMON resistor and capacitor R_{ILIM} and C_{ILIM}
 - CFG0, CFG1 and CFG2 resistors
 - UVLO/EN resistors
- Connect the AGND and PGND pin directly to the exposed pad (EP) to form a star connection at the device.
- Connect the device exposed pad (EP) with several vias to a ground plane to conduct heat away.
- Separate power and signal traces and use a ground plane to provide noise shielding.

The gate drivers incorporate short propagation delays, automatic dead time control, and low-impedance output stages capable of delivering high peak currents. Fast rise, fall times make sure of rapid turn-on and turn-off transitions of the power MOSFETs enabling high efficiency. Stray and parasitic gate loop inductance must be minimized to avoid high ringing.

- Place the high-side and low-side MOSFETs close to the device.
- Connect the gate driver outputs HO1, HO2, LO1 and LO2 with a short trace to minimize inductance.
- Route HO1, HO2 and SW1, SW2 to the MOSFETs as a differential pair using the flux cancellation effect reducing the loop area.
- Place the V_{OUT} capacitors close to the high-side MOSFETs. Use short and wide traces to minimize the power stage loop C_{OUT} to high-side MOSFET drain connection to avoid high voltage spikes at the MOSFET.
- Connect the low-side MOSFET source connection with short and wide traces to the V_{OUT} and V_I capacitors ground to minimize inductance causing high voltage spikes at the MOSFET.
- Use copper areas for cooling at the MOSFETs thermal pads.

To spread the heat generated by the MOSFETs and the inductor, place the inductor away from the power stage (MOSFETs). However, the longer the trace between the inductor and the low-side MOSFET (switch node) the higher the EMI and noise emissions. For highest efficiency, connect the inductor by wide and short traces to minimize resistive losses.

7.4.2 Layout Example

ADVANCE INFORMATION

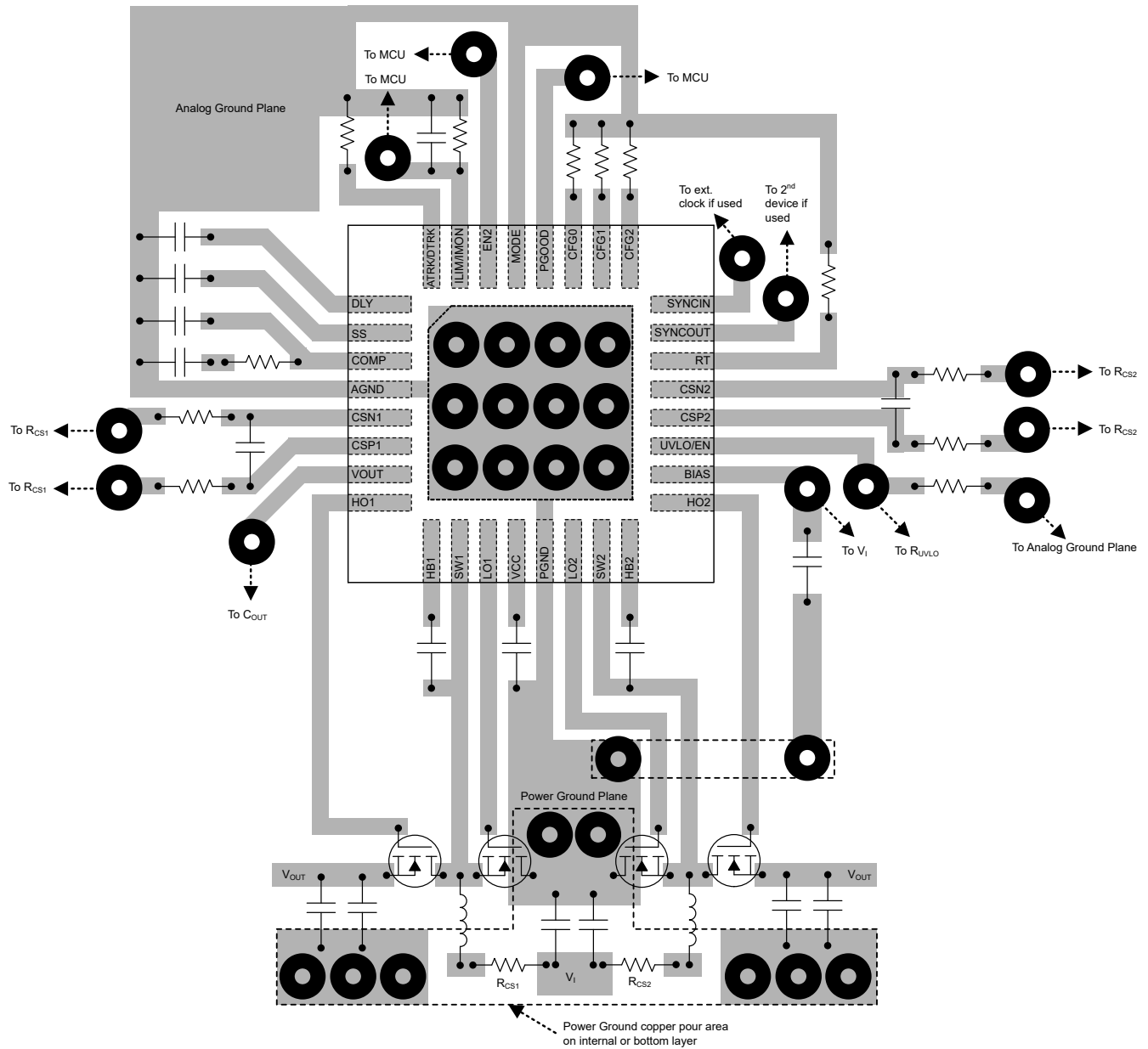


Figure 7-22. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Input Filter Design for Switching Power Supplies application note](#)
- Texas Instruments, [Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout application brief](#)
- Texas Instruments, [How to Determine Bandwidth from the Transient-response Measurement technical article](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

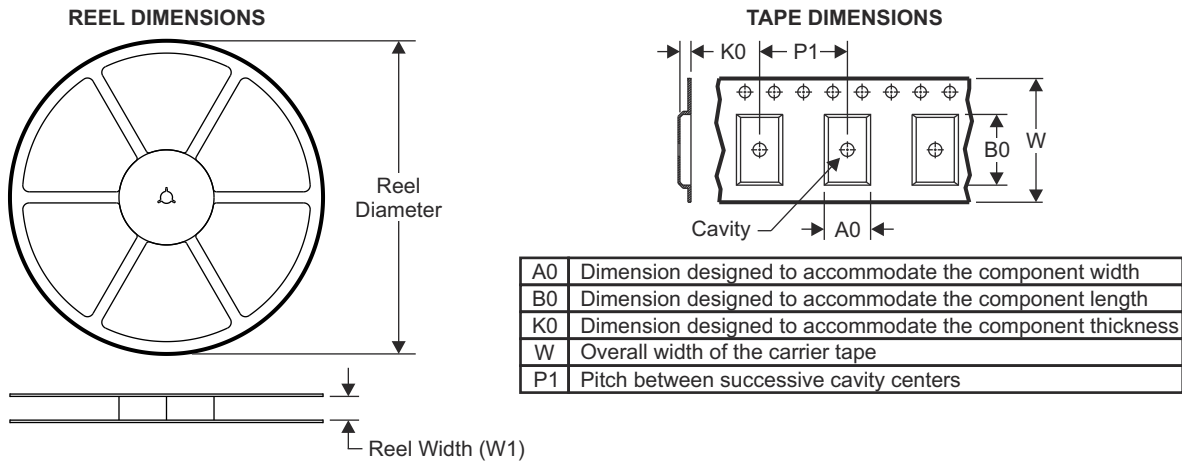
9 Revision History

DATE	REVISION	NOTES
December 2024	*	Initial Release

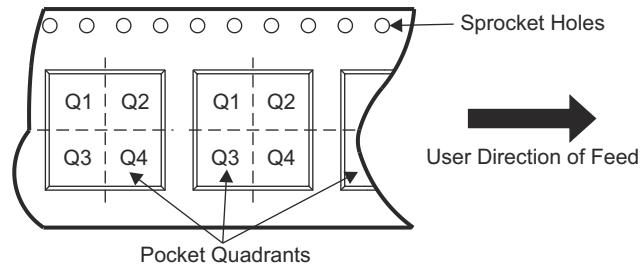
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information



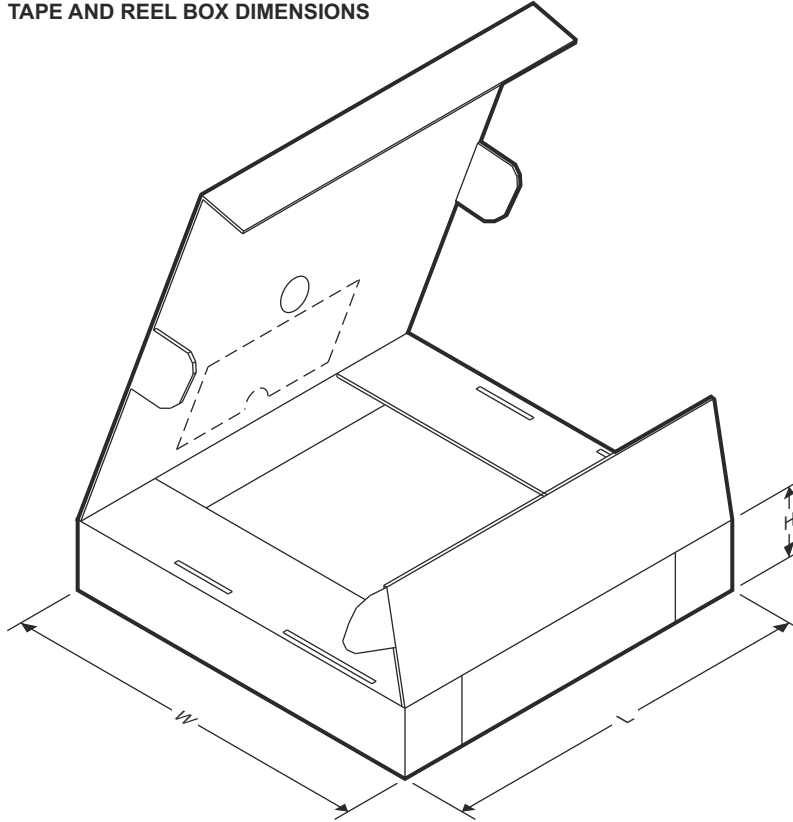
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5125-Q1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION

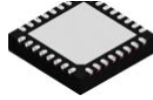
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5125-Q1	VQFN	RHB	32	3000	346.0	346.0	33.0

ADVANCE INFORMATION

RHB0032U

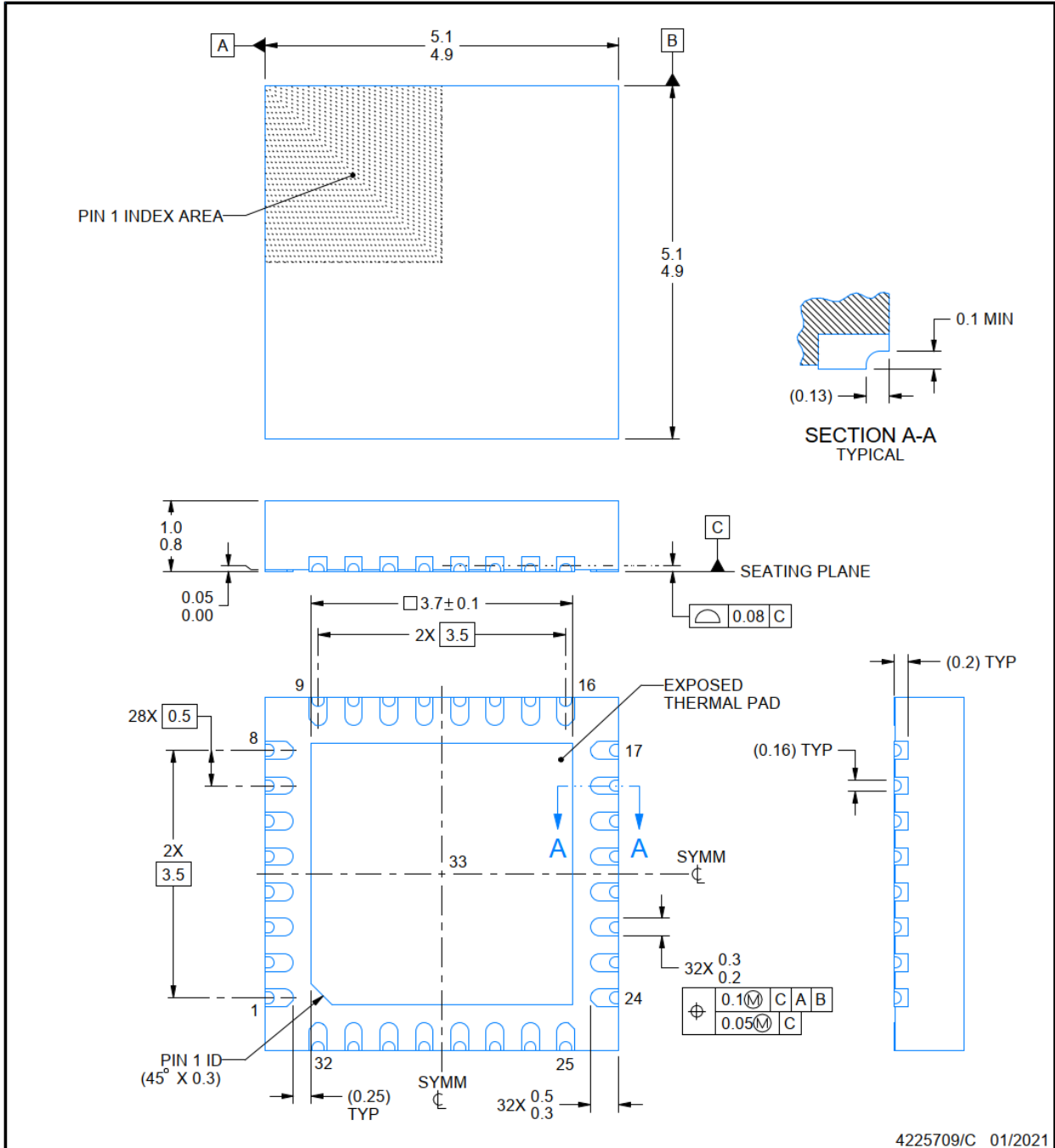


PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



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NOTES:

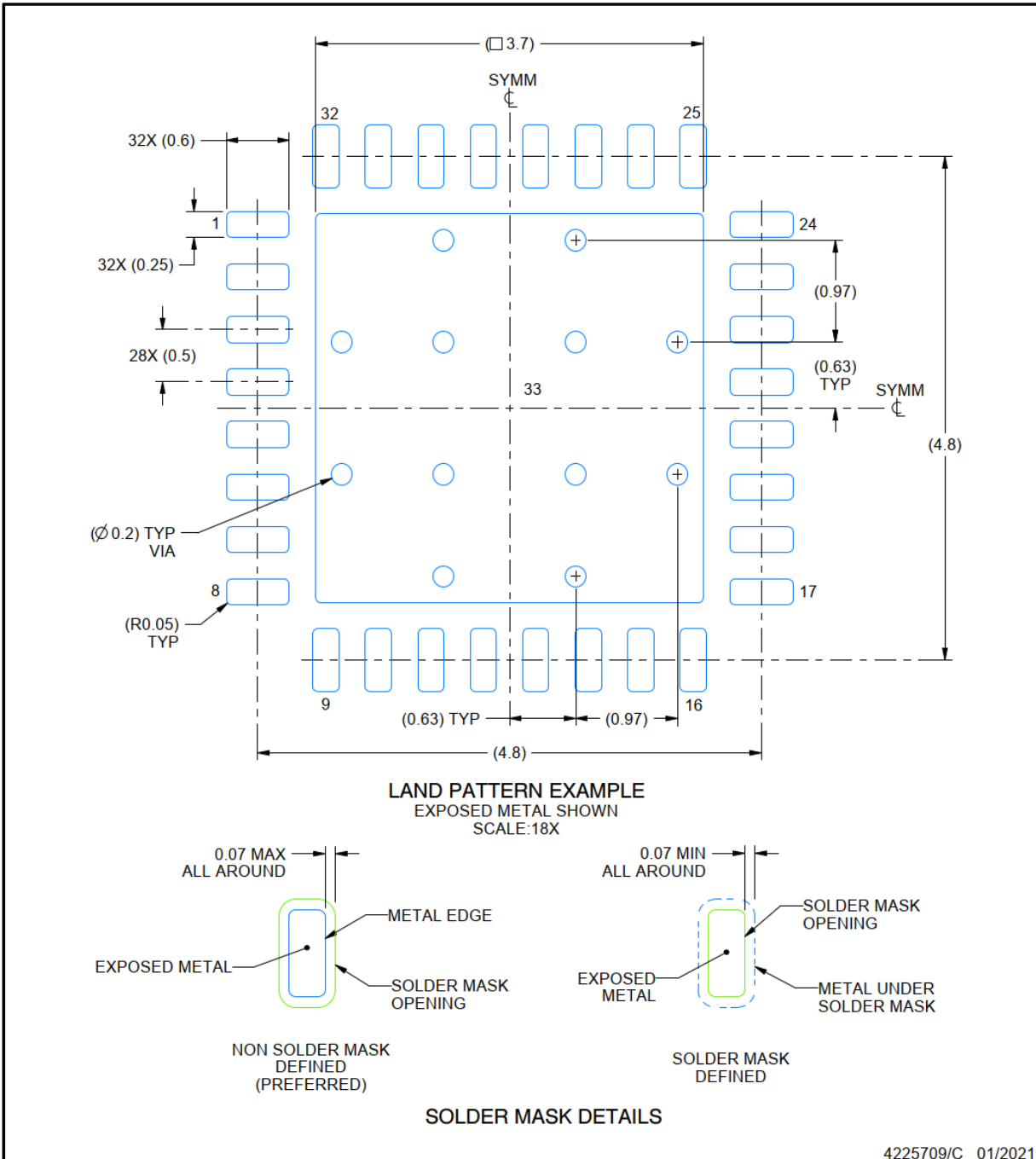
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

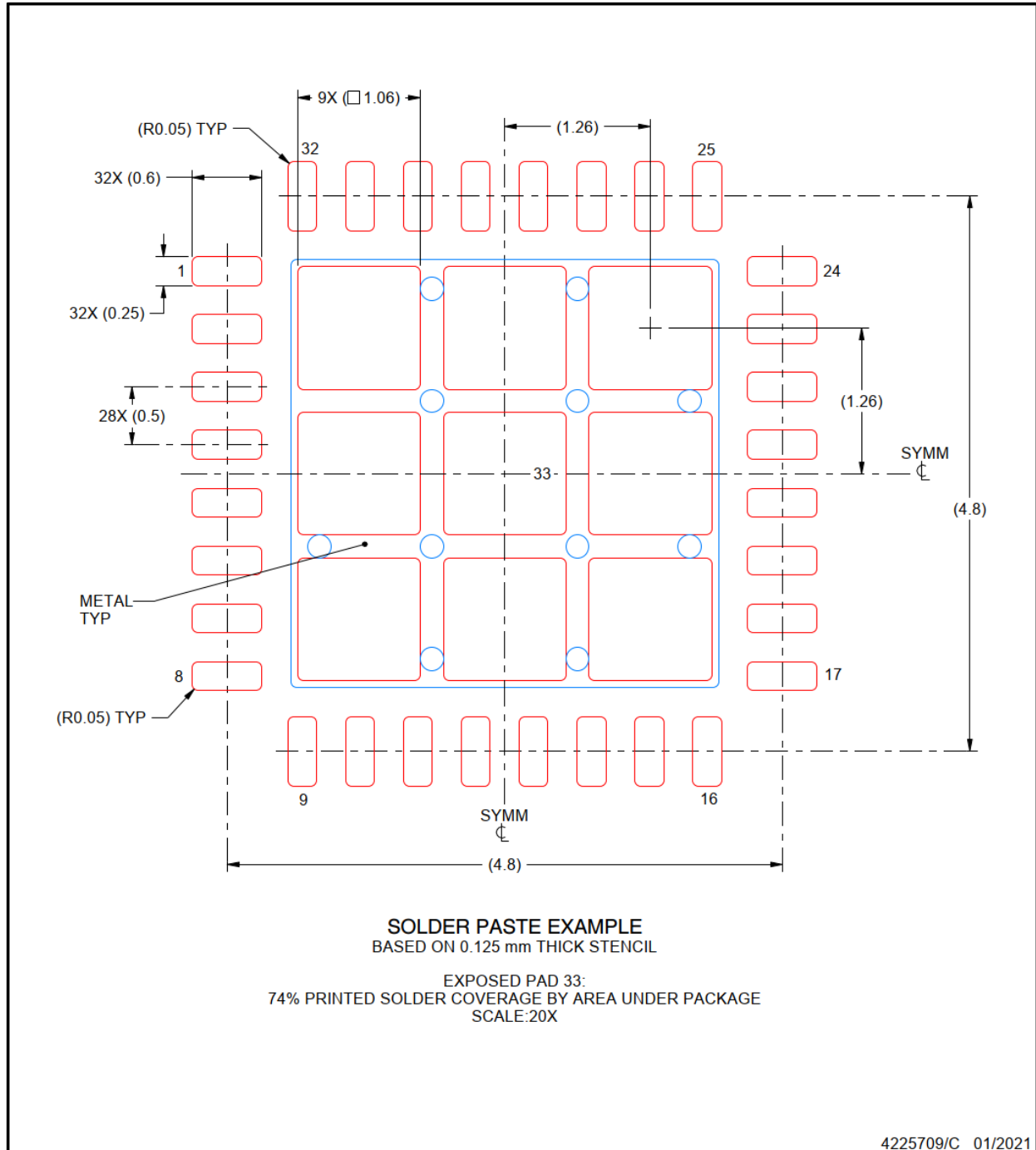
EXAMPLE STENCIL DESIGN

RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XLM5125QRHBRQ1	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

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