TL331LV-Q1, TL391LV-Q1, LM393LV-Q1 and LM339LV-Q1 Low Voltage Automotive Rail to Rail Input Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
- 1.65 V to 5.5 V supply range
- Rail-to-Rail input with Failsafe
- Low input offset voltage 400 µV typical
- 600ns typical propagation delay
- Low quiescent current 25 µA/Ch typical
- Low input bias current 5 pA typical
- Open-drain output
- Full -40°C to +125°C temperature range
- Power-On-Reset (POR) for known start-up
- 2 kV ESD protection
- Improved replacement for TL331-Q1, LM393-Q1 & LM339-Q1 family for V_{CC} ≤ 5 V.
- Alternate pinout for single (TL391-Q1)

2 Applications

- Vacuum robot
- Single phase UPS
- Server PSU
- Cordless power tool
- Wireless infrastructure
- Appliances
- Building automation
- Factory automation & control
- Motor drives
- Infotainment & cluster

3 Description

The LV device family consists of single, dual and quad independent voltage comparators that operate from a wide supply voltage range. The LV devices can drop-in replace the standard TL331-Q1, LM2xx, LM3xx and LM290x-Q1 comparator family in low voltage (≤ 5 V) applications for improved performance and added features.

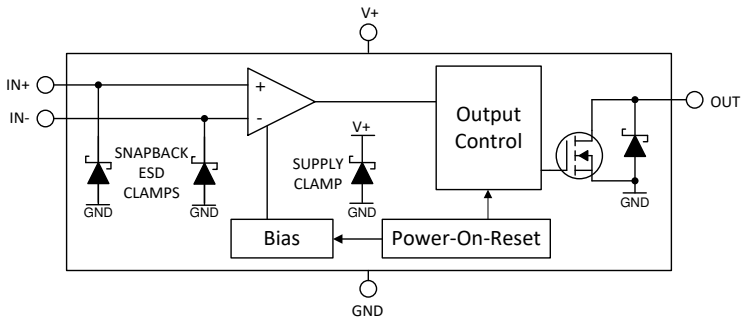
The LV devices include a Power-On-Reset (POR) feature to make sure the output is in a High-Z state until the minimum supply voltage has been reached to prevent output transients during power-up and power-down. The family also feature Rail to Rail inputs that can go up to 6 V without damage or phase inversion.

The LV devices are specified for the temperature range of -40°C to +125°C, which covers the ranges of the TL331-Q1, LM2xx-Q1, LM3xx and LM290x-Q1 comparator families.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TL331LV-Q1, TL391LV-Q1 (Single)	SOT-23 (5)	1.60 mm x 2.90 mm
LM393LV-Q1 (Dual)	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	2.00 mm × 2.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
LM339LV-Q1 (Quad)	SOIC (14)	3.91 mm × 8.65 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	SOT-23 (14)	4.20 mm x 2.00 mm
	WQFN (16) (Preview)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram

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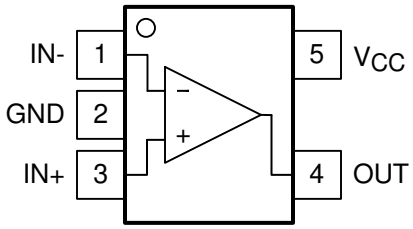
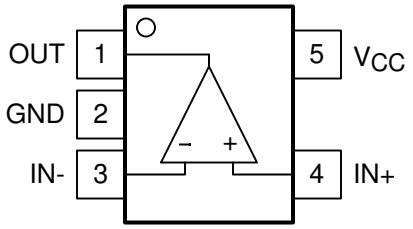
4 Pin Configuration and Functions

4.1 Pin Functions for TL331LV-Q1 and TL391LV-Q1



Note reversed inputs compared to similar common pinout

Figure 4-1. TL331LV-Q1
"TL331-Q1 Type" Pinout
5-Pin SOT-23
Top View



Note reversed inputs compared to similar common pinout

Figure 4-2. TL391LV-Q1
"TS391 type" NW pinout with reversed inputs
5-Pin SOT-23
Top View

PIN			TYPE	DESCRIPTION
	TL331LV-Q1	TL391LV-Q1		
NAME	NO.	NO.		
IN+	3	4	I	Positive Input
IN–	1	3	I	Negative Input
OUT	4	1	O	Open Collector Output
V_{CC}	5	5	—	Positive Power Supply
GND	2	2	—	Ground (Negative Power Supply)

4.2 Pin Functions: LM393LV-Q1

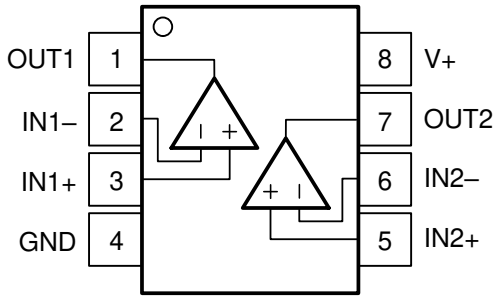
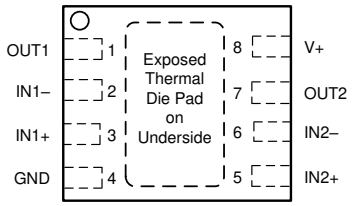


Figure 4-3. D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8
Top View



NOTE: Connect exposed thermal pad directly to GND pin.

Figure 4-4. DSG Package
8-Pad WSON With Exposed Thermal Pad
Top View

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	Output	Output pin of the comparator 1
IN1–	2	Input	Inverting input pin of comparator 1
IN1+	3	Input	Noninverting input pin of comparator 1
GND	4	—	Negative supply
IN2+	5	Input	Noninverting input pin of comparator 2
IN2–	6	Input	Inverting input pin of comparator 2
OUT2	7	Output	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to GND pin

4.3 Pin Functions: LM339LV-Q1

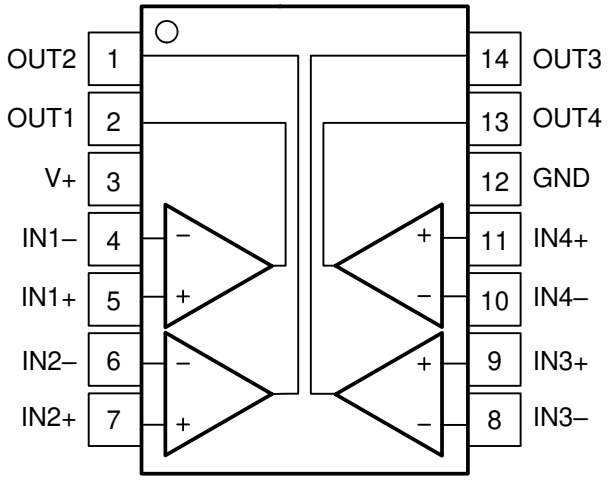
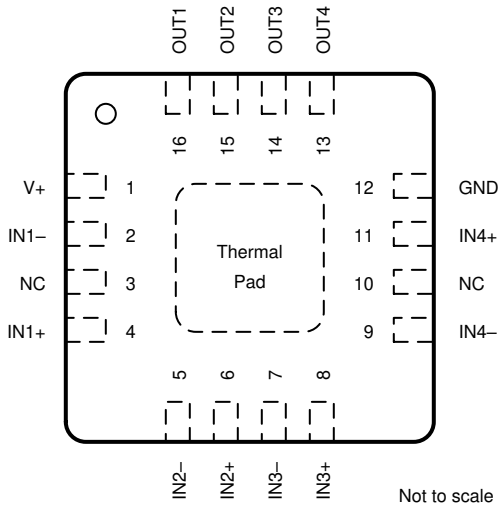


Figure 4-5. D, PW, DYY Package
14-Pin SOIC, TSSOP, SOT-23
Top View



NOTE: Connect exposed thermal pad directly to GND pin.

Figure 4-6. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

Table 4-1. Pin Functions: LM339LV-Q1

PIN			I/O	DESCRIPTION
NAME[1]	SOIC	WQFN		
OUT2	1	15	Output	Output pin of the comparator 2
OUT1	2	16	Output	Output pin of the comparator 1
V+	3	1	—	Positive supply
IN1–	4	2	Input	Negative input pin of the comparator 1
IN1+	5	4	Input	Positive input pin of the comparator 1
IN2–	6	5	Input	Negative input pin of the comparator 2
IN2+	7	6	Input	Positive input pin of the comparator 2
IN3–	8	7	Input	Negative input pin of the comparator 3
IN3+	9	8	Input	Positive input pin of the comparator 3
IN4–	10	9	Input	Negative input pin of the comparator 4
IN4+	11	11	Input	Positive input pin of the comparator 4
GND	12	12	—	Negative supply
OUT4	13	13	Output	Output pin of the comparator 4
OUT3	14	14	Output	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to GND pin

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in channel naming convention.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (GND)	–0.3	6	V
Input pins (IN+, IN–) from GND	–0.3	6	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) from GND	–0.3	6	V
Output short circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, Tstg	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-0111	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (GND)	1.65	5.5	V
Input voltage range (IN+, IN–) from (GND)	–0.1	5.6	V
Ambient temperature, T_A	–40	125	°C

5.4 Thermal Information for TL3x1LV-Q1

THERMAL METRIC (1)		TL3x1LV-Q1 DBV (SOT-23) 5 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	223.7	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	123.2	°C/W
R_{qJB}	Junction-to-board thermal resistance	91.4	°C/W
y_{JT}	Junction-to-top characterization parameter	58.7	°C/W
y_{JB}	Junction-to-board characterization parameter	91.0	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Thermal Information, LM393LV-Q1

THERMAL METRIC (1)		LM393LV-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	167.7	221.7	215.8	175.2	240.0	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	107.0	109.1	105.2	178.1	151.0	°C/W
R_{qJB}	Junction-to-board thermal resistance	111.2	152.5	137.5	139.5	157.0	°C/W
y_{JT}	Junction-to-top characterization parameter	53.1	36.4	39.6	47.2	32.8	°C/W
y_{JB}	Junction-to-board characterization parameter	110.4	150.7	135.9	138.9	155.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	127.3	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Thermal Information, LM339LV-Q1

THERMAL METRIC(1)		LM339LV-Q1				UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)	DYY (SOT-23)	
		14 PINS	14 PINS	16 PINS	14 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	136.0	155.0	134.1	211.1	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	91.2	82.0	122.6	121.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	92.0	98.5	109.3	120.4	°C/W
y_{JT}	Junction-to-top characterization parameter	46.9	25.7	30.9	22.3	°C/W
y_{JB}	Junction-to-board characterization parameter	91.6	97.6	108.3	120.1	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	98.7	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics, TL3x1LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = (GND) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V	–2	±0.4	2	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–3		3	mV
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±1.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current	V_S = 1.8 V and 5 V, No Load, Output Low		26	35	µA
I_Q	Quiescent current	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			50	µA
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C	70	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(GND)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	60	65		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal differential voltage amplification		50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from GND	I_{SINK} = 4 mA, T_A = 25°C		150	200	mV
V_{OL}	Voltage swing from GND	I_{SINK} = 4 mA, T_A = –40°C to +125°C			300	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	60	100		mA

5.8 Switching Characteristics, TL3x1LV-Q1

For V_S (Total Supply Voltage) = (V+) – () = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		20		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ)		1		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (GND), V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ)		50		µs

5.9 Electrical Characteristics, LM393LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = (GND) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V	–2	±0.4	2	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–3		3	mV
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±1.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		25	35	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			50	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C	70	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(GND)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	60	65		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal gain		50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		150	200	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			300	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	60	100		mA

5.10 Switching Characteristics, LM393LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
$T_{PD\text{-}HL}$	Propagation delay time, high-to-low	V_{ID} = –10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
$T_{PD\text{-}LH}$	Propagation delay time, low-to-high	V_{ID} = 10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		20		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ)		1		MHz
POWER ON TIME						

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (GND) , V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ)		50		µs

5.11 Electrical Characteristics, LM339LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = (GND) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V	–2	±0.4	2	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–3		3	mV
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±1.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		25	35	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			50	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C	70	80		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(GND)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	60	65		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (GND) < V_{CM} < (V+), T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal gain		50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (GND)	I_{SINK} = 4 mA, T_A = 25°C		150	200	mV
V_{OL}	Voltage swing from (GND)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			300	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	60	125		mA

5.12 Switching Characteristics, LM339LV-Q1

For V_S (Total Supply Voltage) = (V+) – (GND) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 10 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ)		600		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		20		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ)		1		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (GND) , V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ)		50		µs

5.13 Typical Characteristics

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

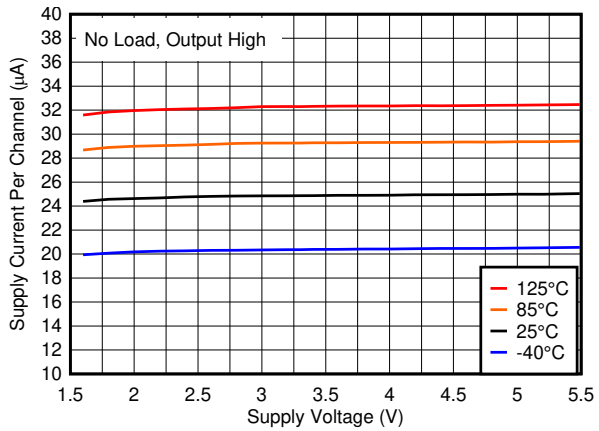


Figure 5-1. Supply Current vs. Supply Voltage

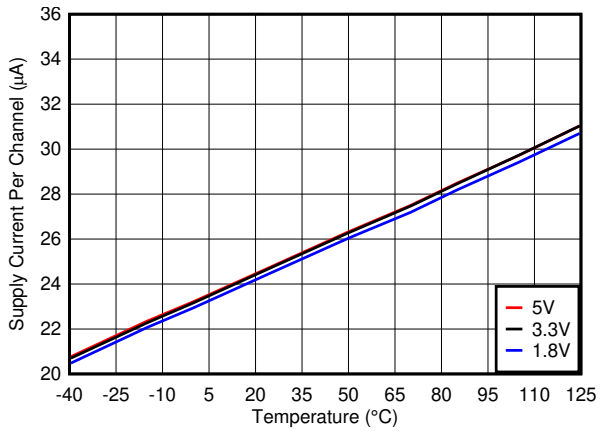


Figure 5-2. Supply Current vs. Temperature

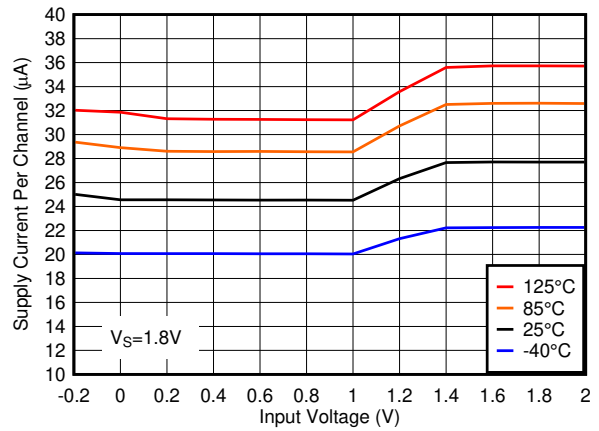


Figure 5-3. Supply Current vs. Input Voltage, 1.8V

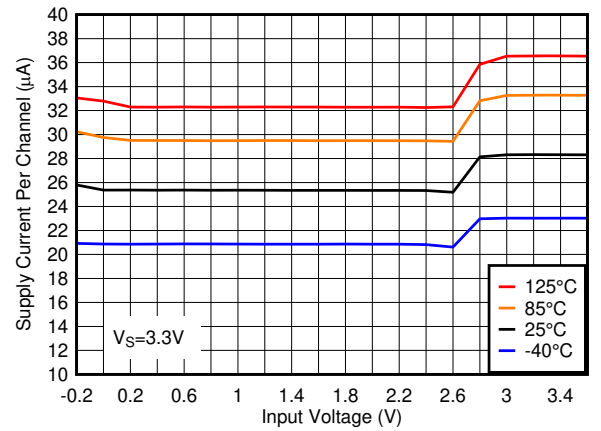


Figure 5-4. Supply Current vs. Input Voltage, 3.3V

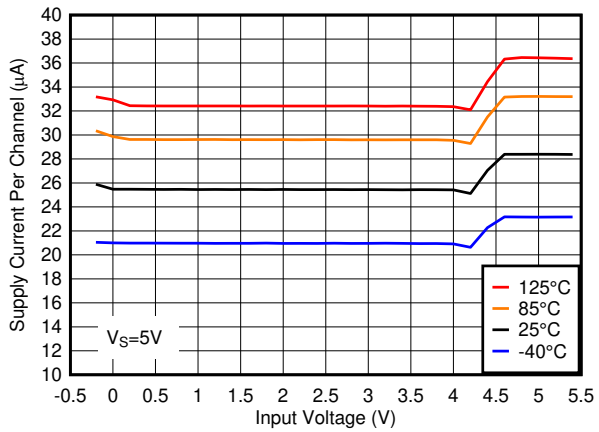


Figure 5-5. Supply Current vs. Input Voltage, 5V

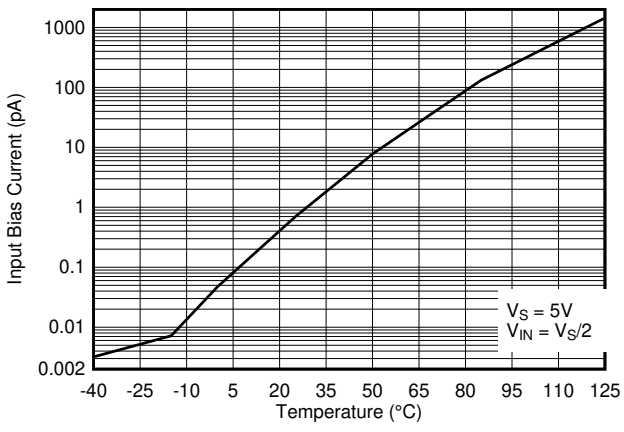


Figure 5-6. Input Bias Current vs. Temperature

5.13 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

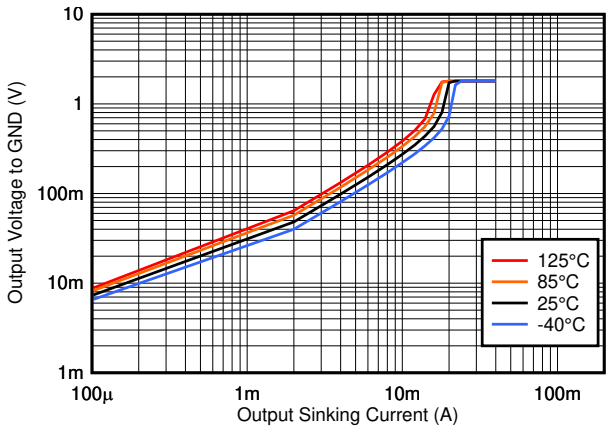


Figure 5-7. Output Sinking Current vs. Output Voltage, 1.8V

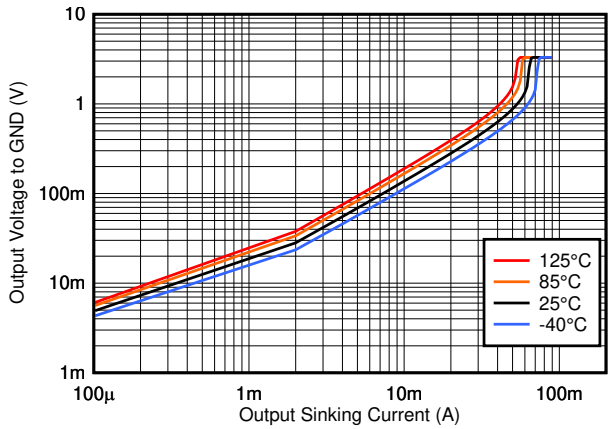


Figure 5-8. Output Sinking Current vs. Output Voltage, 3.3V

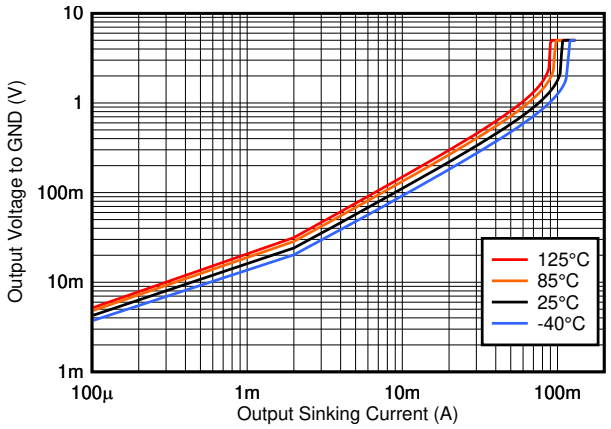


Figure 5-9. Output Sinking Current vs. Output Voltage, 5V

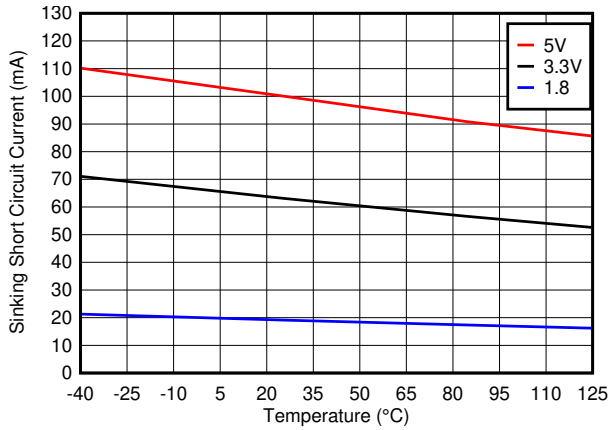


Figure 5-10. Sinking Short Circuit Current vs. Temperature

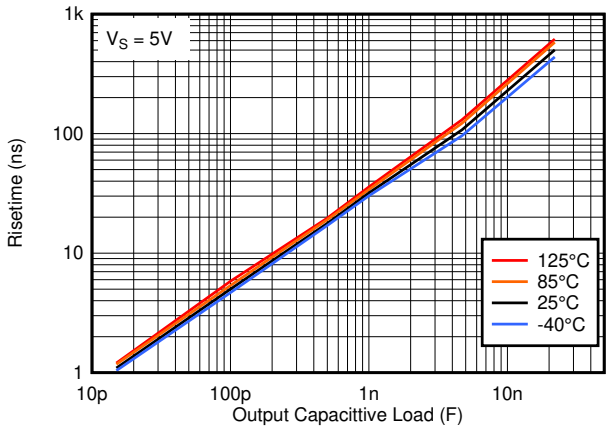


Figure 5-11. Risetime vs. Capacitive Load

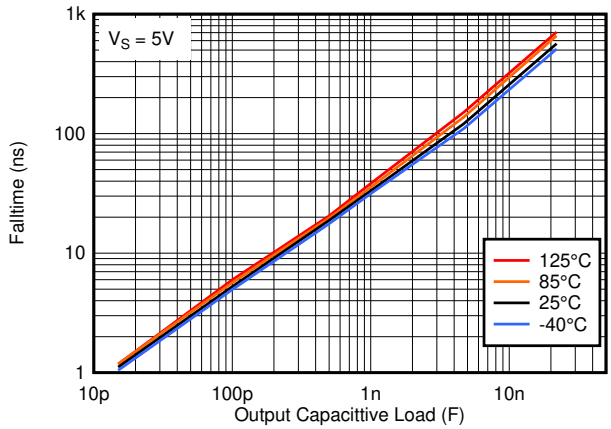


Figure 5-12. Falltime vs. Capacitive Load

5.13 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

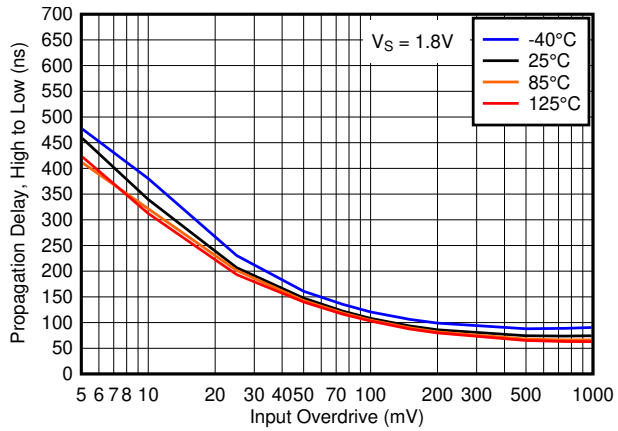


Figure 5-13. Propagation Delay, High to Low, 1.8V

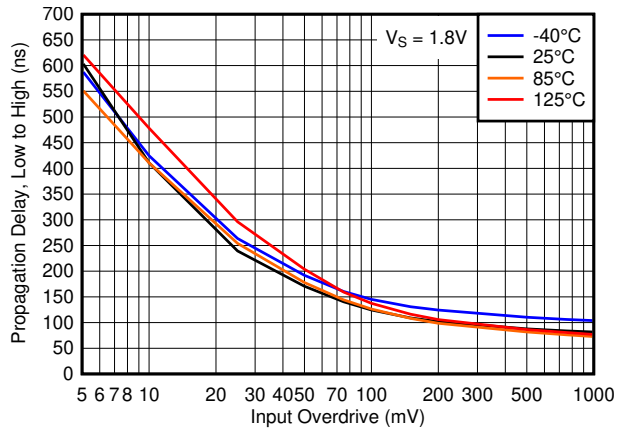


Figure 5-14. Propagation Delay, Low to High, 1.8V

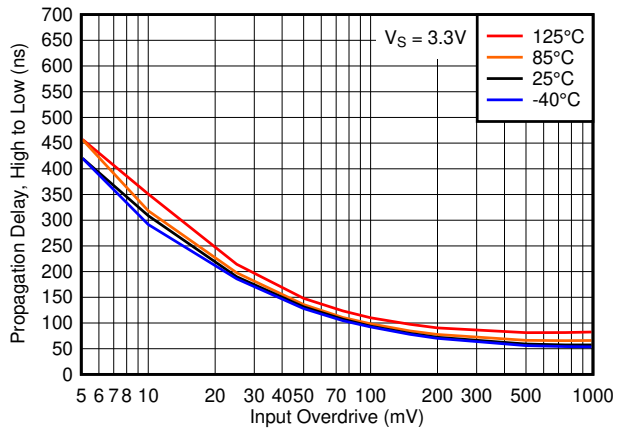


Figure 5-15. Propagation Delay, High to Low, 3.3V

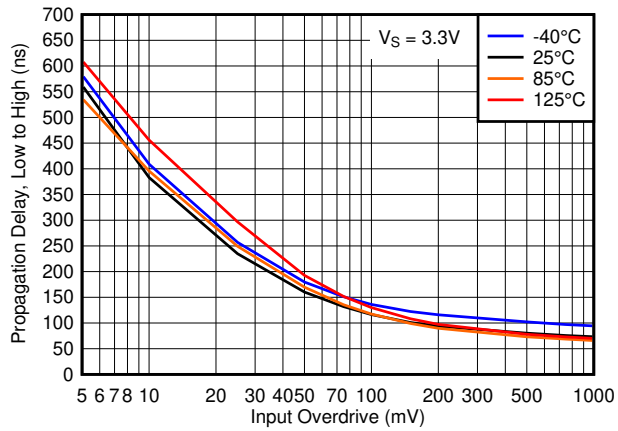


Figure 5-16. Propagation Delay, Low to High, 3.3V

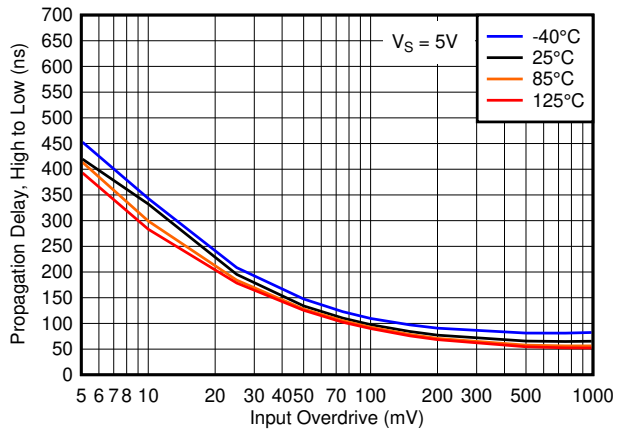


Figure 5-17. Propagation Delay, High to Low, 5V

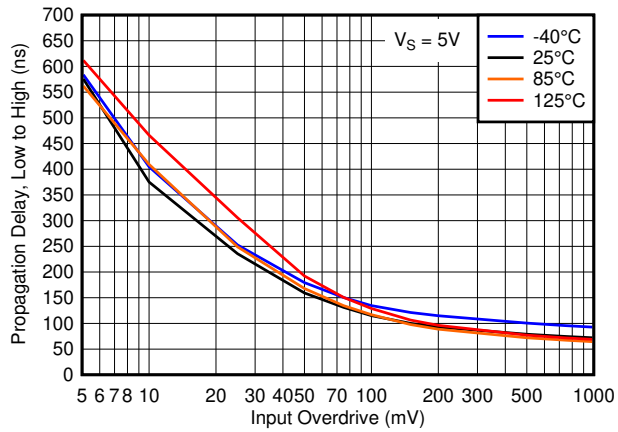


Figure 5-18. Propagation Delay, Low to High, 5V

5.13 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

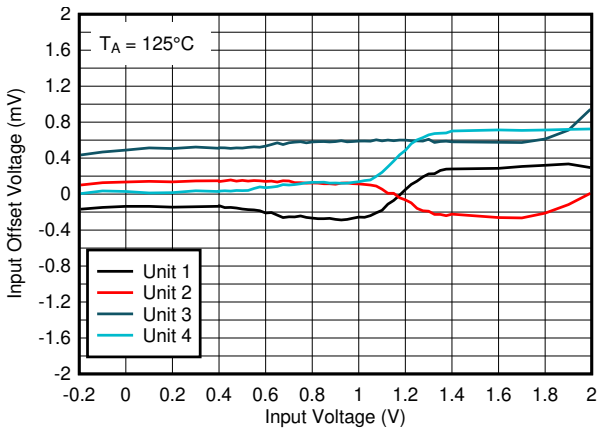


Figure 5-19. Offset Voltage vs. Input Votlage at 125°C, 1.8V

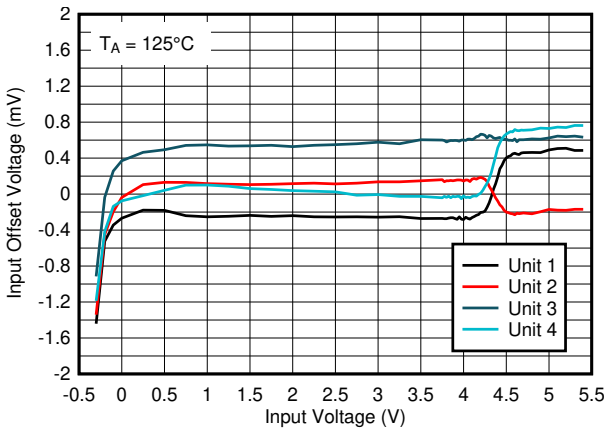


Figure 5-20. Offset Voltage vs. Input Votlage at 125°C, 5V

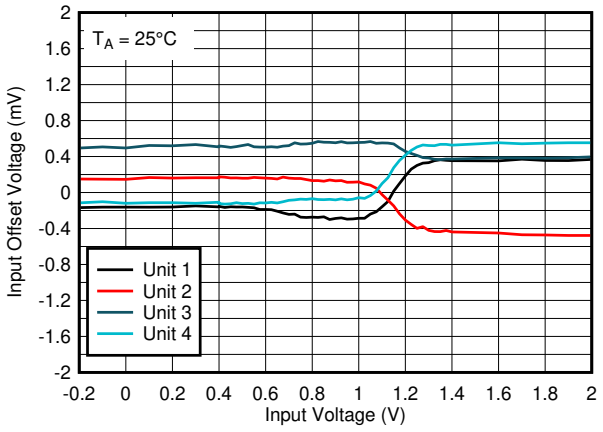


Figure 5-21. Offset Voltage vs. Input Votlage at 25°C, 1.8V

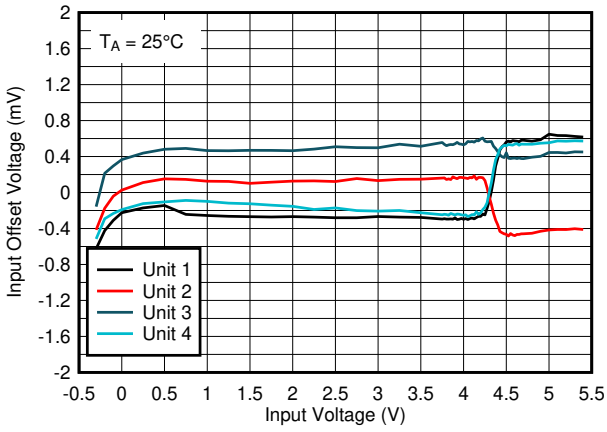


Figure 5-22. Offset Voltage vs. Input Votlage at 25°C, 5V

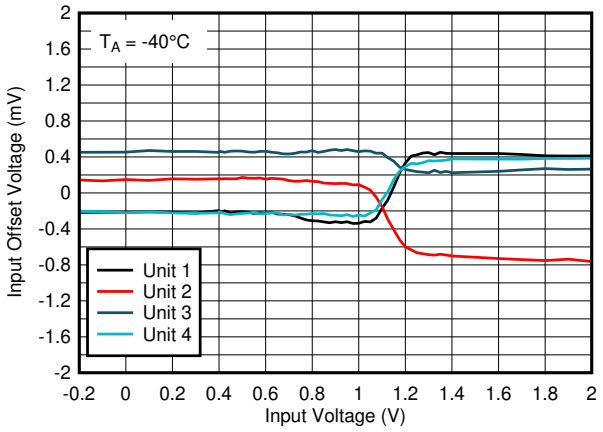


Figure 5-23. Offset Voltage vs. Input Votlage at -40°C, 1.8V

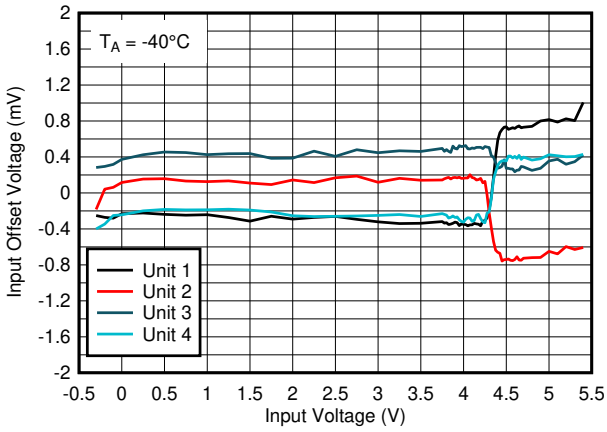


Figure 5-24. Offset Voltage vs. Input Votlage at -40°C, 5V

5.13 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = GND, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

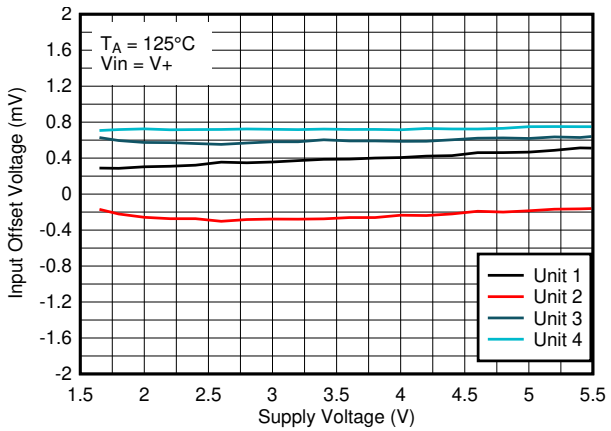


Figure 5-25. Offset Voltage vs. Supply Voltage at 125°C, VIN=V+

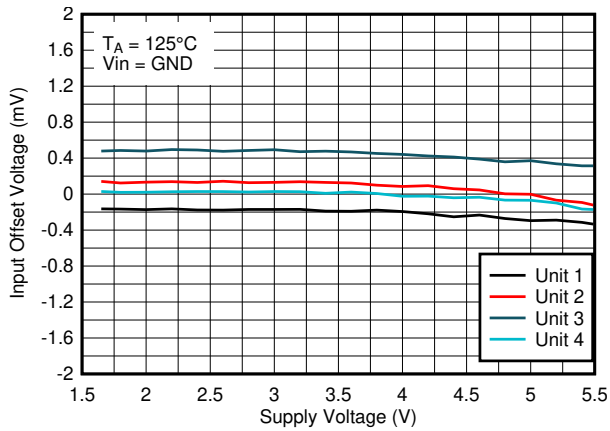


Figure 5-26. Offset Voltage vs. Supply Voltage at 125°C, VIN=0V

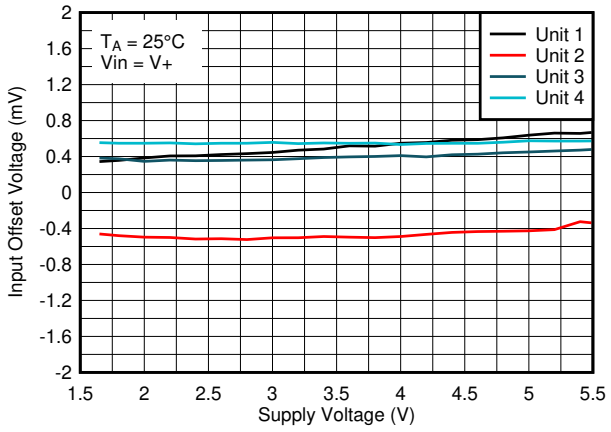


Figure 5-27. Offset Voltage vs. Supply Voltage at 25°C, VIN=V+

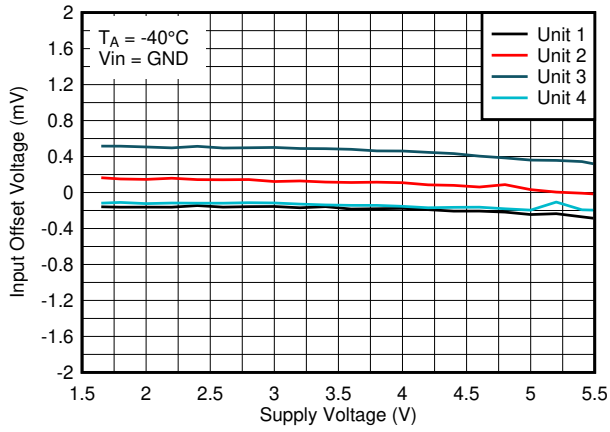


Figure 5-28. Offset Voltage vs. Supply Voltage at 25°C, VIN=0V

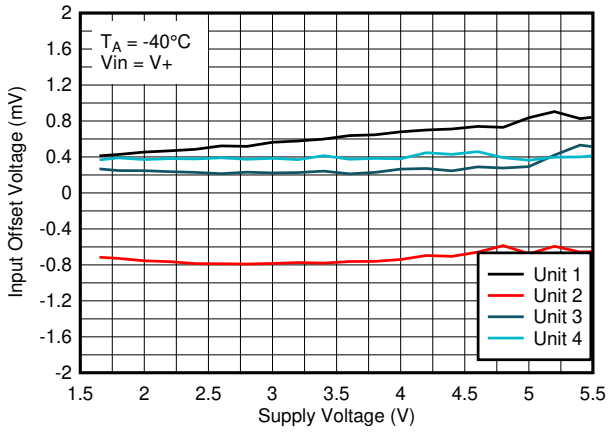


Figure 5-29. Offset Voltage vs. Supply Voltage at -40°C, VIN=V+

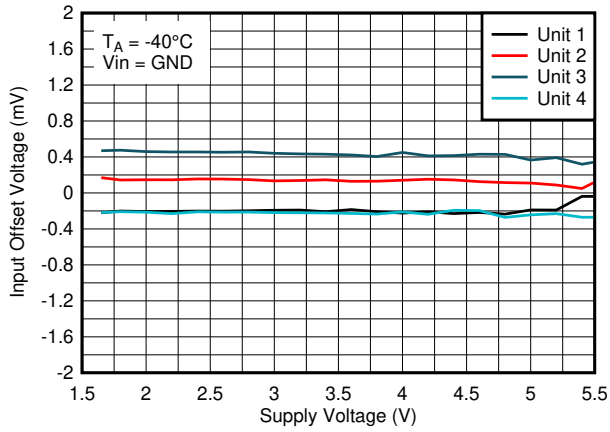


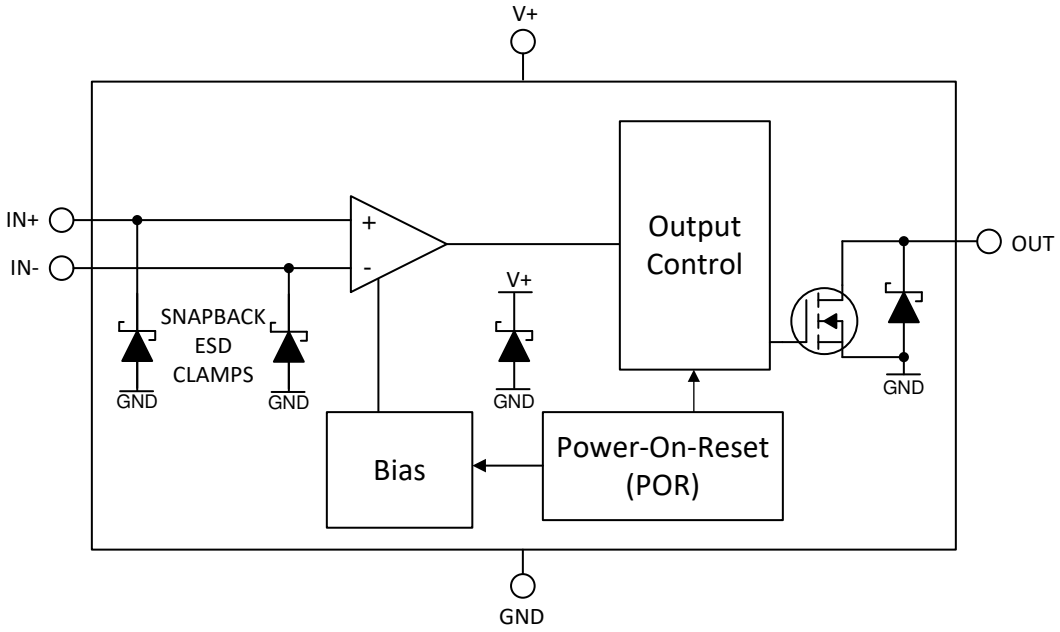
Figure 5-30. Offset Voltage vs. Supply Voltage at -40°C, VIN=0V

6 Detailed Description

6.1 Overview

The LV Family devices are micro-power comparators with open-drain outputs and improved input offset voltage that operate down to 1.65 V while only consuming only 25 µA per channel. The LV family are designed for portable, automotive and industrial applications. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

6.2 Functional Block Diagram



6.3 Feature Description

The LV family devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The LV family feature a rail-to-rail input stage capable of operating up to 100 mV beyond the power supply rails. The comparators also feature an open-drain output stage options with Power On Reset for known start-up conditions.

6.4 Device Functional Modes

6.4.1 Open Drain Output

The LV family features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 5.5 V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime will be dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) will create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs should be left floating, or can be tied to the GND pin if floating pins are not allowed. While an individual output can typically sink up to 100 mA, the total combined current for all channels must be less than 200 mA.

6.4.2 Power-On-Reset (POR)

The LV family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 30µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit will keep the output high impedance (HI-Z) during the POR period (t_{on}).

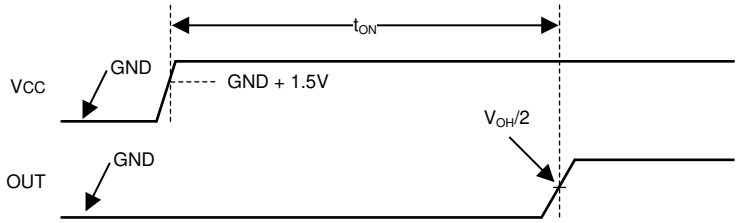


Figure 6-1. Power-On-Reset Timing Diagram

Note that it is the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

A light pull-up (to V+) or pull-down (to GND) resistor can be used to pre-bias the output condition to prevent the output from floating.

6.4.3 Inputs

6.4.3.1 Rail to Rail Input

The LV family input voltage range extends from 100mV below GND to 100 mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V+ or GND.

6.4.3.2 Fault Tolerant Inputs

The LV family inputs are fault tolerant up to 5.5V independent of V+. Fault tolerant is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0 V and 5.5 V, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain datasheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay, which can lead to unpredictable behavior.

6.4.3.3 Input Protection

The input bias current is typically 5 pA for input voltages between V+ and GND. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to GND. As the input voltage goes under GND, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.4 ESD Protection

The LV family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to GND, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapbacks momentarily "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener. There is no ESD clamp from the inputs to V+.

The open-drain output protection also consists of a ESD clamp between the output and GND to allow the output to be pulled above V+ to a maximum of 5.5V. There is no ESD clamp from the output to V+.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

TI does not specify the performance of the ESD clamps and external clamping diodes should be added if the inputs or output could exceed the maximum ratings as part of normal operation.

6.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

6.4.6 Hysteresis

The LV family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" (oscillate) when the absolute differential voltage near zero, as the comparator triggers on it's own internal wideband noise. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 7.1.2 in the following section.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

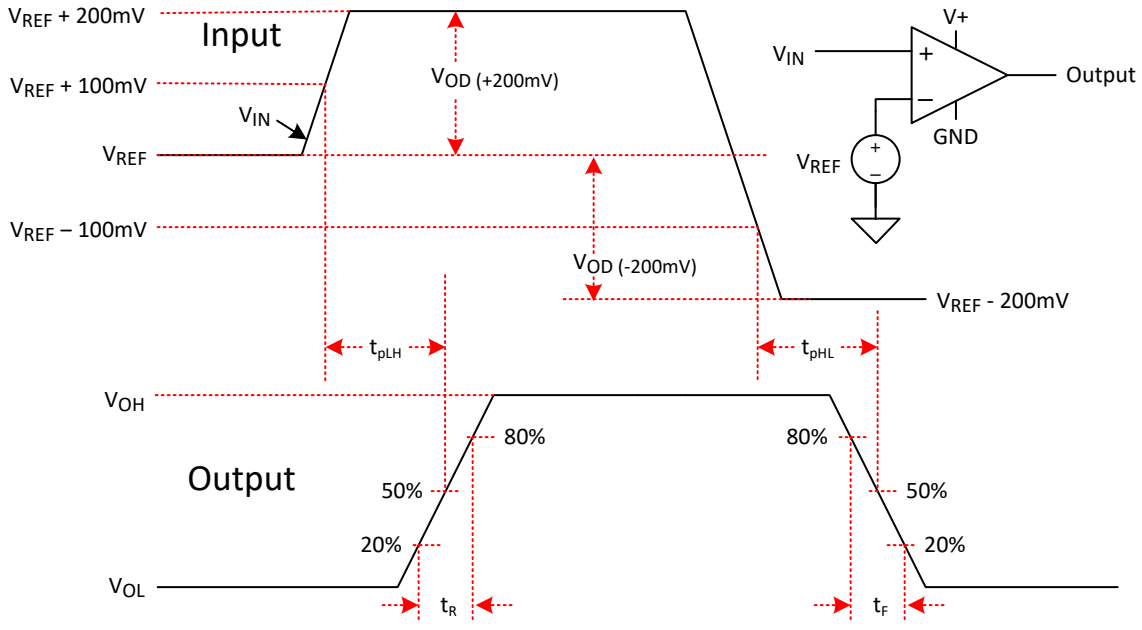


Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

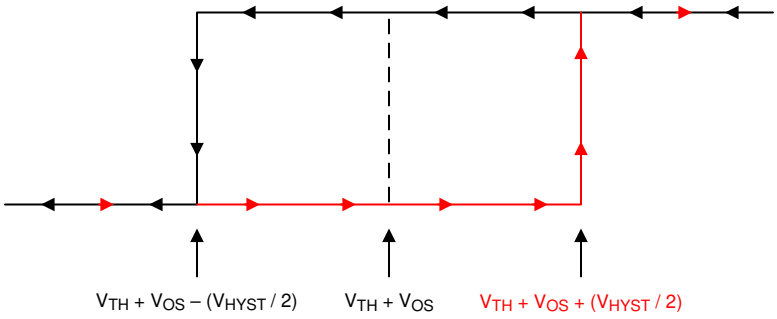


Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 7-3.

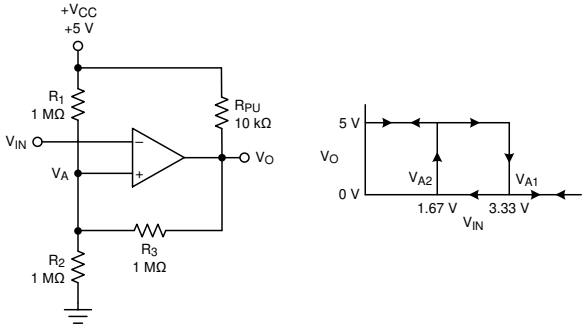


Figure 7-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-3. Note that R_{PU} should be considered in series with R3 when the output is high. R_{PU} should be at least 10x less than R3.

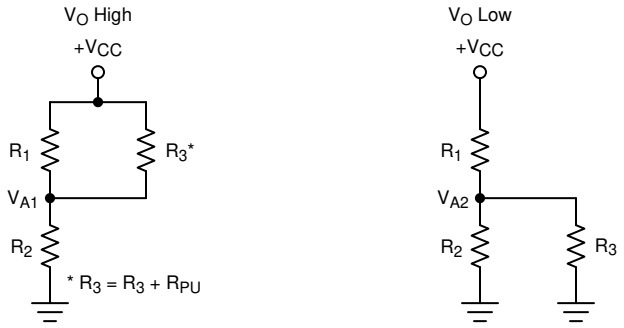


Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 7-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 7-5,

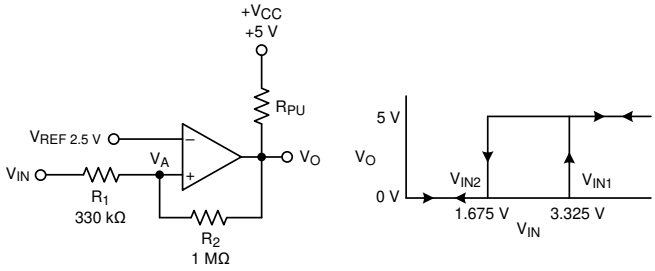


Figure 7-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-6 Note that R_{PU} should be considered in series with R2 when the output is high. R_{PU} should be at least 10x less than R2.

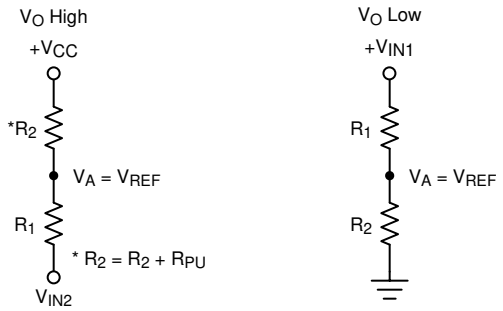


Figure 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-7 shows a simple window comparator circuit. Window comparators require open drain outputs if the outputs are directly connected together.

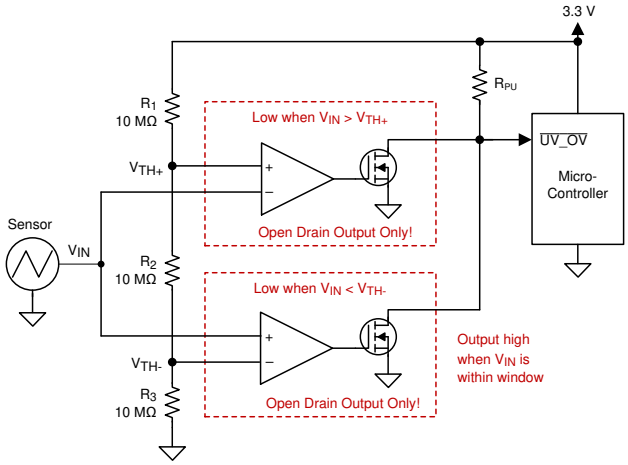


Figure 7-7. Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-7. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in Figure 7-8.

7.2.1.3 Application Curve

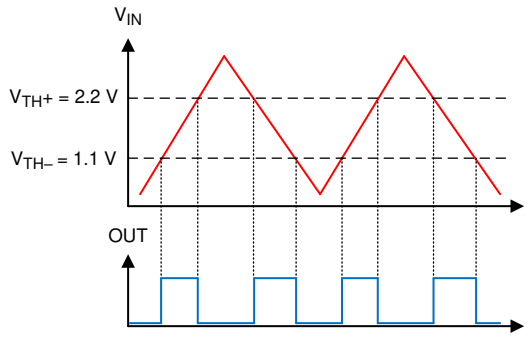


Figure 7-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

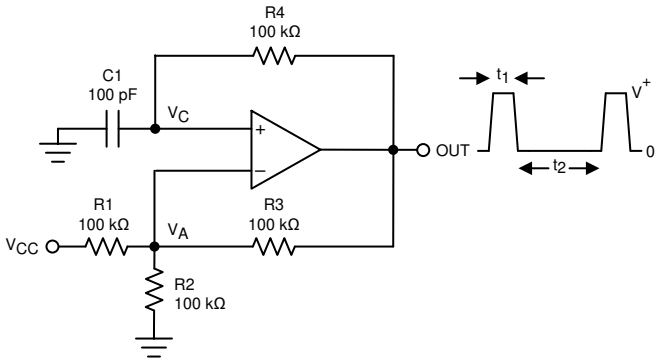


Figure 7-9. Square-Wave Oscillator

7.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. R4 should be over several kilo-ohms to minimize loading the output.

7.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

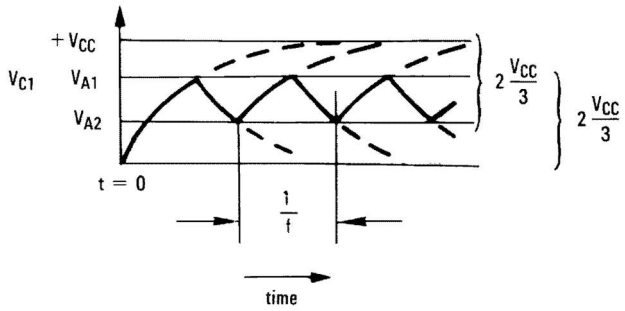


Figure 7-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 7-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 for each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln 2.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times In2) \tag{9}$$

7.2.2.3 Application Curve

Figure 7-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100\ pF$, $C_L = 20\ pF$

- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10 pF

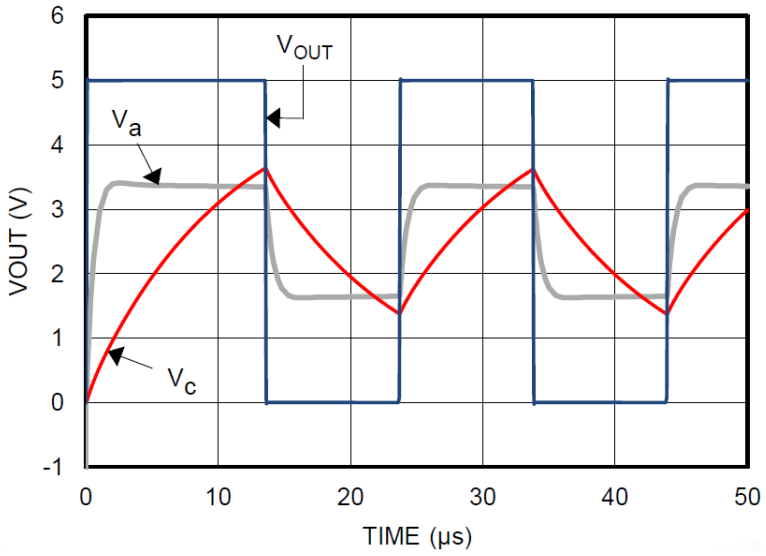


Figure 7-11. Square-Wave Oscillator Output Waveform

7.2.3 Adjustable Pulse Width Generator

Figure 7-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

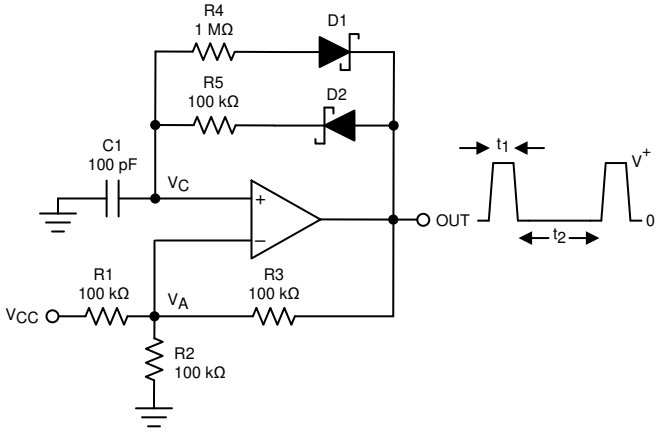


Figure 7-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Shottky) must be taken into account by altering output high and low voltages in the calculations. R_{PU} should be at least 10x less than the smallest value of R4 or R5.

7.2.4 Time Delay Generator

The circuit shown in Figure 7-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

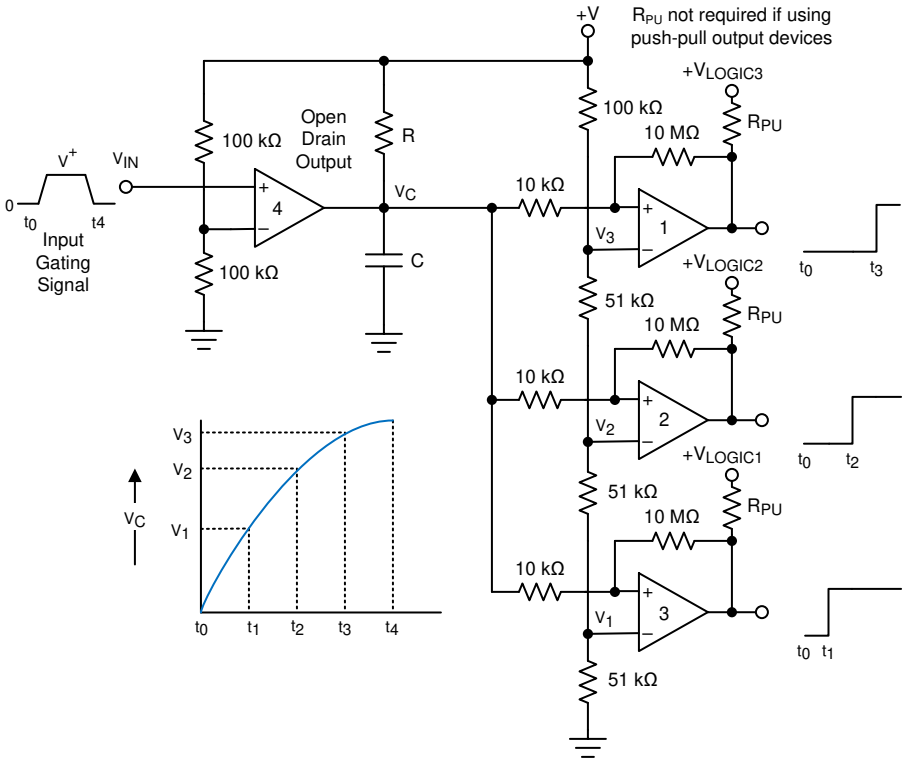


Figure 7-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10 kΩ and 10 MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100 kΩ and C = 0.01 µF to 1 µF.

All outputs will immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

7.2.5 Logic Level Shifter

The output is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

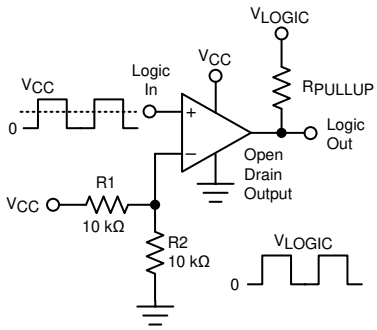


Figure 7-14. Universal Logic Level Shifter

The two 10 kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage should match the driven logic input "high" level.

7.2.6 One-Shot Multivibrator

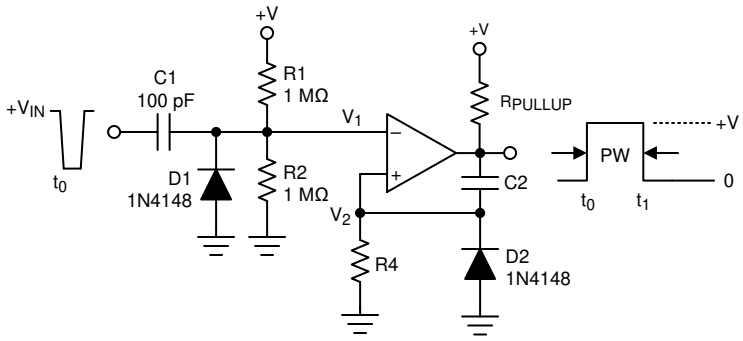


Figure 7-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

7.2.7 Bi-Stable Multivibrator

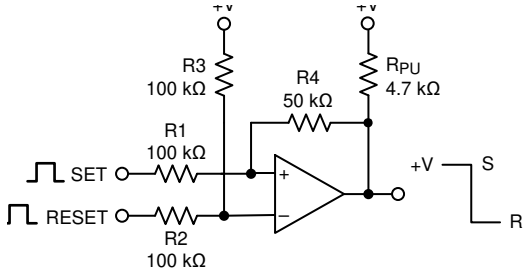


Figure 7-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

7.2.8 Zero Crossing Detector

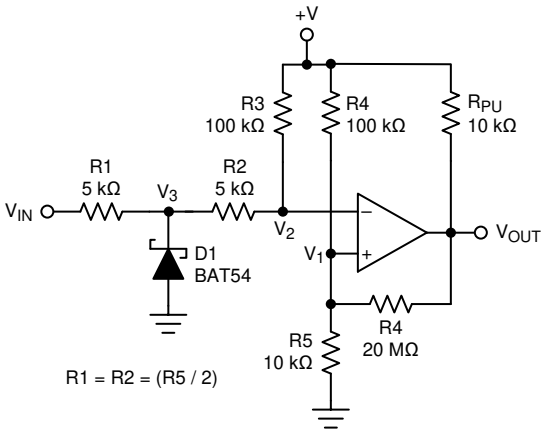


Figure 7-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

7.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The noninverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing V_{REF} average voltage.

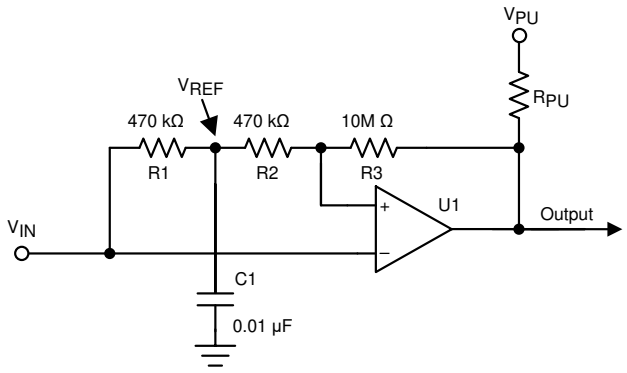


Figure 7-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

Figure 7-19 shows the results of a 9600 baud data signal riding on a varying baseline.

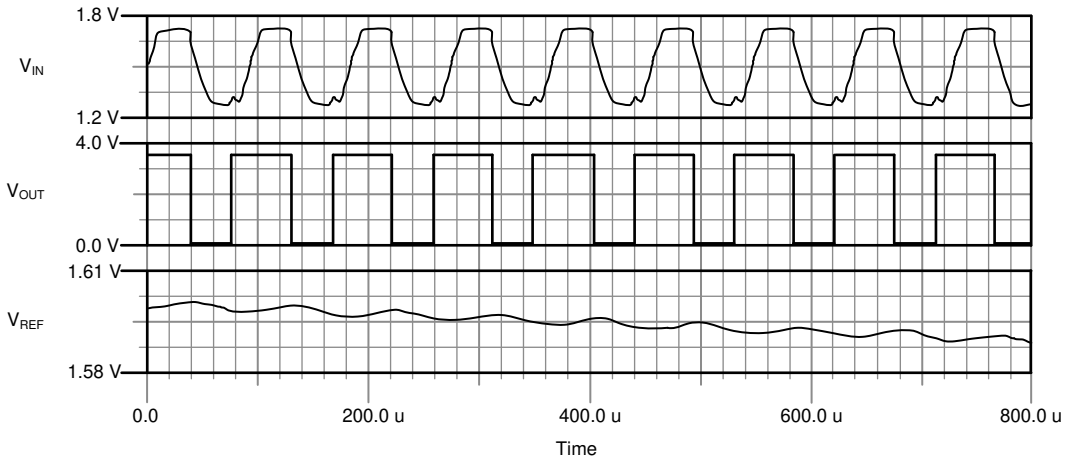


Figure 7-19. Pulse Slicer Waveforms

7.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed

supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may also be powered from "split" supplies (V+, V- and GND), with V- applied to the GND pin.

Input signals must stay within the specified input range (between V+ and V-) for both supply types.

Note that the ouptut will now swing "low" (VOL) to V- potential and not system GND on split supplies.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

7.4.2 Layout Example

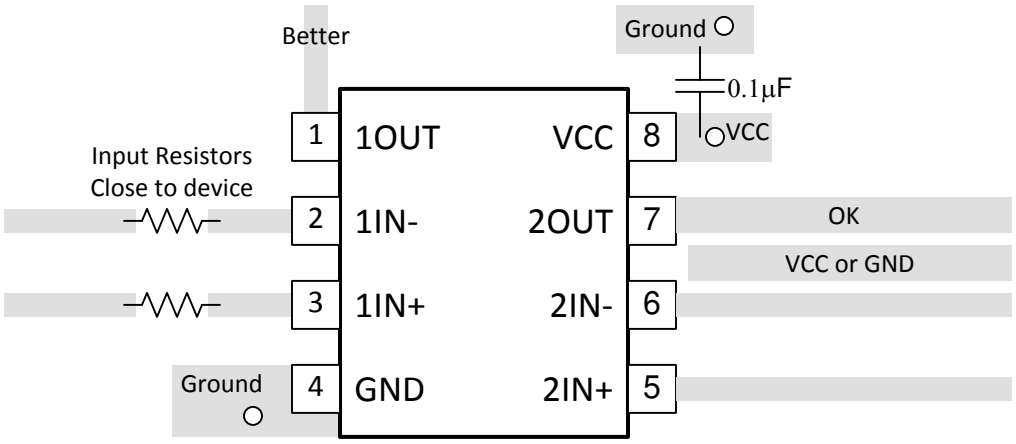


Figure 7-20. Dual Layout Example

8 Device and Documentation Support

8.1 Related Documentation

Analog Engineers Circout Cookbook: Amplifers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Zero crossing detection using comparator circuit - SNOA999

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2023) to Revision E (November 2023)	Page
• Updated front page status	1

Changes from Revision C (January 2022) to Revision D (March 2023)	Page
• Added Single to front page text, device info, pinout, thermal and EC tables	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM339LVQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM339LVQD	Samples
LM339LVQDYYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM339LVQ	Samples
LM339LVQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L339LVQ	Samples
LM393LVQDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H4FQ	Samples
LM393LVQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IHTQ	Samples
LM393LVQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	393LVQ	Samples
LM393LVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM393Q	Samples
LM393LVWDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2T2H	Samples
TL331LVQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T33Q	Samples
TL391LVQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM339LV-Q1, LM393LV-Q1, TL331LV-Q1, TL391LV-Q1 :

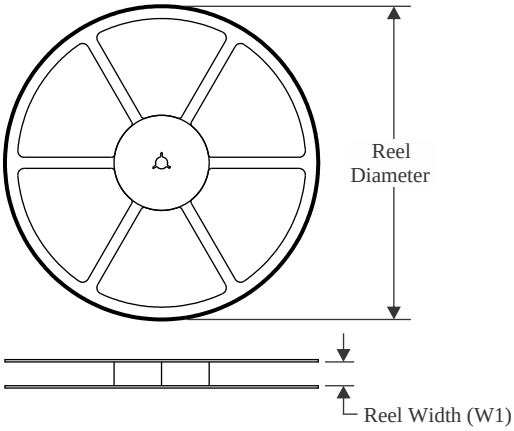
- Catalog : LM339LV, LM393LV, TL331LV, TL391LV

NOTE: Qualified Version Definitions:

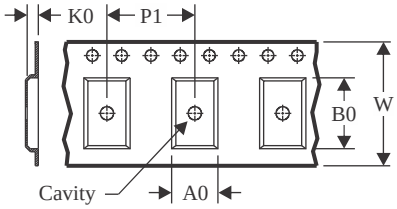
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

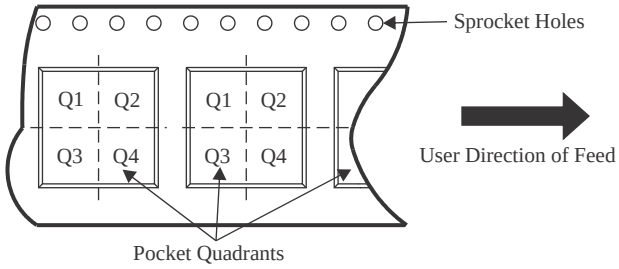


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

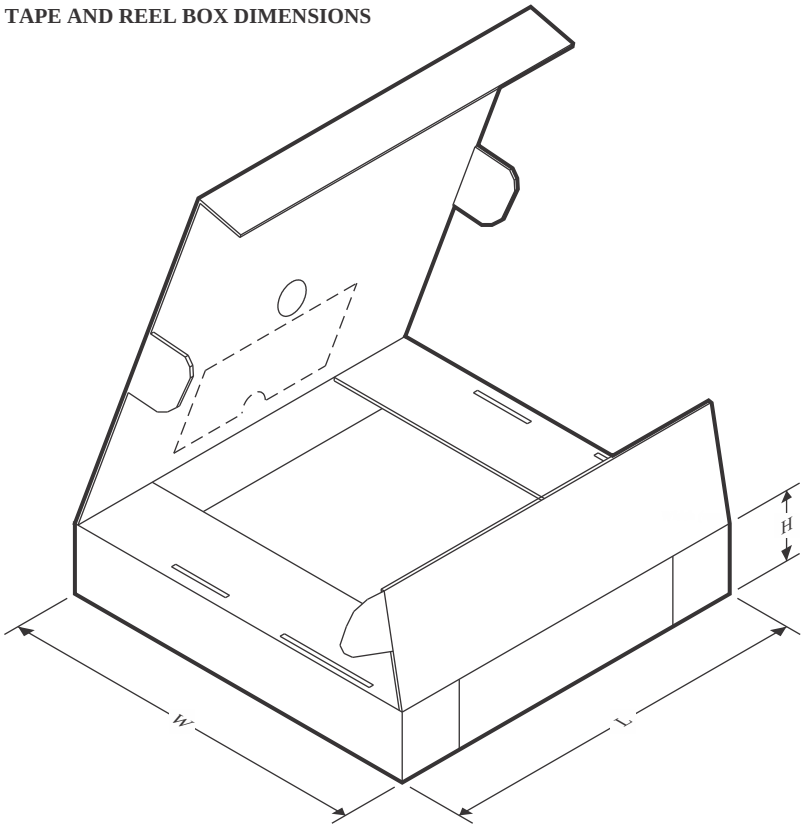
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM339LVQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339LVQDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
LM339LVQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM393LVQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM393LVQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393LVQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393LVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393LVWDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TL331LVQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL391LVQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

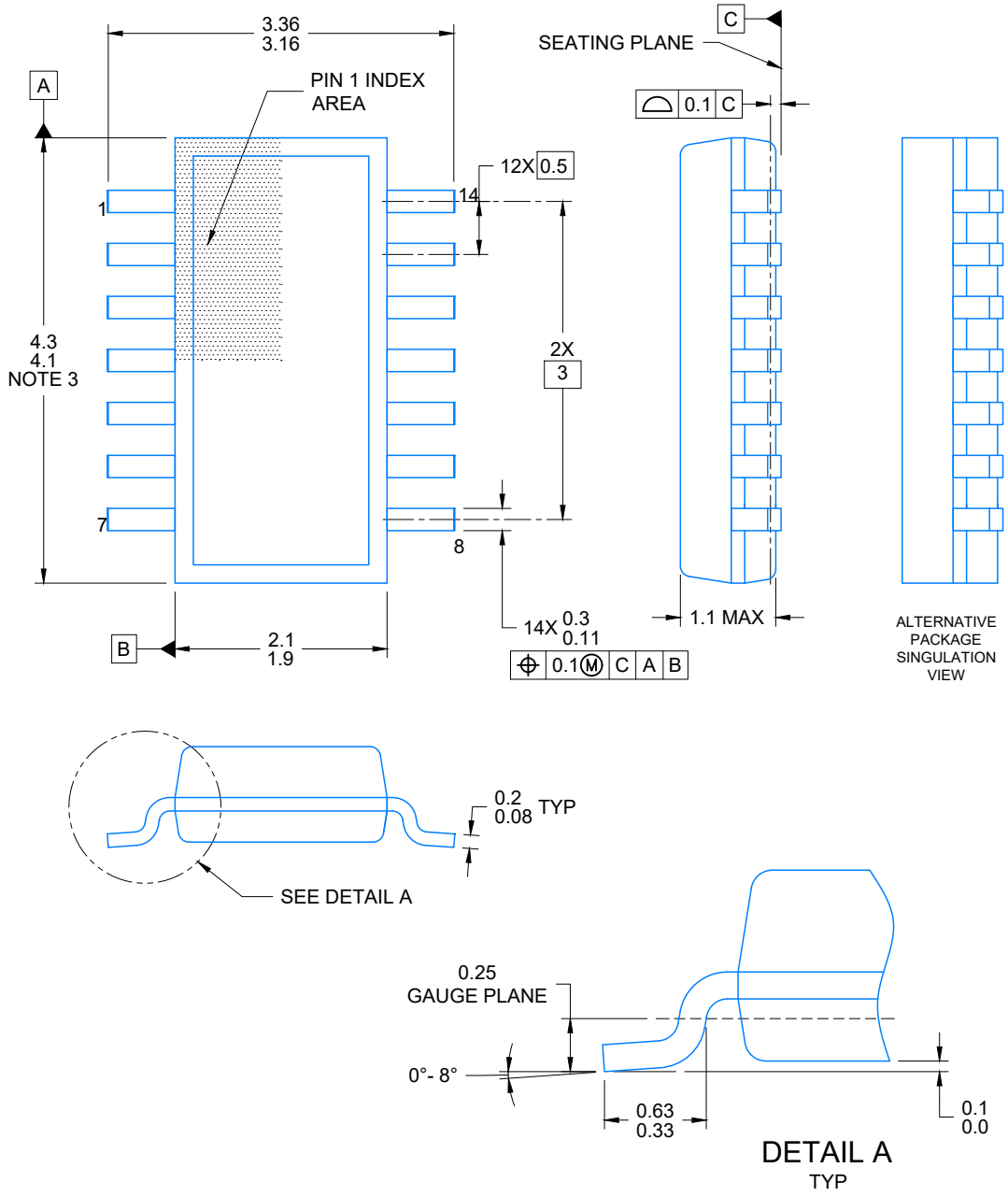
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM339LVQDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
LM339LVQDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
LM339LVQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
LM393LVQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM393LVQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM393LVQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
LM393LVQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393LVWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TL331LVQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL391LVQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DYY0014A

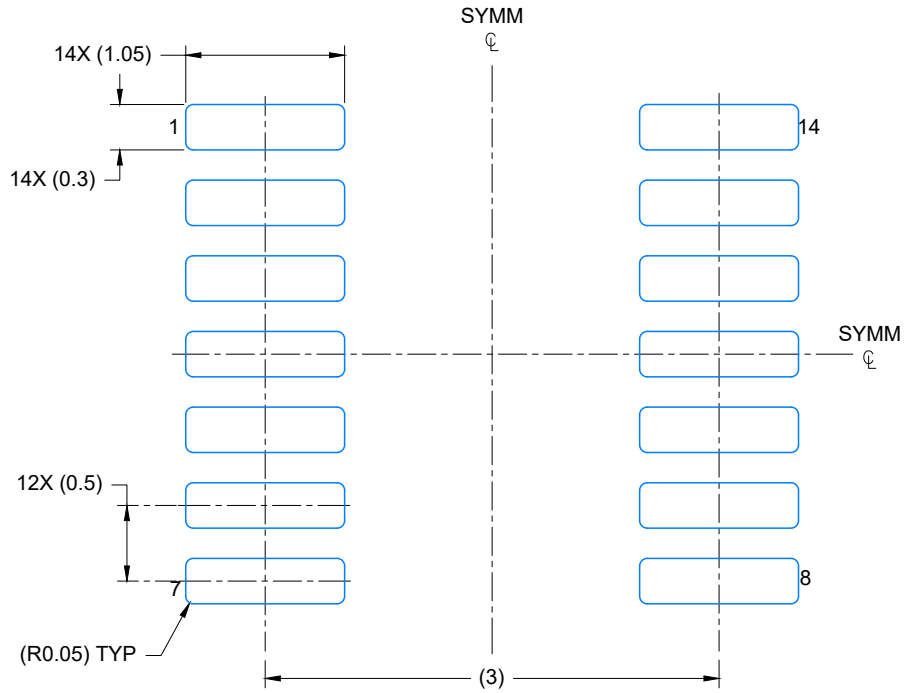
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

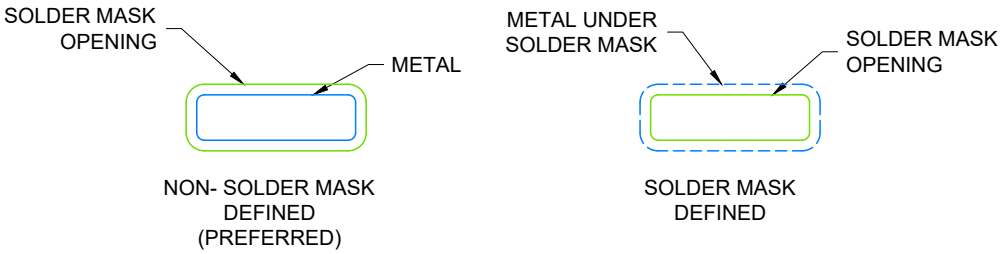


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

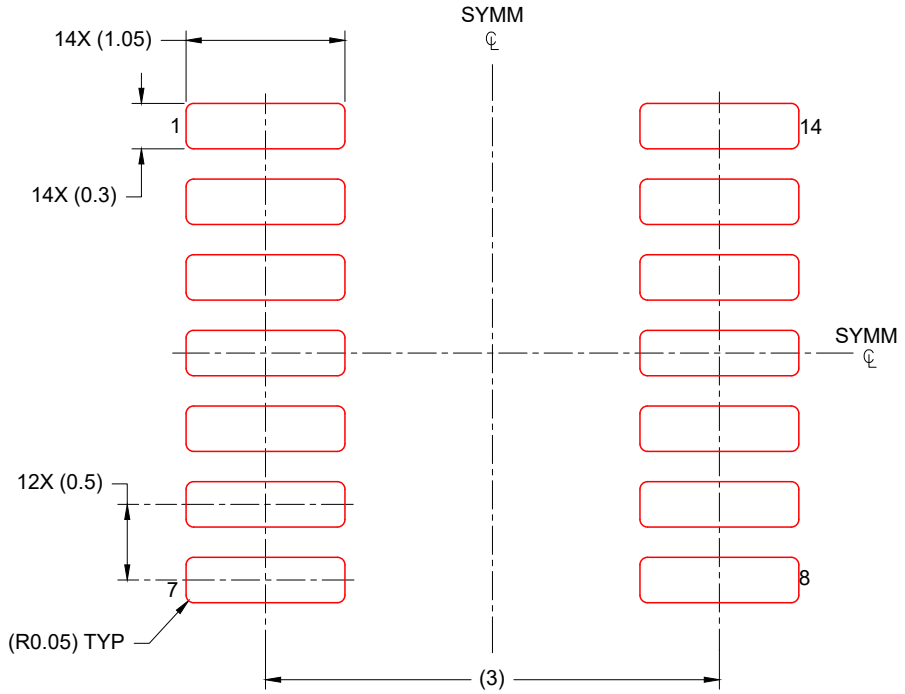


SOLDER MASK DETAILS

4224643/C 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



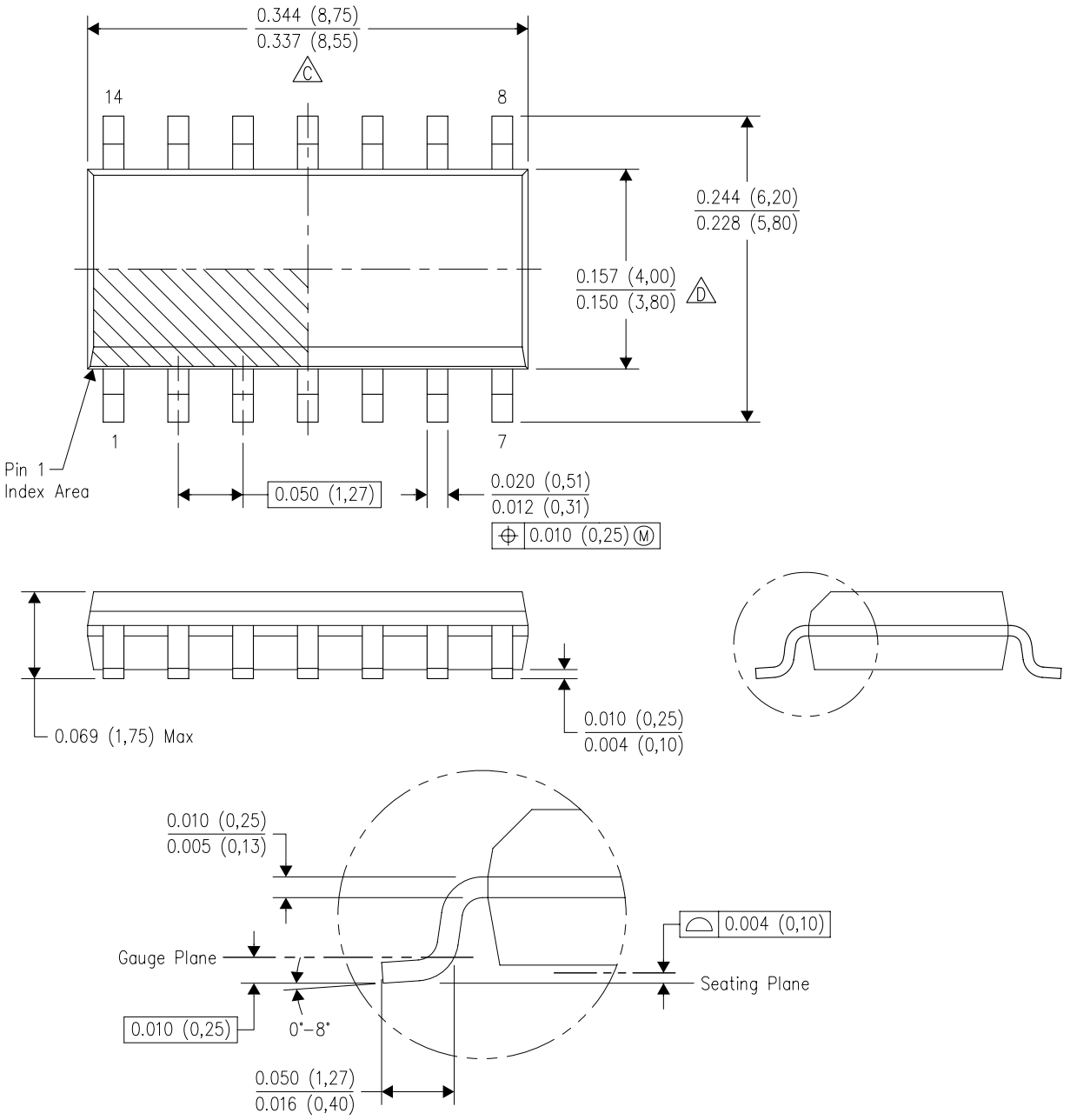
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/C 04/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

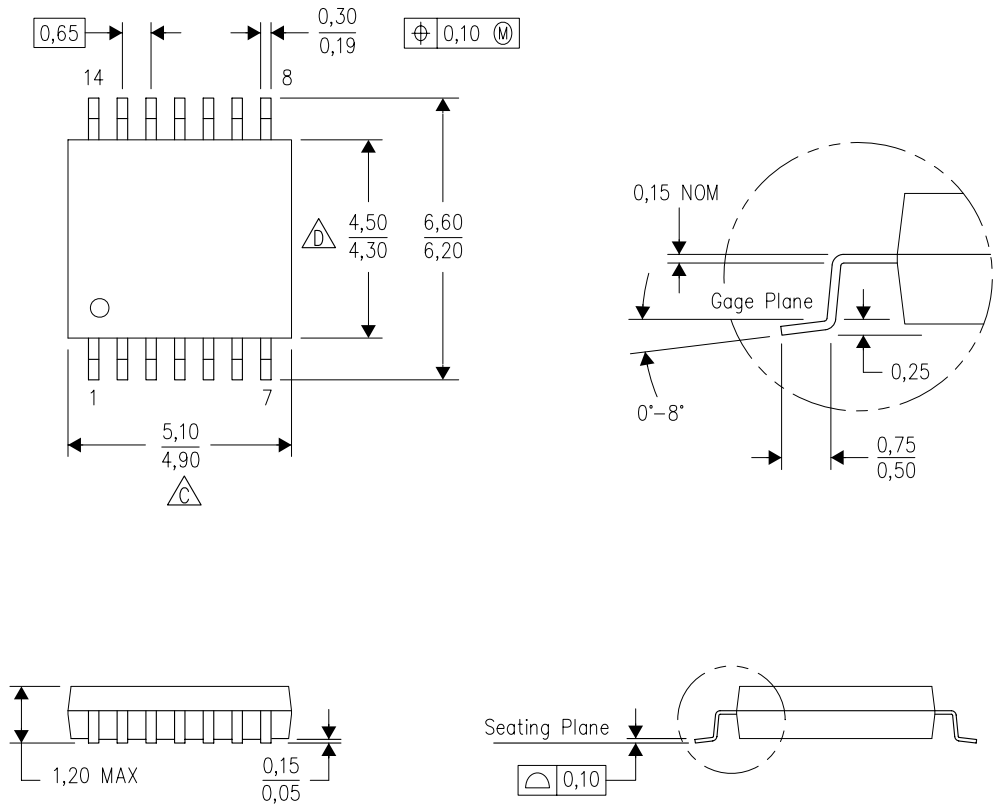
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

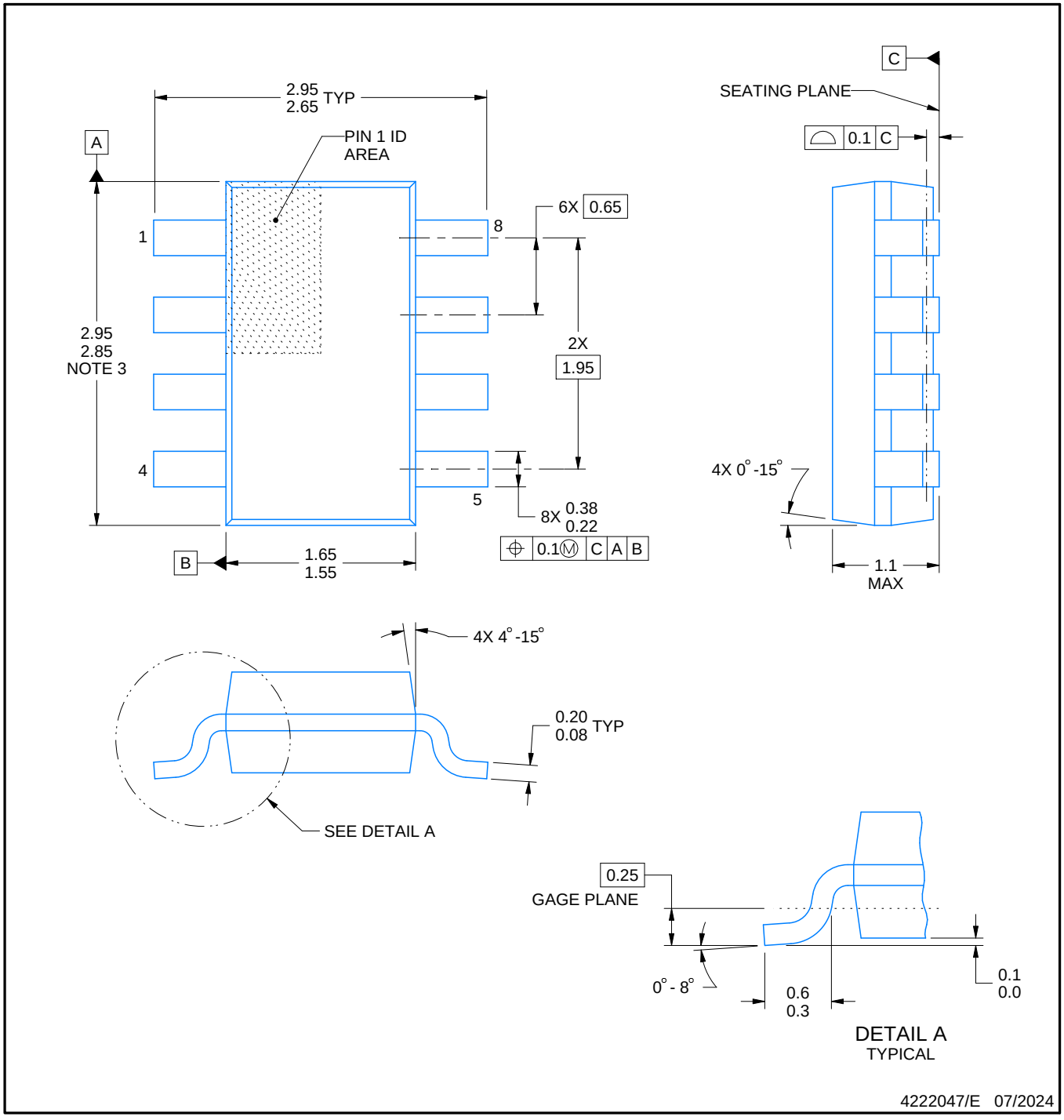
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PACKAGE OUTLINE

DDF0008A

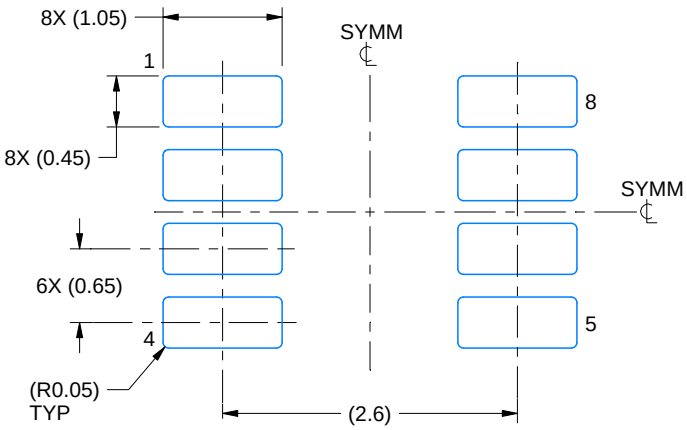
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

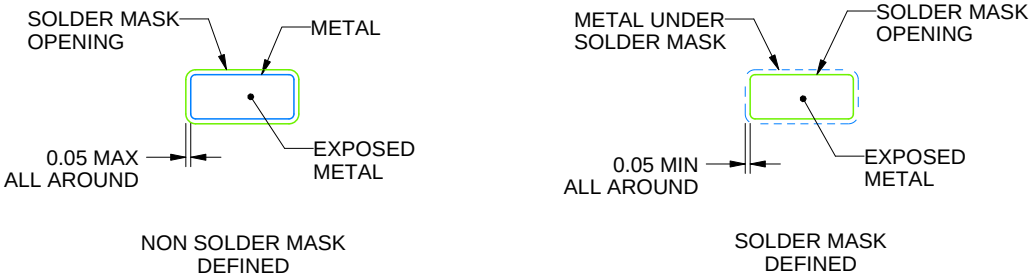


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

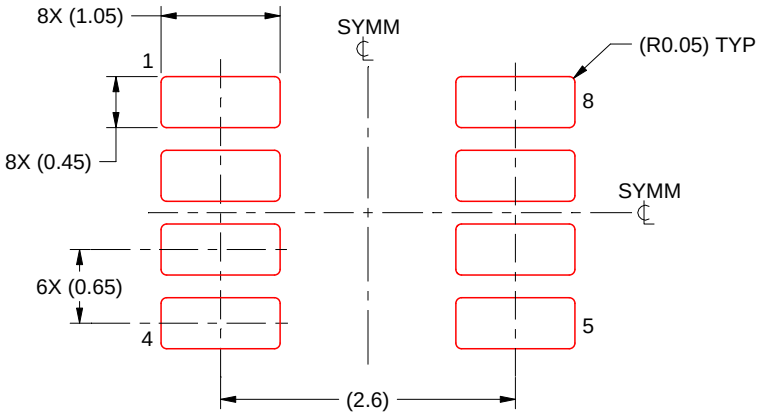
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

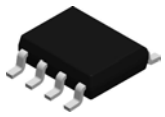


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

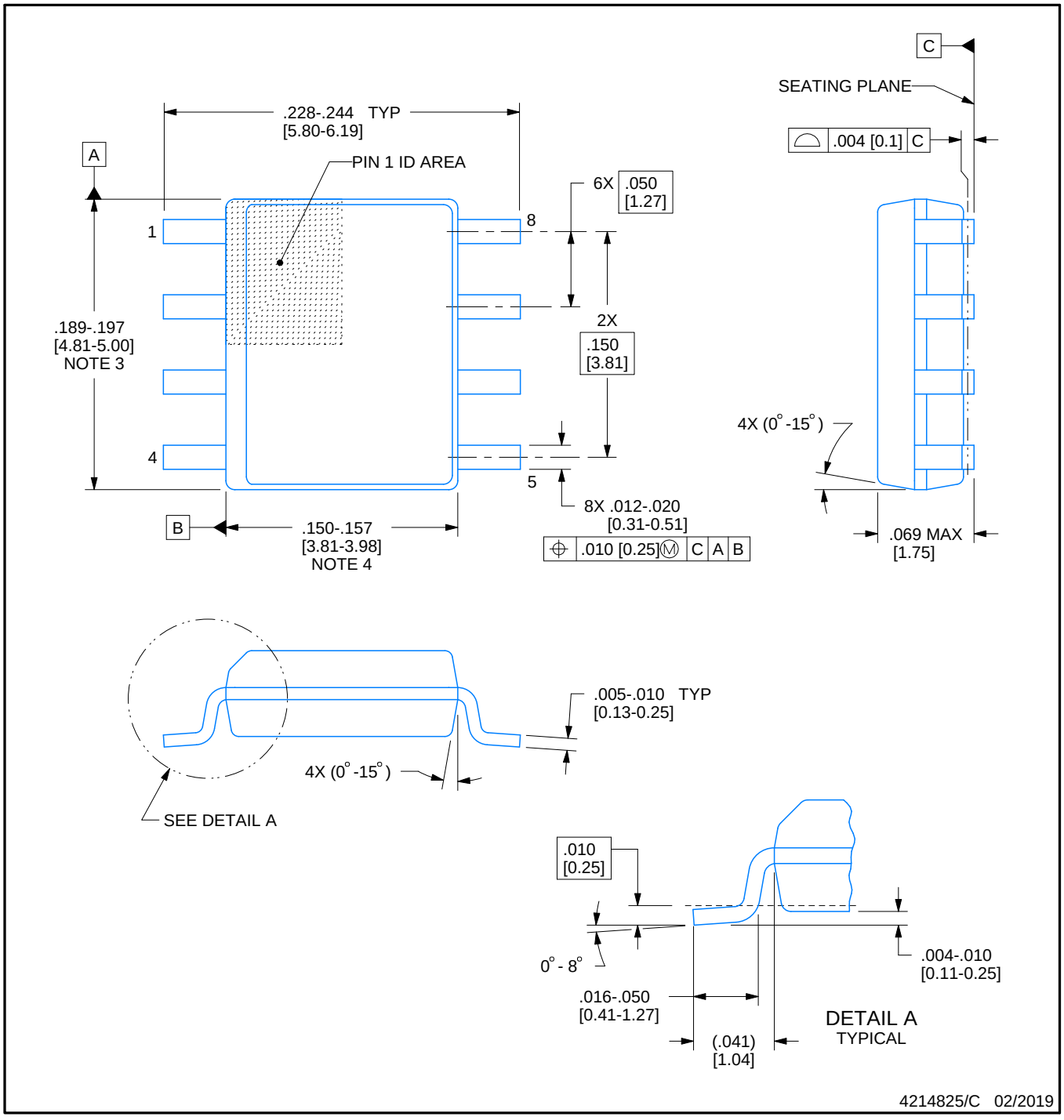


PACKAGE OUTLINE

D0008A

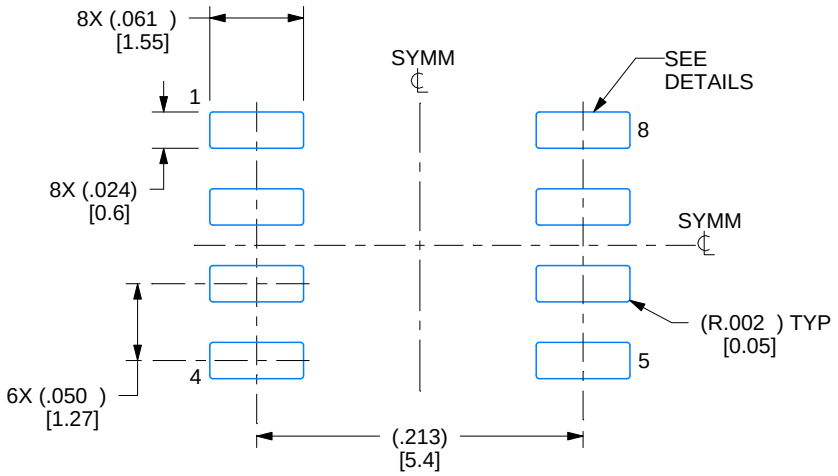
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

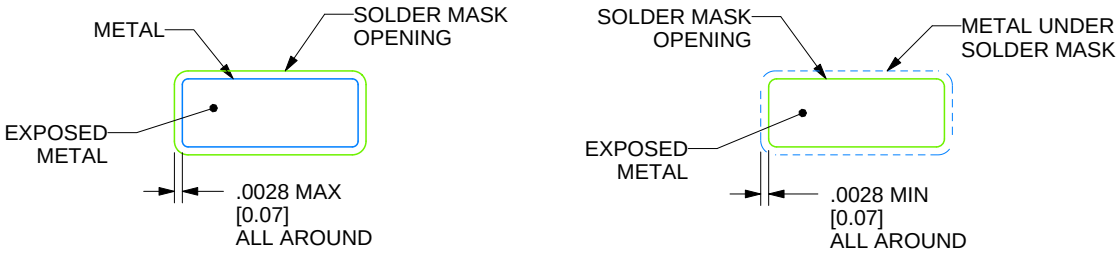


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

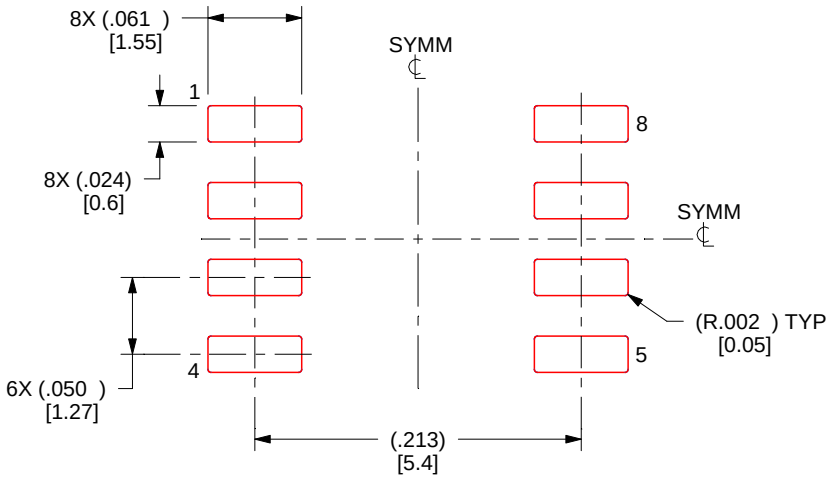
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

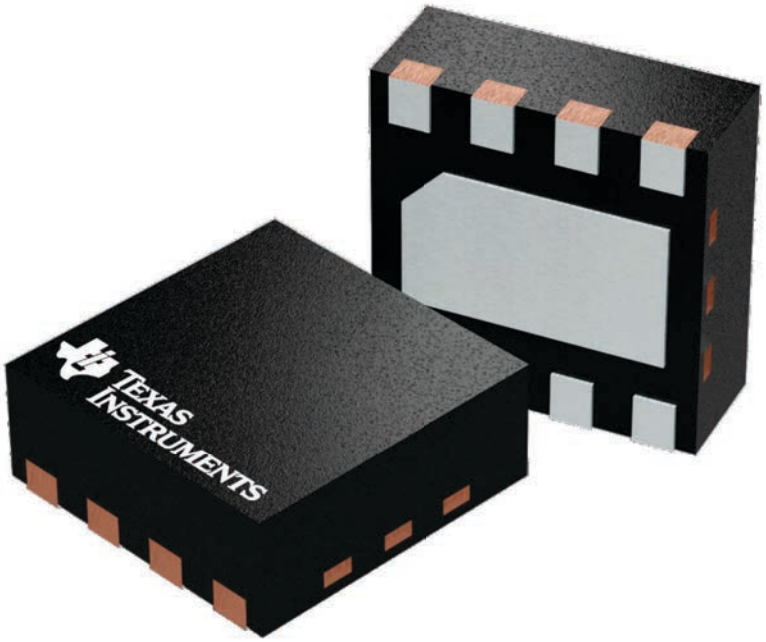
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



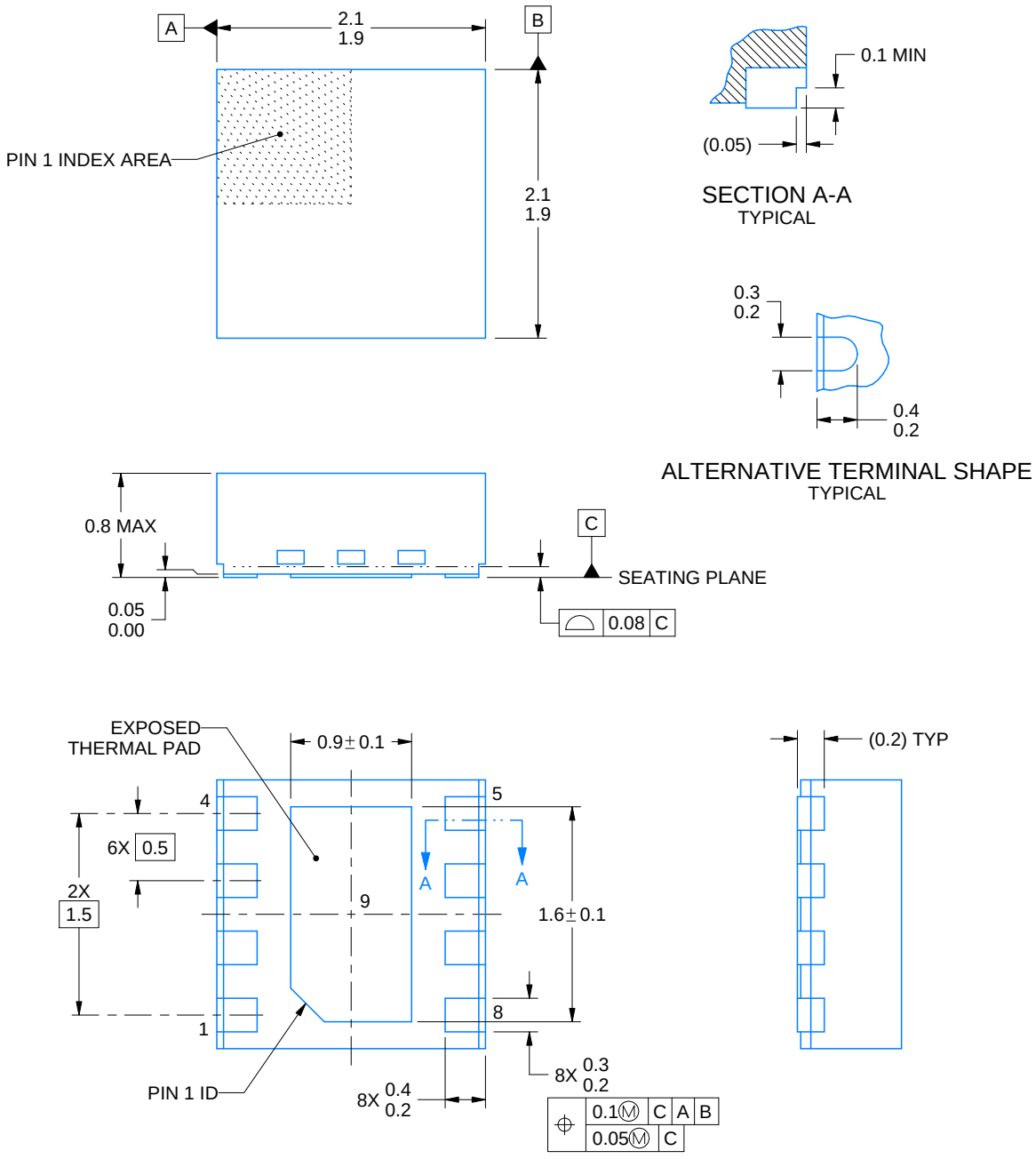
4224783/A

PACKAGE OUTLINE

DSG0008B

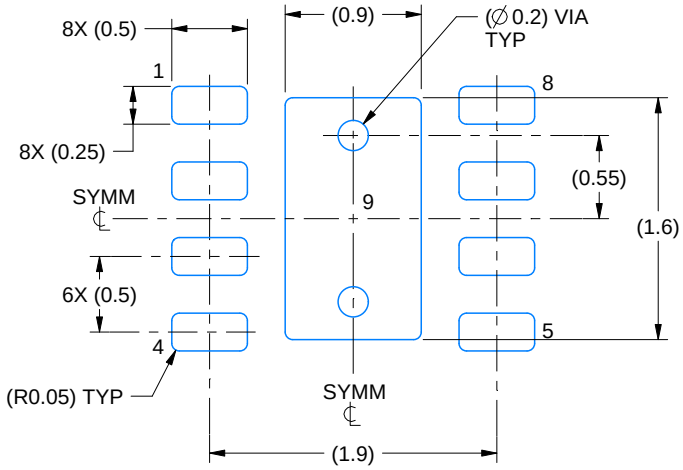
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

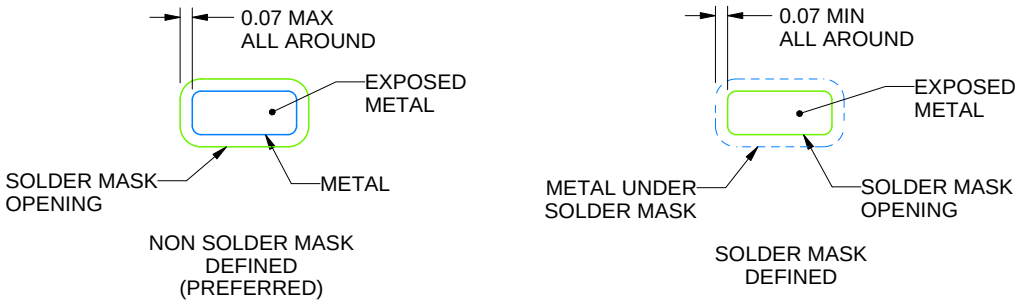


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

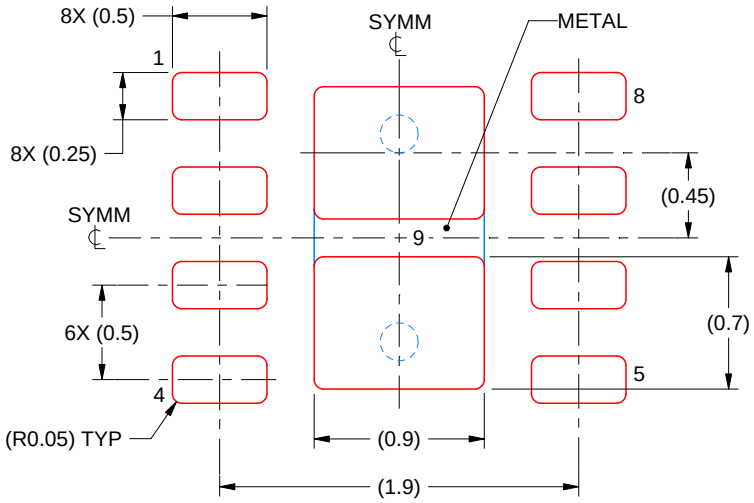
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

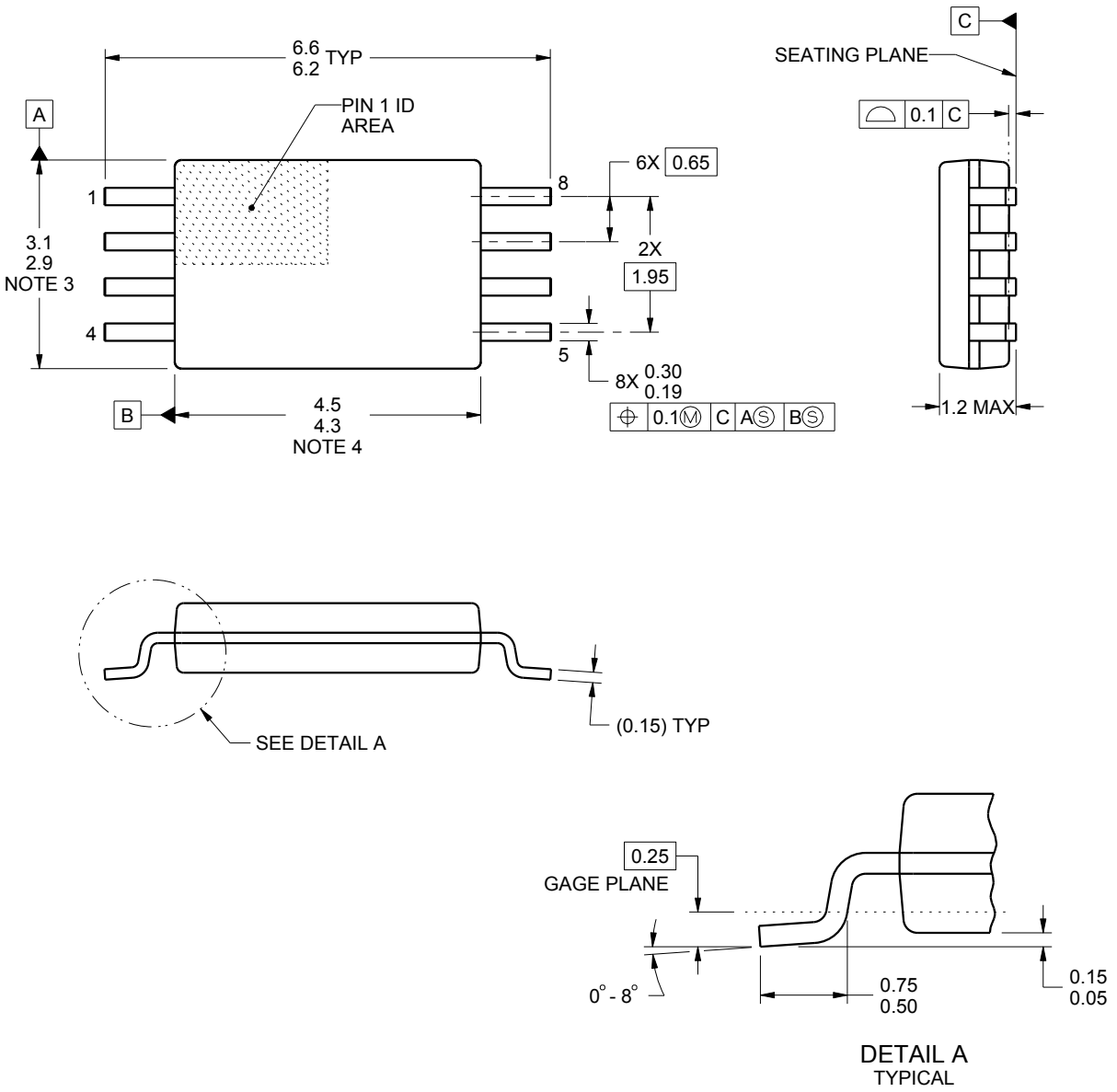
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

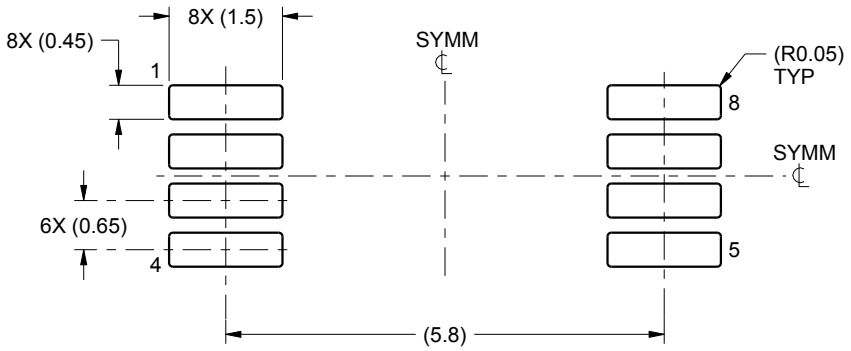
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

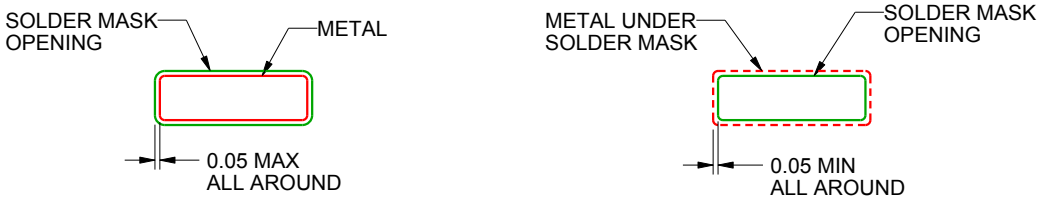


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

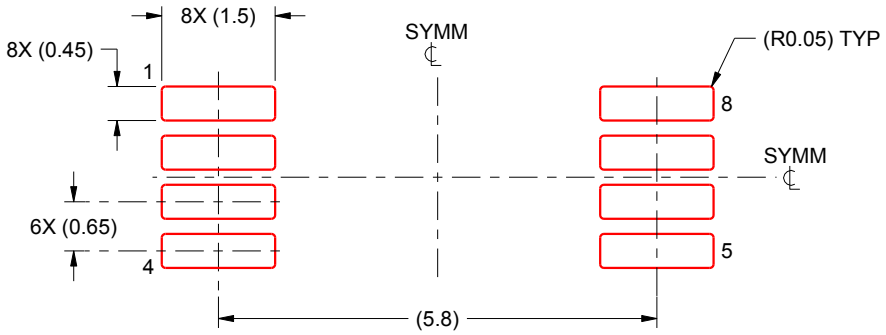


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

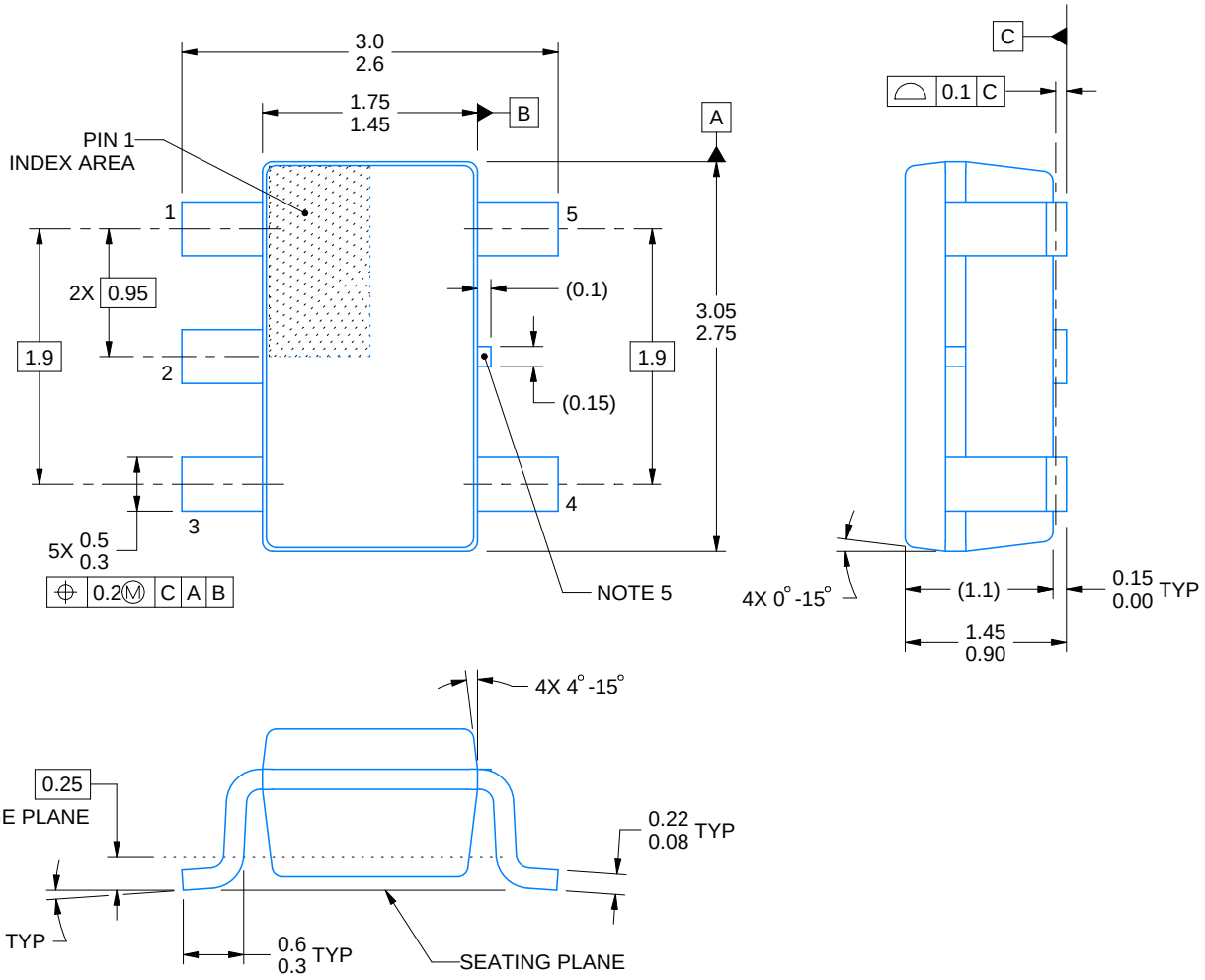
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

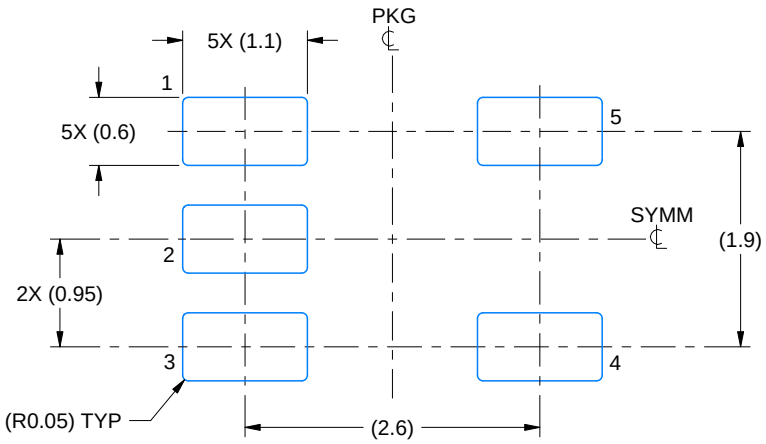
SMALL OUTLINE TRANSISTOR



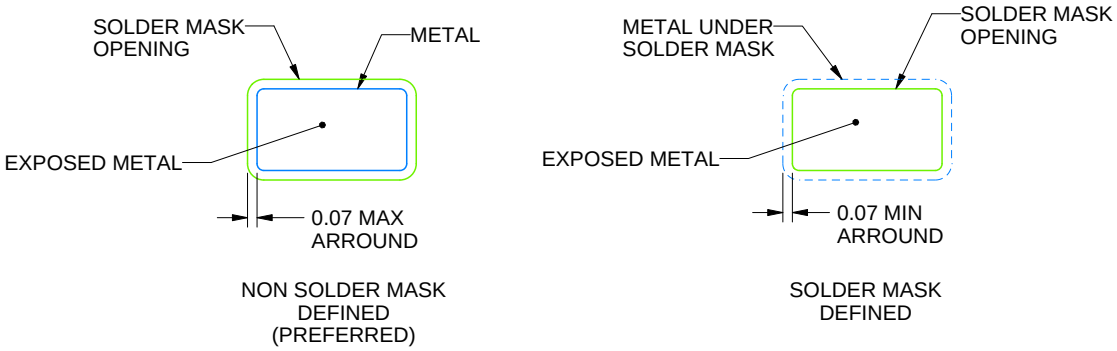
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

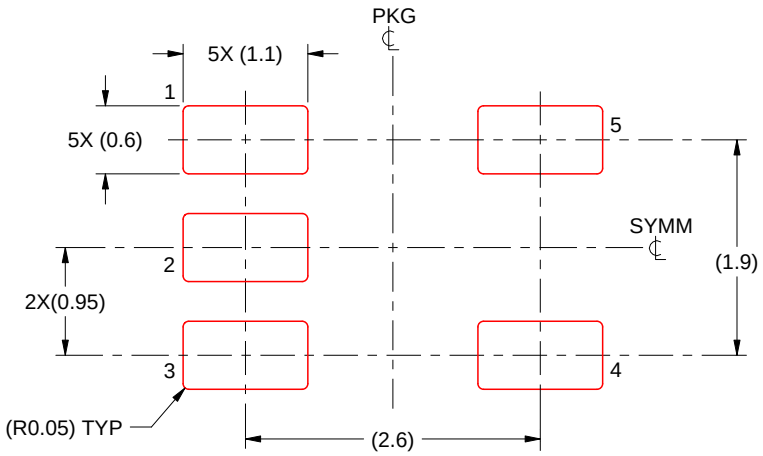


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

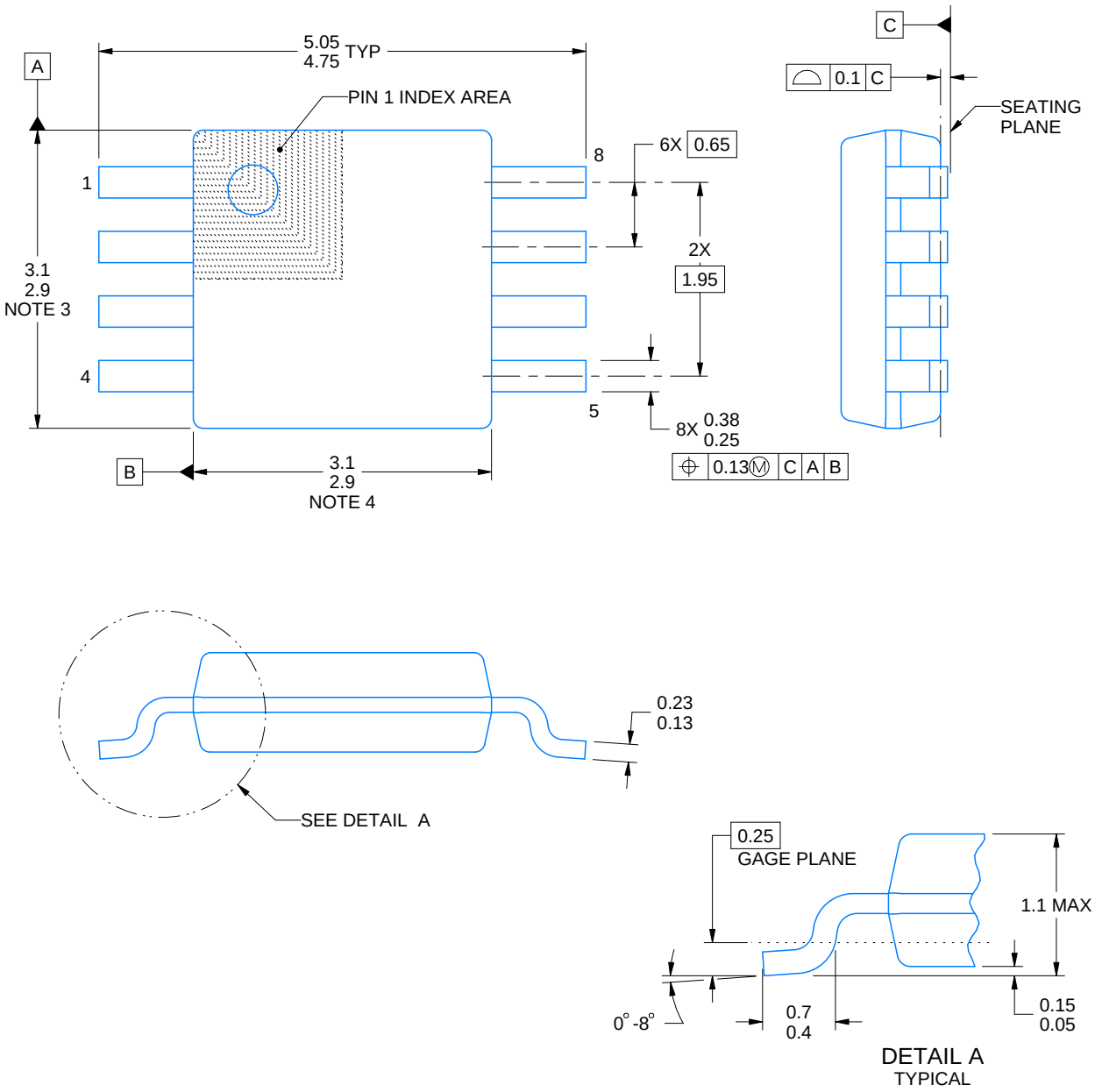
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

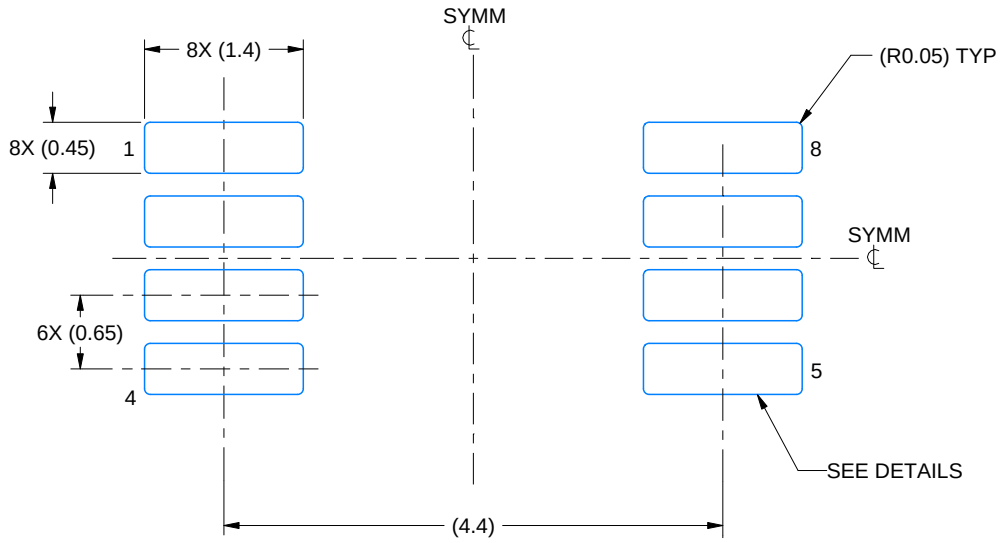
SMALL OUTLINE PACKAGE



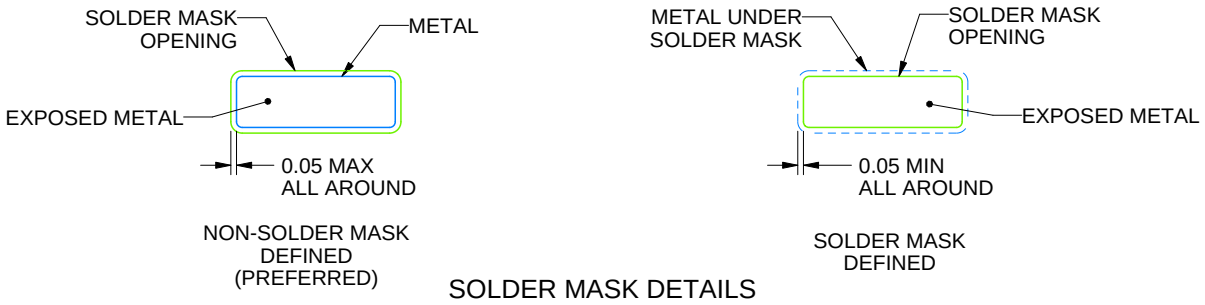
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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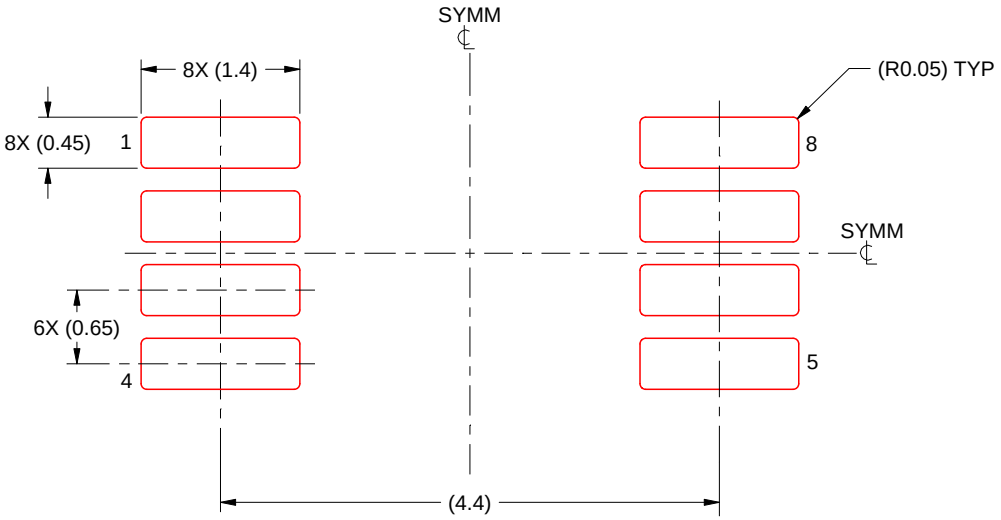
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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