JFE2140 Ultra-Low Noise, Matched, Dual, Low-Gate Current, Discrete, Audio, N-Channel JFET

Texas Instruments
Burr-Brown Audio

1 Features

- Ultra-low noise:
  - Voltage noise:
    - 0.9 nV/√Hz at 1 kHz, I_{DS} = 5 mA
    - 1.1 nV/√Hz at 1 kHz, I_{DS} = 2 mA
  - Current noise: 1.6 fA/√Hz at 1 kHz
- Low V_{GS} mismatch: 4 mV (max)
- Low gate current: 10 pA (max)
- Low input capacitance: 13 pF at V_{DS} = 5 V
- High gate-to-drain and gate-to-source breakdown voltage: –40 V
- High transconductance: 30 mS
- Packages: SOIC, 2-mm × 2-mm WSON

2 Applications

- Microphone inputs
- Hydrophones and marine equipment
- DJ controllers, mixers, and other DJ equipment
- Professional audio mixer or control surface
- Guitar amplifier and other music instrument amp
- Condition monitoring sensor

3 Description

The JFE2140 is a Burr-Brown™ Audio, matched-pair discrete JFET built using Texas Instruments' modern, high-performance, analog bipolar process. The JFE2140 features performance not previously available in older discrete JFET technologies. The JFE2140 offers excellent noise performance across all current ranges, where the quiescent current can be set by the user from 50 µA to 20 mA. When biased at 5 mA, the device yields 0.9 nV/√Hz of input-referred noise, giving ultra-low noise performance with extremely high input impedance (> 1 TΩ). In addition, the matching between JFETs is tested to ±4 mV, providing low offset and high CMRR performance for differential pair configurations. The JFE2140 also features integrated diodes connected to separate clamp nodes to provide protection without the addition of high leakage, nonlinear external diodes.

The JFE2140 can withstand a high drain-to-source voltage of 40-V, as well as gate-to-source and gate-to-drain voltages down to –40 V. The temperature range is specified from –40°C to +125°C.

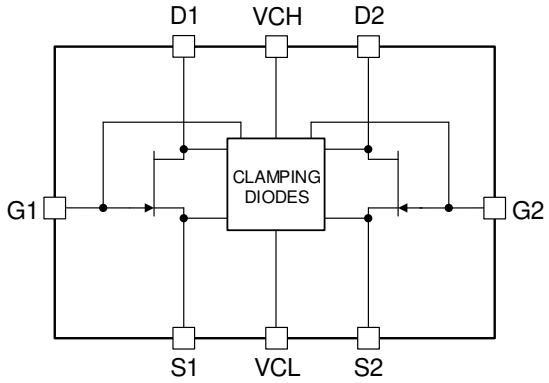
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
JFE2140	D (SOIC, 8)	4.9 mm × 6 mm
	DSG (WSON, 8)	2 mm × 2 mm

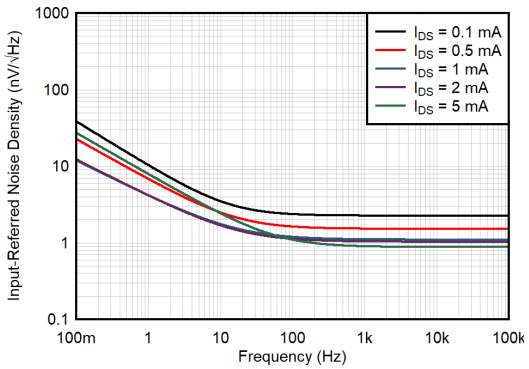
(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Summary

PARAMETER		VALUE
V_{GSS}	Gate-to-source breakdown voltage	–40 V
V_{DSS}	Drain-to-source breakdown voltage	±40 V
C_{ISS}	Input capacitance	13 pF
$V_{GS1} – V_{GS2}$	Differential gate-to-source voltage matching (max)	±4 mV
T_J	Junction temperature	–40°C to +125°C
I_{DSS}	Drain-to-source saturation current	18 mA



Simplified Schematic



Ultra-Low Input Voltage Noise

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2022) to Revision B (August 2023)	Page
• Changed DSG (WSON, 8) package status from preview to production data (active)	1
• Changed parameter descriptions from "gate-to-source voltage" to "gate-to-source breakdown voltage" and from "drain-to-source voltage" to "drain-to-source breakdown voltage" in *Device Summary* table to match *Electrical Characteristics.*	1
• Added "max" to parameter description "differential gate-to-source voltage matching" in *Device Summary* table	1
• Added values for DSG (WSON, 8) package to *Thermal Information table*	4
• Added condition "V_{DS} = 5 V" to Figure 6-7, *Gate Current vs Gate-to-Source Voltage*	6
• Added clarification that the threshold voltage is equivalent to the gate-to-source cutoff voltage (V_{GSC}) in *Common-Source Amplifier.*	13
• Added JFE2140EVM user's guide and JFE2140 Ultra-Low-Noise Preamplifier application note to *Related Documentation*	21

Changes from Revision * (August 2021) to Revision A (March 2022)	Page
• Changed ESD JEDEC specification to JS-002	4
• Changed gate-to-source voltages from –1.2 V to –1.3 V (100 µA), –0.9 V to –1.1 V (2 mA)	5
• Changed Y-axis range from 0 to 33 to 0 to 16 on Figure 6-1, *Drain-to-Source Current vs Gate-to-Source Voltage*	6

5 Pin Configuration and Functions

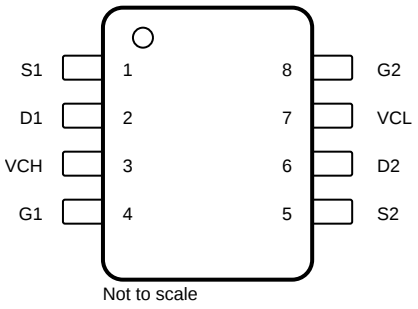


Figure 5-1. D Package, 8-Pin SOIC (Top View)

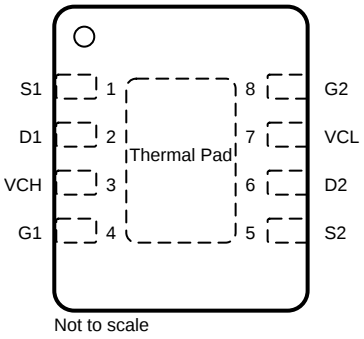


Figure 5-2. DSG Package, 8-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1	2	Output	Drain, channel 1
D2	6	Output	Drain, channel 2
G1	4	Input	Gate, channel 1
G2	8	Input	Gate, channel 2
S1	1	Output	Source, channel 1
S2	5	Output	Source, channel 2
VCH	3	—	Positive diode clamp voltage. Float this pin if clamp diodes are not used.
VCL	7	—	Negative diode clamp voltage. Float this pin if clamp diodes are not used.
Thermal Pad	Thermal Pad	—	Exposed thermal pad. This pad is internally connected to the V_{CL} node. Connect this pad to the same node as V_{CL} or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{DS}	Drain-to-source voltage		–40	40	V
V_{GS}, V_{GD}	Gate-to-source voltage, gate-to-drain voltage		–40	0.1	V
V_{VCH}	Voltage between VCH to D, G, or S			40	V
V_{VCL}	Voltage between VCL to D, G, or S		–40		
I_{VCL}, I_{VCH}	Clamp diode current	DC		20	mA
		50-ms pulse(3)		200	
I_{DS}	Drain-to-source current		–50	50	mA
I_{GS}, I_{GD}	Gate-to-source current, gate-to-drain current		–20	20	mA
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	175	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All gate, drain and source voltages are referred to the same-channel JFET (that is, V_{GS} applies to both V_{G1S1} and V_{G2S2}).
(3) Maximum diode current pulse specified for 50 ms at 1% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_{DS}	Drain-to-source current	0.02		I_{DSS}	mA
V_{GS}	Gate-to-source voltage	–1.2		0	V
T_J	Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		JFE2140		UNIT
		D (SOIC)	DSG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.8	84.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.0	104.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	49.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.1	6.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.4	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	26.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, I_{DS} = 2 mA, V_{DS} = 10 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
e_n	Input-referred noise	I_{DS} = 100 µA	f = 1 kHz		2.5		nV/√Hz
			f = 10 Hz		5.4		
			f = 0.1 Hz to 10 Hz		0.26		$µV_{PP}$
		I_{DS} = 2 mA	f = 1 kHz		1.1		nV/√Hz
			f = 10 Hz		2.4		
			f = 0.1 Hz to 10 Hz		0.12		$µV_{PP}$
e_i	Input current noise, each input	f = 1 kHz, I_{DS} = 2 mA, V_{DS} = 5 V			1.6		fA/√Hz
INPUT CURRENT							
I_G	Input gate current	V_{DS} = 2 V, V_{VCH} = 5 V, V_{VCL} = –5 V			1	±10	pA
		V_{DS} = 0 V, V_{GS} = –30 V			0.2	±60	
			T_A = –40°C to +85°C			0.85	nA
			T_A = –40°C to +125°C			9	
INPUT VOLTAGE							
V_{GSS}	Gate-to-source breakdown voltage	V_{DS} = 0 V, I_G = –100 µA				−40	V
V_{GSC}	Gate-to-source cutoff voltage	V_{DS} = 10 V, I_{DS} = 0.1 µA		−1.5	−1.15	−0.9	V
V_{GS}	Gate-to-source voltage	I_{DS} = 100 µA		−1.3	−0.85	−0.7	V
		I_{DS} = 2 mA		−1.1	−0.6	−0.5	
$ΔV_{GS}$	Differential V_{GS} mismatch	I_{DS} = 2 mA			1	4	mV
			T_A = –40°C to +125°C		1.1	4.2	
	Differential V_{GS} mismatch drift	T_A = –40°C to +125°C			1.7	±10	µV/°C
INPUT IMPEDANCE							
R_{IN}	Gate input resistance	V_{GS} = –30 V to –1 V, V_{DS} = 0 V			1		TΩ
C_{ISS}	Input capacitance	V_{DS} = 0 V			17		pF
		V_{DS} = 5 V			13		
OUTPUT							
I_{DSS}	Drain-to-source saturation current	V_{GS} = 0 V		12	18	23	mA
			T_A = –40°C to +125°C	10		28	
	Drain-to-source saturation current ratio	V_{GS} = 0 V, I_{DSS1} / I_{DSS2}		0.95	1	1.05	
	Transconductance	I_{DS} = 100 µA			2.1		mS
		I_{DS} = 2 mA			10		
G_{FS}	Full conduction transconductance	V_{GS} = 0 V		24	30		mS
V_{DSS}	Drain-to-source breakdown voltage	I_{DS} = 100 µA		40	43		V
C_{OSS}	Output capacitance	I_{DS} = 2 mA			4.5		pF

6.6 Typical Characteristics

at T_A = 25°C, I_{DS} = 2 mA, common-source configuration, and V_{DS} = 10 V (unless otherwise noted)

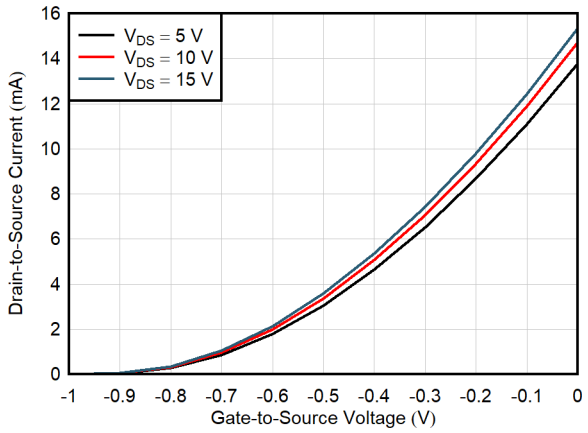


Figure 6-1. Drain-to-Source Current vs Gate-to-Source Voltage

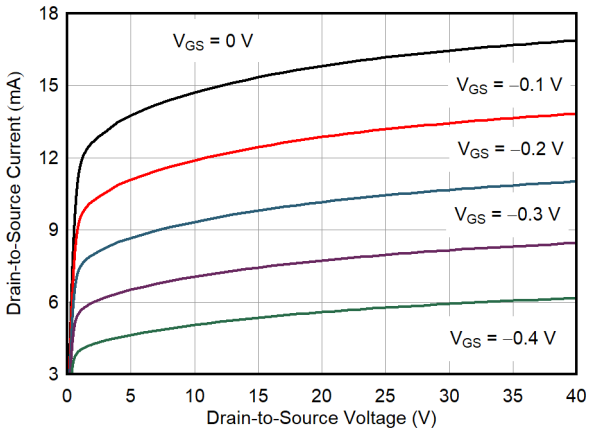


Figure 6-2. Drain-to-Source Current vs Drain-to-Source Voltage

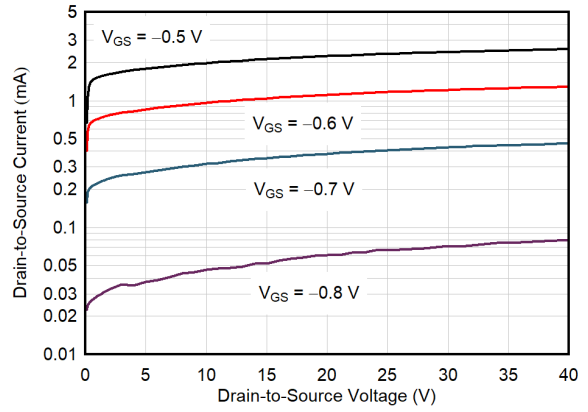


Figure 6-3. Drain-to-Source Current vs Drain-to-Source Voltage

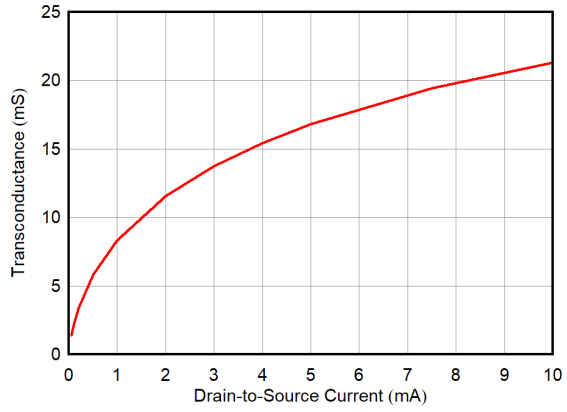


Figure 6-4. Common Source Transconductance vs Drain-to-Source Current

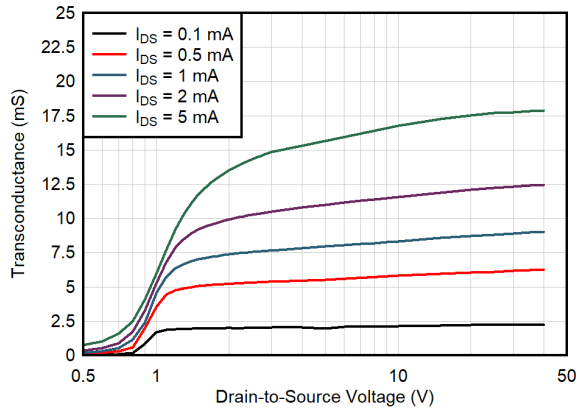


Figure 6-5. Common Source Transconductance vs Drain-to-Source Voltage

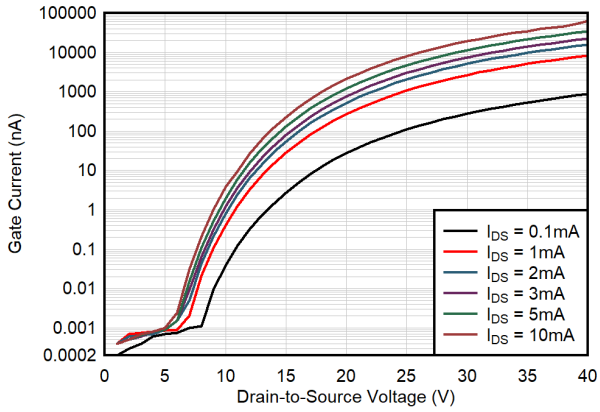
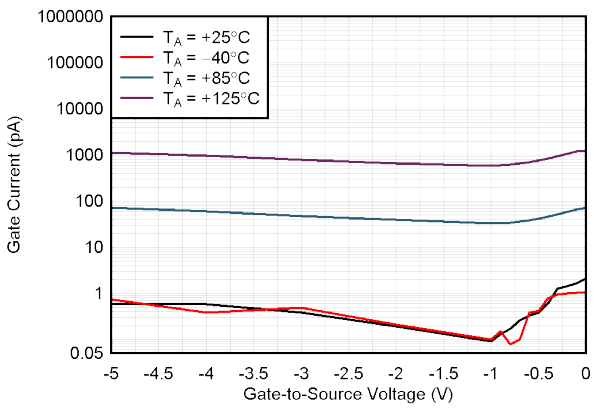


Figure 6-6. Gate Current vs Drain-to-Source Voltage

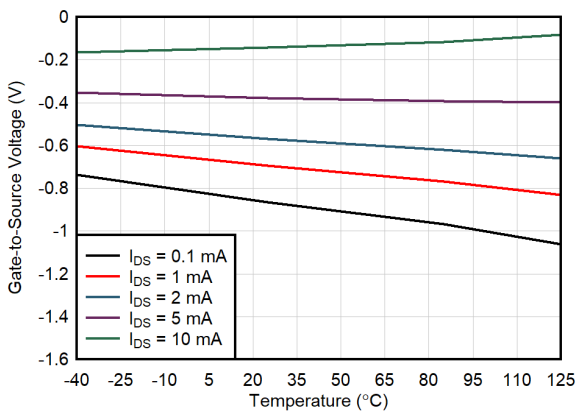
6.6 Typical Characteristics (continued)

at T_A = 25°C, I_{DS} = 2 mA, common-source configuration, and V_{DS} = 10 V (unless otherwise noted)



V_{DS} = 5 V

Figure 6-7. Gate Current vs Gate-to-Source Voltage



V_{DS} = 5 V

Figure 6-8. Gate-to-Source Voltage vs Temperature

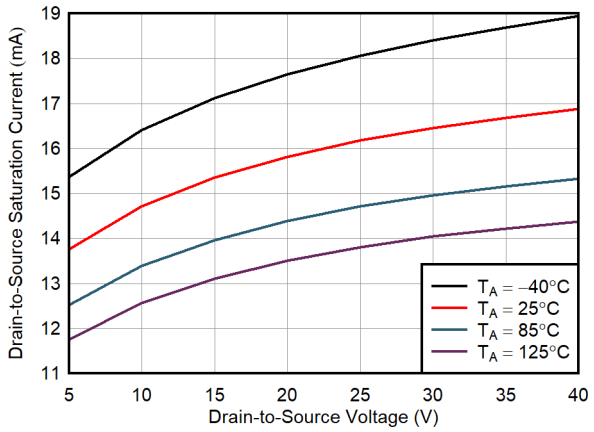
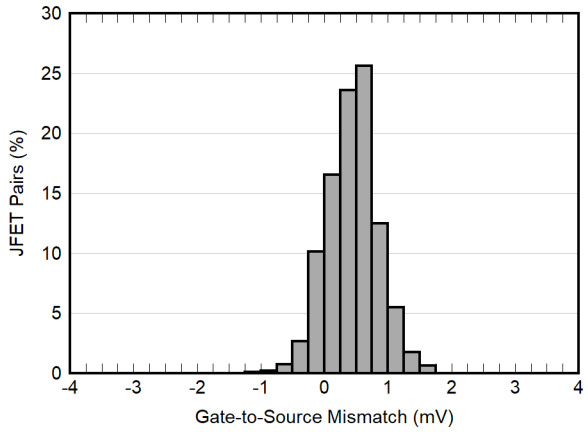
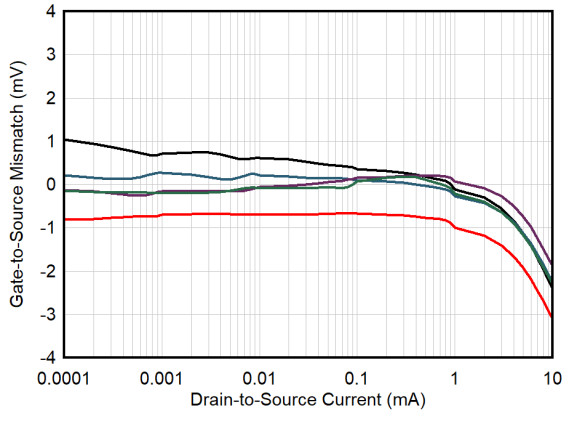


Figure 6-9. I_{DSS} vs Drain-to-Source Voltage



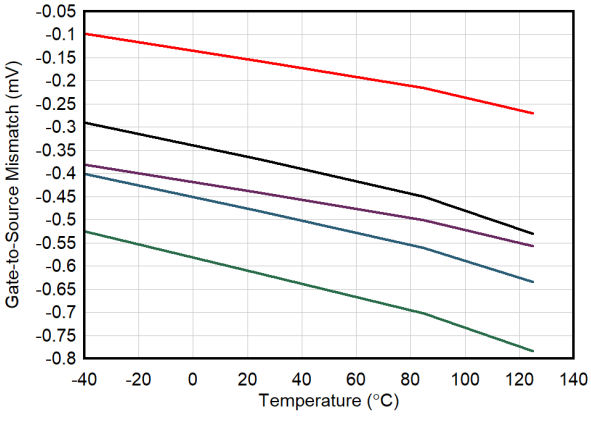
V_{GS}(Ch.1) – V_{GS}(Ch.2) I_{DS} = 2 mA

Figure 6-10. V_{GS} Mismatch Histogram



V_{GS}(Ch.1) – V_{GS}(Ch.2) V_{DS} = 5 V 5 Units

Figure 6-11. V_{GS} Mismatch vs Drain-to-Source Current



V_{GS}(Ch.1) – V_{GS}(Ch.2) I_{DS} = 2 mA 5 Units

Figure 6-12. V_{GS} Mismatch vs Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, I_{DS} = 2 mA, common-source configuration, and V_{DS} = 10 V (unless otherwise noted)

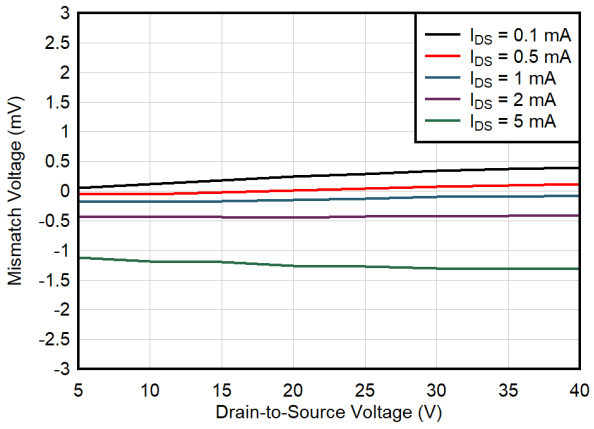


Figure 6-13. V_{GS} Mismatch vs V_{DS}

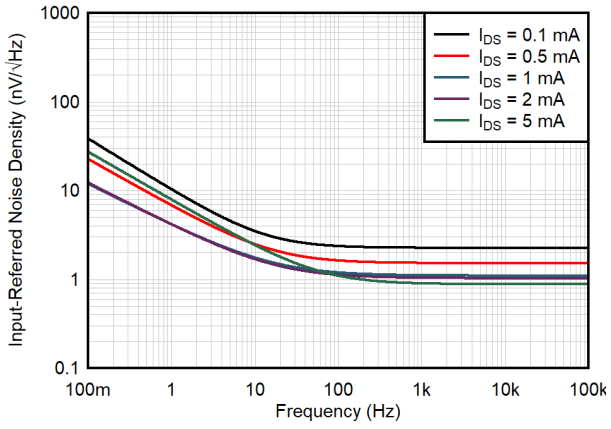


Figure 6-14. Input-Referred Noise Density vs Frequency

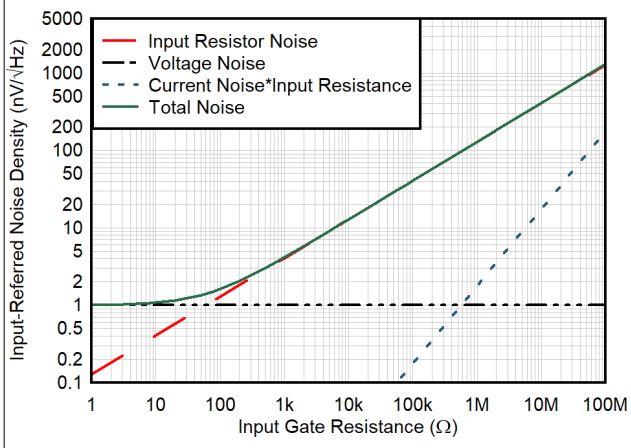


Figure 6-15. Noise Density Contributors vs Input Gate Resistance

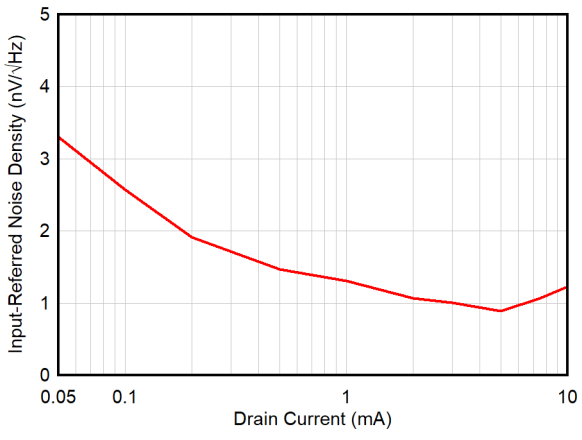


Figure 6-16. Input-Referred Noise Spectral Density vs Drain-to-Source Current

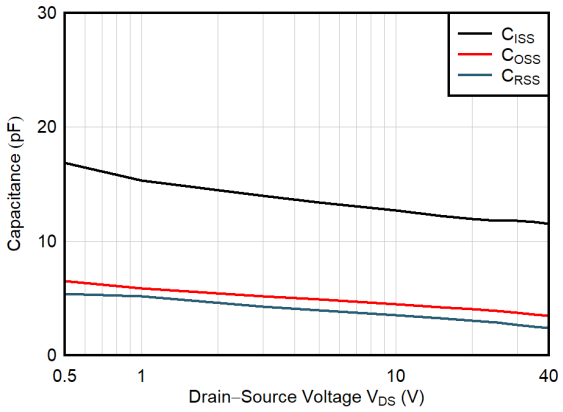


Figure 6-17. Input, Output, and Reverse Transfer Capacitance vs Drain-to-Source Voltage

7 Parameter Measurement Information

7.1 AC Measurement Configurations

The circuit configuration used for noise measurements is seen in Figure 7-1. The nominal I_{DS} current is configured in the schematic by calibrating V–. After I_{DS} is fixed, the V_{DS} voltage is set by calibrating V+. For input-referred noise data, the gain of the circuit is calibrated from V_{IN} to V_{OUT} and used for the input-referred gain calculation.

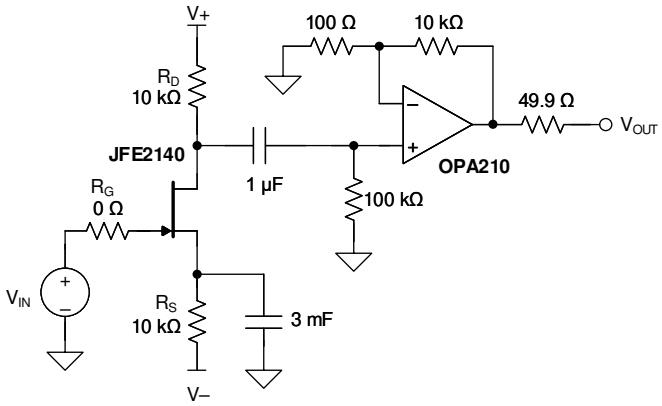


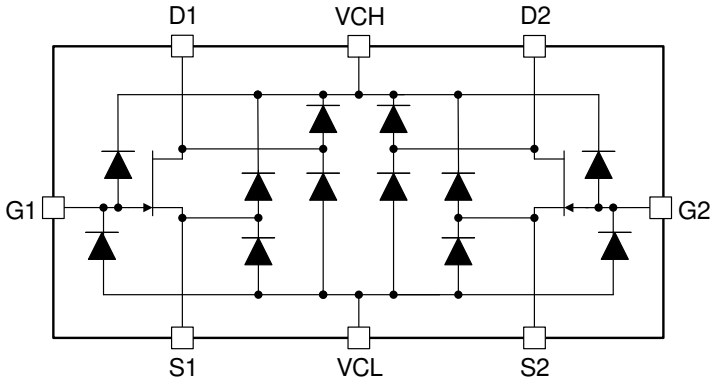
Figure 7-1. AC Measurement Reference Schematic

8 Detailed Description

8.1 Overview

The JFE2140 is a ultra-low noise, matched-input pair N-type JFET designed to create low-noise gain stages for very high output impedance sensors or microphones. Advanced, high precision processing technology gives the JFE2140 tight channel-to-channel matching, extremely low-noise performance, a high gm/C_{ISS} ratio, and ultra-low gate-current performance. The integrated Input-protection diodes clamp high-voltage spurious input signals without the need for additional input diodes that can add leakage current or distortion-creating nonlinear capacitance. The JFE2140 provides a next-generation device to implement low-noise amplifiers for piezoelectric sensors, transducers, large-area condenser microphones, and hydrophones in small-package options.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precision Matching

The JFE2140 features matched-pair, n-type JFET transistors fabricated on a high-precision analog process. Precision matching between opposite JFETs is required in differential-pair configurations, where any mismatch between input devices results in gain and common-mode rejection degradation. Precision matching also minimizes offset voltages that produce excessive error voltages in high-gain, dc-coupled composite amplifiers. Matching distribution for a production lot of units can be seen in Figure 6-10.

8.3.2 Ultra-Low Noise

Junction field effect transistors (JFETs) are commonly used as an input stage in high-input-impedance, low-noise designs in audio, SONAR, vibration analysis, and other technologies. The JFE2140 is a new generation JFET device that offers very low noise performance at the lowest possible current consumption in high-input-impedance amplifier designs. The JFE2140 is manufactured on a high-performance analog process technology, giving tighter process parameter control than a standard JFET.

Designs that feature operational amplifiers (op amps) as the primary gain stage are common, but these designs are not able to achieve the lowest possible noise as a result of the inherent challenges and tradeoffs required from a full operational amplifier design. Noise in JFET designs can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100 Hz. The JFE2140 achieves extremely low 1/f noise in this range. Thermal noise is noise in the region greater than 1 kHz and depends on the gain, or gm, of the circuit. The gm is a function of the drain-to-source bias current; therefore, thermal noise is also a function of drain-to-source bias current. Figure 6-14 shows both 1/f and thermal noise with multiple bias conditions measured using the circuit shown in Figure 7-1.

Noise is typically modeled as a voltage source (voltage noise) and current source (current noise) on the input. The 1/f and thermal noise can be represented as voltage noise. Current noise is dominated by current flow into the gate, and is called *shot noise*. The JFE2140 features extremely low gate current, and therefore, extremely low current noise. Figure 6-15 shows how source impedance on the input is the dominant noise source. In nearly all cases, noise created as a result of current noise is negligible.

8.3.3 Low Gate Current

The JFE2140 features a maximum gate current of 10 pA at room temperature, making the device an excellent choice for maximizing the gain and dynamic range from extremely high impedance sensors. Additionally, any noise contributions as a result of gate current are minimized because of the negligible shot noise at low current levels. As with all JFET devices, when the drain-to-source voltage increases, the gate current also increases. Keep the drain-to-source voltage to less than 5 V for the lowest gate input current operation.

8.3.4 Input Protection

The JFE2140 features input protection diodes that are used for surge clamping and ESD events. The diodes are rated to withstand high current surges for short times, steering current from the gate (G) pin to the VCH and VCL pins. The diodes also feature very low leakage, removing the need for external protection devices that can have high leakage currents or nonlinear capacitance that degrade the distortion performance.

8.4 Device Functional Modes

The JFE2140 functionality is identical to standard N-channel depletion JFET devices. The gate-to-source (V_{GS}) voltage, drain-to-source voltage (V_{DS}) and drain-to-source current (I_{DS}) determine the region of operation.

- For $V_{GS} < V_{GSC}$: JFE2140 conduction channel is closed; I_{DS} is only determined by junction leakage current.
- For $V_{GS} > V_{GSC}$: Two modes of operation can exist depending on V_{DS}. When V_{DS} is less than the linear (saturation) region threshold (see Figure 8-1), the device operates in the linear region, meaning that the device behaves as a resistor connected from drain-to-source with minimal variation from any changes in V_{GS}. When V_{DS} is greater than the linear (saturation) region threshold, I_{DS} has a strong dependance on V_{GS}, where the relationship is described by the parameter gm.

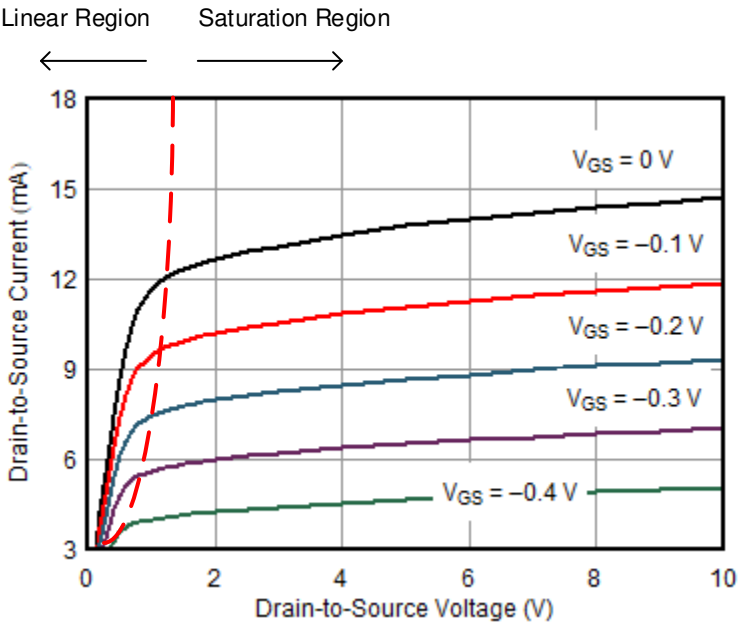


Figure 8-1. V_{DS} vs I_{DS}

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Protection Diodes

The JFE2140 features diodes that are used to help clamp voltage surges that can occur on the input sensor to the gate. The diodes are connected between the gates, sources, and drains of each JFET to two separate pins, VCL and VCH. The clamping mechanism works by *steering* current from the gate into the VCL or VCH nodes when the voltage at the gate, source or drain is less than VCL or greater than VCH. Figure 9-1 shows an example of a microphone input circuit where a dc blocking capacitor operates with a large dc voltage. When the microphone input is dropped or shorted, the dc blocking capacitor discharges into the VCL or VCH nodes, thus helping eliminate large signal transient voltages on the gate. There are also clamping diodes from the drain and source to VCL and VCH, respectively. The clamping diodes can withstand high surge currents up to 200 mA for 50 ms; however, limit dc current to less than 20 mA.

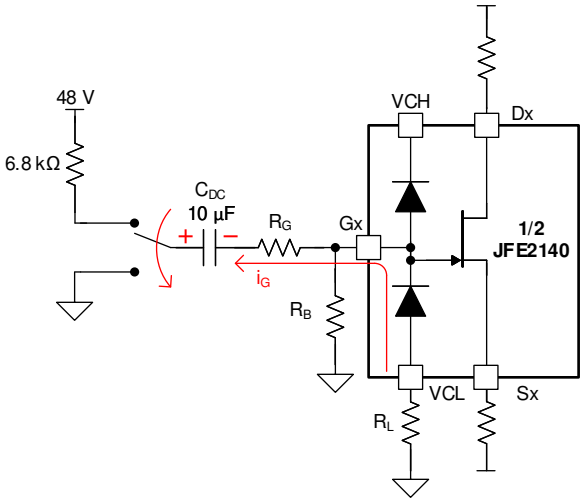


Figure 9-1. JFE2140 Clamping Diode Example

The example in Figure 9-1 shows the diode clamp used to protect the JFET against overvoltage in a phantom-powered microphone circuit. Phantom power typically delivers 48 V through a 6.8-kΩ pullup resistor to a microphone or dynamic load. If the microphone is disconnected, dc blocking capacitor C_{DC} can be biased up to 48 V. If the input to the capacitor is then shorted to ground (shown by the switch in Figure 9-1), the gate voltage can exceed the absolute maximum rating for V_{GS}. In this case, the blocking diode is used, along with current limiting resistors R_G and R_L, to clamp the gate voltage to a safe level. Be aware that the thermal noise of R_G couples directly into the gate input; therefore, make sure to minimize the resistance of R_G.

The clamping diodes are not required for operation. The V_{GS} voltage can withstand –40 V, so clamping is not required if the V_{GS} voltage is kept greater than this limit. If the diodes are not needed, leave the VCL and VCH nodes floating.

9.1.2 Cascode Configuration

The JFE2140 can be configured as a *cascoded* JFET front end. Cascode refers to using a second transistor in-series with the input transistor; see Figure 9-2 for an example.

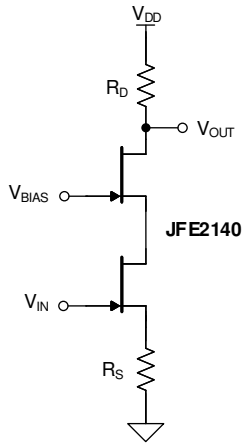


Figure 9-2. JFE2140 connected in Cascode Configuration

Using a cascode configuration, as shown in Figure 9-2, increases the output impedance of the stage, resulting in higher gain, as well as buffers the input node from gate current that flows when the V_{DS} voltages are higher. The V_{BIAS} node must be forced to a voltage greater than what is required to allow both JFETs to remain in the saturated region. A JFET is not required to be used as the cascode device; the benefits of cascoding can be realized with other transistor types, while still maintaining the low-noise, high-impedance benefits of the JFE2140.

9.1.3 Common-Source Amplifier

The common-source amplifier is a commonly used open-loop gain stage for JFET amplifiers, the basic circuit is shown in Figure 9-3.

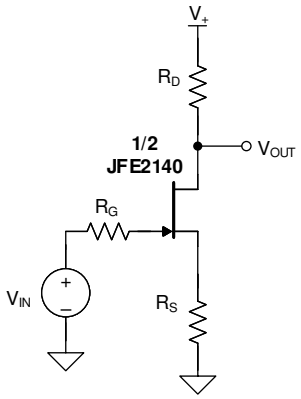


Figure 9-3. Common-Source Amplifier

The equation for gain of the circuit in Figure 9-3 is shown in Equation 1.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{gm^{*}R_D}{1+gm^{*}R_S} \quad (1)$$

Generally, higher gain results in improved noise performance. Gain increases as the bias current is increased as a result of increasing gm (see Figure 6-4). As a result, the input-referred noise decreases as bias current is increased (see Figure 6-14). Any JFET design must make a tradeoff between current consumption and noise performance. The JFE2140, however, delivers significantly lower noise performance than most operational amplifiers at the same current consumption. The bias current (I_{DS}) is set by the value of the source resistor,

R_S, and the threshold voltage, V_T, of the JFE2140. For JFETs, this threshold voltage is equivalent to the gate-to-source cutoff voltage, V_{GSC}. A graph showing nominal I_{DS} vs R_S is shown in Figure 9-4.

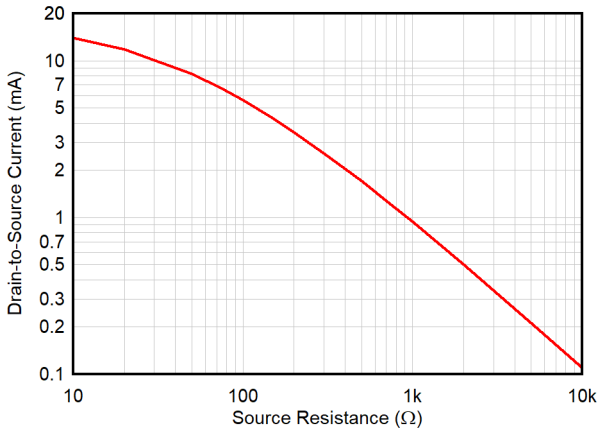


Figure 9-4. Drain-to-Source Current vs R_S, V_{DS} = 5 V

The bias current varies according to the resistor and threshold voltage tolerances. Additionally, thermal noise associated with R_S couples directly into the gain of the circuit, degrading the overall noise performance. To improve the circuit in Figure 9-5, use a current-source biasing scheme. Current-source biasing removes the JFET threshold variation from the biasing scheme, and allows for lower-value filtering capacitance (C_S) for equivalent filtering due to the high output impedance of current sources.

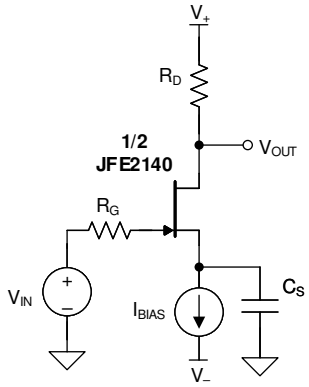


Figure 9-5. Common-Source Amplifier With Current-Source Biasing

9.1.4 Composite Amplifiers

The JFE2140 can be configured to provide a low-noise, high-input impedance front-end stage for a typical op amp. Open-loop transistor gain stages shown previously suffer from wide gain variations that are dependent on the forward transcondutance of the JFE2140. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results by allowing for a fixed gain determined by external resistors, and improving the noise and bandwidth of the operational amplifier. The JFE2140 gain stage provides a boost to the open-loop performance of the system, extending the bandwidth beyond what the operational amplifier alone can provide, and gives a high-input impedance, ultra-low noise input stage to interface with high source impedance microphones.

Figure 9-6 shows a generic schematic representation of a voltage-feedback composite amplifier. The component requirements and tradeoffs are listed in Table 9-1.

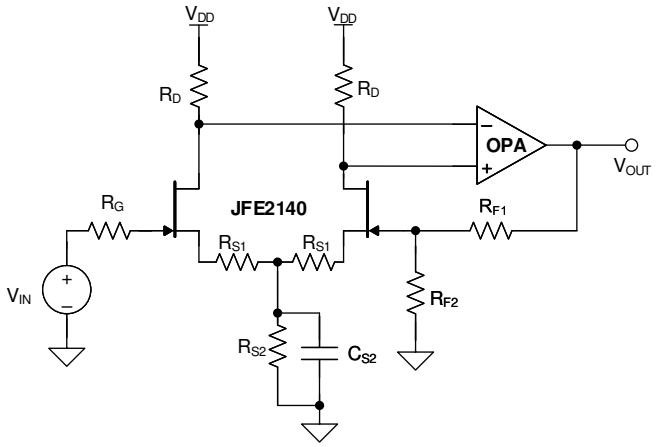


Figure 9-6. Low Noise, High Input Impedance Composite Amplifier

The gain of Figure 9-6 can be calculated using the following equation:

$$A = 1 + \frac{R_{F1}}{R_{F2}} \quad (2)$$

Table 9-1. Composite Amplifier Component List and Function

COMPONENT	DESCRIPTION
R_{S1}	Degeneration resistors. These resistors reduce the overall gain of the JFET stage, but improve the linearity performance. Also, when used in differential configurations (see OPA1637 reference design), the resistors reduce CMRR errors that occur as a result of input mismatch voltages.
R_{S2}	Bias-current setting resistor. This resistor, along with R_{S1}, determine the bias current when using resistive biasing (see Figure 9-4). Be aware that both R_{S1} and R_{S2} resistance directly impact noise performance.
R_G	Gate resistor. This resistor is used to help limit current flow into the gate in overvoltage cases. For improved dc precision, match R_G to the equivalent parallel resistance of R_{S1} || R_{S2}. Use the low resistance values to minimize the thermal noise impact on the circuit.
R_D	Drain resistor. This resistor sets the JFET stage gain in common source biasing, along with gm and R_{S1} + R_{S2}. Higher resistance increases gain, but lowers the nominal V_{DS} voltage.
R_{F1}	Feedback resistor 1. Along with R_{F2}, this resistor sets the gain of the composite amplifier.
R_{F2}	Feedback resistor 2. Along with R_{F1}, this resistor sets the gain of the composite amplifier.
R_{S2}	Source resistor 2. Along with R_{S1}, this resistor sets the dc bias current where the JFET is nominally operated.
C_S	Source capacitor. This capacitor reduces the noise coupling from R_{S2}.

9.2 Typical Applications

9.2.1 Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

The JFE2140 can be configured to provide a low-noise, high-input impedance single-ended amplifier stage that can be optimized for ultra-low noise performance at low power levels. This configuration is designed for battery-powered audio applications such as guitar pedals, amplifiers and handheld recorders. The OPA1692, a low-power, dual audio amplifier, is used for the composite voltage-feedback amplifier, as well as a *rail-splitting* amplifier that centers the ground voltage between the battery positive and negative voltage.

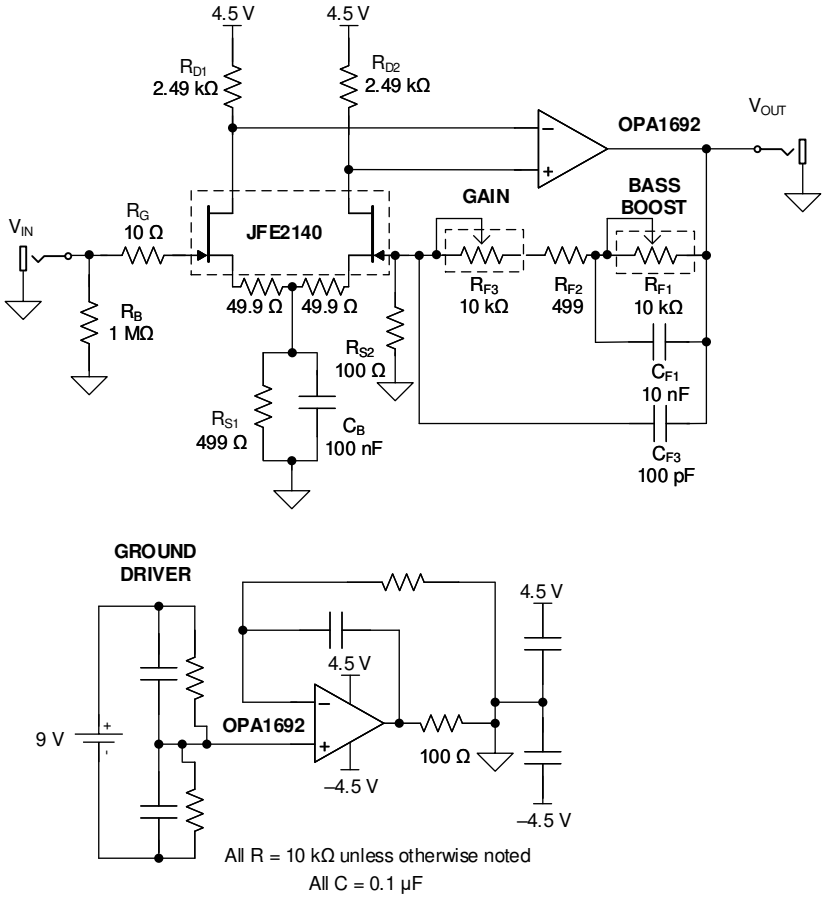


Figure 9-7. Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

9.2.1.1 Design Requirements

PARAMETER	DESIGN GOAL
Gain	15 dB to 40 dB nominal with low-frequency boost
Frequency response	1 Hz to 20 kHz
Noise	< 3 nV/√Hz at 1 kHz
Total current consumption	< 4 mA
Input current	< 100 pA

9.2.1.2 Detailed Design Procedure

This design provides single-ended, adjustable gain from 15 dB to 40 dB with extremely high input impedance at a very low frequency response. The power consumption is optimized for battery-powered audio applications.

- The JFE2140 is configured as a differential pair in a voltage-feedback composite amplifier. This configuration allows for low-frequency gain without large dc-blocking capacitors.
- The bias current is set by selecting the desired bias current and noise tradeoff (see Figure 6-16). To set the bias current point, adjust the source resistance according to Figure 9-4.
- After the bias current is selected, set the JFET stage gain as high as possible. To avoid pushing the device into the linear region of operation, use the largest drain resistor ($R_{D1,2}$) possible while maintaining a minimum of 1 V across the drain-to-source nodes.
- The overall gain can be configured with the feedback resistors R_{F1}, R_{F2} and R_{F3}. Capacitor C_{F3} can be required depending on the gain configuration for amplifier stability; use amplifier stability best practices to maintain stability at both maximum and minimum gain configurations.

9.2.1.3 Application Curves

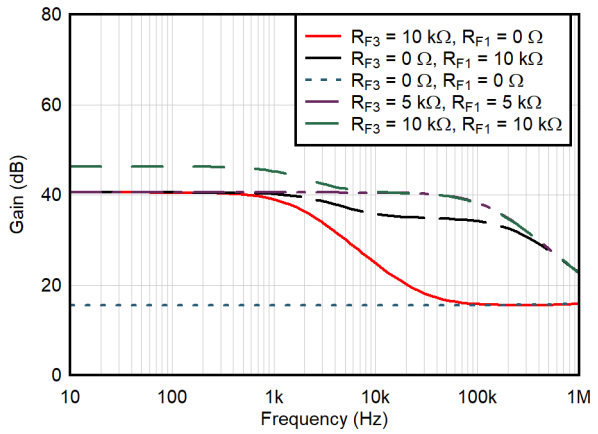


Figure 9-8. Gain/Phase

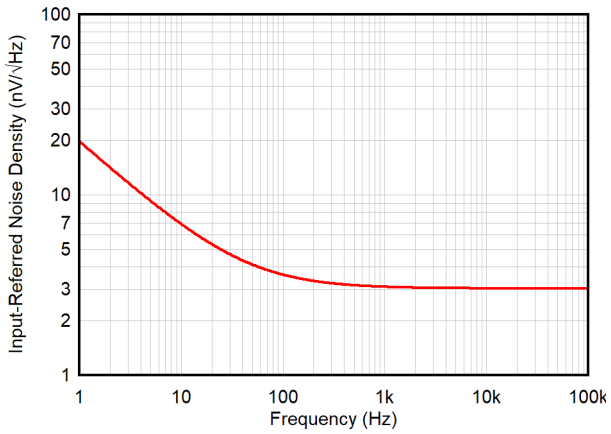


Figure 9-9. Input-Referred Noise Density

9.2.2 Differential Front-End Design

Differential pair architectures are useful for differential small signal amplification where high common-mode voltage rejection (CMRR) is required. In typical differential amplifiers or fully-differential amplifiers (FDA), the tolerance of the resistors alone dominates the CMRR performance. In addition, these amplifiers cannot be configured with high input impedance because of the requirement of input resistors. When used on the front-end of an FDA, the precision-matching on the JFE2140 removes the requirement of extremely low resistor matching (< 1%) by creating a matched-input gain stage. In addition, high input impedance significantly reduces the effects of source impedance mismatch on CMRR performance, creating a differential input designed for noisy environments that are common in professional audio.

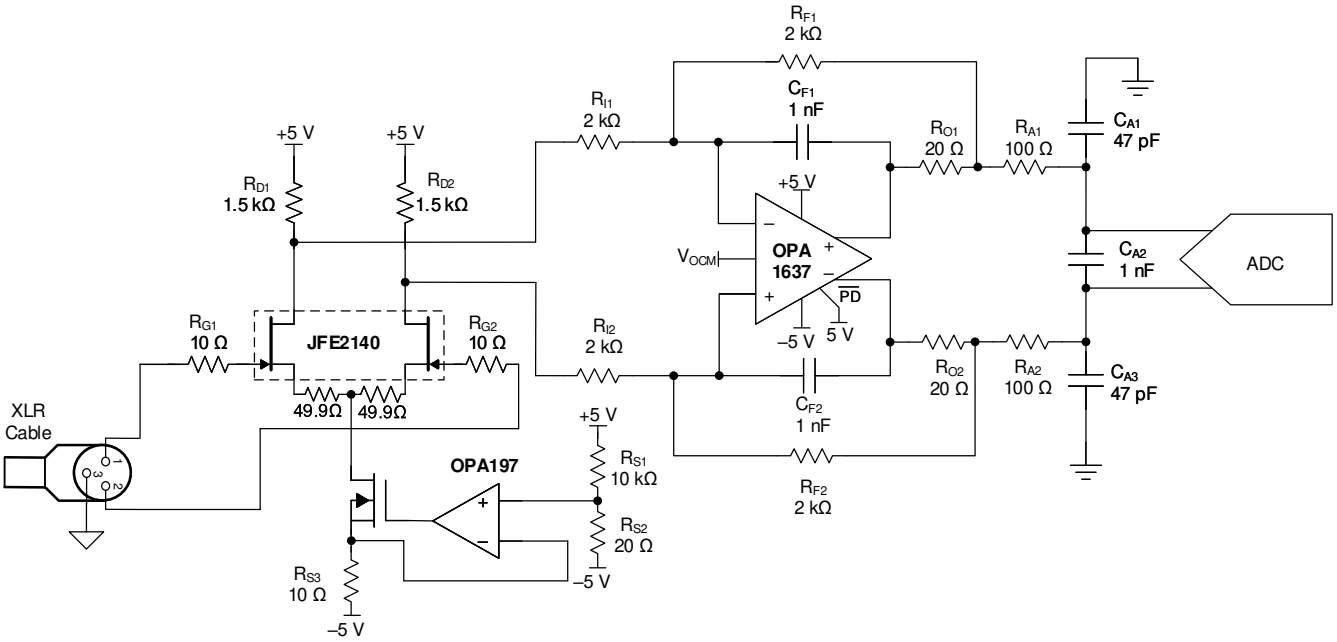


Figure 9-10. The JFE2140 as a High Input Impedance Front End for the OPA1637

9.2.2.1 Application Curves

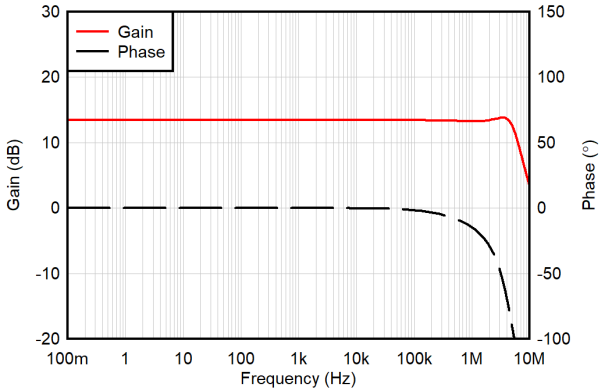
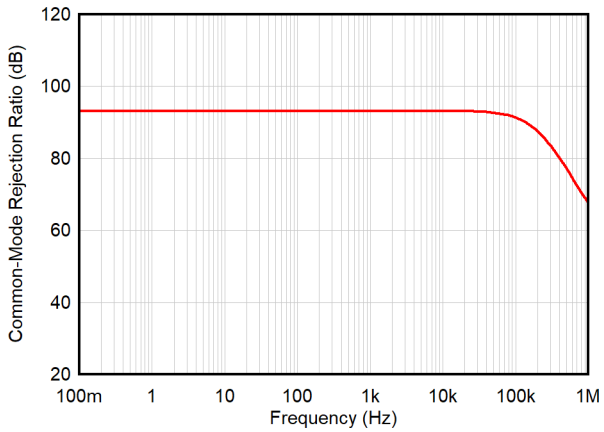


Figure 9-11. Gain and Phase vs Frequency



1-mV mismatch between JFETs

Figure 9-12. CMRR vs Frequency

9.3 Power Supply Recommendations

The JFE2140 is a dual, matched JFET transistor pair with clamping diodes. There are no specific power-supply connections; however, take care not to exceed any absolute maximum voltages on any of the pins if system supply voltages greater than or equal to 40 V are used.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Keep high impedance input signals away from noisy traces.
- Make sure supply voltages are adequately filtered.
- Minimize distance between source-connected and drain-connected components to the JFE2140.
- Consider a driven, low-impedance guard ring around the critical gate traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.4.2 Layout Example

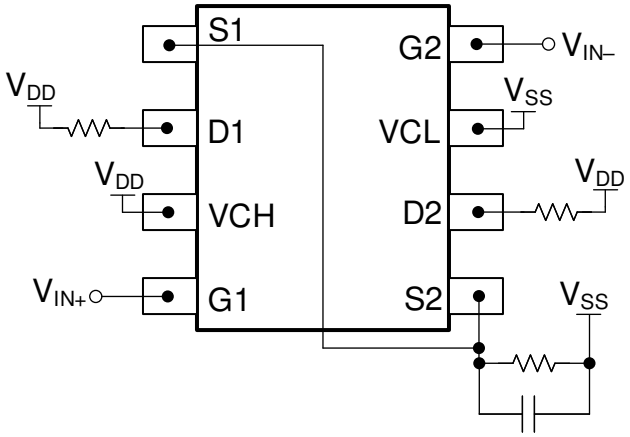


Figure 9-13. JFE2140 Layout Example: Differential Pair Configuration

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

10.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

10.1.1.4 Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *JFE2140 Ultra-Low-Noise Preamplifier* application note
- Texas Instruments, *JFE2140 Evaluation Module* user's guide
- Texas Instruments, *OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers* data sheet
- Texas Instruments, *OPAx210 2.2-nV/√Hz Precision, Low-Power, 36-V Operational Amplifiers* data sheet
- Texas Instruments, *OPA1692 Low-Power, Low-Noise and Low-Distortion SoundPlus™ Audio Operational Amplifiers* data sheet
- Texas Instruments, *OPAx197 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage Operational Amplifiers* data sheet

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JFE2140DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	JF2140	Samples
JFE2140DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2J9U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

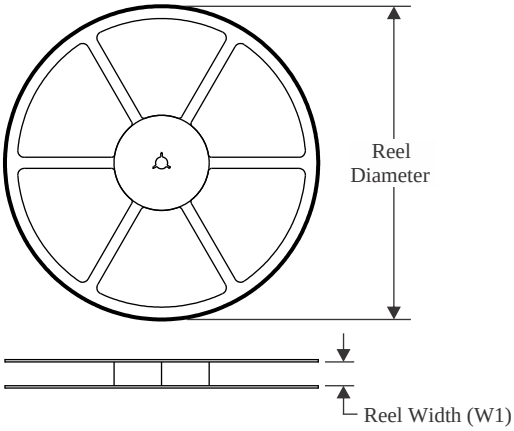
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

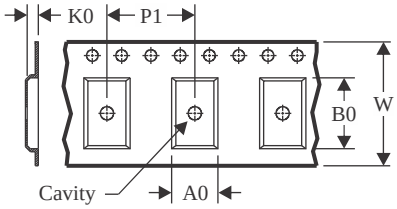
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

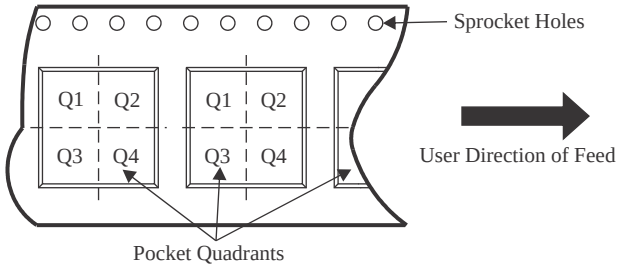


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

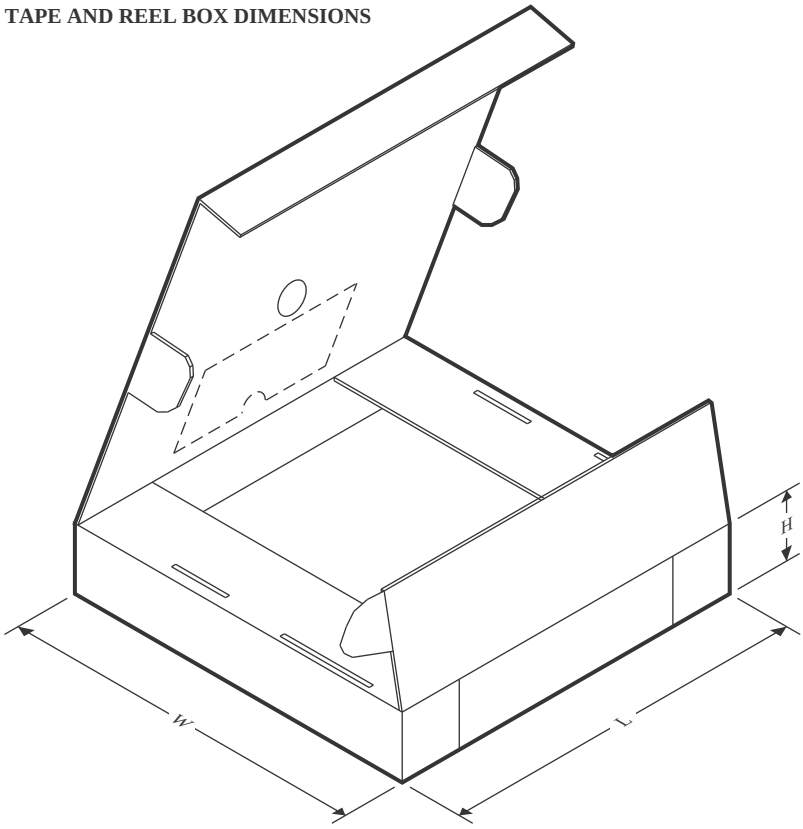
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

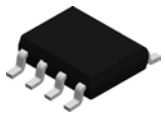
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
JFE2140DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
JFE2140DR	SOIC	D	8	2500	356.0	356.0	35.0

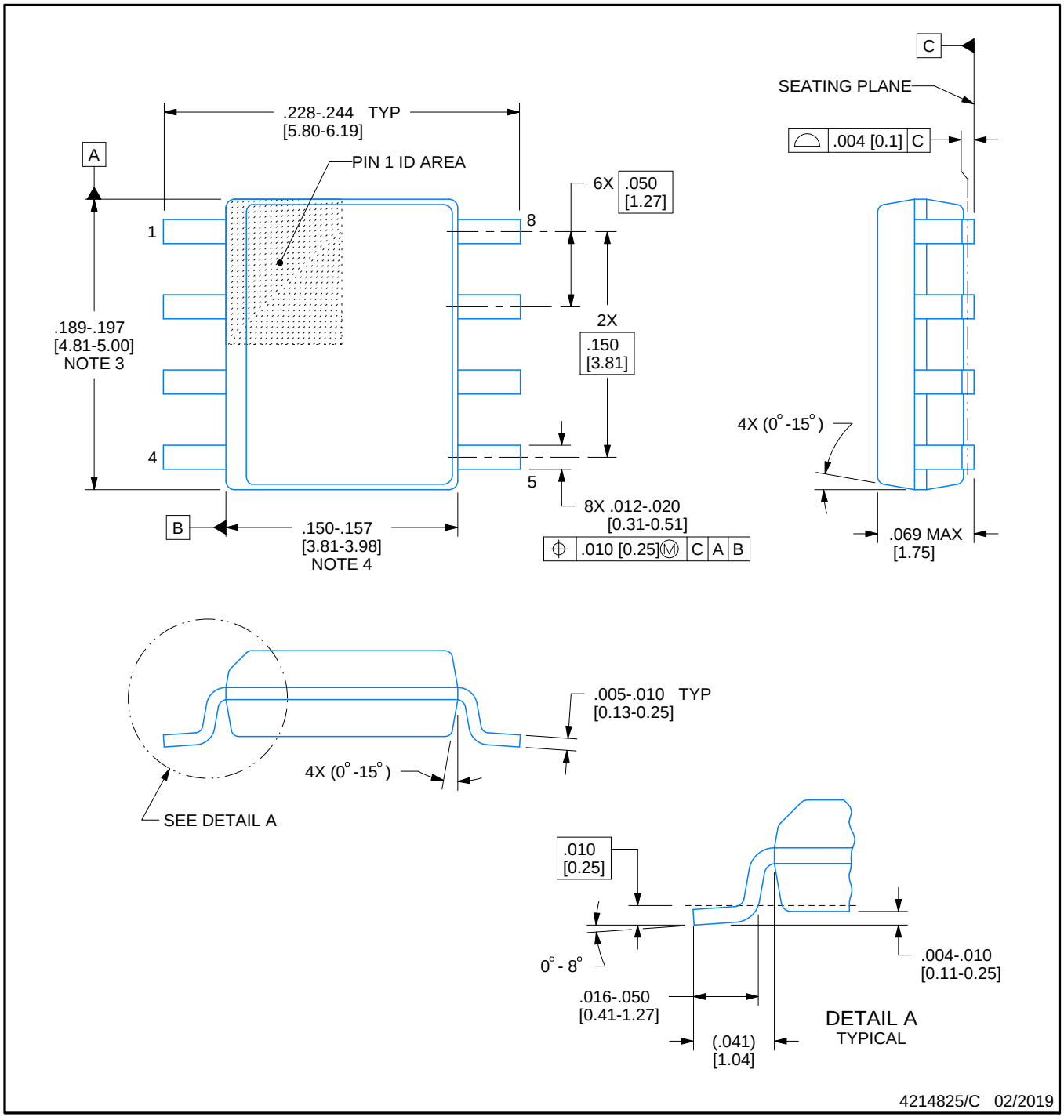


PACKAGE OUTLINE

D0008A

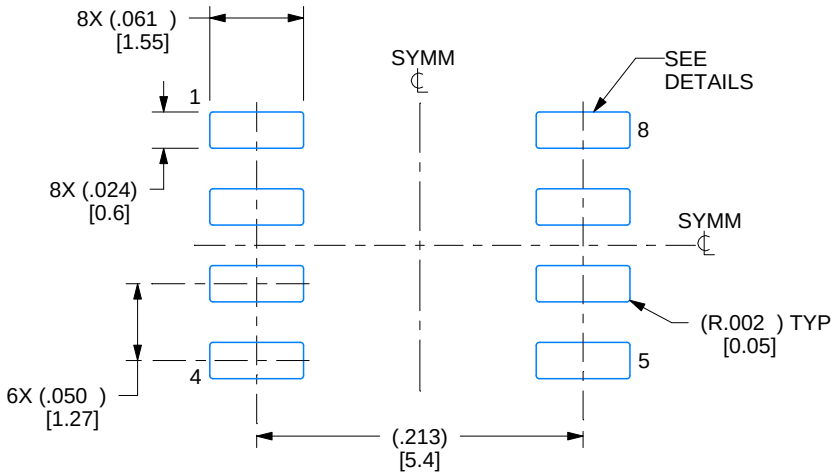
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

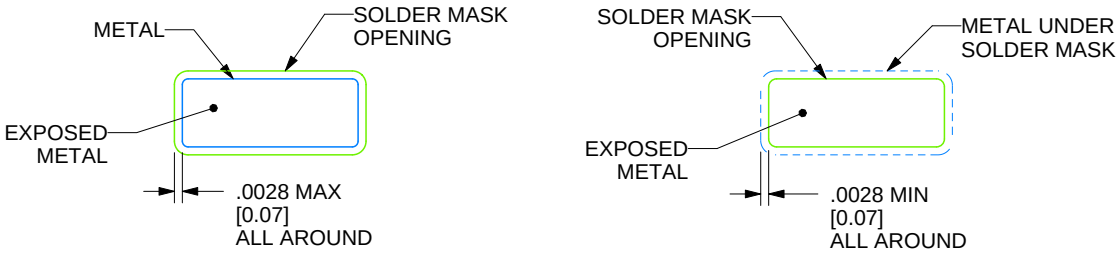


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

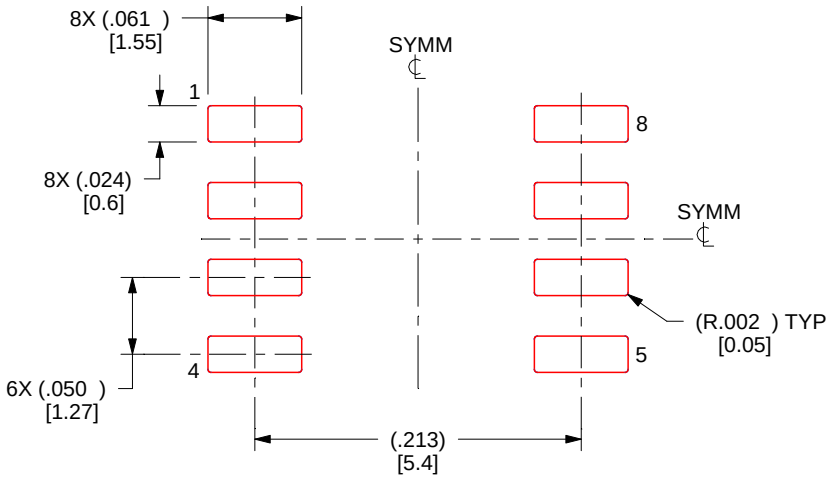
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

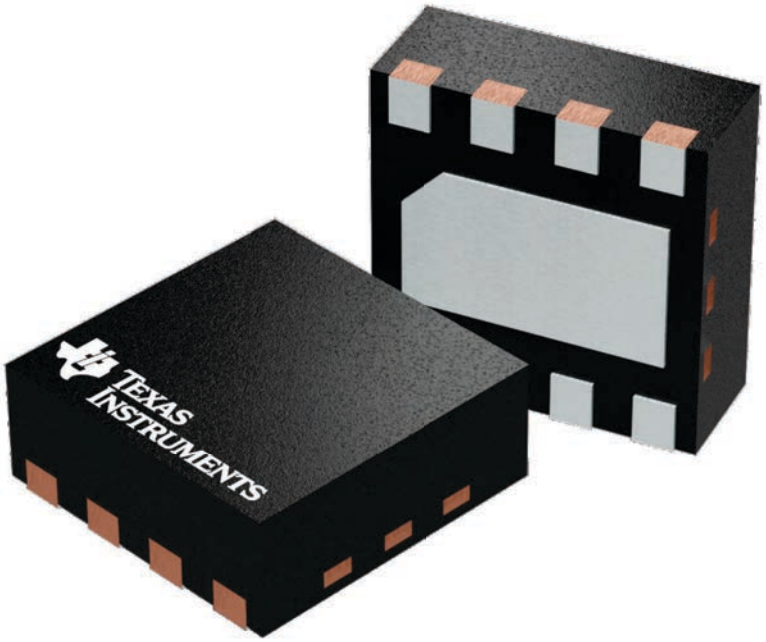
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



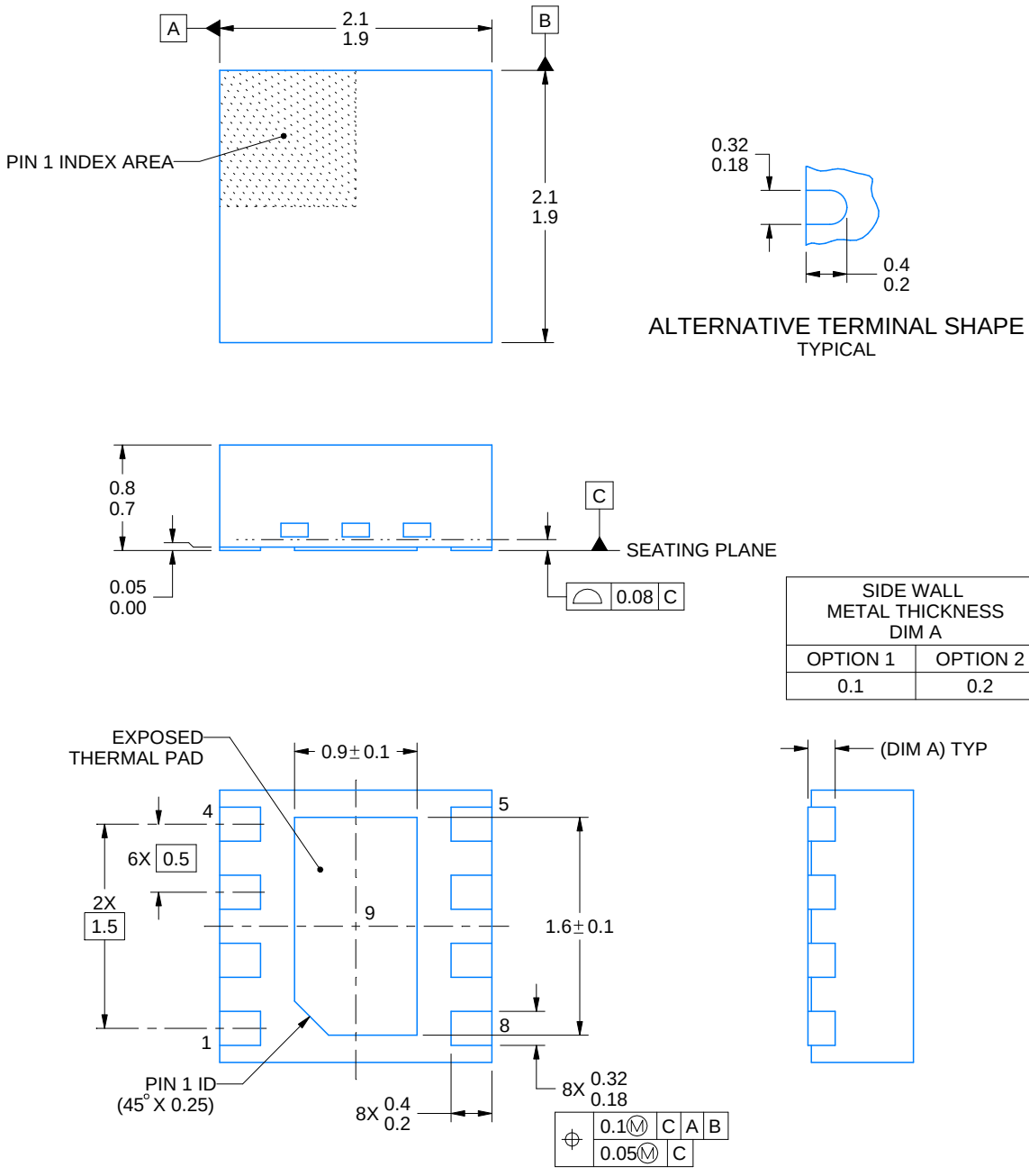
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

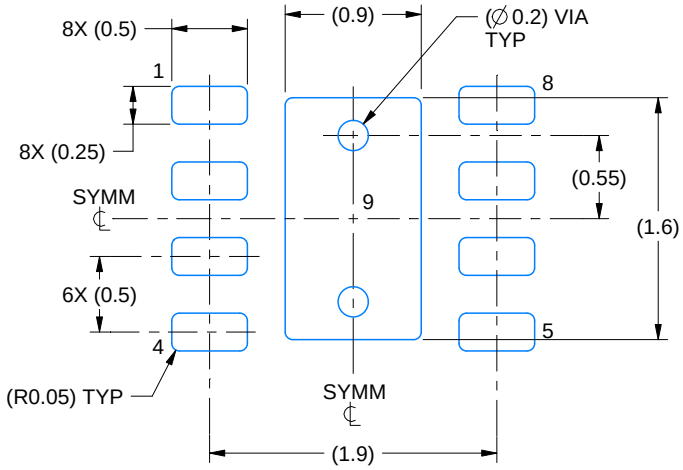
PLASTIC SMALL OUTLINE - NO LEAD



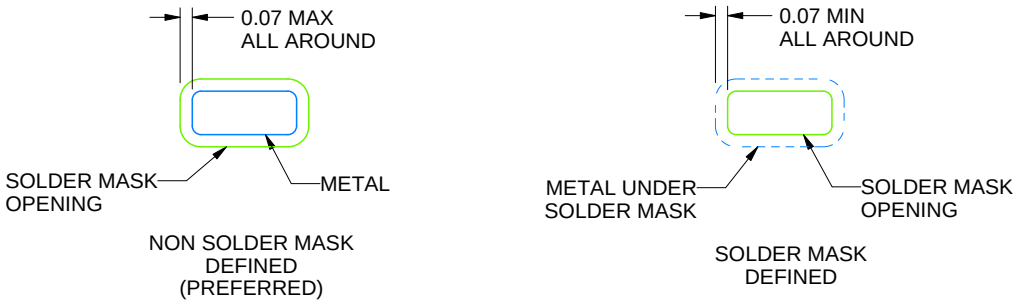
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

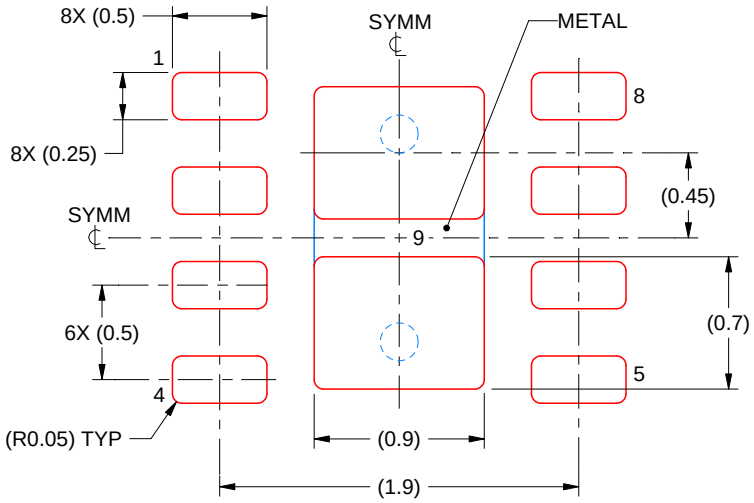


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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