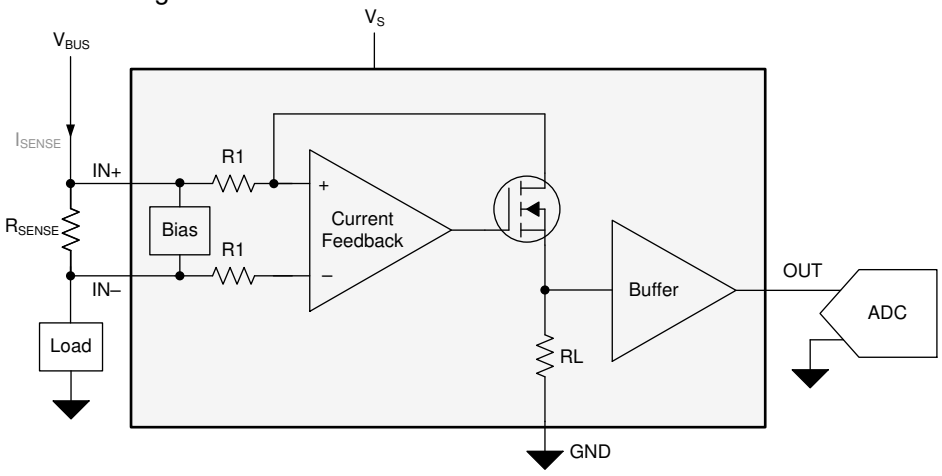
INA950-SEP 2.7V to 80V, 1.1MHz, Ultra-Precise, Current-Sense Amplifier

1 Features

- VID V62/25635
- Radiation - Total Ionizing Dose (TID):
  - TID performance assurance up to 30krad(Si)
  - Radiation Lot Acceptance Testing (RLAT) for every wafer lot up to 30krad(Si)
- Radiation - Single-Event Effects (SEE):
  - Single Event Latch-Up (SEL) immune up to 43MeV-cm^2 /mg at 125°C
  - Single Event Transient (SET) characterized up to LET = 47.5MeV-cm2 /mg
- Space Enhanced Plastic
  - Operating temperature from –55°C to +125°C
  - Controlled baseline
  - Au bondwire and NiPdAu lead finish
  - Outgassing test performed per ASTM E595
  - One fabrication, assembly, and test site
  - Extended product life cycle
  - Product traceability
- Wide common-mode voltage:
  - Operational voltage: 2.7V to 80V
  - Survival voltage: −20V to 85V
- Excellent CMRR:
  - 160dB DC
  - 85dB AC at 50kHz
- Gain of 20V/V
  - Gain error: ±0.1% (maximum)
  - Gain drift: ±1.5ppm/°C
- Offset voltage: ±12µV (maximum)
- Offset drift: ±0.05µV/°C
- High bandwidth: 1.1MHz
- Slew rate: 2V/µs
- Quiescent current: 370µA

2 Applications

- Satellite electrical power system (EPS)
- Command and data handling (C&DH)
- Radar imaging payload
- Communications payload



Typical Application

3 Description

The INA950-SEP is an ultra-precise, current-sense amplifier that can measure voltage drops across shunt resistors over a wide common-mode range from 2.7V to 80V. The ultra-precise current measurement accuracy is achieved thanks to the combination of an ultra-low offset voltage of ±12µV (maximum), a small gain error of ±0.1% (maximum), and a high DC CMRR of 160dB (typical). The INA950-SEP is not only designed for DC current measurement, but also for high-speed applications (such as fast overcurrent protection, for example) with a high bandwidth of 1.1MHz and an 85dB AC CMRR (at 50kHz).

The INA950-SEP provides the capability to make ultra-precise current measurements by sensing the voltage drop across a shunt resistor over a wide common- mode range from 2.7V to 80V. The INA950-SEP is available in the TSSOP-8 package.

The INA950-SEP operates from a single 2.7V to 5.5V supply while only drawing 370µA from the supply (typical). The low offset of the zero-drift architecture enables current sensing with low ohmic shunts as specified over the operating temperature range (−55°C to 125°C).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA950-SEP	PW (TSSOP, 8)	3.00mm × 4.4mm

(1) The package size (length × width) is a nominal value and includes pins, where applicable.
(2) For more information, see Section 10.

Table of Contents

1 Features....1
2 Applications....1
3 Description....2
4 Pin Configuration and Functions....4
5 Specifications....5
5.1 Absolute Maximum Ratings....5
5.2 ESD Ratings....5
5.3 Recommended Operating Conditions....5
5.4 Thermal Information....5
5.5 Electrical Characteristics....6
5.6 Typical Characteristics....7
6 Detailed Description....11
6.1 Overview....11
6.2 Functional Block Diagram....11
6.3 Feature Description....12
6.4 Device Functional Modes....14
7 Application and Implementation....15
7.1 Application Information....15
7.2 Typical Application....17
7.3 Power Supply Recommendations....19
7.4 Layout....19
8 Device and Documentation Support....20
8.1 Documentation Support....20
8.2 Receiving Notification of Documentation Updates....20
8.3 Support Resources....20
8.4 Trademarks....20
8.5 Electrostatic Discharge Caution....20
8.6 Glossary....20
9 Revision History....20
10 Mechanical, Packaging, and Orderable Information....20
10.1 Mechanical Data....21
PACKAGING INFORMATION....24
10.2 Tape and Reel Information....25

4 Pin Configuration and Functions

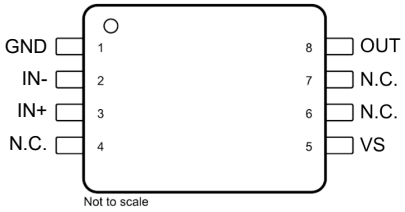


Figure 4-1. INA950-SEP: PW Package 8-Pin TSSOP Top View

Table 4-1. Pin Functions: INA950-SEP

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1	Ground	Ground
IN–	2	Input	Connect to load side of shunt resistor.
IN+	3	Input	Connect to supply side of shunt resistor.
N.C.	4,6,7	-	No internal connection.
OUT	8	Output	Output voltage
VS	5	Power	Power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage	–0.3	6	V
V_{IN+}, V_{IN-} (2)	Analog inputs, differential (V_{IN+}) – (V_{IN-})	–30	30	V
	Analog inputs, common mode (V_{IN+} or V_{IN-})	–20	90	
V_{OUTx}	Analog outputs, output voltage	GND – 0.3	Vs + 0.3	V
T_A	Operating temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) VIN+ and VIN– are the voltages at the VIN+ and VIN– pins, respectively.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range(1)	V_S	48	80	V
V_S	Operating supply range	2.7		5.5	V
T_A	Ambient temperature	–55		125	°C

(1) Common-mode voltage can go below V_S under certain conditions. See Minimum Common-Mode Voltage vs Supply or additional information on operating range.

5.4 Thermal Information

THERMAL METRIC(1)		INA950-SEP PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0.5V / Gain, V_{CM} = $V_{IN–}$ = 48V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection ratio	V_{CM} = 2.7V to 80V, T_A = –55°C to +125°C	140	160		dB
		f = 50kHz		85		
V_{os}	Offset voltage, input referred			±6	±25	µV
dV_{os}/dT	Offset voltage drift	T_A = –55°C to +125°C		±0.05		µV/°C
PSRR	Power supply rejection ratio, input referred	V_S = 2.7V to 5.5V, T_A = –55°C to +125°C		±0.05	±0.5	µV/V
I_B	Input bias current	I_{B+}, V_{SENSE} = 0mV, V_{CM} = 80V, T_A = –55°C to +125°C	10	20	30	µA
		$I_{B–}$, V_{SENSE} = 0mV, V_{CM} = 80V, T_A = –55°C to +125°C	10	20	30	µA
OUTPUT						
G	Gain			20		V/V
	Gain error	GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV		±0.02	±0.1	%
	Gain error drift	T_A = –55°C to +125°C		±1.5		ppm/°C
	Nonlinearity error			0.01		%
	Maximum capacitive load	No sustained oscillations, no isolation resistor		500		pF
VOLTAGE OUTPUT						
	Swing to V_S power supply rail	R_{LOAD} = 10kΩ, T_A = –55°C to +125°C		V_S – 0.07	V_S – 0.2	V
	Swing to ground	R_{LOAD} = 10kΩ, V_{SENSE} = 0V, T_A = –55°C to +125°C		0.005	0.025	V
FREQUENCY RESPONSE						
BW	Bandwidth	C_{LOAD} = 5pF, V_{SENSE} = 200mV		1100		kHz
SR	Slew rate			2		V/µs
	Settling time	V_{OUT} = 4V ± 0.1V step, output settles to 0.5%		9		µs
		V_{OUT} = 4V ± 0.1V step, output settles to 1%		5		
NOISE						
Ve_n	Voltage noise density			50		nV/√Hz
POWER SUPPLY						
V_S	Supply voltage	T_A = –55°C to+125°C	2.7		5.5	V
I_Q	Quiescent current			370	500	µA
		T_A = –55°C to +125°C			600	

5.6 Typical Characteristics

All specifications at T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0.5V / Gain, and V_{CM} = $V_{IN–}$ = 48V (unless otherwise noted).

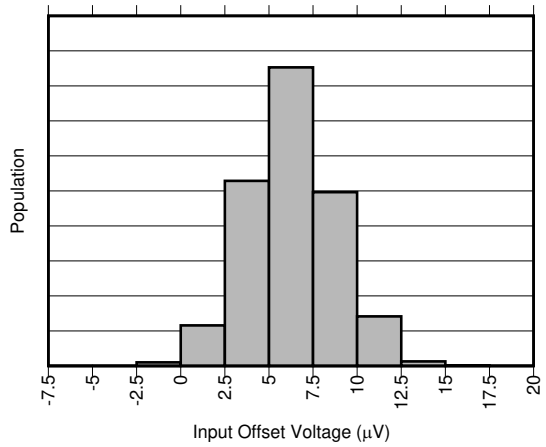


Figure 5-1. Input Offset Production Distribution

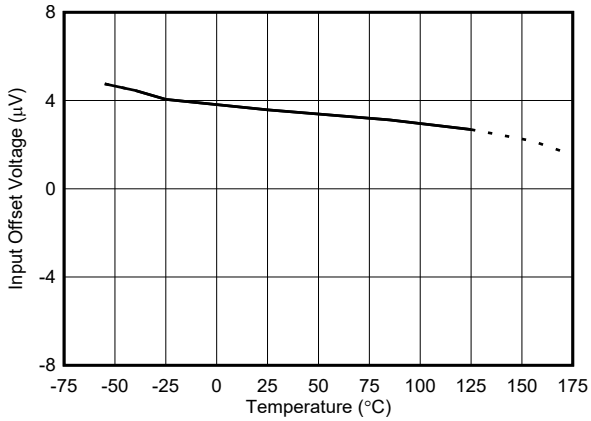


Figure 5-2. Input Offset Voltage vs. Temperature

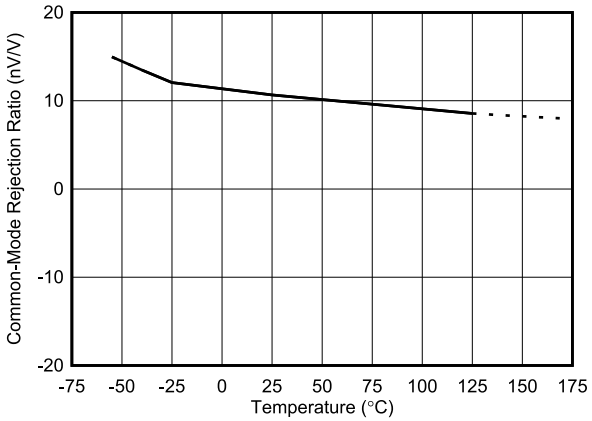


Figure 5-3. Common-Mode Rejection Ratio vs. Temperature

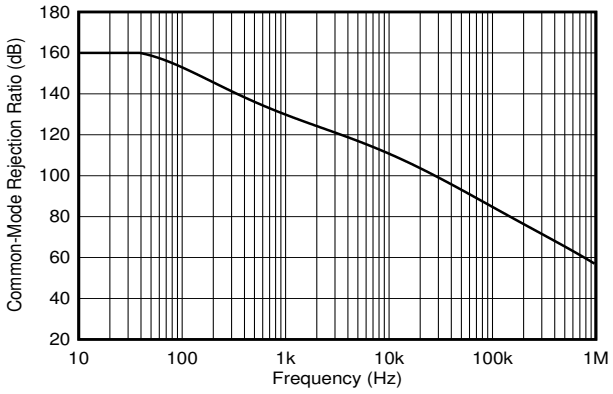
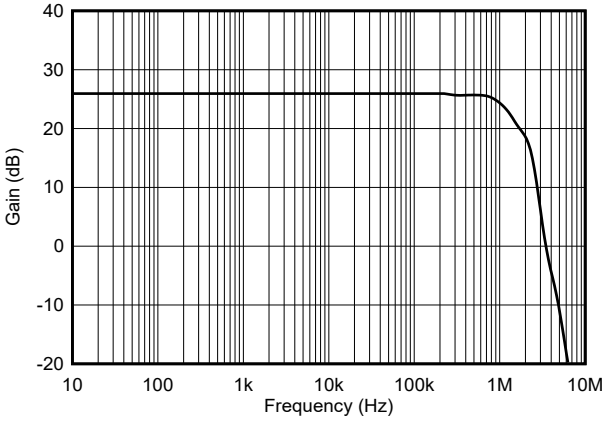


Figure 5-4. Common-Mode Rejection Ratio vs. Frequency



V_{SENSE} = 4V / Gain

Figure 5-5. Gain vs. Frequency

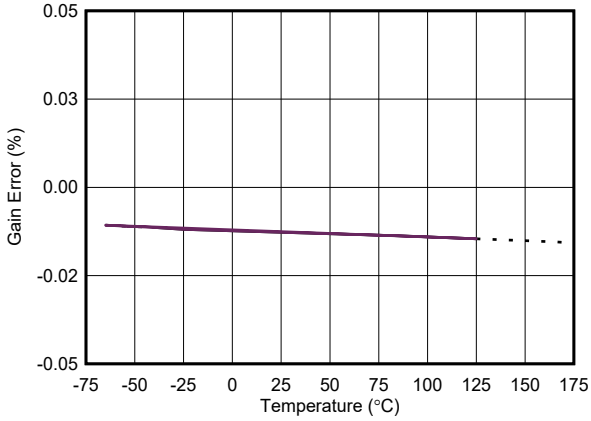


Figure 5-6. Gain Error vs. Temperature

5.6 Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0.5V / Gain, and V_{CM} = $V_{IN–}$ = 48V (unless otherwise noted).

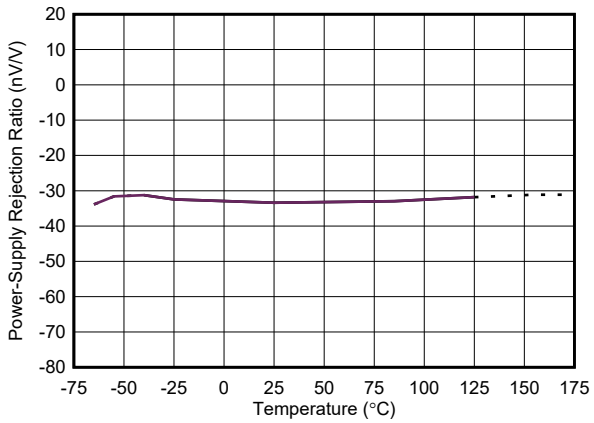


Figure 5-7. Power-Supply Rejection Ratio vs. Temperature

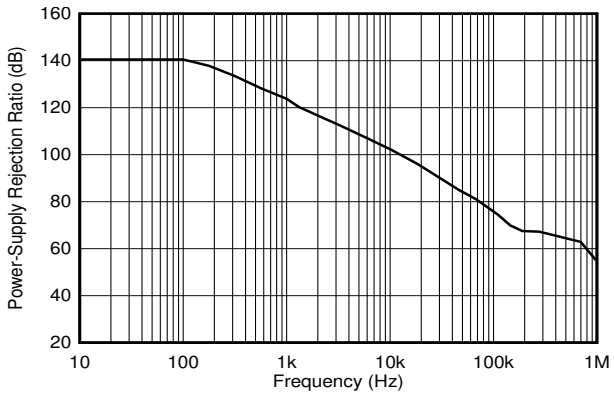
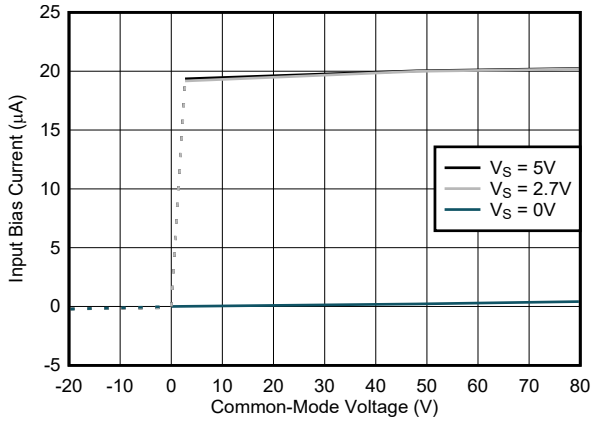


Figure 5-8. Power-Supply Rejection Ratio vs. Frequency



V_{SENSE} = 0V

Figure 5-9. Input Bias Current vs. Common-Mode Voltage

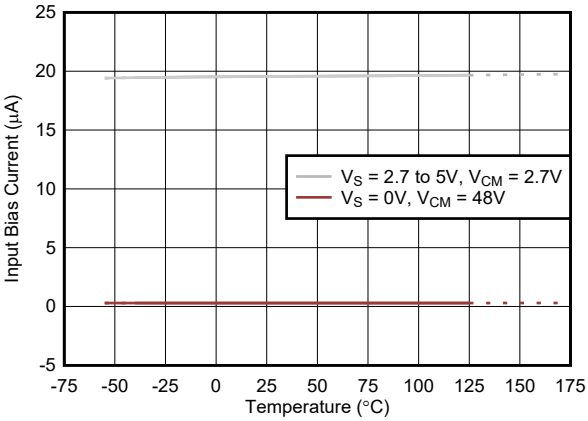


Figure 5-10. Input Bias Current vs. Temperature

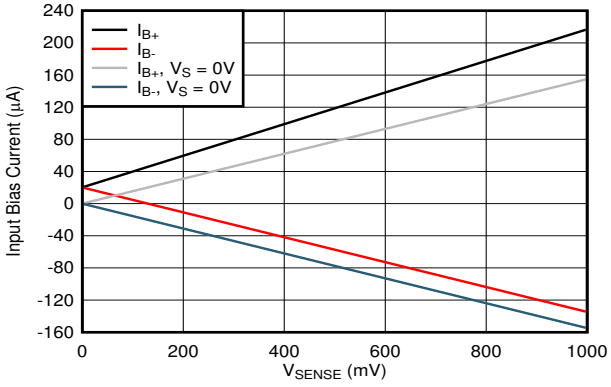
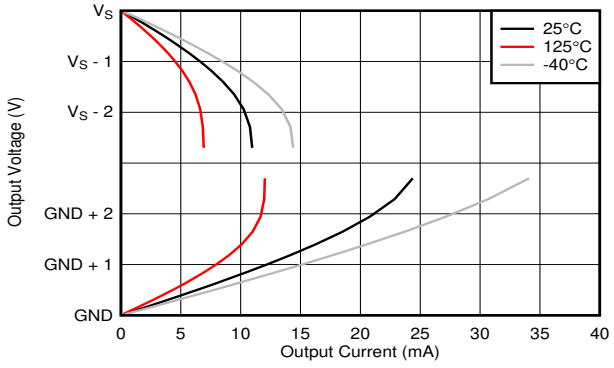


Figure 5-11. Input Bias Current vs. V_{SENSE}

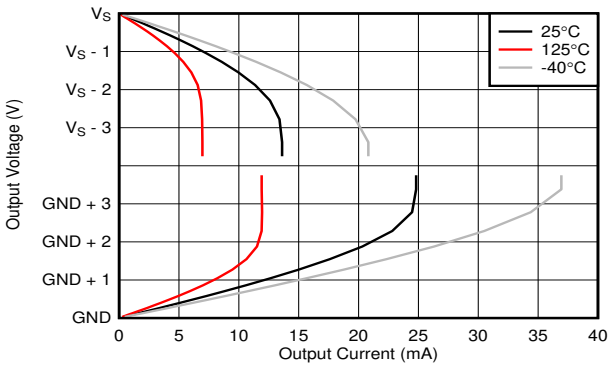


V_S = 2.7V

Figure 5-12. Output Voltage vs. Output Current

5.6 Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0.5V / Gain, and V_{CM} = $V_{IN–}$ = 48V (unless otherwise noted).



V_S = 5V

Figure 5-13. Output Voltage vs. Output Current

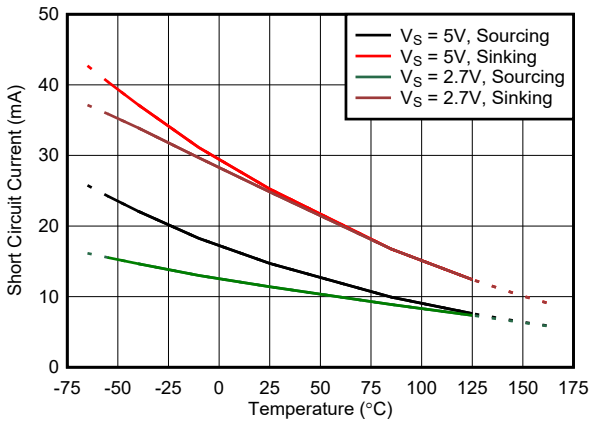


Figure 5-14. Short-Circuit Current vs. Temperature

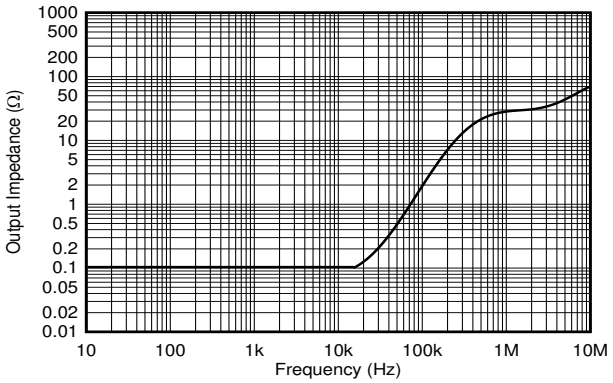
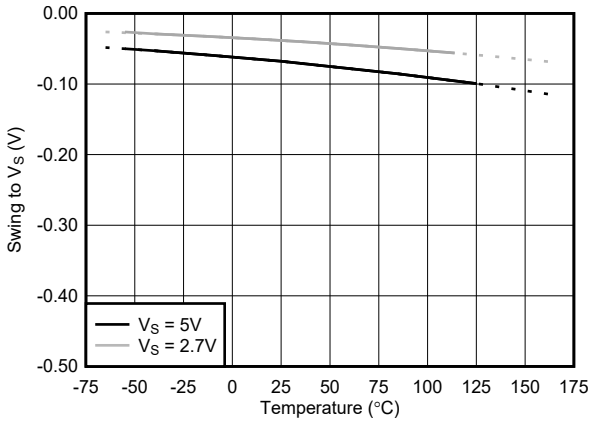
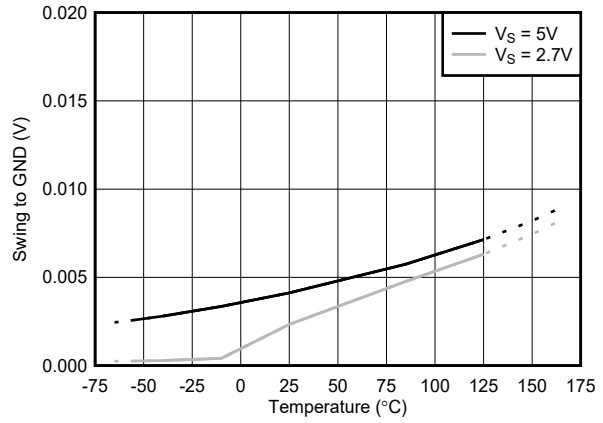


Figure 5-15. Output Impedance vs. Frequency



R_L = 10kΩ

Figure 5-16. Swing to Supply vs. Temperature



R_L = 10kΩ

Figure 5-17. Swing to GND vs. Temperature

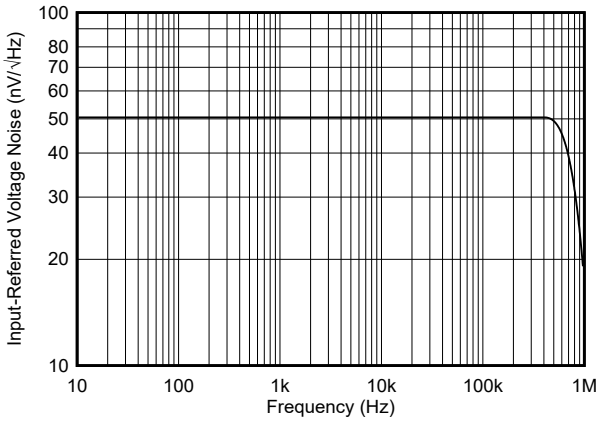


Figure 5-18. Input-Referred Noise vs. Frequency

5.6 Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0.5V / Gain, and V_{CM} = $V_{IN–}$ = 48V (unless otherwise noted).

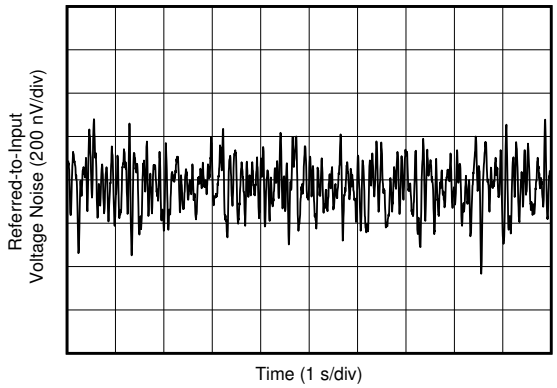


Figure 5-19. Input-Referred Noise

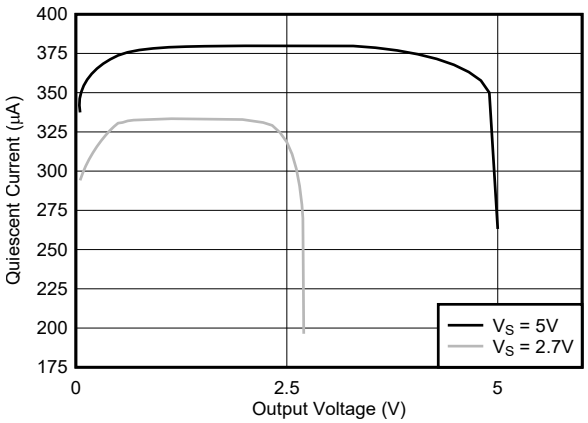


Figure 5-20. Quiescent Current vs. Output Voltage

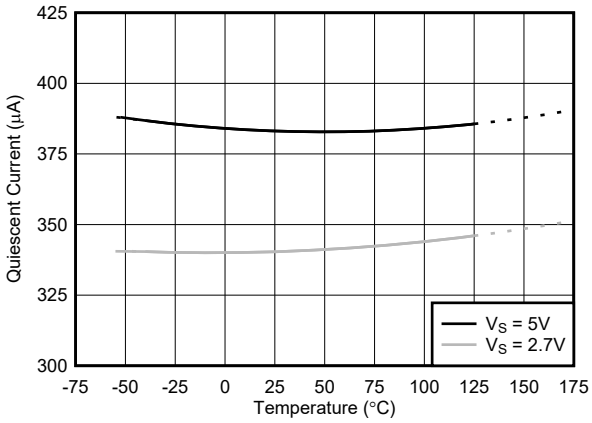


Figure 5-21. Quiescent Current vs. Temperature

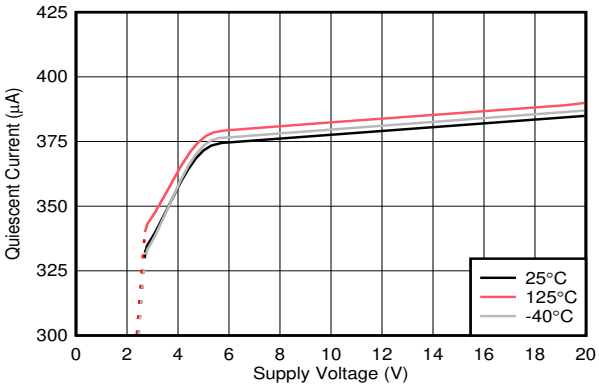


Figure 5-22. Quiescent Current vs. Supply Voltage

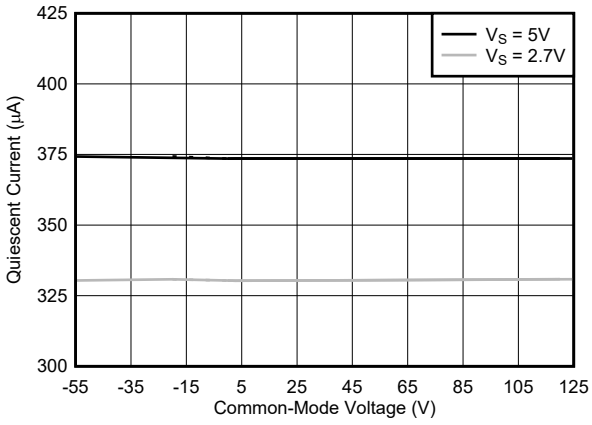
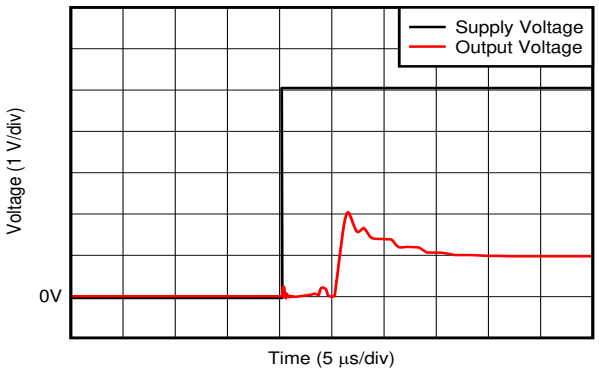


Figure 5-23. Quiescent Current vs. Common-Mode Voltage



V_{SENSE} = 0mV

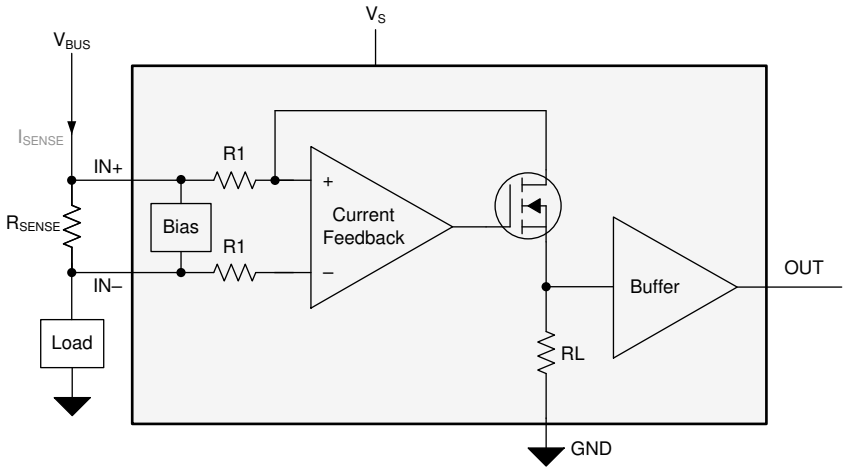
Figure 5-24. Start-Up Response

6 Detailed Description

6.1 Overview

The INA950-SEP is a high-side only current-sense amplifier that offers a wide common-mode range, precision zero-drift topology, excellent common-mode rejection ratio (CMRR), high bandwidth, and fast slew rate. Different gain versions are available to optimize the output dynamic range based on the application. The INA950-SEP is designed using a transconductance architecture with a current-feedback amplifier that enables low bias currents of 20µA and a common-mode voltage of 80V.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Amplifier Input Common-Mode Range

The INA950-SEP supports large input common-mode voltages from 2.7V to 80V and features a high DC CMRR of 160dB (typical) and a 85dB AC CMRR at 50kHz. The minimum common-mode voltage as shown in Figure 6-1 is restricted by the supply voltage. The topology of the internal amplifiers INA950-SEP restricts operation to high-side, current-sensing applications.

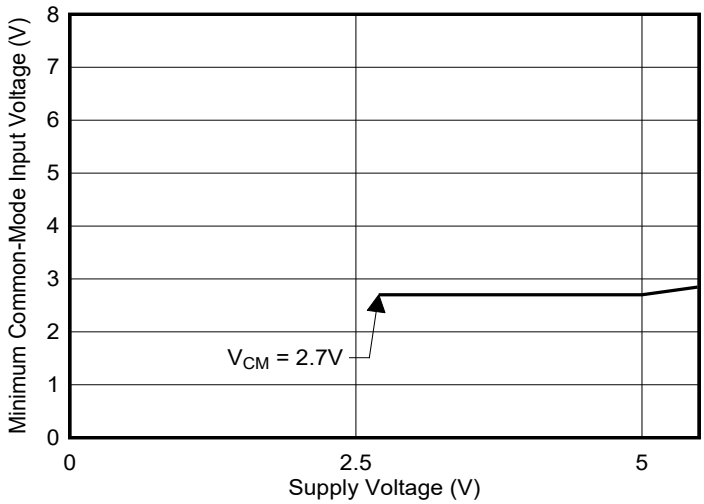


Figure 6-1. Minimum Common-Mode Voltage vs. Supply

6.3.2 Input-Signal Bandwidth

Figure 5-5 shows the INA950-SEP –3dB bandwidth for the INA950-SEP. High bandwidth provides the throughput and fast response required for rapid detection and processing of overcurrent events.

The device bandwidth also depends on the applied V_{SENSE} voltage. Figure 6-2 shows the bandwidth performance profile of the device over frequency as output voltage increases. As shown in Figure 6-2, the device exhibits the highest bandwidth with higher V_{SENSE} voltages.

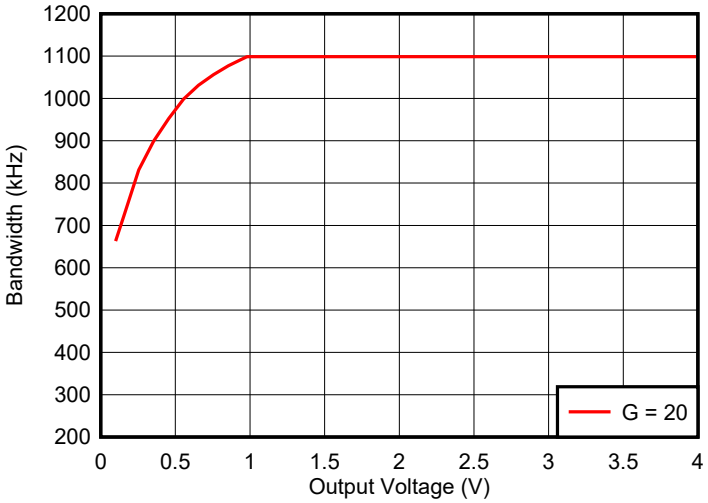


Figure 6-2. Bandwidth vs Output Voltage

6.3.3 Low Input Bias Current

The INA950-SEP input bias current draws 20µA (typical) even with common-mode voltages as high as 80V. This current enables precision current sensing in applications where the sensed current is small or in applications that require lower input leakage current.

6.3.4 Low V_{SENSE} Operation

The INA950-SEP enables accurate current measurement across the entire valid V_{SENSE} range. The zero-drift input architecture of the INA950-SEP provides the low offset voltage and low offset drift required to measure low V_{SENSE} levels accurately across the wide operating temperature of –55°C to +125°C. The capability to measure low sense voltages enables accurate measurements at lower load currents, and also allows reduction of the sense resistor value for a given operating current, which minimizes the power loss in the current-sensing element.

6.3.5 Wide Fixed-Gain Output

The INA950-SEP gain error is < 0.1% at room temperature for most gain options, with a maximum drift of 5ppm/°C over the full temperature range of –55°C to +125°C.

The INA950-SEP closed-loop gain is set by a precision, low-drift internal resistor network. The ratio of these resistors are excellently matched, although the absolute values can vary significantly. TI does not recommend adding additional resistance around the INA950-SEP to change the effective gain because of this variation. Table 6-1 describes the typical values of the internal gain resistors seen in the functional diagram above.

Table 6-1. Fixed Gain Resistors

GAIN	R1	RL
20 (V/V)	25kΩ	500kΩ

6.4 Device Functional Modes

6.4.1 Unidirectional Operation

The INA950-SEP measures the differential voltage developed by current flowing through a resistor that is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*. Figure 6-3 shows that the INA950-SEP operates in unidirectional mode only, meaning the device only senses current sourced from a power supply to a system load.

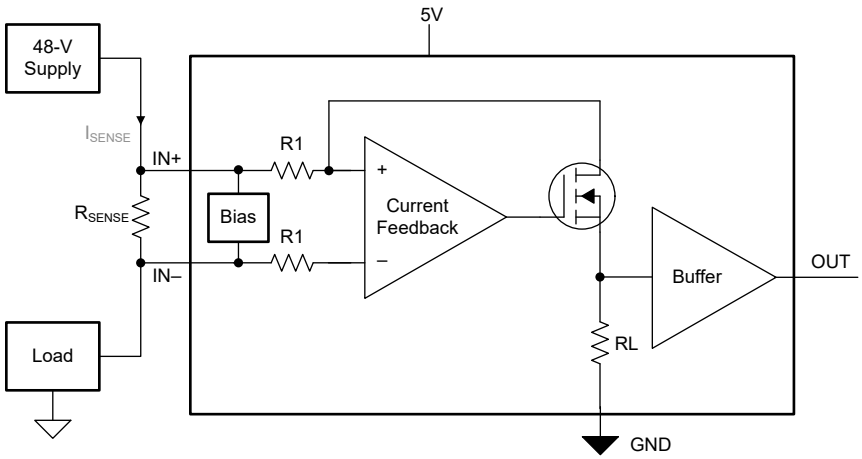


Figure 6-3. Unidirectional Application

The linear range of the output stage is limited to how close the output voltage can approach ground under zero-input conditions. The zero current output voltage of the INA950-SEP is very small, with a maximum of GND + 25mV. Apply a sense voltage of (25mV / Gain) or greater to keep the INA950-SEP output in the linear region of operation.

6.4.2 High Signal Throughput

With a bandwidth of 1.1MHz at a gain of 20V/V and a slew rate of 2V/µs, the INA950-SEP is specifically designed for detecting and protecting applications from fast inrush currents. As shown in Table 6-2, the INA950-SEP responds in less than 2µs for a system measuring a 75A threshold on a 2mΩ shunt.

Table 6-2. Response Time

PARAMETER		EQUATION	Value
V_S	Supply Voltage		5V
G	Gain		20V/V
I_{MAX}	Maximum current		100A
$I_{Threshold}$	Threshold current		75A
R_{SENSE}	Current sense resistor value		2mΩ
V_{OUT_MAX}	Output voltage at maximum current	$V_{OUT} = I_{MAX} \times R_{SENSE} \times G$	4V
V_{OUT_THR}	Output voltage at threshold current	$V_{OUT\_THR} = I_{THR} \times R_{SENSE} \times G$	3V
SR	Slew rate		2V/µs
	Output response time	$T_{response} = V_{OUT\_THR} / SR$	< 2µs

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The INA950-SEP amplifies the voltage developed across a current-sensing resistor as current flows through the resistor to the load. The wide input common-mode voltage range and high common-mode rejection of the INA950-SEP allows use over a wide range of voltage rails while still maintaining an accurate current measurement.

7.1.1 R_{SENSE} and Device Gain Selection

The accuracy of any current-sense amplifier is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. Equation 1 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (1)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that flows through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain results from the power-supply voltage, V_S, and device swing-to-rail limitations. To verify that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 2 provides the maximum values of R_{SENSE} and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \quad (2)$$

where:

- I_{MAX} is the maximum current that flows through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in this data sheet.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then selecting a lower gain device is possible to avoid positive swing limitations.

The negative swing limitation places a limit on how small the sense resistor value can be for a given application. Equation 3 provides the limit on the minimum value of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} \quad (3)$$

where:

- I_{MIN} is the minimum current that flows through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SN} is the negative output swing of the device.

Table 7-1 shows an example of the different results obtained from using five different gain versions of the INA950-SEP. From the table data, the highest gain device allows a smaller current-shunt resistor and decreased power dissipation in the element.

Table 7-1. R_{SENSE} Selection and Power Dissipation

PARAMETER(1)		EQUATION	RESULTS
V_S	Supply Voltage		5V
G	Gain		20V/V
V_{SENSE}	Ideal differential input voltage (Ignores swing limitation and power-supply variation.)	$V_{SENSE} = V_{OUT} / G$	250mV
R_{SENSE}	Current-sense resistor value	$R_{SENSE} = V_{SENSE} / I_{MAX}$	25mΩ
P_{SENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}2$	2.5 W

(1) Design example with 10A, full-scale current with maximum output voltage set to 5V.

7.1.2 Input Filtering

Note

Input filters are not required for accurate measurements using the INA950-SEP, and use of filters in this location is not recommended. If filter components are used on the input of the amplifier, follow the guidelines in this section to minimize the effects on performance.

Based strictly on user design requirements, external filtering of the current signal can be desired. The initial location that can be considered for the filter is at the output of the current-sense amplifier. Although placing the filter at the output satisfies the filtering requirements, this location changes the low output impedance measured by any circuitry connected to the output voltage pin. The other location for filter placement is at the current-sense amplifier input pins. This location also satisfies the filtering requirement, but the components must be carefully selected to minimally impact device performance. Figure 7-1 shows a filter placed at the input pins.

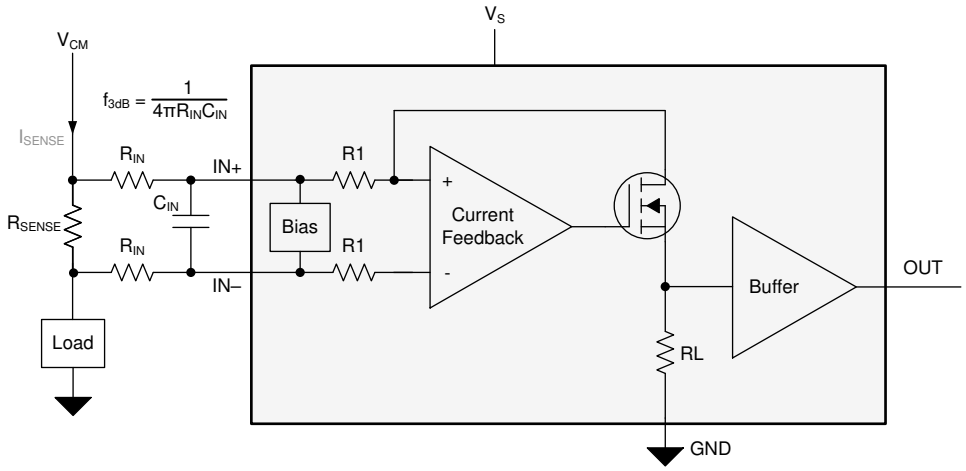


Figure 7-1. Filter at Input Pins

External series resistance provides a source of additional measurement error, so keep the value of these series resistors to 10Ω or less to reduce loss of accuracy. The internal bias network shown in Figure 7-1 creates a mismatch in input bias currents (see Section 5.6) when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, a mismatch is created in the voltage drop across the filter resistors. This voltage is a differential error voltage in the shunt resistor voltage. In addition to the

absolute resistor value, mismatch resulting from resistor tolerance can significantly impact the error because this value is calculated based on the actual measured resistance.

Use Equation 4 to calculate the measurement error expected from the additional external filter resistors, and use Equation 5 to calculate the gain error factor.

$$\text{Gain Error (\%)} = 100 \times (\text{Gain Error Factor} - 1) \quad (4)$$

$$\text{Gain Error Factor} = \frac{R_B \times R1}{(R_B \times R1) + (R_B \times R_{IN}) + (2 \times R_{IN} \times R1)} \quad (5)$$

Where:

- R_{IN} is the external filter resistance value.
- R1 is the INA950-SEP input resistance value specified in Table 6-1.
- R_B in the internal bias resistance, which is 6600Ω ± 20%.

The gain error factor, shown in Equation 4, can be calculated to determine the gain error introduced by the additional external series resistance. Equation 4 calculates the deviation of the shunt voltage, resulting from the attenuation and imbalance created by the added external filter resistance. Table 7-2 provides the gain error factor and gain error for several resistor values.

Table 7-2. Example Gain Error Factor and Gain Error for 10Ω External Filter Input Resistors

DEVICE (GAIN)	GAIN ERROR FACTOR	GAIN ERROR (%)
20	0.99658	–0.34185

7.2 Typical Application

The INA950-SEP is a unidirectional, current-sense amplifier capable of measuring currents through a resistive shunt with shunt common-mode voltages from 2.7V to 80V. Figure 7-2 shows the circuit configuration for monitoring current in a high-side radio frequency (RF) power amplifier (PA) application.

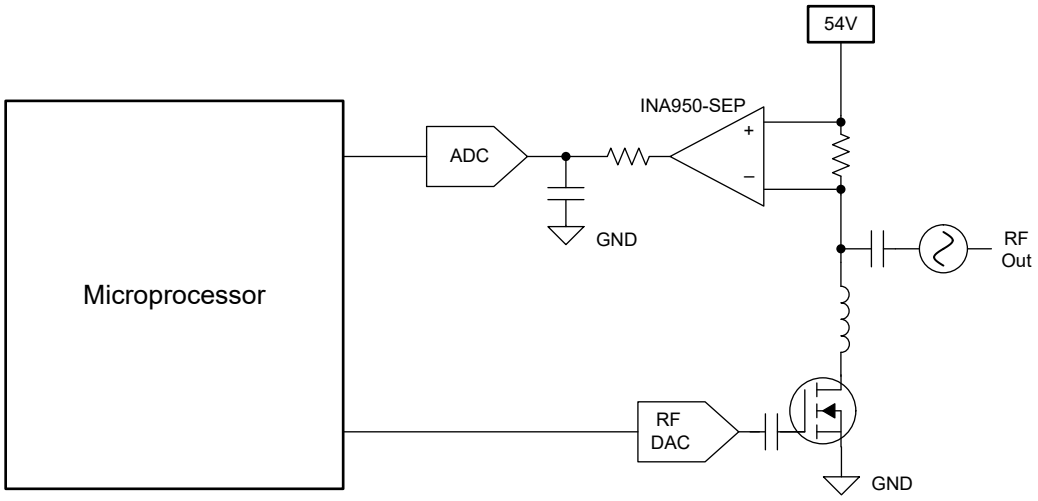


Figure 7-2. Current Sensing in a PA Application

7.2.1 Design Requirements

V_{SUPPLY} is set to 5V and the common-mode voltage set to 54V. Table 7-3 lists the design setup for this application.

Table 7-3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
INA950-SEP supply voltage	5V
High-side supply voltage	5V
Maximum sense current (I_{MAX})	5A
Gain option	20V/V

7.2.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based on the choice of gain, value of the maximum current to be sensed (I_{MAX}), and the power-supply voltage (V_S). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP}. Under the given design parameters, Equation 6 calculates the maximum value for R_{SENSE} as 48mΩ.

$$R_{SENSE} < \frac{V_{SP}}{I_{MAX} \times GAIN} \tag{6}$$

Although 45.3mΩ is less than the maximum value calculated, 45.3mΩ is selected for this design example because this value is still large enough to provide an adequate signal at the current-sense amplifier output and is a standard 1% value.

7.2.2.1 Overload Recovery With Negative V_{SENSE}

The INA950-SEP is a unidirectional current-sense amplifier that is meant to operate with a positive differential input voltage (V_{SENSE}). If negative V_{SENSE} is applied, the device is placed in an overload condition and requires time to recover when V_{SENSE} returns positive. The required overload recovery time increases with more negative V_{SENSE}.

7.2.3 Application Curve

Figure 7-3 shows the output response of the device to a high-frequency sinusoidal current.

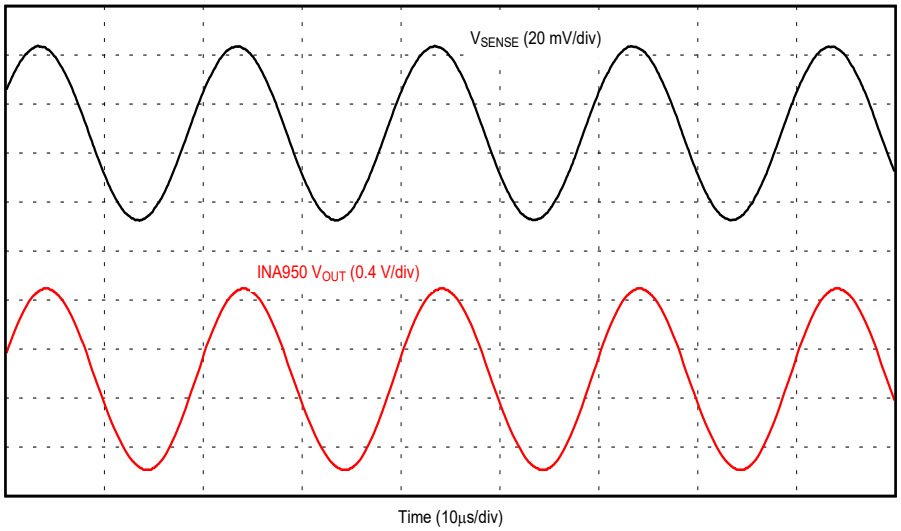


Figure 7-3. INA950-SEP Output Response

7.3 Power Supply Recommendations

The input circuitry of the INA950-SEP can accurately measure beyond the power-supply voltage. The power supply can be 5.5V, whereas the load power-supply voltage at IN+ and IN– can go up to 80V. The output voltage range of the OUT pin is limited by the voltage on the VS pin and the device swing to the supply specification.

7.4 Layout

7.4.1 Layout Guidelines

TI always recommends to follow good layout practices:

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close to the device power supply and ground pins as possible. The recommended value of this bypass capacitor is 0.1µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current-sense resistor to the device, keep the trace lengths as short as possible.

7.4.2 Layout Examples

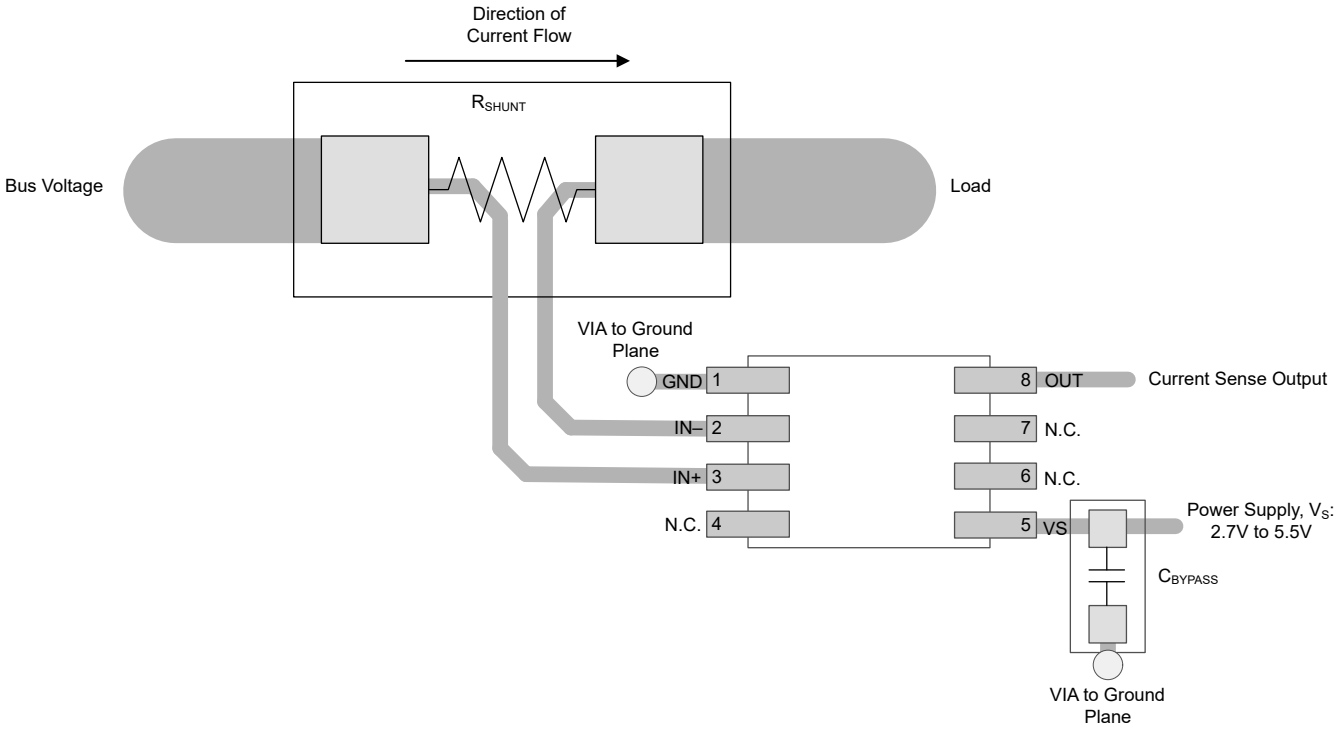


Figure 7-4. Recommended Layout for the INA950-SEP

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *INA950-SEP Production Flow and Reliability Report* radiation report
- Texas Instruments, *INA950-SEP Total Ionizing Dose (TID) Report* radiation report
- Texas Instruments, *INA950-SEP Single-Event Effects (SEE) Radiation Test Report* radiation report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

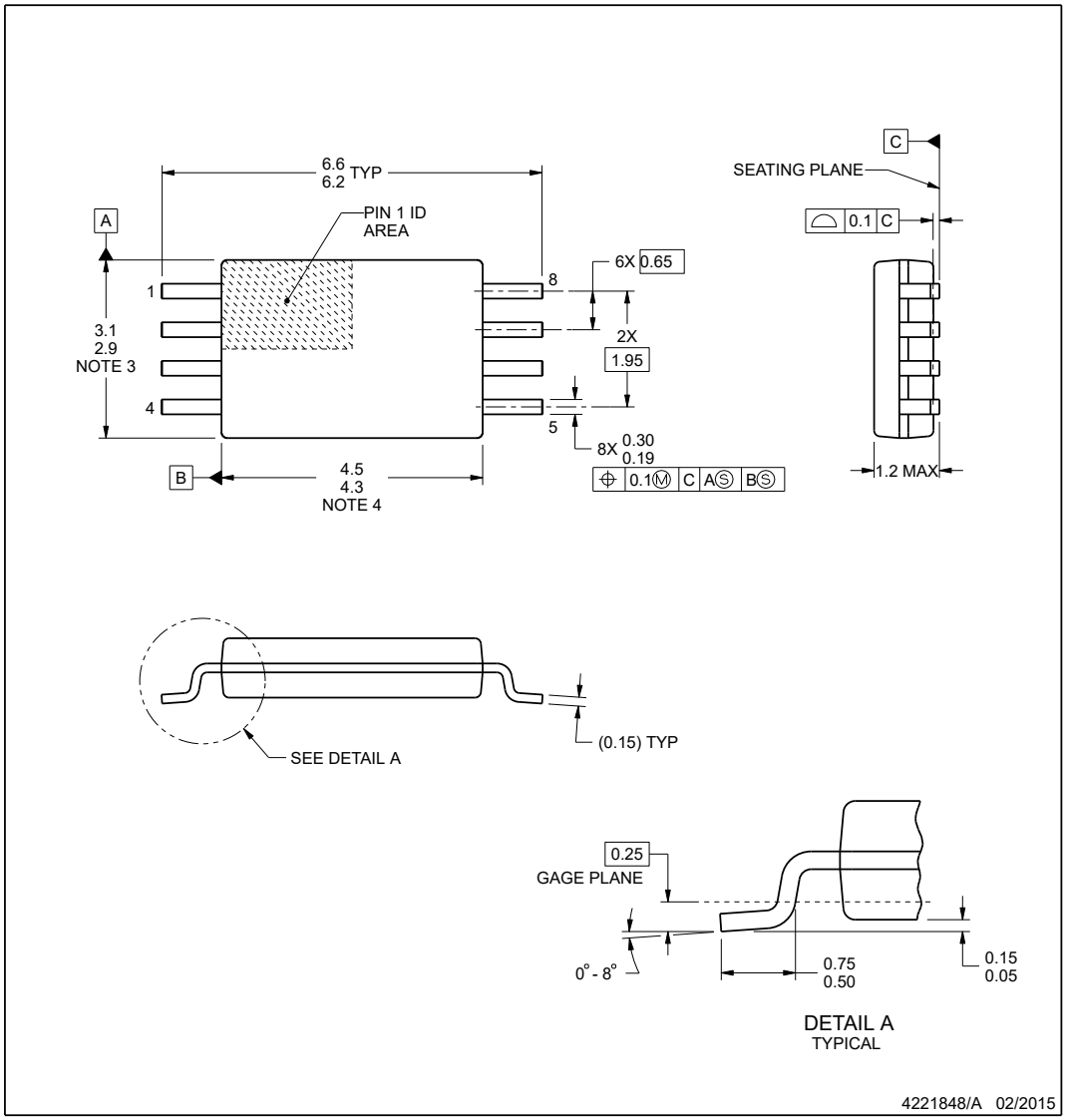
10.1 Mechanical Data

PW0008A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



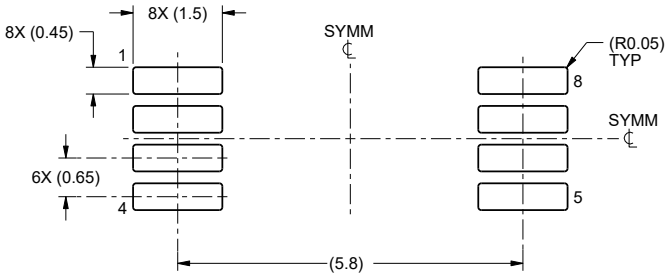
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

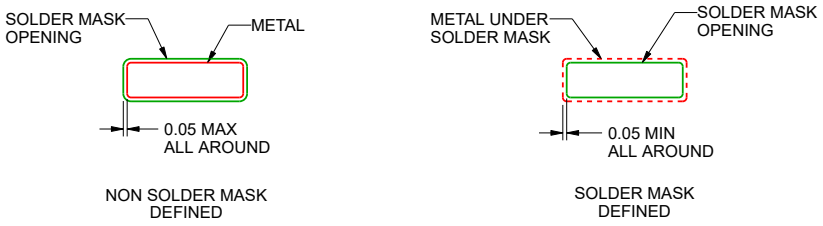
EXAMPLE BOARD LAYOUT

PW0008A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

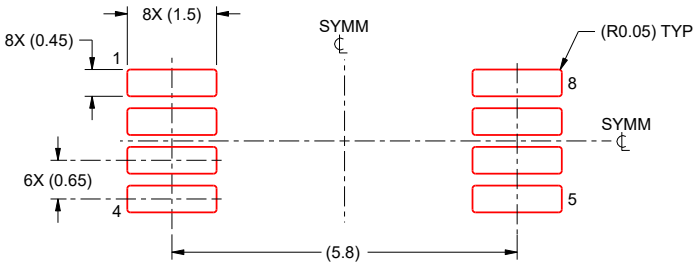
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead finish/ Ball material(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
NA950A1MPW TSEP	PRE_PROD	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-3-260C-1 68 HR	-55°C - 125°C	950SEP

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

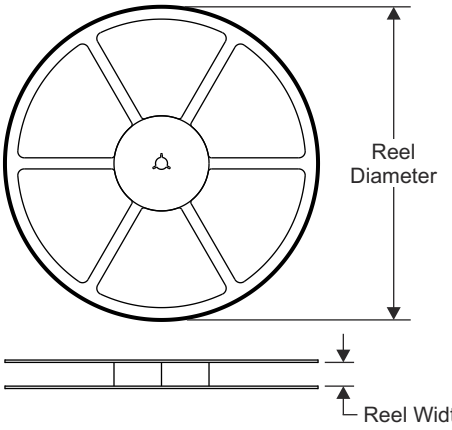
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

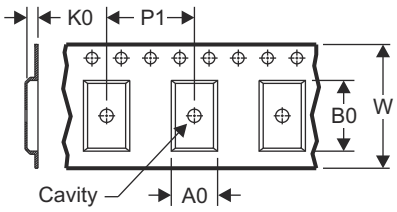
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

10.2 Tape and Reel Information

REEL DIMENSIONS

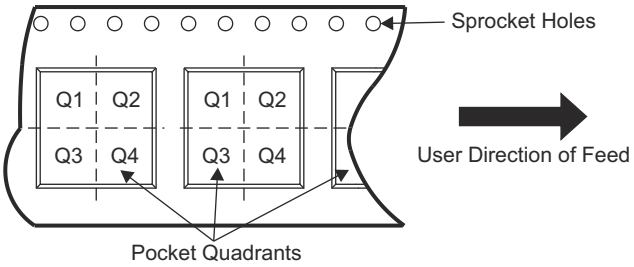


TAPE DIMENSIONS



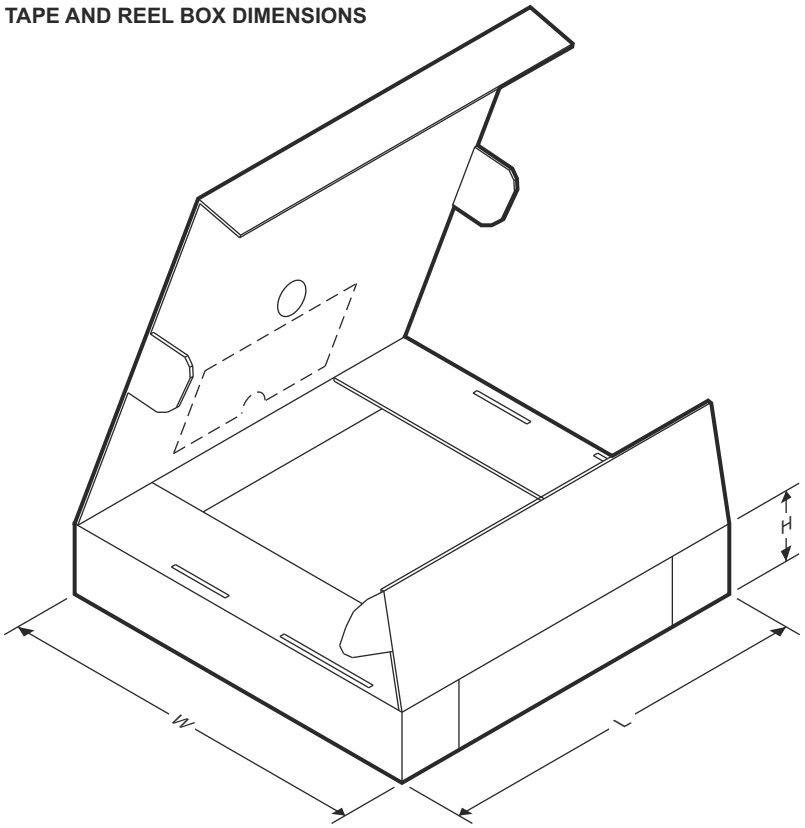
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA950A1MPWTSEP	TSSOP	PW	8	250	180	12.4	7	3.6	1.6	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NA950A1MPWTSEP	TSSOP	PW	8	250	210	185	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA950A1MPWTSEP	ACTIVE	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	950SEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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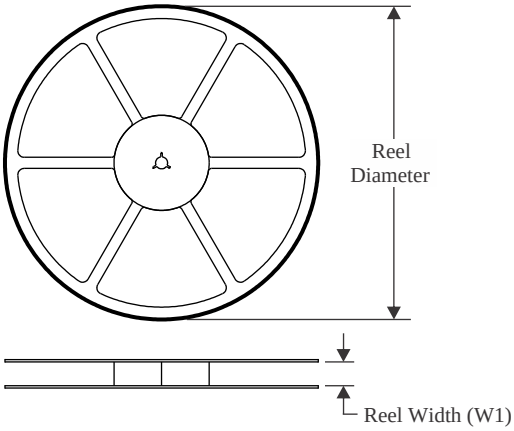
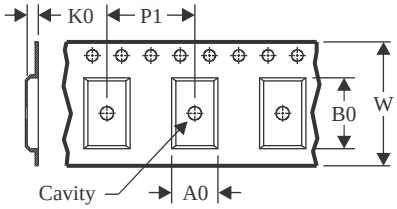
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
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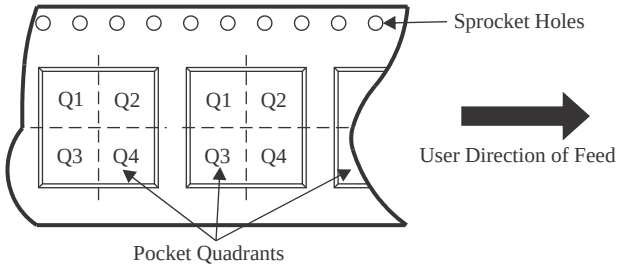
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

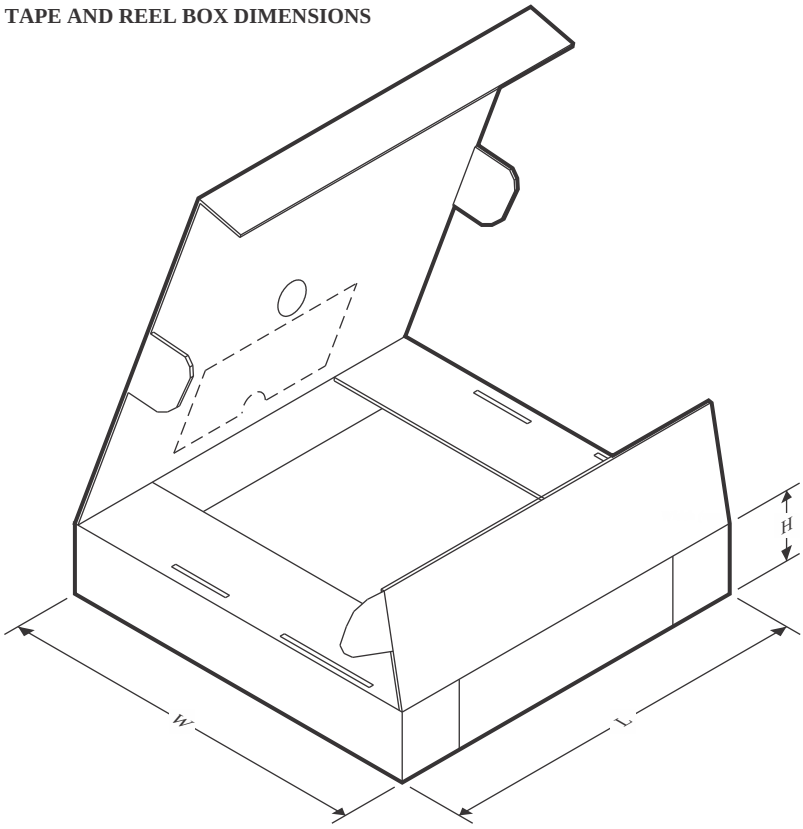
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA950A1MPWTSEP	TSSOP	PW	8	250	180.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

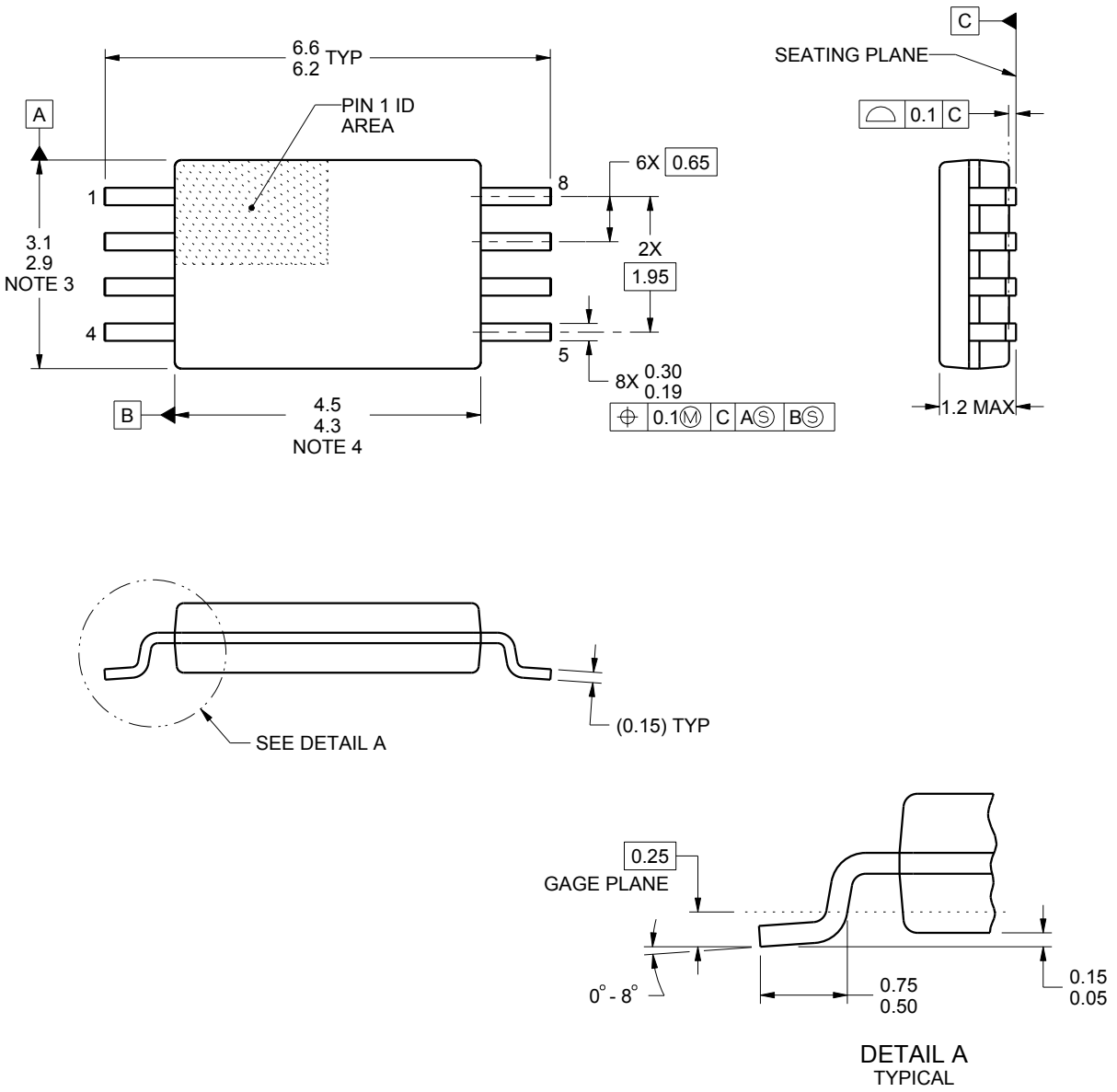
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA950A1MPWTSEP	TSSOP	PW	8	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0008A

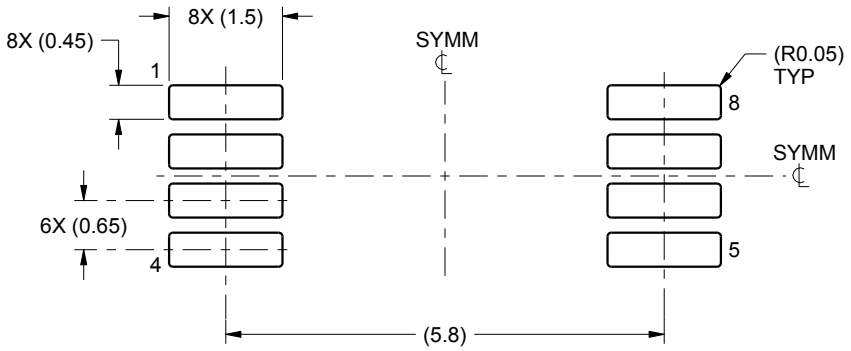
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

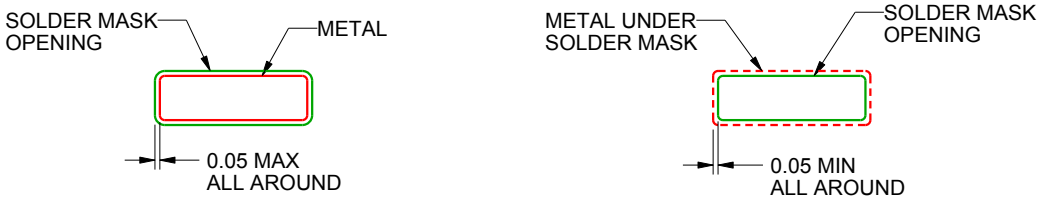


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

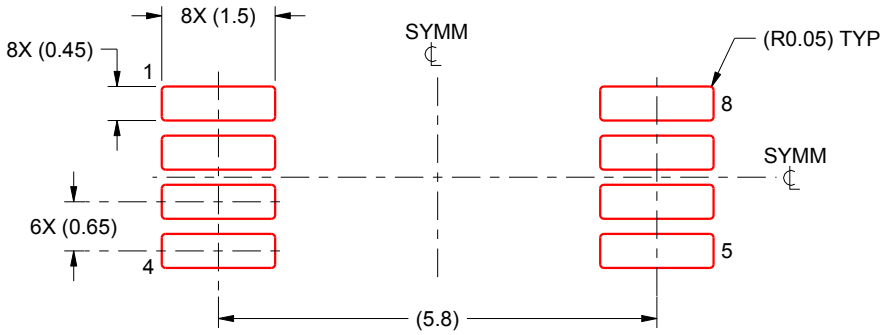


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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