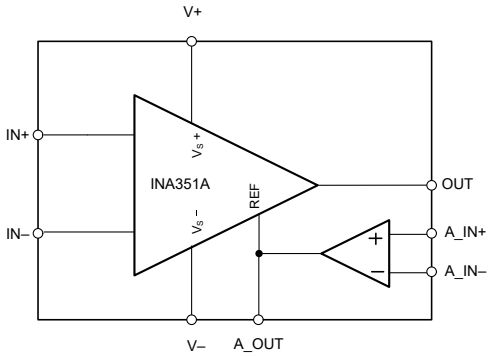
INA351A - Low Power, 1.8-V to 5.5-V Small-Size Instrumentation Amplifier with Configurable Reference Amplifier

1 Features

- Fixed gain of 10V/V instrumentation amp with configurable reference amp
- INA performance for 10-bit to 14-bit systems
  - CMRR: 95 dB (typical)
  - Gain error: 0.015% (typical)
  - Bandwidth: 100 kHz (typical)
- Reference amp can be used for:
  - External DC error calibration with servo loop
  - Providing buffered voltage of external circuits
  - Filtering or adjustment of reference voltage
- Ultra-small package option (2mm x 2mm)
- Drives 1 nF with under 10% overshoot (typical)
- Optimized quiescent current: 110 µA (typical)
- Supply range: 1.8 V (±0.9 V) to 5.5 V (±2.75 V)
- Specified temperature range: –40°C to 125°C

2 Applications

- Electrocardiogram
- Pressure transmitter
- Weigh scale
- Flow transmitter
- Wearable fitness and activity monitor
- Blood glucose monitor
- Temperature sensing with RTD



Simplified Internal Schematic

3 Description

INA351A is a fixed gain of 10 instrumentation amplifier with a configurable reference amplifier in a small package. This instrumentation amp (INA) is built with precision-matched resistors to achieve excellent CMRR and gain error performance in a small, low-cost form factor. This makes INA351A a great solution to replace discrete INA implementations to achieve higher performance and more compact designs with minimal impact to bill of materials (BOM) costs.

The integrated, configurable reference amplifier can be used as a buffer for external use or as part of a closed-loop calibration circuit to achieve better DC precision. The closed-loop calibration can be accomplished by implementing a servo loop amplifier to calibrate DC errors from sensors (like offset, offset drift and so forth) at the INA output when the INA input signal is at a slightly higher frequency than DC depending on the application.

INA351A achieves 86 dB of minimum CMRR, an accurate 0.1% of maximum gain error and only consumes a maximum of 135 µA quiescent current at room temperature. The INA can directly drive sub-1 kHz, 10-bit to 14-bit, delta-sigma analog-to-digital converters (ADC) without an ADC driver, making it a great choice for portable, battery-powered medical applications like electrocardiograms or wearable health monitors.

Package Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
INA351A	DSG (WSON, 8)	2 mm × 2 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See *Device Comparison* table.

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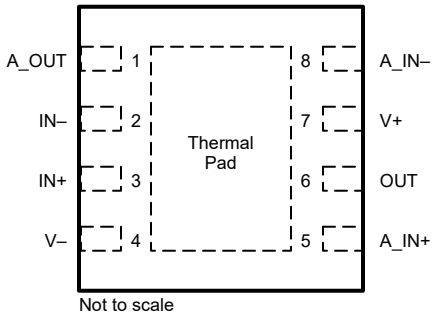
4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial Release

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS
		WSON DSG
INA351A	1	8

6 Pin Configuration and Functions



Note: Connect Thermal Pad to (V−)

Figure 6-1. DSG Package, 8-Pin WSON With Exposed Thermal Pad (Top View)

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN–	2	I	Instrumentation amplifier negative (inverting) input
IN+	3	I	Instrumentation amplifier positive (non-inverting) input
OUT	6	O	Instrumentation amplifier output
A_IN+	5	I	Reference amplifier positive (non-inverting) input. This pin usually connects to a reference voltage externally.
A_OUT	1	O	Reference amplifier output. This is connected internally to the 60 kΩ resistor of the INA which is also called as REF node.
A_IN–	8	I	Reference amplifier negative (inverting) input.
V–	4	—	Negative supply
V+	7	—	Positive supply

(1) I = input, O = output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6	V
Signal input pins	Common mode voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(2)	–10	10	mA
Output short-circuit(4)		Continuous		
Operating Temperature, T_A		–55	150	°C
Junction Temperature, T_J			150	
Storage Temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less
(3) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.
(4) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S = (V+) – (V–)	Single-supply	1.8	5.5	V
	Dual-supply	±0.9	±2.75	
Input Voltage Range		(V–)	(V+)	V
Specified temperature	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA351A DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, V_{A_IN+} = V_S / 2, $V_{A\_IN–}$ = V_{A_OUT}, G = 10, R_L = 10 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Offset Voltage, RTI[1]	V_S = 5.5 V	T_A = 25°C		±0.2	±1.3	mV
	Offset Voltage over T, RTI[1]	V_S = 5.5 V	T_A = –40°C to 125°C			±1.4	mV
	Offset temp drift, RTI[2]	V_S = 5.5 V	T_A = –40°C to 125°C		±0.60		µV/°C
PSRR	Power-supply rejection ratio		T_A = 25°C		20	75	µV/V
Z_{IN-DM}	Differential Impedance				100 || 5		GΩ || pF
Z_{IN-CM}	Common Mode Impedance				100 || 9		GΩ || pF
V_{CM}	Input Stage Common Mode Range[3]			(V–)		(V+)	V
CMRR DC	Common-mode rejection ratio, RTI	V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 5.5 V	86	103		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 3.3 V		94		
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	V_S = 5.5 V	62	75		
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			±0.75		pA
I_{OS}	Input offset current	V_{CM} = V_S / 2			±0.40		pA
NOISE VOLTAGE							
e_{NI}	Input referred voltage noise density[5]	f = 1 kHz			36		nV/√Hz
		f = 10 kHz			35		
E_{NI}	Input referred voltage noise[5]	f_B = 0.1 Hz to 10 Hz			3.0		$µV_{PP}$
i_n	Input current noise	f = 1 kHz			22		fA/√Hz
GAIN							
GE	Gain error[4]	V_{REF} = V_S/2	V_O = (V–) + 0.1 V to (V+) – 0.1V		±0.02	±0.10	%
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
V_{OL}	Negative rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
C_L Drive	Load capacitance drive	V_O = 100 mV step, Overshoot < 20%			500		pF
Z_O	Closed-loop output impedance	f = 10 kHz			51		Ω
I_{SC}	Short-circuit current	V_S = 5.5 V			±20		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	V_{IN} = 10 mV_{pk-pk}			100		kHz
THD + N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, R_L = 100 kΩ f = 1 kHz, 80-kHz measurement BW			0.035		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V_{IN_EMIRR} = 100 mV			96		dB
SR	Slew rate	V_S = 5 V, V_O = 2 V step			0.20		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			14		µs
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			24		
	Overload recovery	V_{IN} = 1 V			8		µs
REFERENCE AMPLIFIER							
REF - V_{OS}	Ref. input offset voltage	V_S = 5.5 V[4]			±0.6	±2.25	mV
REF - V_{OS}	Ref. input offset voltage drift	V_S = 5.5 V			±0.8		µV/°C

7.5 Electrical Characteristics (continued)

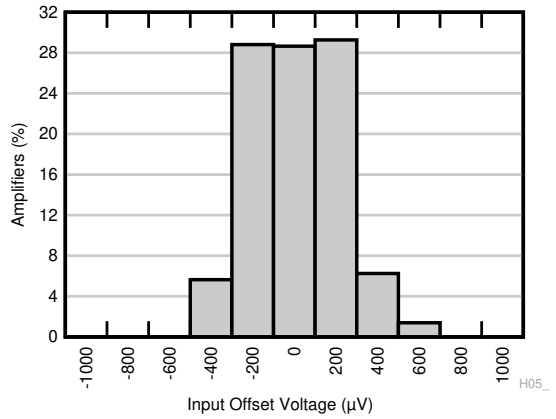
For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, V_{A_IN+} = V_S / 2, $V_{A\_IN–}$ = V_{A_OUT}, G = 10, R_L = 10 kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF - I_B	Ref. input bias current	V_S = 5.5 V			±1		pA
REF - Z_{INCM}	Ref. common mode input impedance				100 || 0.5		GΩ || pF
REF - E_N	Ref. input voltage noise	f = 0.1 to 10 Hz			8.7		μV_{PP}
REF - e_N	Ref. input voltage noise density	f = 10 kHz			64		nV/√Hz
REF - V_{IN}	Ref. input voltage range	V_S = 5.5 V		(V–)		(V+)	V
REF - A_{OL}	Ref. open loop voltage gain	(V–) + 0.1 V < V_O < (V+) – 0.1 V	V_S = 5.5 V		120		dB
REF - GBW	Ref. gain-bandwidth product	V_S = 5.5 V			360		kHz
REF - t_S	Ref. settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = 1, C_L = 10 pF			25		µs
REF - PM	Ref. phase margin	V_S = 5.5 V, G = 1, C_L = 10 pF			65		°
REF - V_O	Ref. voltage output swing from rail	V_S = 5.5 V, G = 1				175	mV
REF - I_{SC}	Ref. short circuit current	V_S = 5.5 V, G = 1		±3			mA
POWER SUPPLY							
V_S	Power-supply voltage	Single-supply		1.8		5.5	V
		Dual-supply		±0.85		±2.75	
I_Q	Quiescent current	V_{IN} = 0 V			110	135	µA
		T_A = –40°C to 125°C				147	

(1) Total offset, referred-to-input (RTI): V_{OS} = (V_{OSI}) + (V_{OSO} / G).
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Input common mode voltage range of the just the input stage of the instrumentation amplifier. The entire INA351 input range depends on the combination input common-mode voltage, differential voltage, gain, A_OUT voltage and power supply voltage. *Typical Characteristic* curves will be added with more information.
(4) Min and Max values are specified by characterization.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$

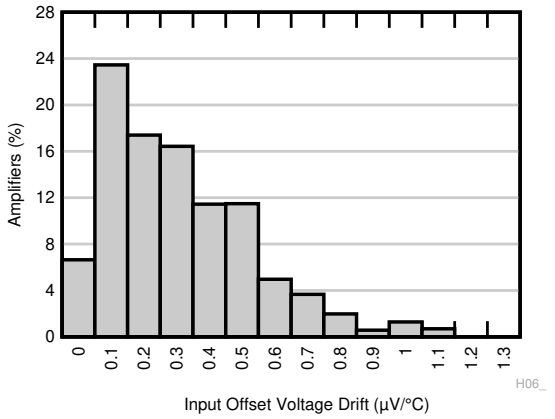
7.6 Typical Characteristics

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)



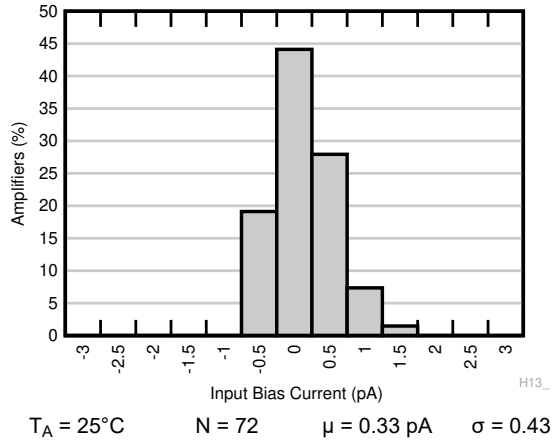
N = 36 µ = 23 µV σ = 0.180 mV

Figure 7-1. Typical Distribution of Input Referred Offset Voltage



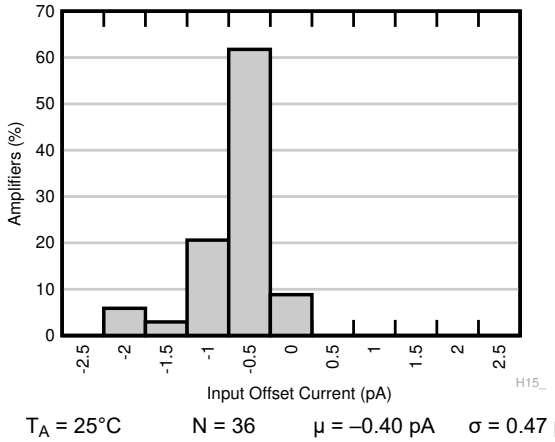
N = 36 µ = 0.23 µV/°C σ = 0.36 µV/°C

Figure 7-2. Typical Distribution of Input Referred Offset Drift



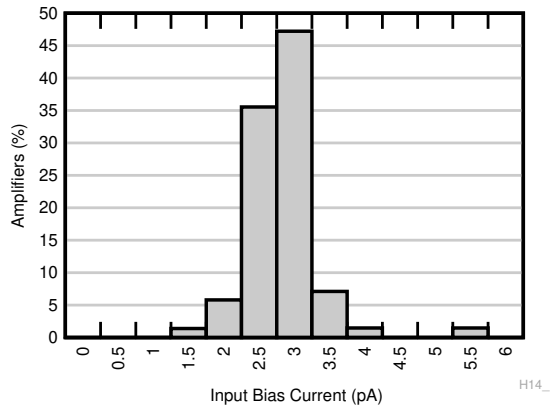
T_A = 25°C N = 72 µ = 0.33 pA σ = 0.43 pA

Figure 7-3. Typical Distribution of Input Bias Current



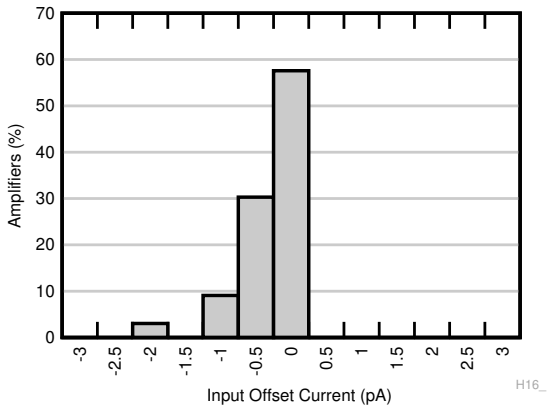
T_A = 25°C N = 36 µ = –0.40 pA σ = 0.47 pA

Figure 7-4. Typical Distribution of Input Offset Current



T_A = 85°C N = 72 µ = 3.3 pA σ = 0.53 pA

Figure 7-5. Typical Distribution of Input Bias Current

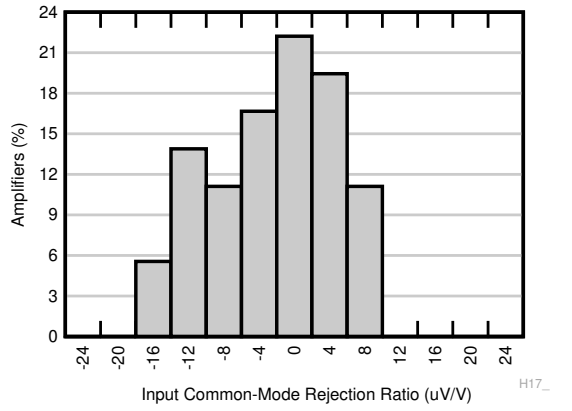


T_A = 85°C N = 36 µ = 0.05 pA σ = 0.30 pA

Figure 7-6. Typical Distribution of Input Offset Current

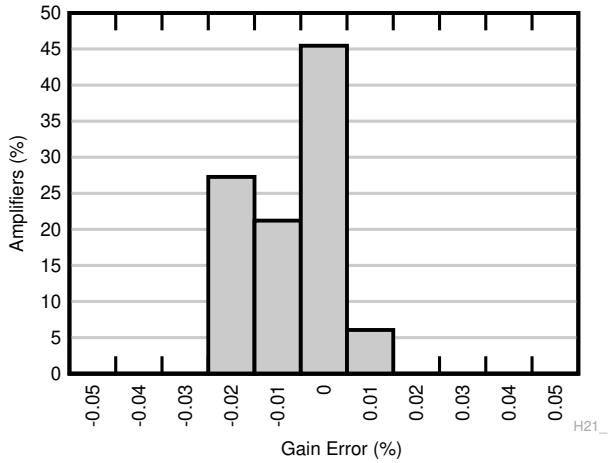
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)



N = 36 μ = -0.30 μV/V σ = 7.10 μV/V

Figure 7-7. Typical Distribution of CMRR



N = 36 μ = 0.002 % σ = 0.02 %

Figure 7-8. Typical Distribution of Gain Error

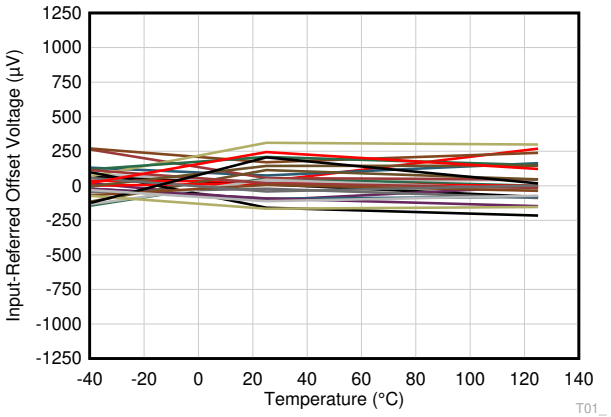


Figure 7-9. Input Referred Offset Voltage vs Temperature

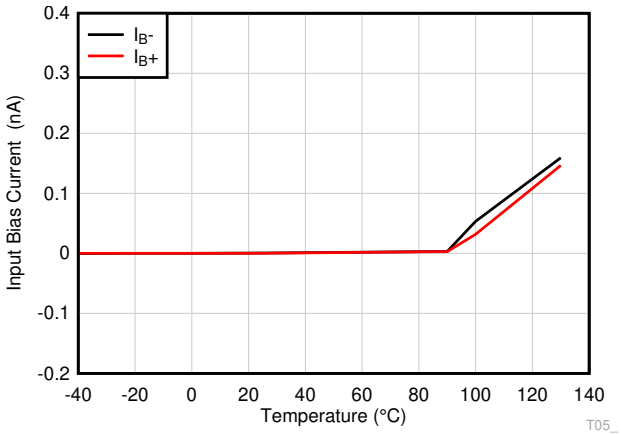


Figure 7-10. Input Bias Current vs Temperature

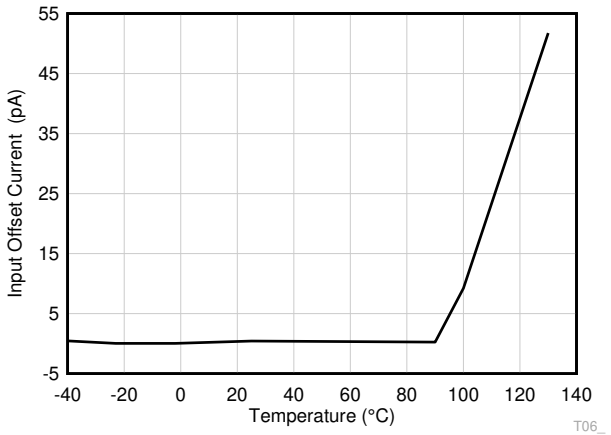


Figure 7-11. Input Offset Current vs Temperature

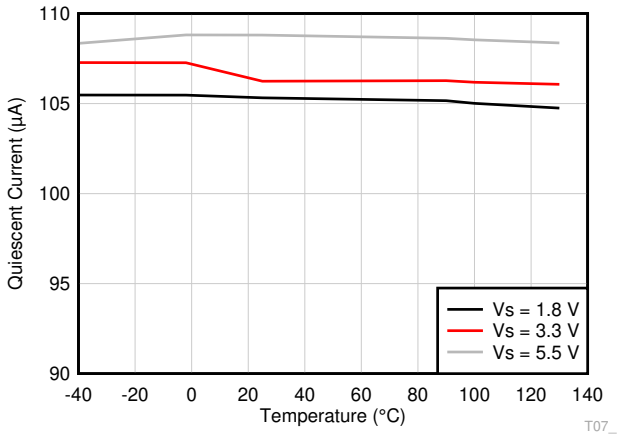


Figure 7-12. Quiescent Current vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)

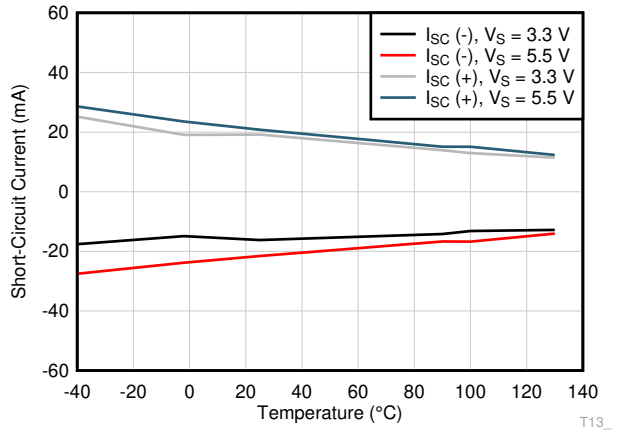


Figure 7-13. Short Circuit Current vs Temperature

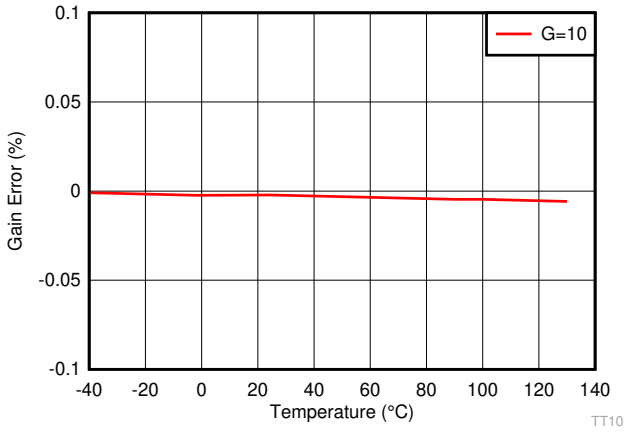


Figure 7-14. Gain Error vs Temperature

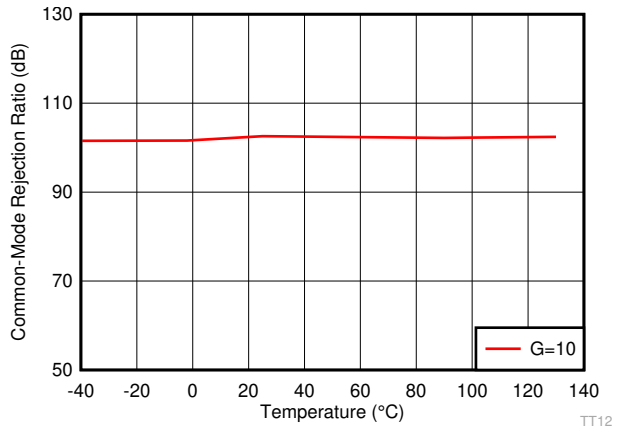
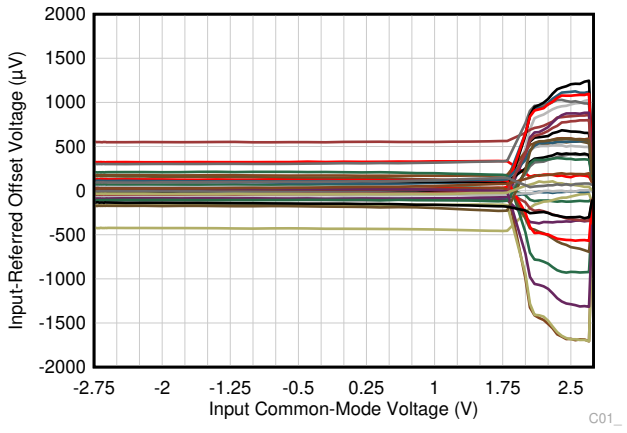
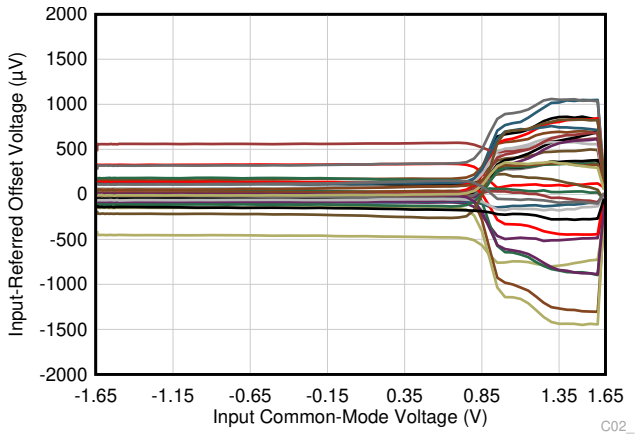


Figure 7-15. CMRR vs Temperature



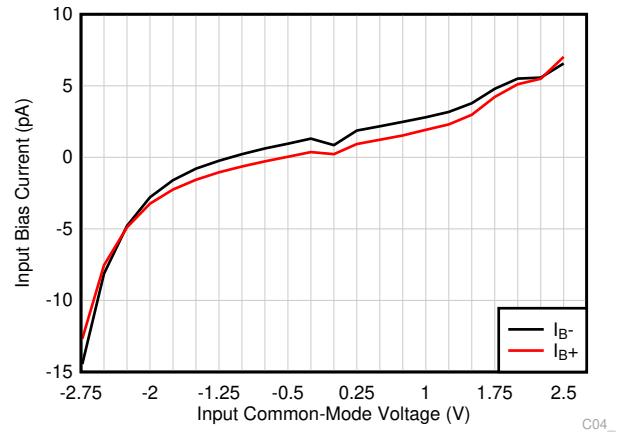
V+ = 2.75 V and V– = –2.75 V

Figure 7-16. Input Referred Offset Voltage vs Input Common-Mode Voltage



V+ = 1.65 V and V– = –1.65 V

Figure 7-17. Input Referred Offset Voltage vs Input Common-Mode Voltage

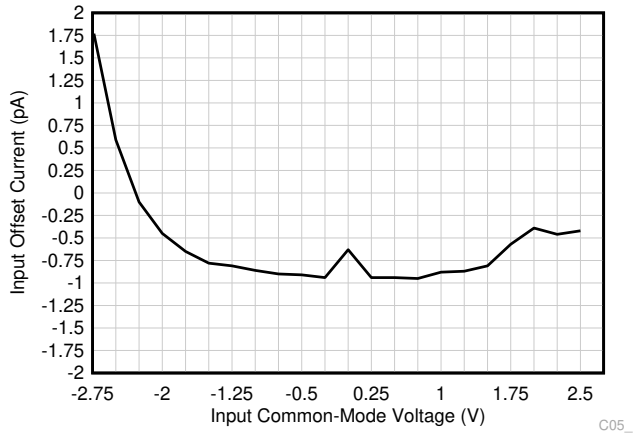


V+ = 2.75 V and V– = –2.75 V

Figure 7-18. Input Bias Current vs Input Common-Mode Voltage

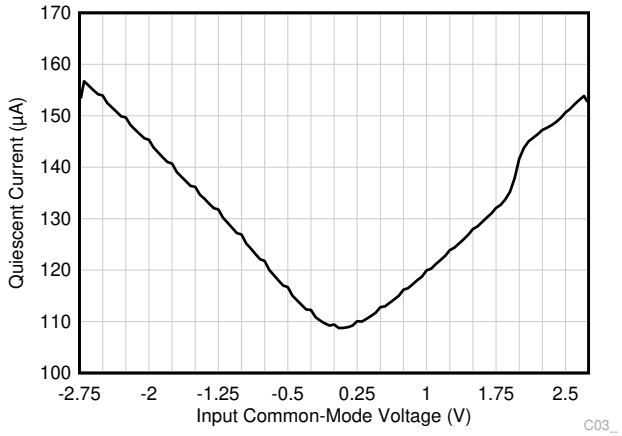
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)



V+ = 2.75 V and V– = –2.75 V

Figure 7-19. Input Offset Current vs Input Common-Mode Voltage



V+ = 2.75 V and V– = –2.75 V

Figure 7-20. Quiescent Current vs Input Common-Mode Voltage

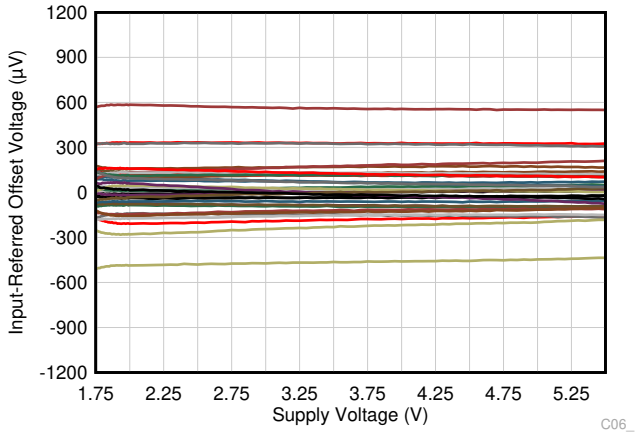


Figure 7-21. Input Referred Offset Voltage vs Supply Voltage

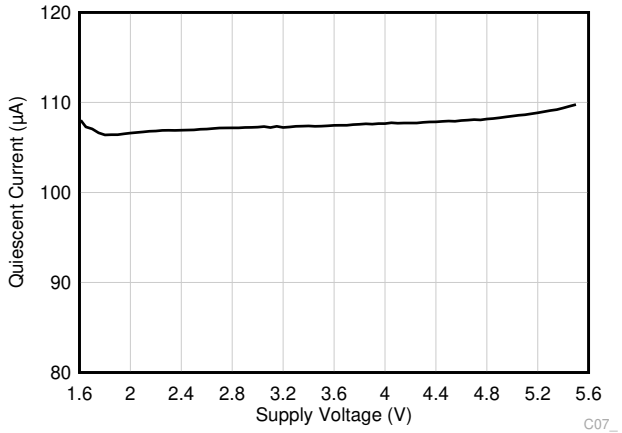


Figure 7-22. Quiescent Current vs Supply Voltage

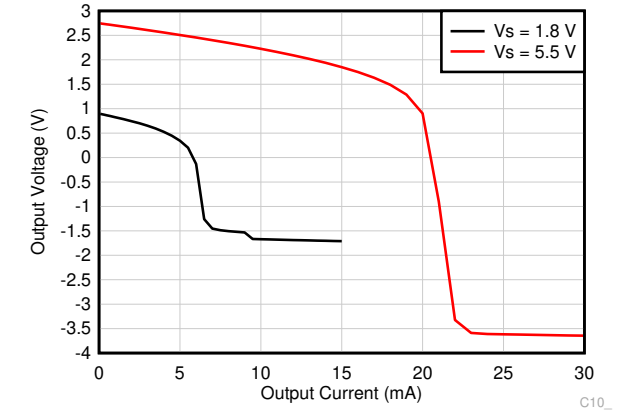


Figure 7-23. Output Voltage vs Output Current (Sourcing)

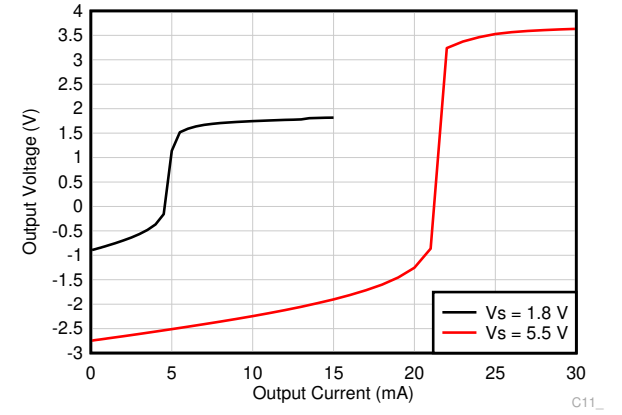


Figure 7-24. Output Voltage vs Output Current (Sinking)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)

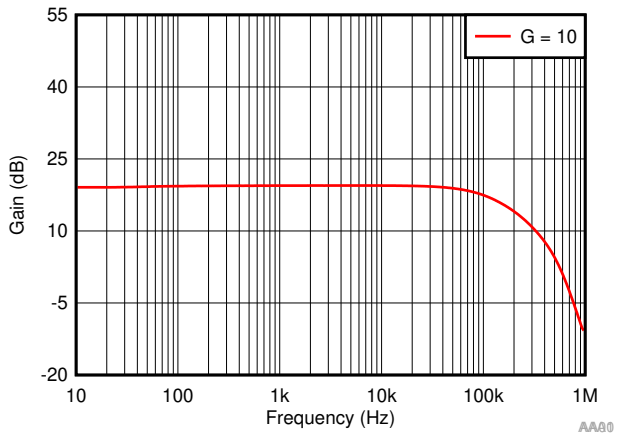


Figure 7-25. Closed-Loop Gain vs Frequency

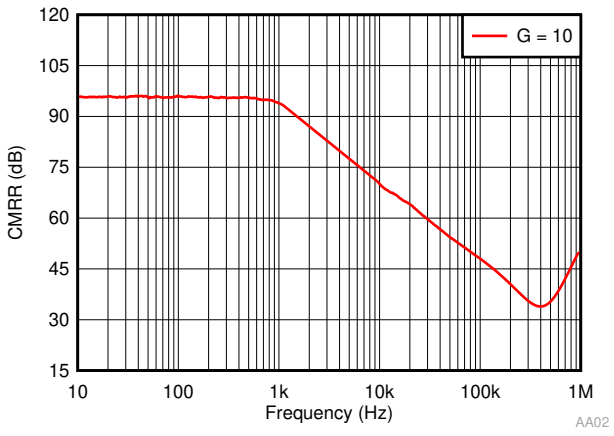


Figure 7-26. CMRR (Referred to Input) vs Frequency

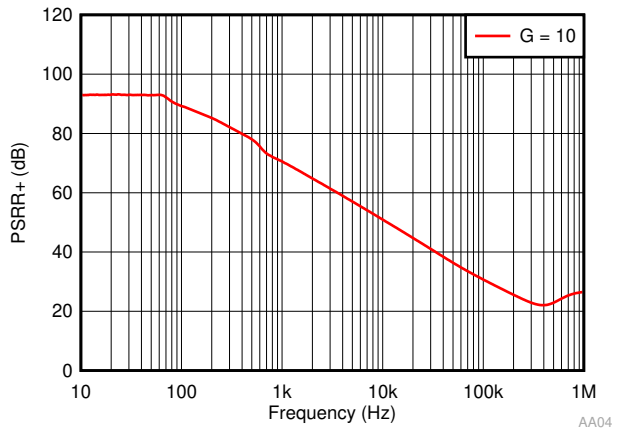


Figure 7-27. PSRR+ (Referred to Input) vs Frequency

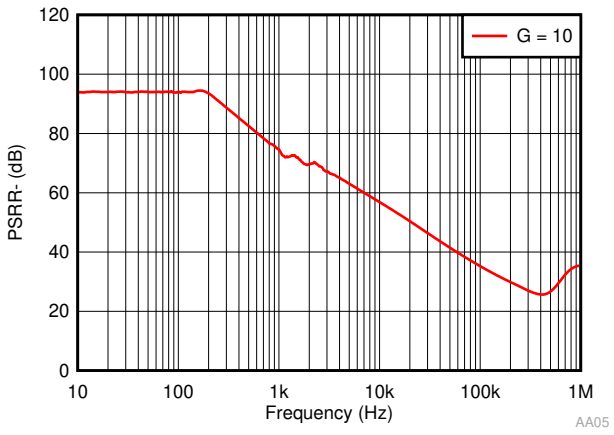


Figure 7-28. PSRR– (Referred to Input) Vs Frequency

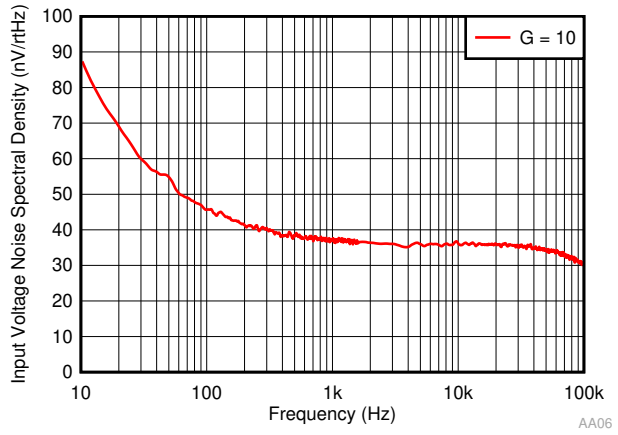


Figure 7-29. Input Referred Voltage Noise Spectral Density

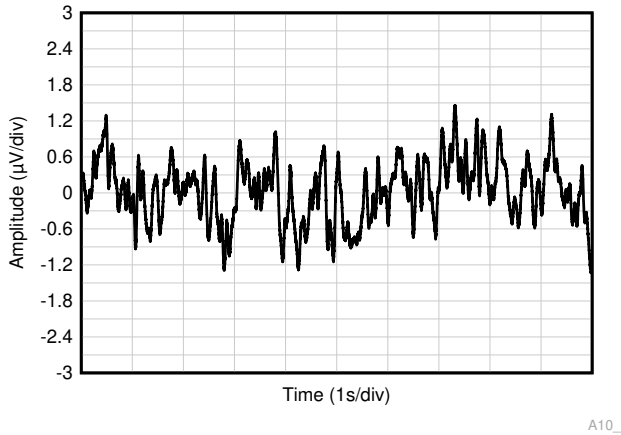


Figure 7-30. 0.1 Hz to 10 Hz Voltage Noise in Time Domain

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)

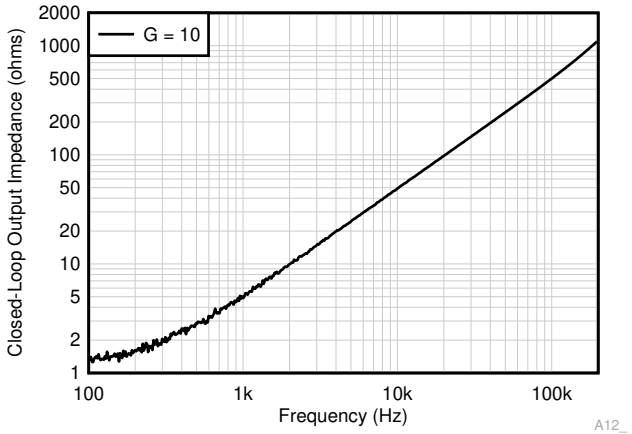


Figure 7-31. Closed-Loop Output Impedance vs Frequency

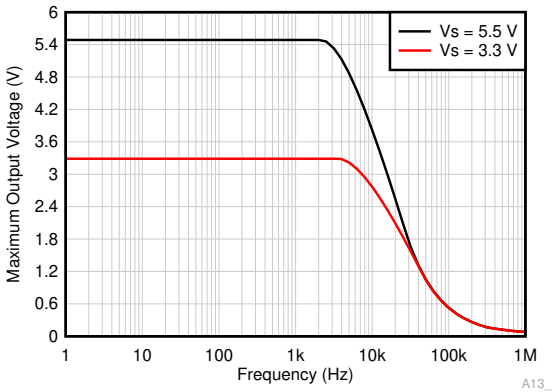
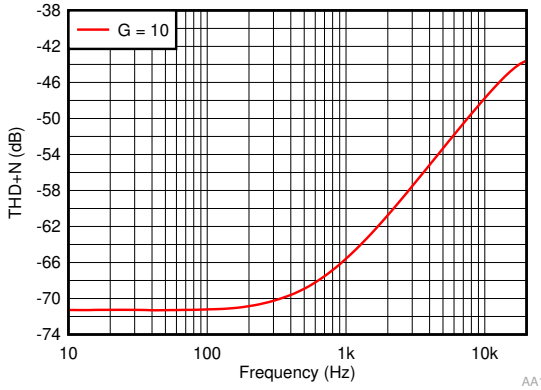
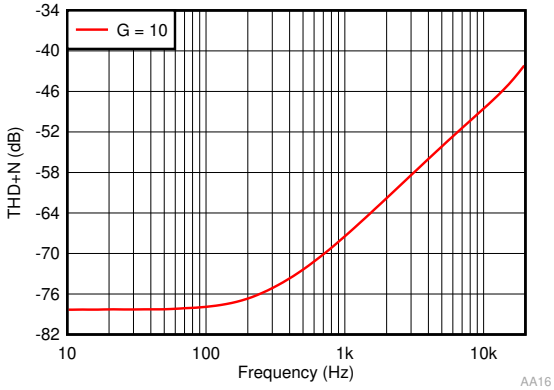


Figure 7-32. Maximum Output Voltage vs Frequency



V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 10 kΩ V_{OUT} = 0.5 V_{RMS}

Figure 7-33. THD + N Frequency



V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 100 kΩ V_{OUT} = 1 V_{RMS}

Figure 7-34. THD + N Frequency

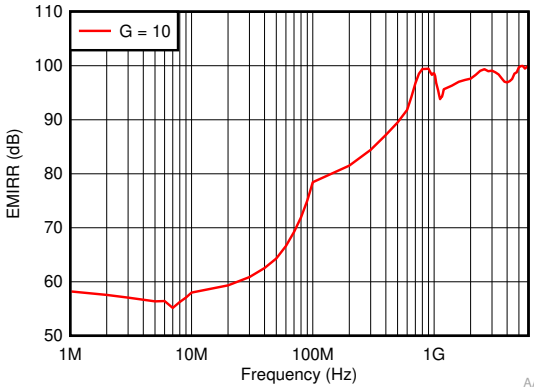
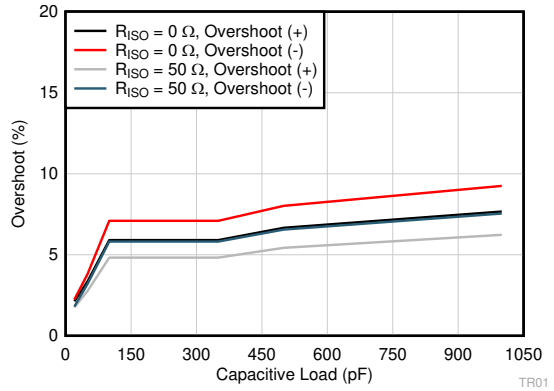


Figure 7-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

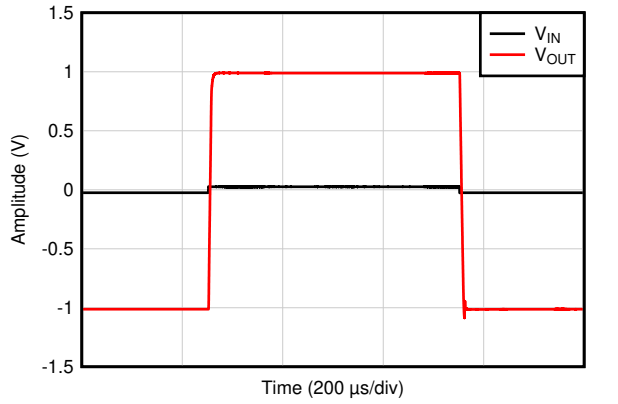


V_S = 5.5 V V_{OUT} = 100 mV_{PP}

Figure 7-36. Small-Signal Overshoot vs Capacitive Load

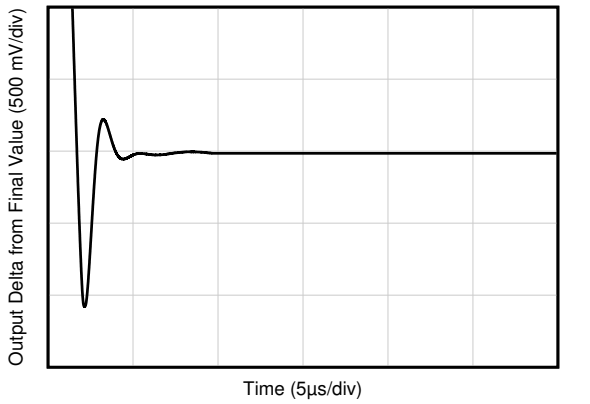
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)



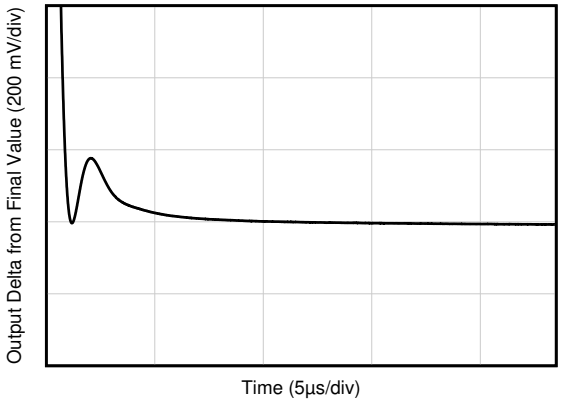
V+ = 2.75 V V– = –2.75 V V_{OUT} = 2 V_{PP}

Figure 7-37. Large Signal Step Response



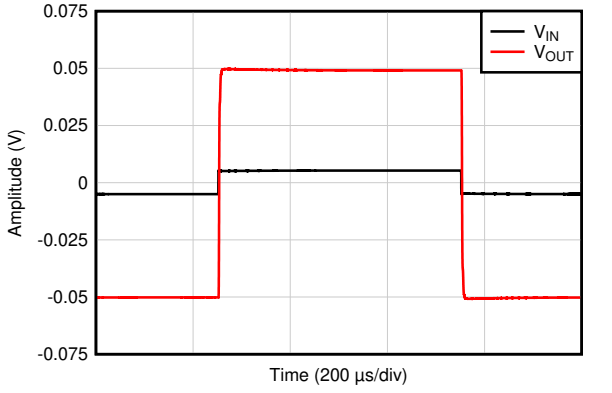
V+ = 2.75 V V– = –2.75 V V_{OUT} = 2 V_{PP}

Figure 7-38. Large Signal Settling Time (Falling Edge)



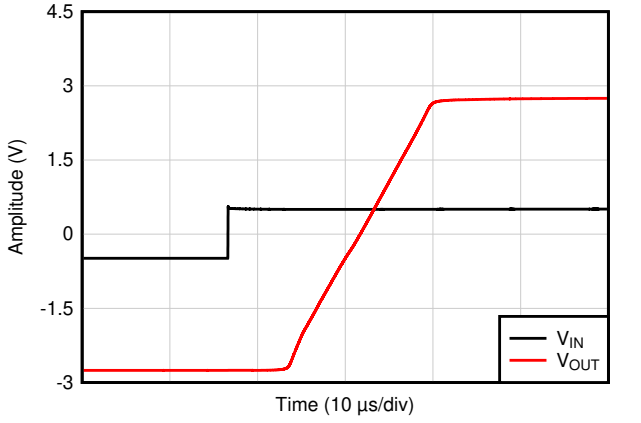
V+ = 2.75 V V– = –2.75 V V_{OUT} = 2 V_{PP}

Figure 7-39. Large Signal Settling Time (Rising Edge)



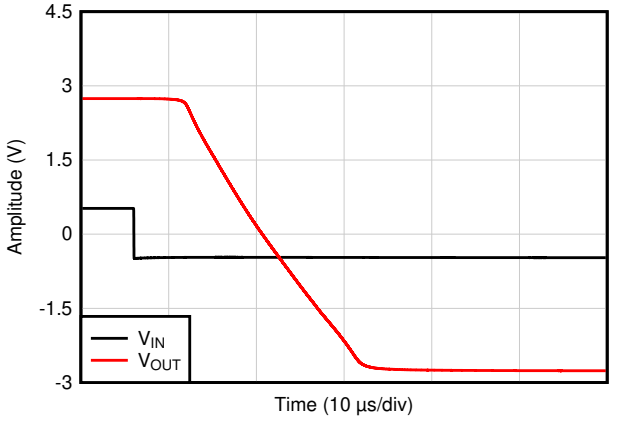
V+ = 2.75 V V– = –2.75 V V_{OUT} = 0.1 V_{PP}

Figure 7-40. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V V_{IN} = 1 V_{PP}

Figure 7-41. Over-Load Recovery (Rising Edge)

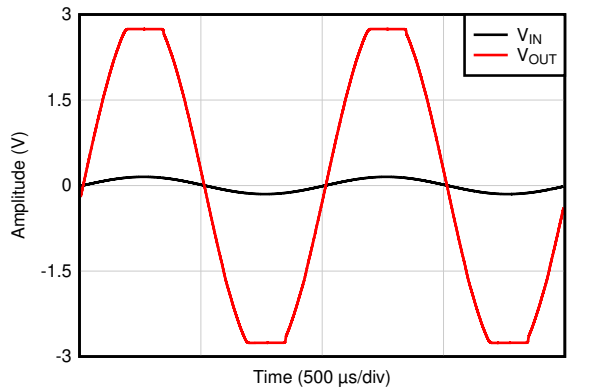


V+ = 2.75 V V– = –2.75 V V_{IN} = 1 V_{PP}

Figure 7-42. Over-Load Recovery (Falling Edge)

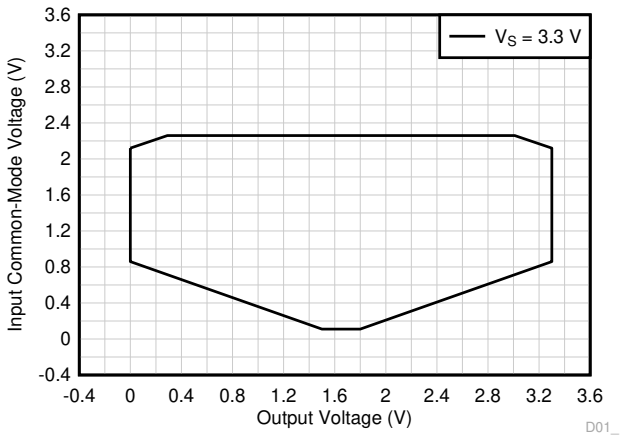
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2, V_{A_IN+} = V_S / 2, V_{A_OUT} = V_{A_IN-} and G = 10 (unless otherwise noted)



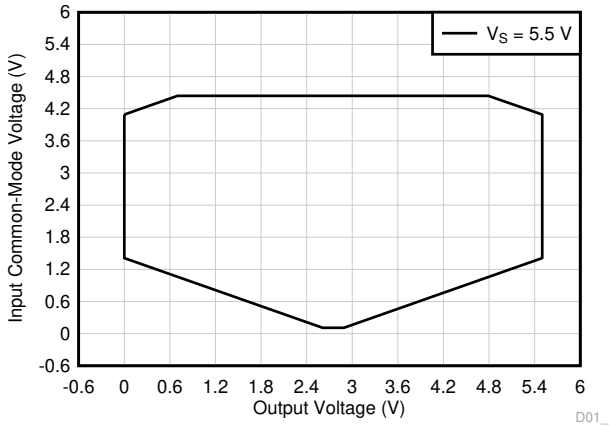
V+ = 2.75 V V– = –2.75 V V_{IN} = 0.6 V_{PP}

Figure 7-43. No Phase Reversal



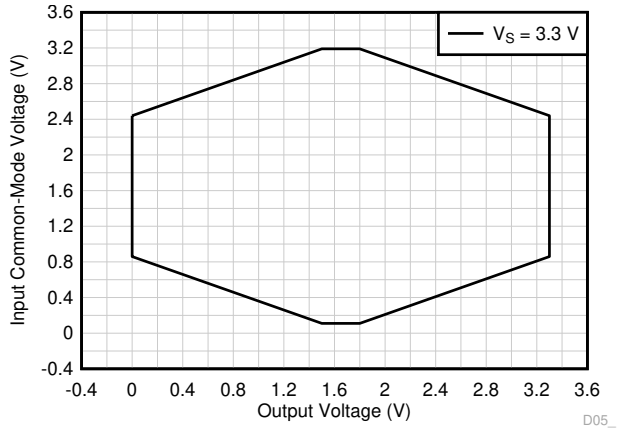
V_S = 3.3 V

Figure 7-44. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



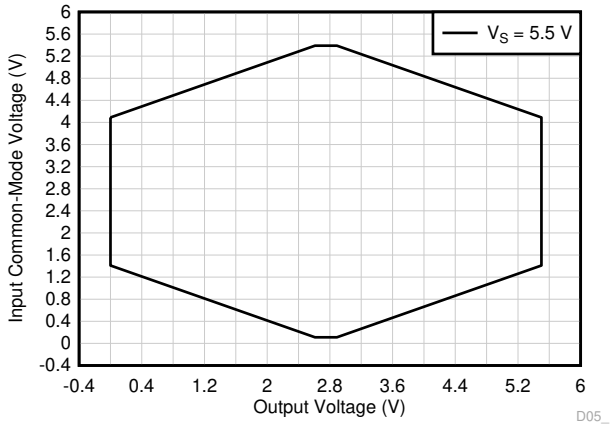
V_S = 5.5 V

Figure 7-45. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 3.3 V

Figure 7-46. Input Common-Mode Voltage vs Output Voltage



V_S = 5.5 V

Figure 7-47. Input Common-Mode Voltage vs Output Voltage

8 Detailed Description

8.1 Overview

INA351A is a G = 10 instrumentation amplifier with configurable reference amplifier designed to provide an integrated, small size, cost-effective solution for applications employing discrete implementation of INA using commodity amplifiers and resistors. This integrated instrumentation amplifier is built using four operational amplifiers and seven precision matched integrated resistors. With 86dB minimum CMRR and 0.1% maximum gain error, INA351A is suitable to be used directly in sub 10-bit systems without any external calibration. Additional calibration of offset and gain error at a system level can further improve system resolution and accuracy, enabling use in 12-bit to 14-bit precision applications.

INA351A has a configurable reference amplifier with external input and output pins. This reference amplifier's output is connected to the 60-kΩ internal resistor so that any reference voltage on the amplifier input that sets the output common mode of the INA could be buffered. This buffered output voltage is available externally and could be used to bias subsequent amplifier stages.

More importantly, the reference amplifier enables DC error calibration when configured in a servo loop. When the INA input signal is at a slightly higher frequency than DC, the servo amplifier can enable external calibration of total DC errors (offset, drift etc.) at the INA output leading to a overall better DC precision. The INA351A in calibration loop is well suited for medical applications where the low-frequency signals like ECG, EEG, EMG are to be amplified with relatively lower noise and lesser DC errors. It is also suitable for use in industrial applications in higher frequency pressure transducers and lock in amplifier designs.

One of the key features of INA351A is that the device does not need any external resistors to set the gain. Often these external resistors require tighter tolerance and careful routing, which adds to system complexity and cost. The device is highly suitable for voltage sensing in space-constrained applications such as patient monitoring, sleep diagnostics, electronic hospital beds, and blood glucose monitoring. INA351A can enable these systems to reduce their overall size and cost while providing optimal performance.

8.2 Functional Block Diagram

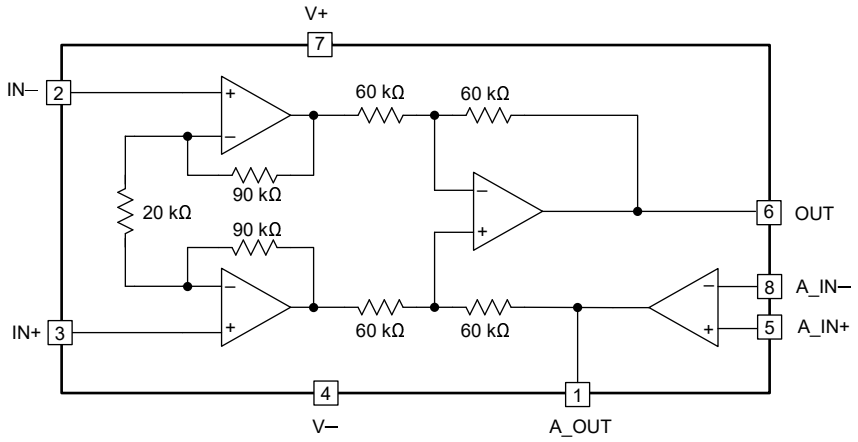


Figure 8-1. Simplified Internal Schematic

8.3 Feature Description

8.3.1 Gain-Setting

8.3.1.1 Gain Error and Drift

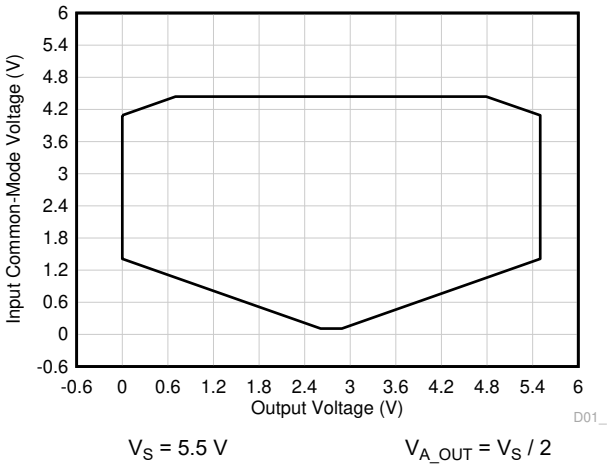
Gain error in INA351A is limited by the mismatch of the integrated precision resistors and is specified based on characterization results. Gain error of maximum 0.1% can be expected for this INA. Gain drift in INA351A is limited by the slight mismatch of the temperature coefficient of the integrated resistors. Since these integrated resistors are precision matched with low temperature coefficient resistors to begin with, the overall gain drift is much better in comparison to discrete implementation of the instrumentation amplifiers built using external resistors.

8.3.2 Input Common-Mode Voltage Range

INA351A has two gain stages, the first stage has a common-mode gain of 1 and a differential gain of 10. The second stage is configured in a difference-amplifier configuration with differential gain of 1 and ideally rejects all of the input common mode completely. The second stage also provides a gain of 1 from voltage at A_OUT to set the output common-mode voltage.

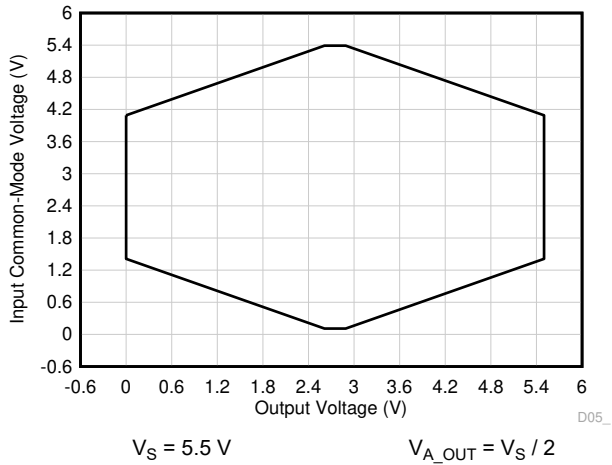
The linear input voltage range of the INA351A, even for a rail-to-rail first stage, is dictated by both the signal swing at output of the first stage as well as the input common-mode voltage range output swing of the second stage. In order to maximize performance, it is critical to keep the INA351A within its linear range for a given combination of reference amp's output voltage (A_OUT connects to REF), and input common-mode voltage for a particular input differential. Input common-mode voltage (V_{CM}) vs output voltage graphs (V_{OUT}) in this section show a particular A_OUT voltage and gain configuration to outline the linear performance region of INA351A. A good common-mode rejection can be expected when operating with in the limits of the V_{CM} vs V_{OUT} graph. Note that the INA351A linear input voltage cannot be close to or extend beyond the supply rails, as the output of the first stage will be driven into saturation.

The common-mode range for the most common operating conditions is outlined in the following figures. Figure 8-2 shows the region of operation where a minimum of 86 dB can be achieved. Figure 8-3 has much wider region of operation with a lower minimum CMRR of 62 dB, because the input signal crosses over the transition region of the input pairs to achieve rail-to-rail operation. The common-mode range for other operating conditions is best calculated with the INA V_{CM} vs V_{OUT} tool located under the *Amplifiers and Comparators* section of the Analog Engineer's Calculator on ti.com. INA351-HCM model can be specifically used for applications requiring high CMRR and corresponds to performance shown in Figure 8-2. INA351xxS model can be used for applications where the input common mode can be expected to vary rail-to-rail and the model corresponds to performance shown in Figure 8-3, where CMRR drops to 62-dB minimum.



V_S = 5.5 V V_{A_OUT} = V_S / 2

Figure 8-2. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 5.5 V V_{A_OUT} = V_S / 2

Figure 8-3. Input Common-Mode Voltage vs Output Voltage

8.3.3 EMI Rejection

The INA351A uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the INA351A benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-4 shows the results of this testing on the INA351A. Table 8-1 provides the EMIRR IN+ values for the INA351A at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

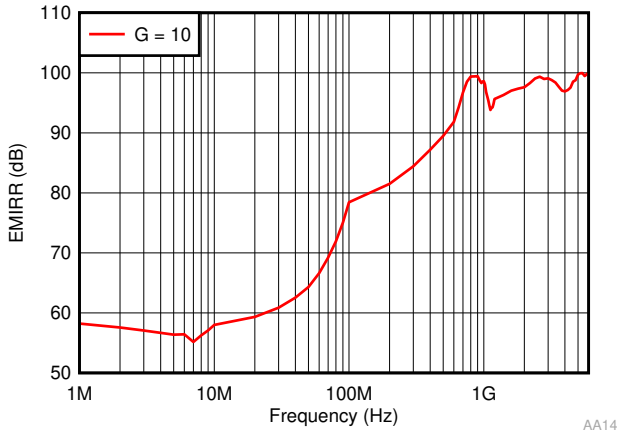


Figure 8-4. EMIRR Testing

Table 8-1. INA351A EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	88 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	99 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	97 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	98 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	97 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	99 dB

8.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

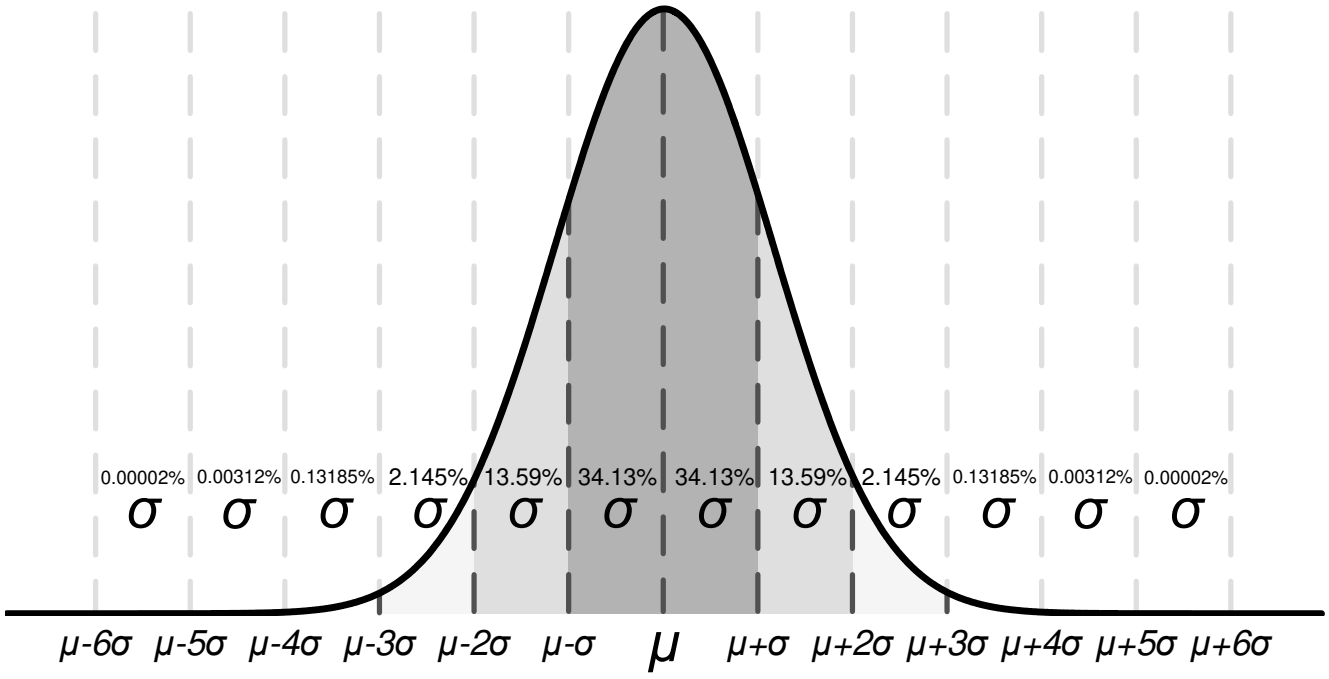


Figure 8-5. Ideal Gaussian Distribution

Figure 8-5 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

Designers can use this chart to calculate approximate probability of a specification in a unit; for example, the INA351A typical input referred voltage offset is 200 μV, so 68.2% of all INA351A devices are expected to have an offset from –200 μV to +200 μV. At 4 *σ* (±800 μV), 99.9937% of the distribution has an offset voltage less than ±800 μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are verified by TI, and units outside these limits are removed from production material. For example, the INA351A family has a maximum offset voltage of 1.3 mV at 25°C, and even though this corresponds to 6 σ (≈1 in 500 million units), which is extremely unlikely, TI verifies that any unit with larger offset than 1.3 mV are removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for the designers application, and design worst-case conditions using this value. As stated earlier, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guard band to design a system around. In this case, the INA351A family does not have a maximum or minimum for offset voltage drift, but based on Figure 7-2 and the typical value of 0.65 μV/°C in the *Electrical Characteristics* table, the 6-σ value for offset voltage drift can be calculated to 3.9 μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset drift without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot verify the performance of a device. This information must be used only to estimate the performance of a device.

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 8-6 shows the ESD circuits contained in the INA351A devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where these diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

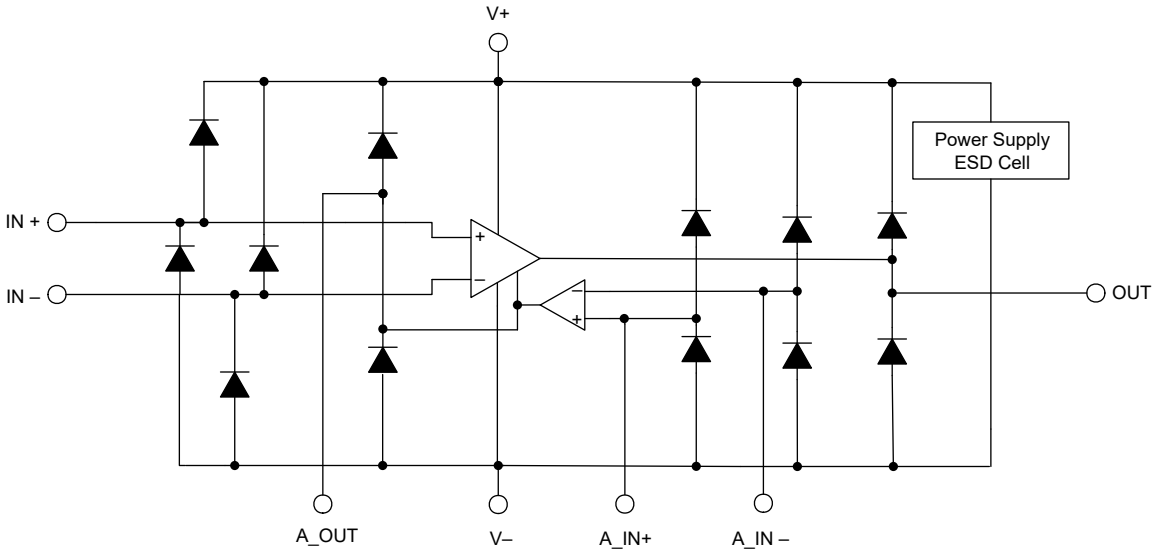


Figure 8-6. Equivalent Internal ESD Circuitry

8.4 Device Functional Modes

INA351A has only one functional mode. The device can be powered in single supply or dual supply configurations as long as the device is supplied with V_S = (V+) – (V–) = 1.8 V to 5.5 V as specified in the recommended operating conditions.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Amplifier

The output voltage of the INA351A is developed with respect to the voltage on the pin A_OUT. The voltage on the A_OUT pin sets the common-mode voltage of the instrumentation amplifier OUT pin. In single-supply operation with a bipolar input, setting the output common-mode to a precise mid-supply level is useful and required (for example, 2.75-V in a 5.5-V supply environment) to allow the output signal to swing negative and positive in equal proportions. Traditionally, this is accomplished using a resistive divider from supply and an external reference buffer.

In INA351A, the reference amplifier is integrated on-chip and it is sufficient to only have the resistive divider from supply. With that, the reference amplifier can be connected in G = 1 as shown in Figure 9-1 to provide buffered reference voltage internally to the INA as well as to additional circuits for external use.

Moreover, INA351A has a provision to include servo loop based calibration for external DC offset, drift from the sensor as well as the internal INA offset, drift. This is accomplished using the internal reference amplifier and the three external passive components (R_1, R_2, and C_2) as shown in Figure 9-2. The ratio of resistors R_2 with respect to R_1 sets the gain in the calibration loop to attenuate the DC errors at lower frequencies around DC. At higher frequencies, the capacitor, C_2 shorts R_2 to put the reference buffer in G = 1. This enables the instrumentation amplifier's input differential voltage to influence the INA output at higher frequencies while the reference amplifier in servo loop influences the INA output at lower frequencies around DC. Care should be taken to limit the gain in servo loop so as to maintain sufficient stability. Also, the value of C_2, R_2 should be chosen based on the frequency of input signal at the INA input. Now, the resulting residual DC error after calibration would be that of the reference amplifier itself which is minor in comparison to higher DC offset from the instrumentation amplifier, sensor.

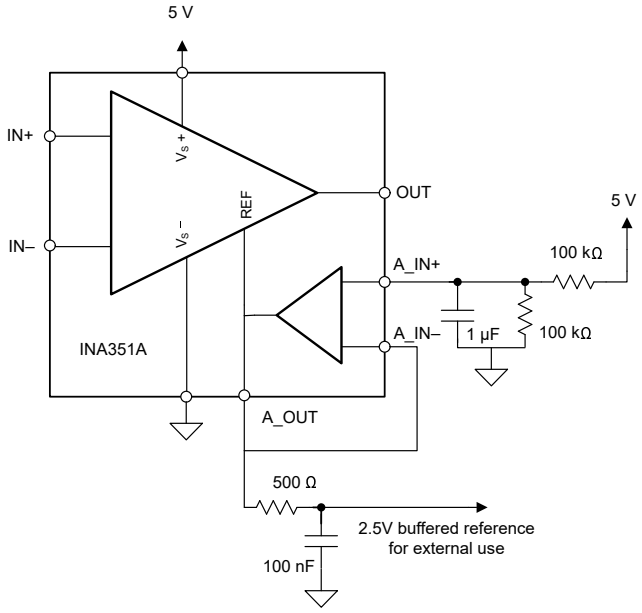


Figure 9-1. INA351A in Reference Buffer Configuration

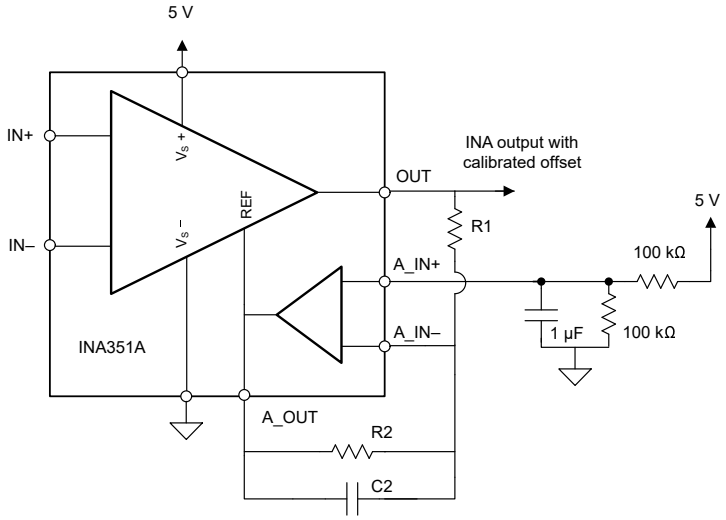


Figure 9-2. INA351A in Servo-Loop Calibration Configuration

9.1.2 Input Bias Current Return Path

The input impedance of the INA351A is extremely high, but a path must be provided for the input bias current of both inputs. This input bias current is typically a few pico amps but at high temperature this can be a few nano amps. High input impedance means that the input bias current changes little with varying input voltage.

For proper operation, input circuitry must provide a path for this input bias current. Figure 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA351A, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in Figure 9-3). With a higher source impedance, use two equal resistors to provide a balanced input, with the possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.

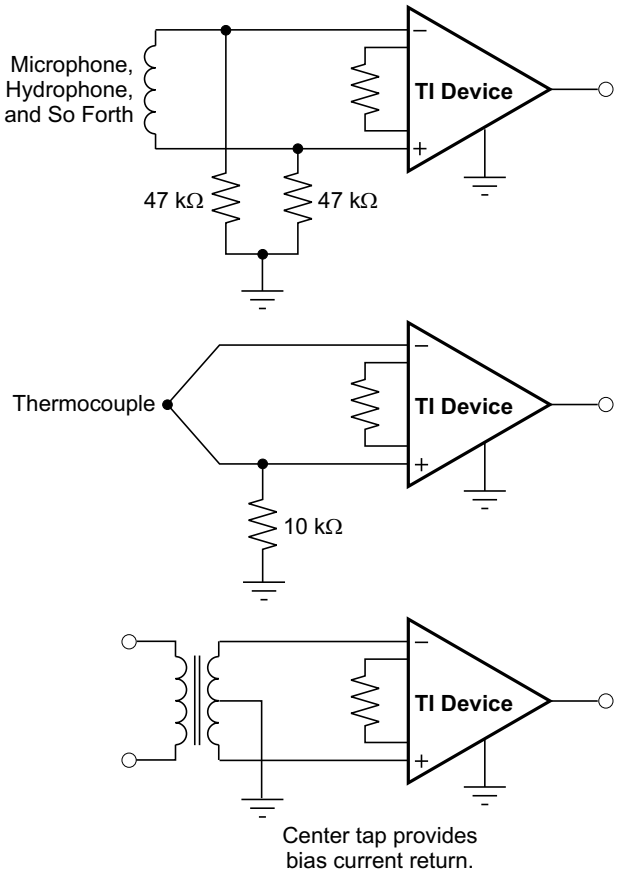


Figure 9-3. Providing an Input Common-Mode Current Path

9.2 Typical Applications

9.2.1 Resistive-Bridge Pressure Sensor

The INA351A is an integrated instrumentation amplifier that measures small differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 110 µA (typical) and has a smaller form factor.

The device is designed for portable applications where sensors measure physical parameters, such as changes in fluid, pressure, temperature, or humidity. An example of a pressure sensor used in the medical sector is in portable infusion pumps or dialysis machines.

The pressure sensor is made of a piezo-resistive element that can be derived as a classical 4-resistor Wheatstone bridge.

Occlusion (infusion of fluids, medication, or nutrients) happens only in one direction, and therefore can only cause the resistive element (R) to expand. This expansion causes a change in voltage on one leg of the Wheatstone bridge, which induces a differential voltage V_{DIFF}.

Figure 9-4 shows an example circuit for an occlusion pressure sensor application, as required in infusion pumps. When blockage (occlusion) occurs against a set-point value, the tubing depresses, thus causing the piezo-resistive element to expand. The signal chain connected to the bridge downstream processes the pressure change and can trigger an alarm.

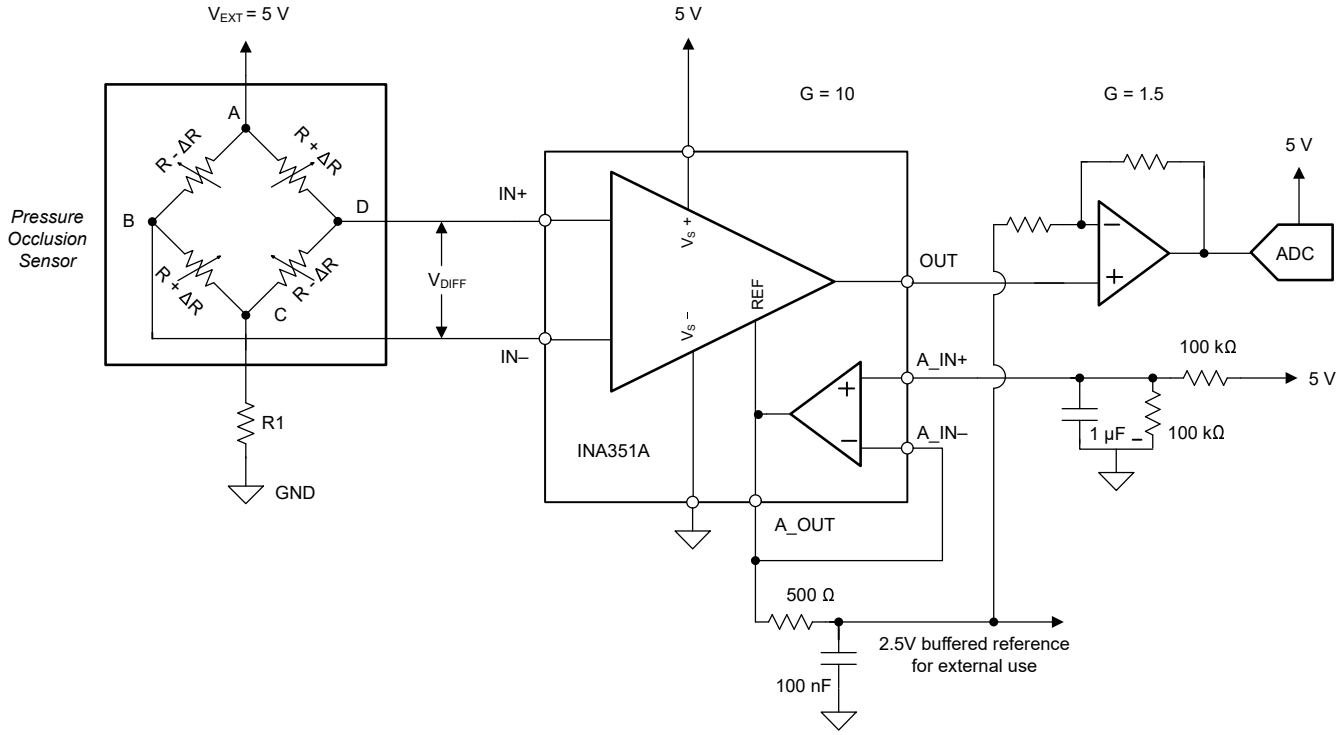


Figure 9-4. Resistive-Bridge Pressure Sensor

Low-tolerance bridge resistors must be used to minimize the offset and gain errors.

Given that there is only a positive differential voltage applied, this circuit is laid out in single-ended supply mode. The excitation voltage, V_{EXT}, to the bridge must be precise and stable; otherwise, measurement errors can be introduced.

9.2.1.1 Design Requirements

For this application, the design requirements are provided in Table 9-1.

Table 9-1. Design Requirements

DESCRIPTION	VALUE
Single supply voltage	V_S = 5.0 V
Excitation voltage	V_{EXT} = 5.0 V
Occlusion pressure range	P = 1 psi to 12 psi, increments of P = 0.5 psi
Occlusion pressure sensitivity	S = 2 ±0.5 (25%) mV/V/psi
Occlusion pressure impedance (R)	R = 4.99 kΩ ±50 Ω (0.1%)
Total pressure sampling rate	Sr = 20 Hz
ADC supply voltage	$V_{ADC(fs)}$ = 5.0 V
Full-scale range of ADC	V_{OUT} = 0.25 V to 4.75 V to avoid saturation

9.2.1.2 Detailed Design Procedure

This section provides basic calculations to lay out the instrumentation amplifier with respect to the given design requirements.

One of the key considerations in resistive-bridge sensors is the common-mode voltage, V_{CM}. If the bridge is balanced (no pressure, thus no voltage change), $V_{CM(zero)}$ is half of the bridge excitation (V_{EXT}). In this example $V_{CM\ (zero)}$ is 2.5 V. For the maximum pressure of 12 psi, the bridge common-mode voltage, $V_{CM(MAX)}$, is calculated by:

$$V_{CM(MAX)} = \frac{V_{DIFF}}{2} + V_{CM(zero)} \quad (1)$$

where

$$V_{DIFF} = S_{MAX} \times V_{EXT} \times P_{MAX} = 2.5\,\frac{mV}{V \times psi} \times 5\,V \times 12\,psi = 150\,mV \quad (2)$$

Thus, the maximum common-mode voltage applied results in:

$$V_{CM(MAX)} = \frac{150\,mV}{2} + 2.5\,V = 2.575\,V \quad (3)$$

Similarly, the minimum common-mode voltage can be calculated as,

$$V_{CM(MIN)} = \frac{-150\,mV}{2} + 2.5\,V = 2.425\,V \quad (4)$$

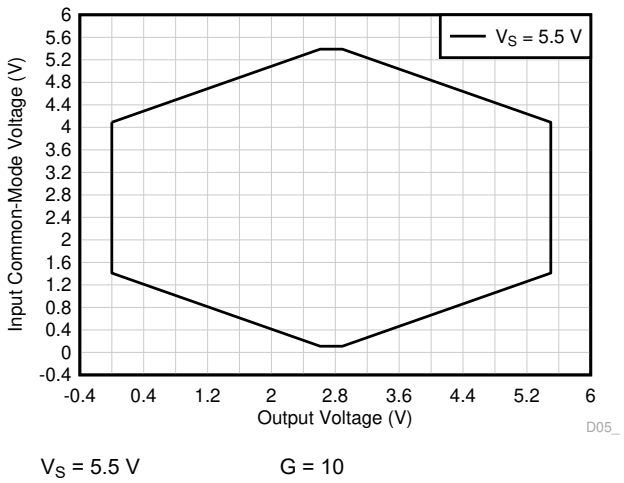
The next step is to calculate the gain required for the given maximum sensor output voltage span, V_{DIFF}, in respect to the required V_{OUT} swing of maximum 4.75V to avoid saturating the amplifier and the ADC running at 5V supply.

The following equation calculates the gain value using the maximum input voltage and the required output voltage:

$$G = \frac{V_{OUT}}{V_{DIFF(MAX)}} = \frac{2.25\,V}{150\,mV} = 15\,V/V \quad (5)$$

Considering, INA351A is an INA in G = 10, an additional gain stage in G = 1.5 is added.

Next, let us make sure that the INA351A can operate within this range checking the *Input Common-Mode Voltage vs Output Voltage* curves in the *Typical Characteristics* section. The relevant figure is also in this section for convenience. Looking at Figure 9-5, we can confirm that a output signal swing of 3 V is supported for the input signal swing between 2.425 V and 2.575 V, thus making sure of the linear operation.



V_S = 5.5 V G = 10

Figure 9-5. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

An additional series resistor in the Wheatstone bridge string (R1) may or may not be required, and can be decided based on the intended output voltage swing for a particular combination of supply voltage, reference voltage and the selected gain for an input common mode voltage range. R1 helps adjust the input common-mode voltage range, and thus can help accommodate the intended output voltage swing. In this particular example, it is not required and can be shorted out.

9.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in Figure 9-4.

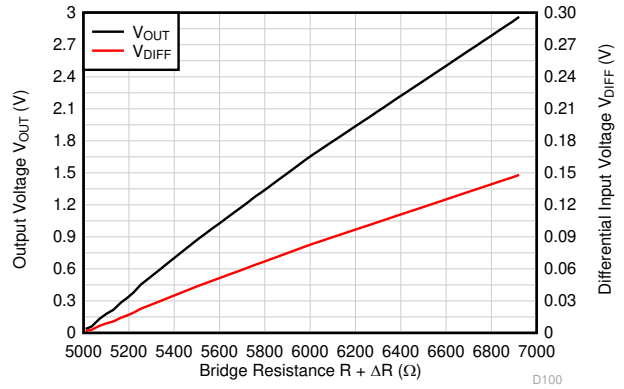


Figure 9-6. Input Differential Voltage, Output Voltage vs Bridge Resistance

9.3 Power Supply Recommendations

The nominal performance of the INA351A is specified with a supply voltage of ±2.75 V. The device also operates using power supplies from ±0.9 V (1.8 V) to ±2.75 V (5.5 V) with excellent performance. Parameters can vary significantly with operating voltage.

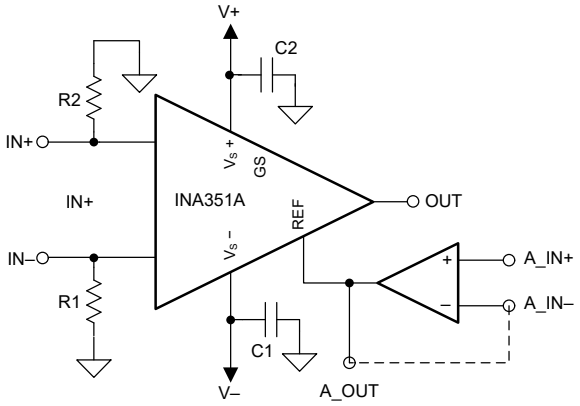
9.4 Layout

9.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply and output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

9.4.2 Layout Example



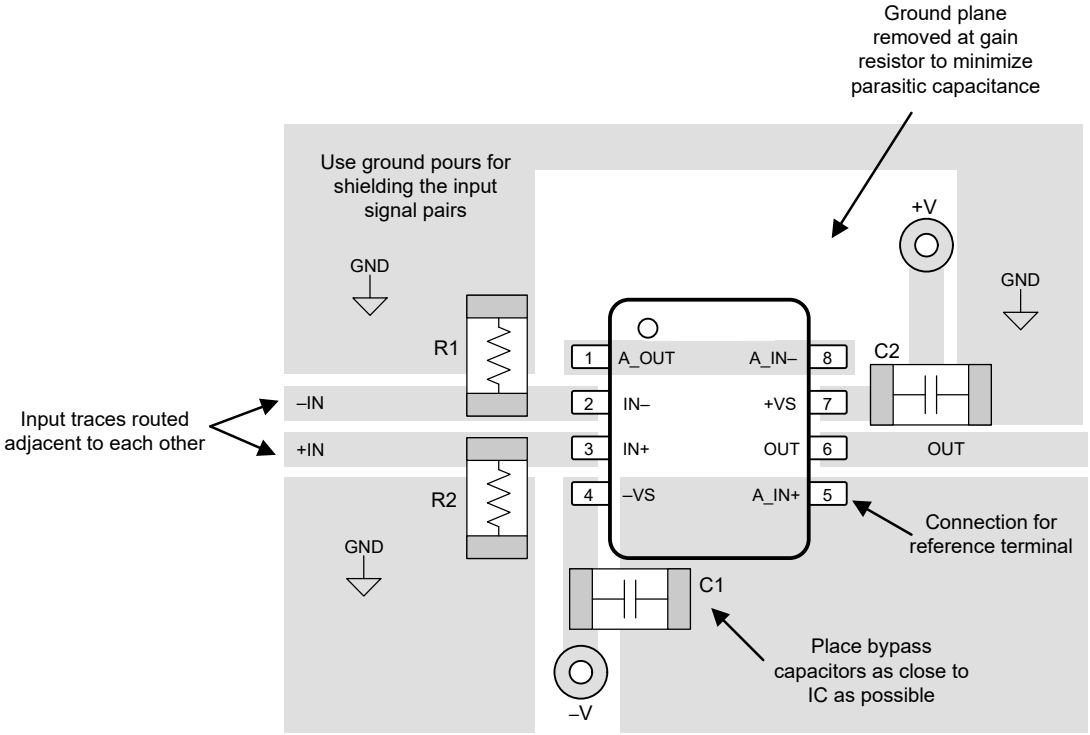


Figure 9-7. Example Schematic and Associated PCB Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineers Calculator*

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA351AIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2TSH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

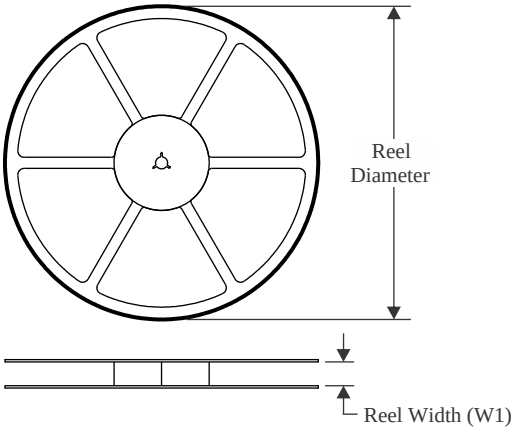
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

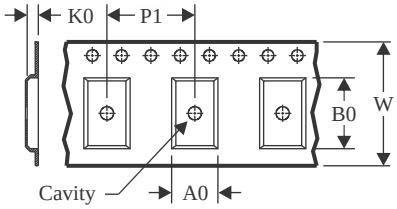
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

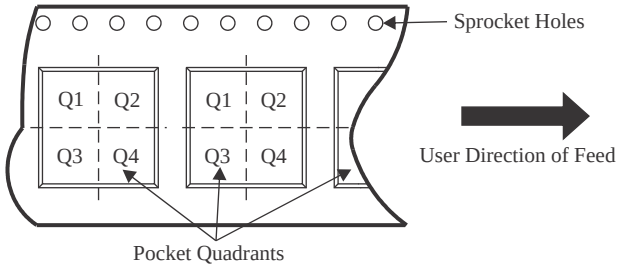


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

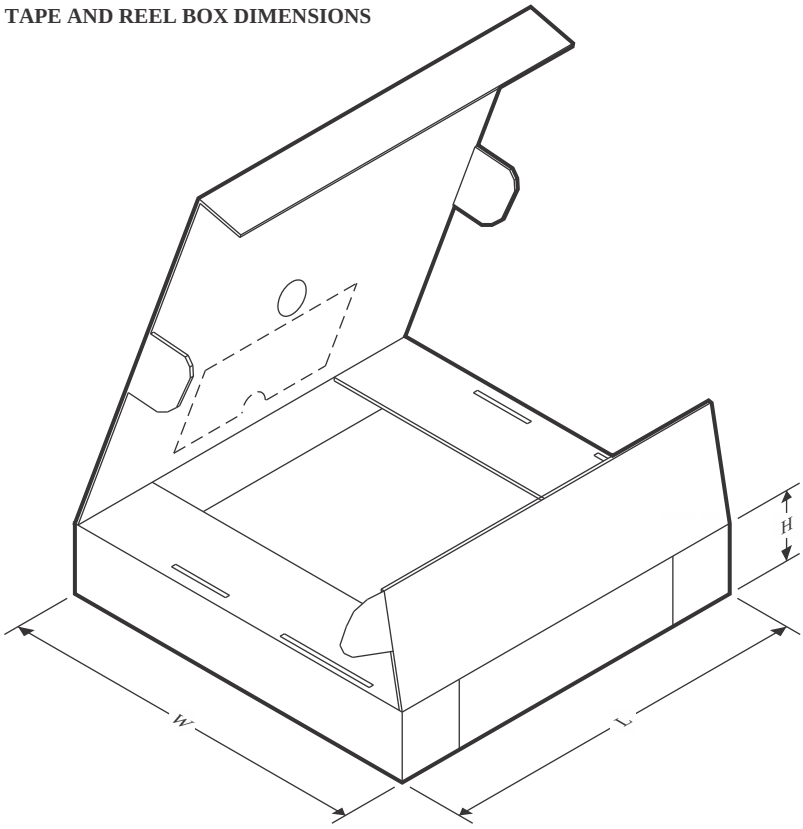
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA351AIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA351AIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

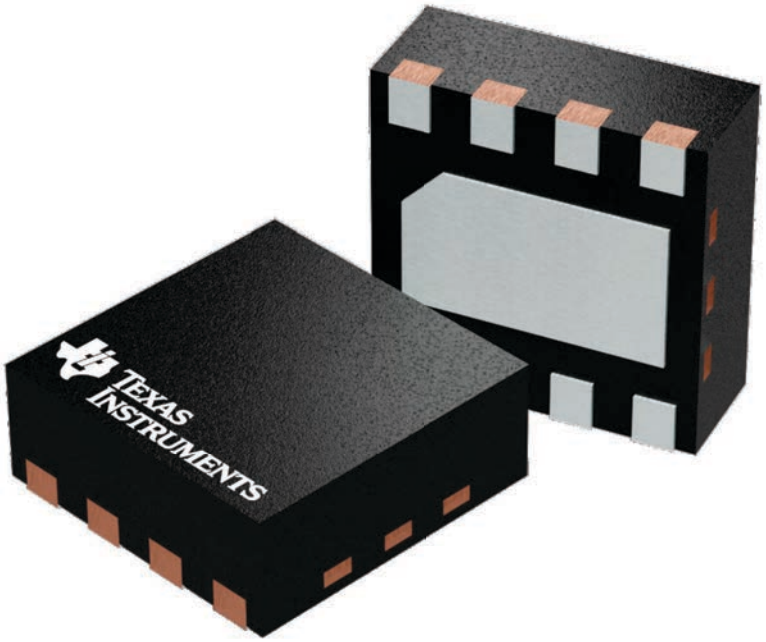
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



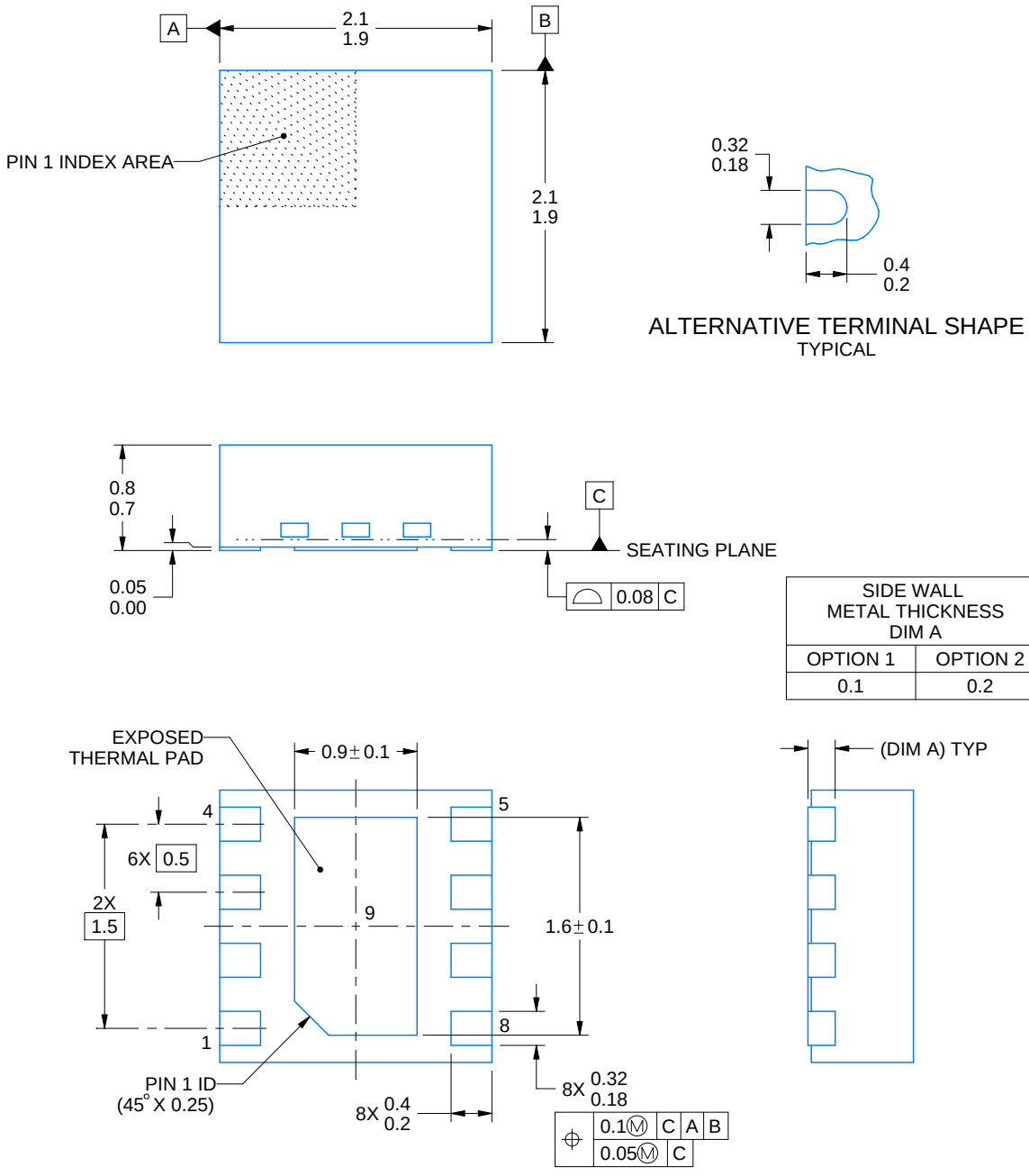
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

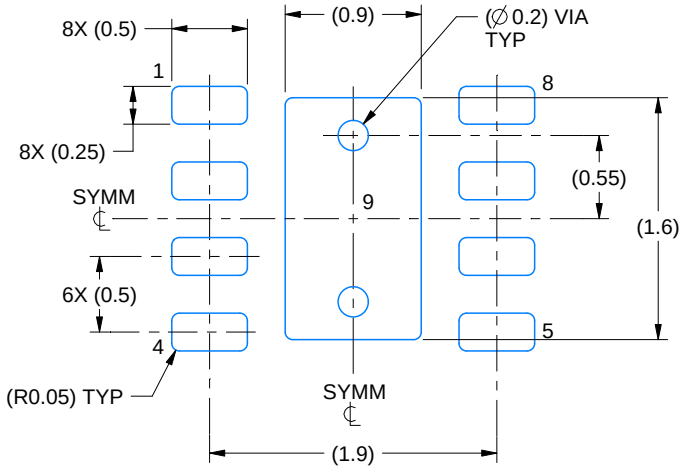
PLASTIC SMALL OUTLINE - NO LEAD



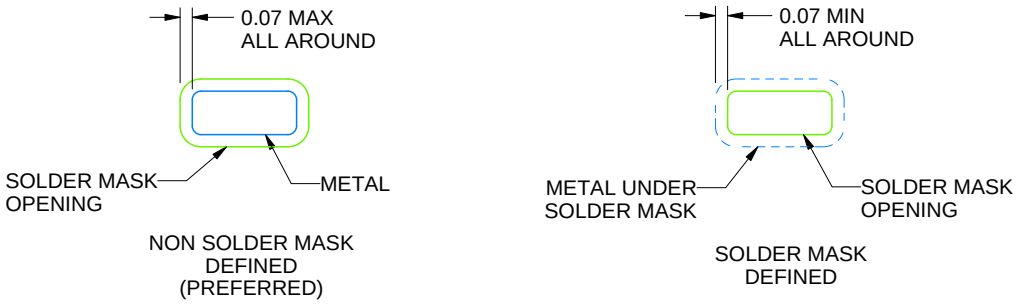
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

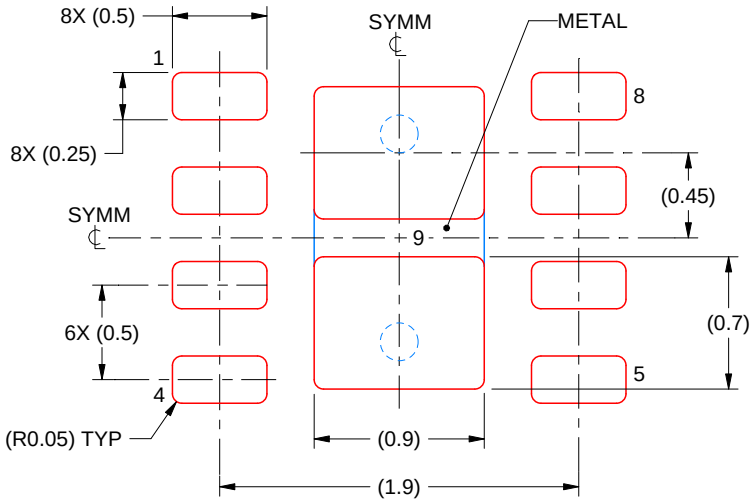


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265