ESD701 Low Capacitance ESD Diode for RF and ADAS Signal Protection

1 Features

- IEC 61000-4-2 ESD Protection:
  - ±15kV contact discharge
  - ±15kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 3A (8/20µs)
- I/O capacitance: 0.3pF (typical)
- Ultra low leakage current: 2nA (typical)
- Low dynamic resistance 0.84Ω (typical)
- Industry standard 0402 package

2 Applications

- Automotive Antenna ESD Protection
- RF Signal ESD Protection
- Near Field Communications (NFC)
- Automotive SerDes w/Power over Coax
- USB Type-C (short-to-Vbus tolerant)

3 Description

The ESD701 is a bidirectional ESD protection diode. The ESD701 is offered in the industry standard 0402 (DPY) package, and offers an IEC 61000-4-2 protection level of 15kV. The device can clamp 8/20µs surges with peak pulse currents up to 3A in accordance with the IEC 61000-4-5 standard.

The low capacitance and low leakage current help to ensure protection against transient events in a variety of systems and applications. This protection is key for many applications, such as smaller form factors and faster data speeds, which are becoming more popular over time.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD701	DPY (X1SON, 2)	1mm × 0.6mm

(1) For more information, see Section 14.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

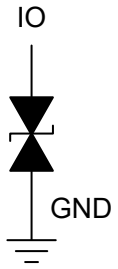

Figure 3-1. Functional Block Diagram

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4 Pin Configuration and Functions

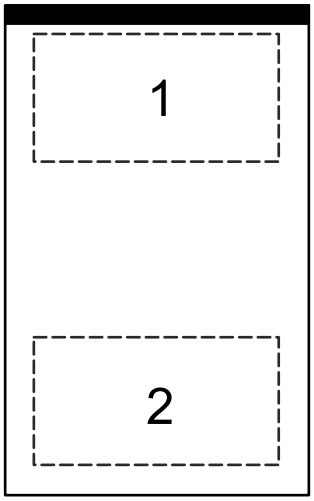

Figure 4-1. DPY Package, 2-Pin X1SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD I/O, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD I/O, connect pin 1 to ground

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		MIN	MAX	UNIT
P_{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 µs) Peak Pulse Power at 25 °C (2)		210	W
I_{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 µs) Peak Pulse Current at 25 °C (2)		3.0	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.

5.2 ESD Ratings -JEDEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	V
		IEC 61000-4-2 Air Discharge, all pins	±15000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating Free Air Temperature	–40		125	°C

5.5 Thermal Information

THERMAL METRIC (1)		ESD701 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	-24		24	V
I_{LEAK}	Leakage current at V_{RWM}	VIO = ±24 V, I/O to GND		2	10	nA
V_{BR}	Breakdown voltage, I/O to GND (1)	I_{IO} = ±10 mA	25.5		35.5	V
V_{HOLD}	Holding voltage (2)	TLP, IO to GND or GND to IO		31		
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (3)	I_{PP} = 3 A, I/O to GND		37		V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (3)	I_{PP} = 3 A, GND to I/O		37		V
V_{CLAMP}	TLP clamping voltage, t_p = 100 ns (4)	I_{PP} = 16 A (100 ns TLP), I/O to GND		41		V
V_{CLAMP}	TLP clamping voltage, t_p = 100 ns (4)	I_{PP} = 16 A (100 ns TLP), GND to I/O		41		V
R_{DYN}	Dynamic resistance (5)	I/O to GND		0.84		Ω
		GND to I/O		0.84		
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, f = 1 MHz		0.3	0.5	pF

(1) V_{BR} is defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.
(3) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5
(4) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008
(5) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.7 Typical Characteristics

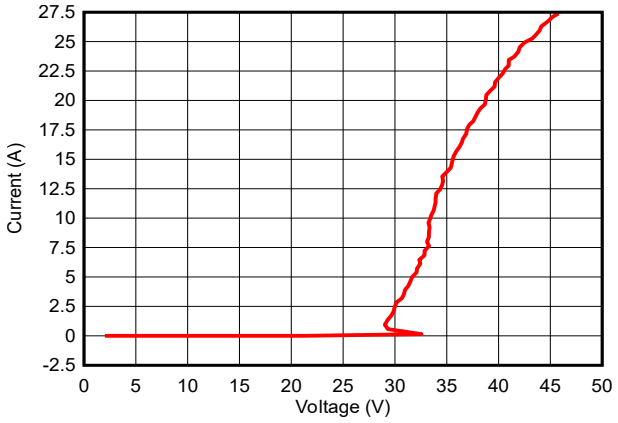

Figure 5-1. Positive TLP Curve

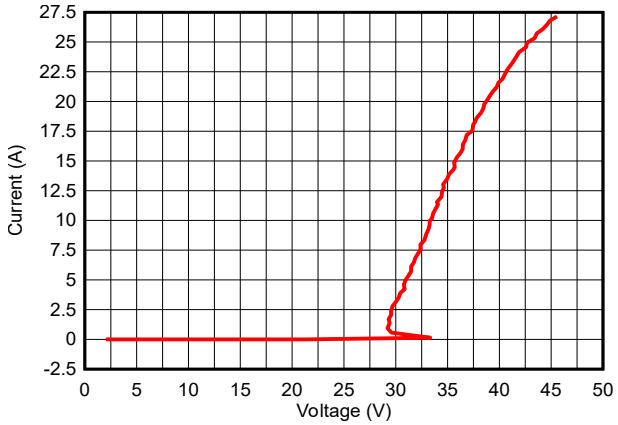

Figure 5-2. Negative TLP Curve

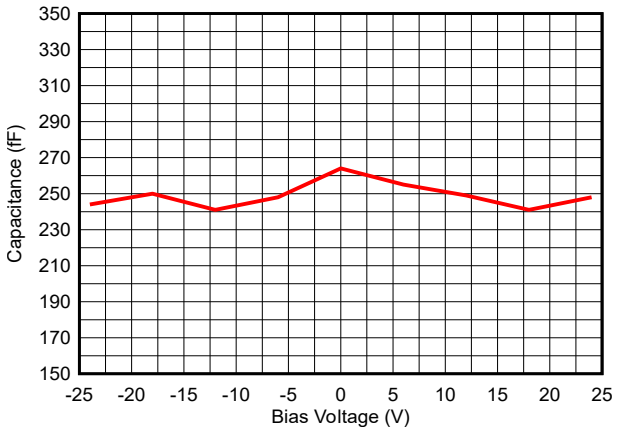

Figure 5-3. Bias Voltage vs. Capacitance

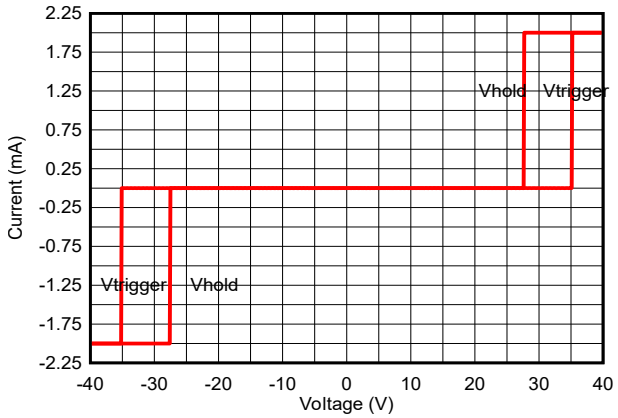

Figure 5-4. DC-IV Curve

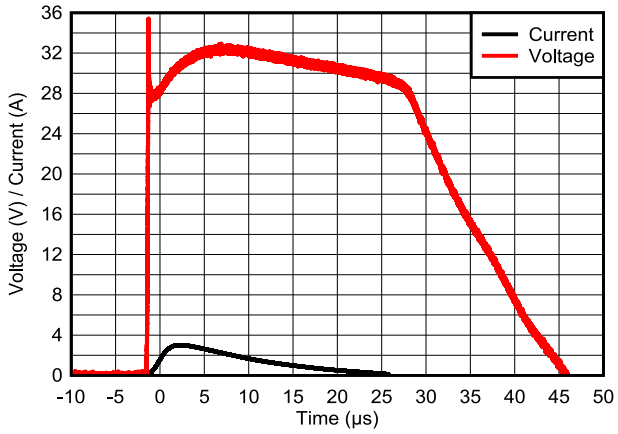

Figure 5-5. 8/20 µs Surge Response

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD701 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide*
- Texas Instruments, *TI's IEC 61000-4-x Testing application note*
- Texas Instruments, *ESD Layout Guide user's guide*
- Texas Instruments, *ESD Protection Diodes EVM user's guide*
- Texas Instruments, *Generic ESD Evaluation Module user's guide*
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet user's guide*

7.2 Receiving Notification of Documentation Updates

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TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Receiving Notification of Documentation Updates

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12 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD701DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	PQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

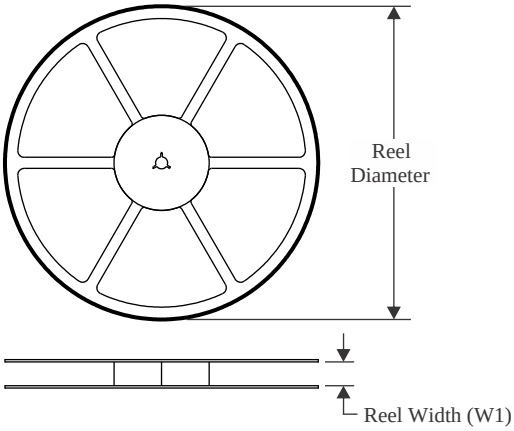
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

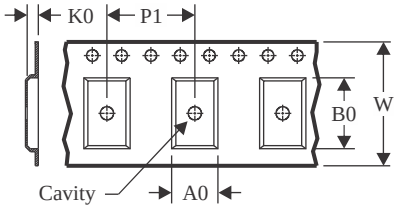
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

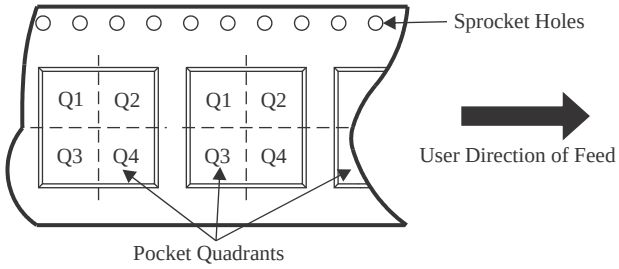


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

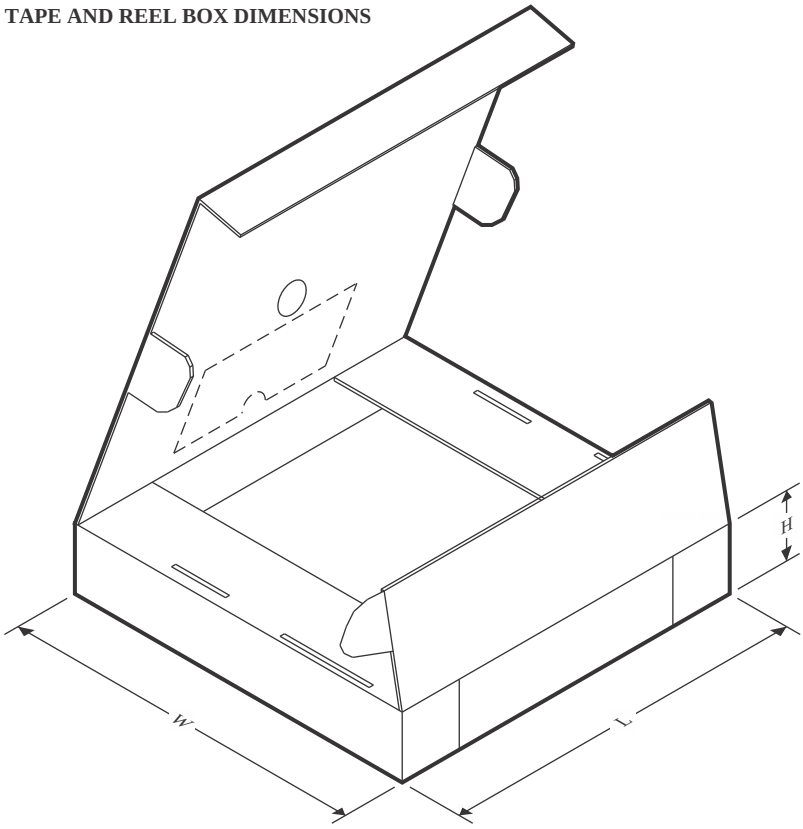
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD701DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD701DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

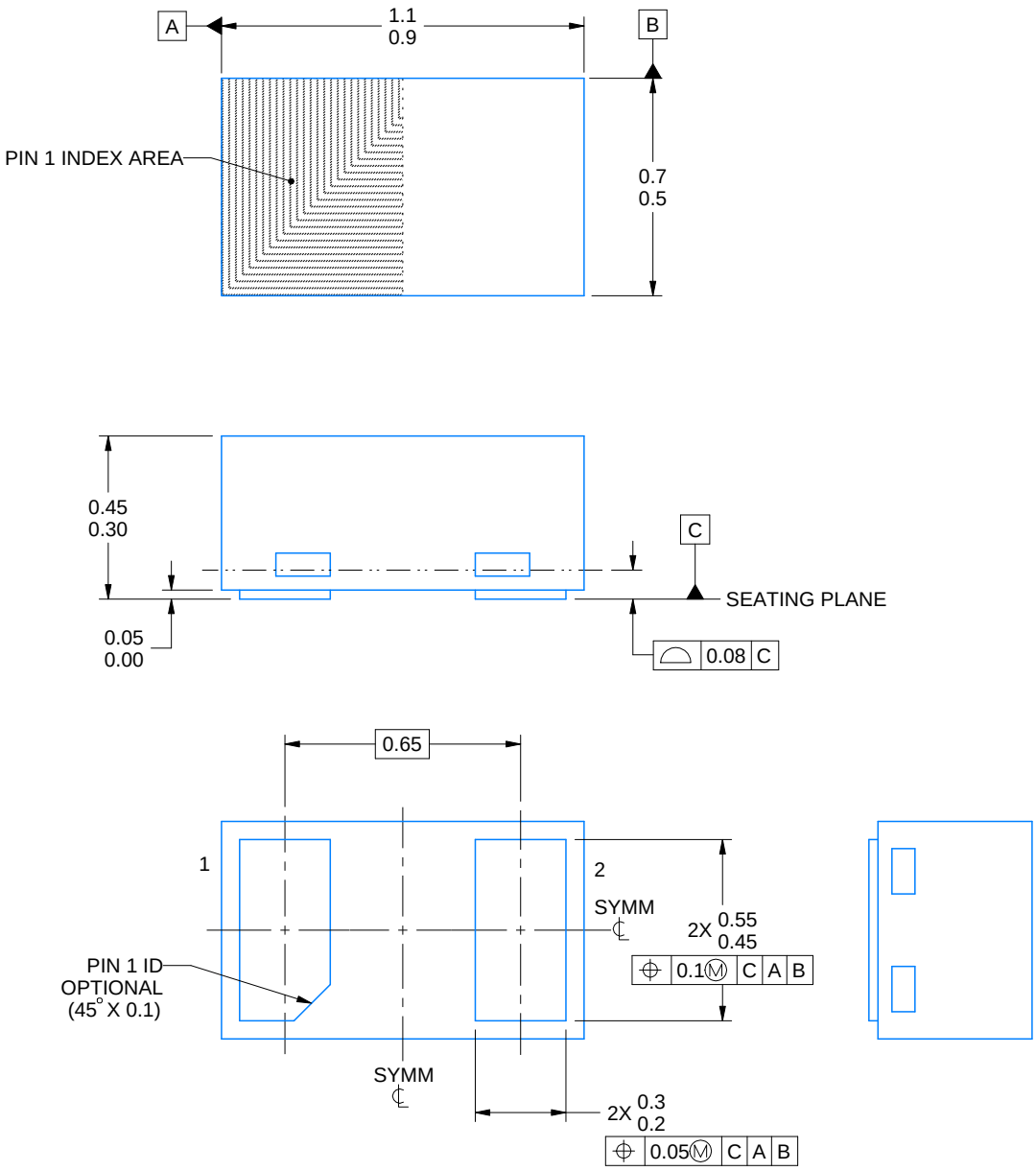
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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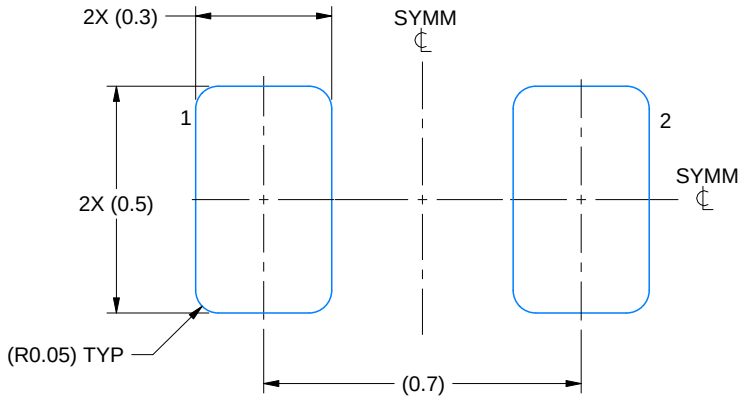
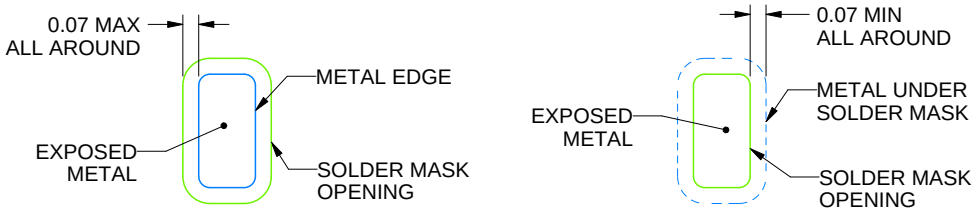
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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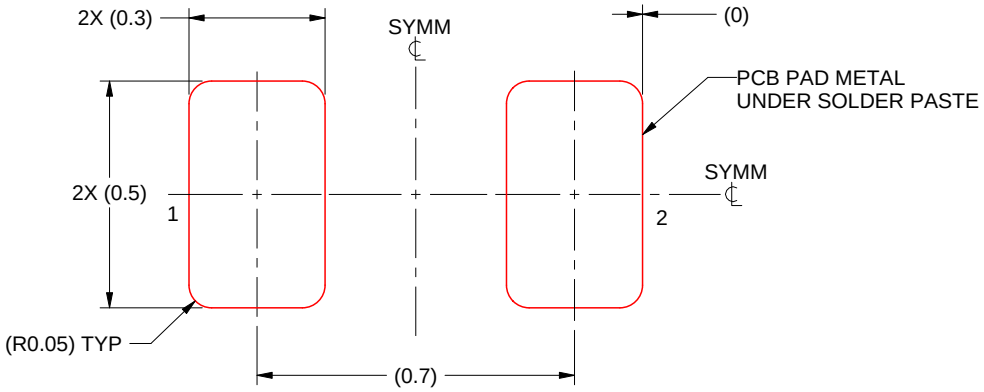
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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