

DLPA2000 Power Management and LED/Lamp Driver IC

1 Features

- High Efficiency RGB LED/Lamp Driver with Buck-Boost DC-to-DC Converter, DMD Supplies, DPP Core Supply, 1.8-V Load Switch, and Measurement System in a Small Chip-Scale Package
- Three Low-Impedance (30 mΩ Typical at 27°C) MOSFET Switches for Channel Selection
- Independent, 10-Bit Current Control per Channel
- 750-mA Max LED Current for DLPA2000 Embedded Applications
- On-Chip Motor Driver
- DMD Regulators
 - Requires Only a Single Inductor
 - VOFS: 10 V
 - VBIAS: 18 V
 - VRST: -14 V
 - Passive Discharge to GND When Disabled
- DPP 1.1-V Core Supply
 - Synchronous Step-Down Converter with Integrated Switching FETs
 - Supports up to 600-mA Output Current
- VLED Buck Boost Converter
 - Power Save Mode at Light Load Current
- Low-Impedance Load Switch
 - V_{IN} Range from 1.8 V to 3.6 V
 - Supports up to 200 mA of Current
 - Passive Discharge to GND When Disabled
- DMD Reset Signal Generation and Power Supply Sequencing
- 33-MHz Serial Peripheral Interface (SPI)
- Multiplexer for Measuring Analog Signals

- Battery Voltage
- LED Voltage, LED Current
- Light Sensor (for White Point Correction)
- Internal Reference Voltage
- External (Thermistor) Temperature Sensor
- Monitoring and Protection Circuits
 - Hot Die Warning and Thermal
 - Low-Battery Warning
 - Programmable Battery Undervoltage Lockout (UVLO)
 - Load Switch UVLO
 - Overcurrent and Undervoltage Protection
- DLPA2000 DSBGA Package
 - 56-Ball 0.4-mm Pitch
 - Die Size: 3.280 mm × 3.484 mm ± 0.03 mm

2 Applications

- DLP™ Display Projector
- DLP™ Mobile Sensing

3 Description

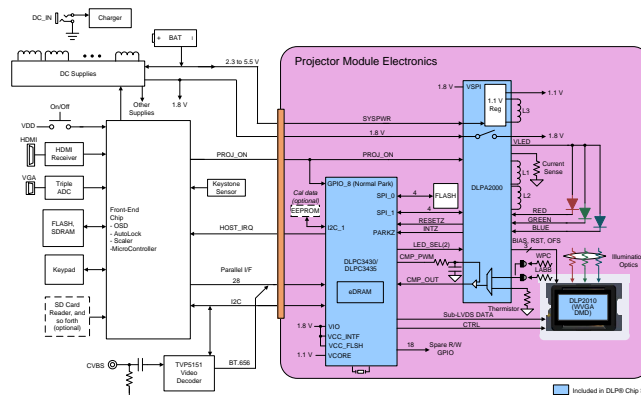
The DLPA2000 is a dedicated PMIC/RGB LED/lamp driver for the DLP2010 and DLP2010NIR digital micromirror devices (DMD) when used with a DLPC3430, DLPC3435, or DLPC150 digital controller. For reliable operation of these chipsets, it is mandatory to use the DLPA2000.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-----------------------------|
| DLPA2000 | DSBGA (56) | 3.28 mm × 3.48 mm ± 0.03 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Figure 1. Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (August 2015) to Revision B

Page

| | |
|---|-----------|
| • Fixed body size dimension typo in Device Information, corrected 3.48 mm ² to 3.48 mm | 1 |
| • Added missing history tags to Revision A that were not listed | 1 |
| • Corrected package family to 'DSBGA' in Pin Functions Diagram, originally labeled as 'DSGBA' | 3 |
| • Added mechanical package designator YFF to Thermal Information | 6 |
| • Changed layout example to show correct image in Figure 46 | 48 |

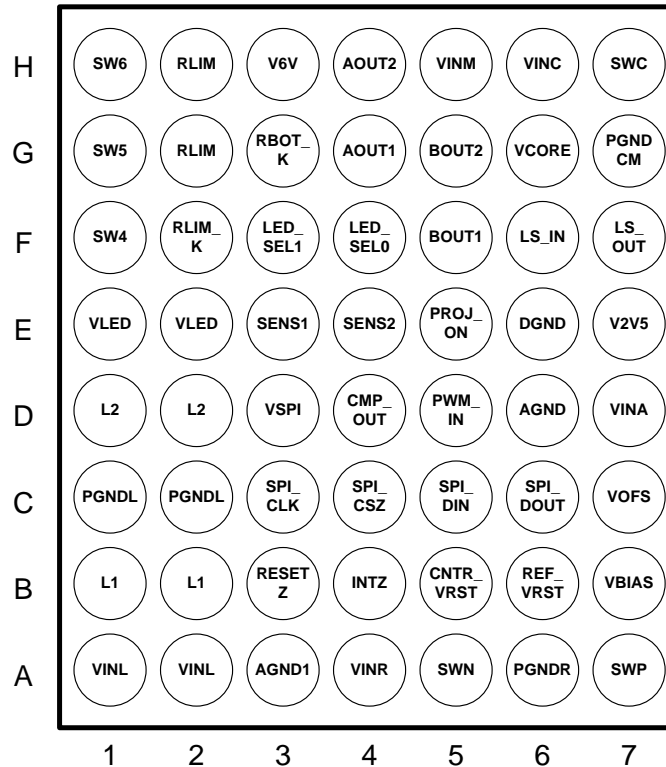
Changes from Original (June 2014) to Revision A

Page

| | |
|--|-----------|
| • Changed max current to 750 mA | 1 |
| • Added Mobile Sensing application | 1 |
| • Added typical Mobile sensing application | 43 |
| • Updated the <i>Power Supply Recommendations</i> to remove information that did not apply to the DLPA2000 | 46 |

5 Pin Configuration and Functions

**YFF PACKAGE
56-PIN DSBGA
BOTTOM VIEW**



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------|--------|-----|---|
| NAME | NUMBER | | |
| VINL | A1 | I | Power supply input for VLED BUCK-BOOST power stage. Connect to system power. |
| | A2 | | |
| AGND1 | A3 | GND | Analog ground. Connect to ground plane. |
| VINR | A4 | I | Power supply input for DMD switch mode power supply (SMPS). Connect to system power. |
| SWN | A5 | I | Connection for the DMD SMPS-inductor (high-side switch). |
| PGNDR | A6 | GND | Power ground for DMD SMPS. Connect to ground plane. |
| SWP | A7 | O | Connection for the DMD SMPS-inductor (low-side switch). |
| L1 | B1 | O | Connection for VLED BUCK-BOOST inductor. |
| | B2 | | |
| RESETZ | B3 | O | Reset output to the DLP system (active low). Pin is held low to reset DLP system. |
| INTZ | B4 | O | Interrupt output signal (open drain). Connect to pull-up resistor or short to ground. |
| CNTR_VRST | B5 | O | Connection to V_{RST} for fast discharge function. |
| REF_VRST | B6 | I | Reference pin for the V_{RST} regulator. Connect to V_{RST} rail through 100-k Ω resistor. |
| VBIAS | B7 | O | V_{BIAS} output rail. Connect to ceramic capacitor. |
| PGNDL | C1 | GND | Power ground for VLED BUCK-BOOST. Connect to ground plane. |
| | C2 | | |
| SPI_CLK | C3 | I | Clock input for SPI interface. |
| SPI_CSZ | C4 | I | SPI chip select (active low). |
| SPI_DIN | C5 | I | SPI data input. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|----------|--------|-------|--|
| NAME | NUMBER | | |
| SPI_DOUT | C6 | O | SPI data output. |
| VOFS | C7 | O | V _{OFS} output rail. Connect to ceramic capacitor. |
| L2 | D1 | I | Connection for VLED BUCK-BOOST inductor. |
| | D2 | | |
| VSPI | D3 | I | Power supply input for SPI interface. Connect to system I/O voltage. |
| CMP_OUT | D4 | O | Analog-comparator output. |
| PWM_IN | D5 | I | Reference voltage input for analog comparator. |
| AGND | D6 | GND | Analog ground. Connect to ground plane. |
| VINA | D7 | POWER | Power supply input for sensitive analog circuitry. |
| VLED | E1 | O | VLED BUCK-BOOST converter output pin. |
| | E2 | | |
| SENS1 | E3 | I | Input signal from light sensor. |
| SENS2 | E4 | I | Input signal from temperature sensor. |
| PROJ_ON | E5 | I | Input signal to enable or disable the IC and DLP projector. |
| DGND | E6 | GND | Digital ground. Connect to ground plane. |
| V2V5 | E7 | O | Internal supply filter pin for digital logic; typical 2.5 V. |
| SW4 | F1 | O | Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly. |
| RLIM_K | F2 | I | Kelvin sense connection to top side of LED current sense resistor. For best accuracy, route this trace directly to the top of the current sense resistor and separate it from the normal trace from the current sense resistor to the RLIM pins. |
| LED_SEL1 | F3 | I | Digital input to the RGB STROBE DECODER. |
| LED_SEL0 | F4 | I | Digital input to the RGB STROBE DECODER. |
| BOUT1 | F5 | O | Motor driver B phase output1. |
| LS_IN | F6 | I | Load switch. |
| LS_OUT | F7 | O | Load switch. |
| SW5 | G1 | O | Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly. |
| RLIM | G2 | O | Connection to LED 'current sense' resistor. Bottom side of sense resistor is connected to GND. |
| RBOT_K | G3 | I | Kelvin sense connection to ground side of LED current sense resistor. |
| AOUT1 | G4 | O | Motor driver A phase output1. |
| BOUT2 | G5 | O | Motor driver B phase output2. |
| VCORE | G6 | I | VCORE BUCK converter feedback pin. |
| PGNDCM | G7 | GND | Power ground for VCORE BUCK and motor driver. |
| SW6 | H1 | O | Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly. |
| RLIM | H2 | O | Connection to LED current sense resistor. Bottom side of sense resistor is connected to GND. |
| V6V | H3 | O | Internal supply filter pin for gate driver circuitry. Typical 6.25 V. |
| AOUT2 | H4 | O | Motor driver A phase output2. |
| VINM | H5 | I | Power supply input for motor driver power stage. Connect to system power. |
| VINC | H6 | I | Power supply input for VCORE BUCK power stage. Connect to system power. |
| SWC | H7 | I/O | Connection for 1.1-V BUCK inductor. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | MIN | MAX | UNIT |
|---|--|-----|------|
| Input voltage at V_{INL} , V_{INA} , V_{INR} , V_{INC} , V_{INM} | -0.3 | 7 | V |
| Ground pins to system ground | -0.3 | 0.3 | V |
| Voltage at SWN | -18.0 | 7 | V |
| Voltage at SWP, V_{BIAS} | -0.3 | 20 | V |
| Voltage at V_{OFS} | -0.3 | 12 | V |
| Voltage at V_{6V} , V_{LED} , L1, L2, SWC, SW4, SW5, SW6, INTZ, PROJ_ON | -0.3 | 7 | V |
| Voltage at all pins, unless noted otherwise | -0.3 | 3.6 | V |
| Source current RESETZ, CMP_OUT | | 1 | mA |
| Source current SPI_DOUT | | 5.5 | mA |
| Sink current RESETZ, CMP_OUT | | 1 | mA |
| Sink current SPI_DOUT, INTZ | | 5.5 | mA |
| Peak output current | Internally limited | | |
| Continuous total power dissipation | Internally limited by thermal shutdown | | |
| T_J Operating junction temperature | -30 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

applicable before the DMD is installed in the final product.

| | MIN | MAX | UNIT |
|-----------------------------------|-----|-----|------|
| ENVIRONMENTAL | | | |
| T_{stg} DMD Storage Temperature | -65 | 150 | °C |

6.3 ESD Ratings

| | VALUE | UNIT |
|-------------------------------------|--|-------|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|--|--|-----|-----|------|
| Input voltage range at V_{INL} , V_{INA} , V_{INR} , V_{INC} , V_{INM} | Full functional and parametric performance | 2.7 | 3.6 | 6 |
| | Extended operating range, limited parametric performance | 2.3 | 3.6 | 6 |
| Voltage range at V_{SPI} | 1.65 | 1.8 | 3.6 | V |
| T_A Operational ambient temperature | -10 | | 85 | °C |
| T_J Operational junction temperature | -10 | | 120 | °C |

6.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DLPA2000 | UNIT |
|-------------------------------|---|-------------|------|
| | | YFF (DSBGA) | |
| | | 56 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽²⁾ | 45 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm x 114.3 mm, and 2-oz. copper for top and bottom plane. Actual thermal impedance will depend on PCB used in the application.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾⁽²⁾)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---|--|-----|------|-----|------|
| SUPPLIES | | | | | | |
| INPUT VOLTAGE | | | | | | |
| V_I | Input voltage range | $V_{INA}, V_{INR}, V_{INL}, V_{INC}$ | 2.7 | 3.6 | 6 | V |
| | Extended input voltage range ⁽¹⁾ | | 2.3 | 3.6 | 6 | |
| V_{LOW_BAT} | Low-battery warning threshold | V_{INA} falling | | 3 | | V |
| | Hysteresis | V_{INA} rising | | 100 | | mV |
| $V_{hys(UVLO)}$ | Undervoltage lockout threshold | V_{INA} falling (through 5-bit trim function) | 2.3 | | 4.5 | V |
| | Hysteresis | V_{INA} rising | | 100 | | mV |
| $V_{STARTUP}$ | Startup voltage | $V_{BIAS}, V_{OFS}, V_{RST}$; loaded with 2 mA | 2.5 | | | V |
| INPUT CURRENT | | | | | | |
| I_Q | ACTIVE mode | Motor current excluded | | 15 | | mA |
| I_{STD} | STANDBY mode | | | 900 | | μA |
| I_{IDLE} | IDLE mode | | | 10 | | μA |
| INTERNAL SUPPLIES | | | | | | |
| V_{V6V} | Internal supply, analog | | | 6.25 | | V |
| C_{LDO_V6V} | Filter capacitor for V6V LDO | | | 100 | | nF |
| V_{V2V5} | Internal supply, logic | | | 2.5 | | V |
| C_{LDO_V2V5} | Filter capacitor for V2V5 LDO | | | 2.2 | | μF |
| DMD REGULATOR | | | | | | |
| $R_{DS(ON)}$ | MOSFET ON-resistance | Switch E (from V_{INR} to SWN) | | 1000 | | mΩ |
| | | Switch F (from SWP to PGNDR) | | 320 | | |
| V_{FW} | Forward voltage drop | Switch G ⁽²⁾ (from SWP to V_{BIAS}) $V_{INR} = 5\text{ V}, V_{SWP} = 2\text{ V}, I_F = 100\text{ mA}$ | | 1.3 | | V |
| | | Switch H (from SWP to V_{OFS}) $V_{INR} = 5\text{ V}, V_{SWP} = 2\text{ V}, I_F = 100\text{ mA}$ | | 1.3 | | |
| t_{DIS} | Rail discharge time | $V_{IN} = 2.9\text{ V}; C_{OUT} = 110\text{ nF}$ | | | 40 | μs |
| t_{PG} | Power-good timeout | Not tested in production | | 6 | | ms |
| I_{LIMIT} | Switch current limit | | | 312 | | mA |
| L | Inductor value | | | 10 | | μH |
| V_{OFS} REGULATOR | | | | | | |
| V_{OFS} | Output voltage | | | 10 | | V |
| | DC output voltage accuracy | $I_{OUT} = 2\text{ mA}$ | -2% | | 2% | |
| | DC load regulation | $V_{IN} = 3.6\text{ V}, I_{OUT} = 0\text{ to }2\text{ mA}$ | | -19 | | V/A |
| | DC line regulation | $V_{INA}, V_{INL}, V_{INR}, V_{INC} 2.7\text{ to }6.0\text{ V}, I_{OUT} = 2\text{ mA}$ | | 35 | | mV/V |
| V_{RIPPLE} | Output ripple | $V_{IN} = 3.6\text{ V}, I_{OUT} = 2\text{ mA}, C_{OUT} = 440\text{ nF}^{(3)}$ | | 375 | | mVpp |
| I_{OUT} | Output current | | 0 | | 3 | mA |

(1) Fully functional but limited parametric performance

(2) Including rectifying diode

(3) To reduce ripple the C_{OUT} can be increased. V_{RIPPLE} is inversely proportional to C_{OUT} .

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾⁽²⁾)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|--|-----|-----|-----|------|
| PG | Power-good threshold (fraction of nominal output voltage) | V _{OFS} rising | | 86% | | |
| | | V _{OFS} falling | | 66% | | |
| R _{DIS} | Output discharge resistor | Active when rail is disabled | | 100 | | Ω |
| C _{OUT} | Output capacitor | Recommended value (output capacitors for V _{OFS} /V _{BIAS} must be equal) | 110 | 220 | | nF |
| | | t _{DISCHARGE} < 40 μs at 2.9 V | 100 | | 110 | nF |

Electrical Characteristics (continued)

 over operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾⁽²⁾)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---|---|-----|--------|-----|------|
| V_{BIAS} REGULATOR | | | | | | |
| V _{BIAS} | Output voltage | | | 18 | | V |
| | DC output voltage accuracy | I _{OUT} = 2 mA | -2% | | 2% | |
| | DC load regulation | V _{IN} = 3.6 V, I _{OUT} = 0 to 2 mA | | -14 | | V/A |
| | DC line regulation | V _{INA} , V _{INL} , V _{INR} , V _{INC} 2.7 to 6 V, I _{OUT} = 2 mA | | 18 | | mV/V |
| V _{RIPPLE} | Output ripple | V _{IN} = 3.6 V, I _{OUT} = 2 mA, C _{OUT} = 440 nF (see ⁽³⁾) | | 375 | | mVpp |
| I _{OUT} | Output current | | 0 | | 4 | mA |
| PG | Power-good threshold (fraction of nominal output voltage) | V _{BIAS} rising | | 86% | | |
| | | V _{BIAS} falling | | 66% | | |
| R _{DIS} | Output discharge resistor | Active when rail is disabled | | 100 | | Ω |
| C _{OUT} | Output capacitor | Recommended value (output capacitors for V _{OFS} / V _{BIAS} must be equal) | 110 | 220 | | nF |
| | | t _{DISCHARGE} < 40 μs at 2.9 V | 100 | | 110 | |
| V_{RST} REGULATOR | | | | | | |
| V _{RST} | Output voltage | | | -14 | | V |
| | DC output voltage accuracy | I _{OUT} = 2 mA | -3% | | 3% | |
| | DC load regulation | V _{IN} = 3.6 V, I _{OUT} = 0 to 2 mA | | 13 | | V/A |
| | DC line regulation | V _{INA} , V _{INL} , V _{INR} , V _{INC} 2.7 to 6 V, I _{OUT} = 2 mA | | -21 | | mV/V |
| V _{RIPPLE} | Output ripple | V _{IN} = 3.6 V, I _{OUT} = 2 mA, C _{OUT} = 440 nF (see ⁽³⁾) | | 375 | | mVpp |
| V _{REF_VRST} | Reference voltage | | | 500 | | mV |
| I _{OUT} | Output current | | 0 | | 4 | mA |
| PG | Power-good threshold (fraction of nominal output voltage) | V _{RST} rising | | 90% | | |
| | | V _{RST} falling | | 90% | | |
| R _{DIS} | Output discharge resistor | Active when rail is disabled | | ±150 | | Ω |
| C _{OUT} | Output capacitor | | 110 | 220 | | nF |
| | | t _{DISCHARGE} < 70 μs at V _{BAT} ≥ 2.7 V | 100 | | 110 | |
| LED DRIVER | | | | | | |
| VLED BUCK-BOOST | | | | | | |
| V _{LED} | Output voltage range | | 1.2 | | 5.5 | V |
| | Default output voltage | SW4, SW5, SW6 in OPEN position | | 3.5 | | |
| V _{OVP} | Output overvoltage protection | Clamps buck-boost output | 5.5 | | 7 | V |
| V _{LED_OVP} | Fault detection threshold | Triggers VLED_OVP interrupt | | 5.4 | | V |
| I _{SW} | Switch current limit | | 3.5 | 4.0 | 4.5 | A |
| R _{DS(ON)} | MOSFET ON-resistance | Switch A (from V _{INL} to L1) | | 50 | | mΩ |
| | | Switch B (from L1 to PGNDL) | | 50 | | |
| | | Switch C (from L2 to PGNDL) | | 50 | | |
| | | Switch D (from L2 to VLED) | | 50 | | |
| f _{SW} | Switching frequency | | | 2.25 | | MHz |
| C _{OUT} | Output capacitance | | | 2 × 22 | | μF |
| RGB STROBE CONTROLLER SWITCHES | | | | | | |
| R _{DS(ON)} | Drain-source ON-resistance | SW4, SW5, SW6 | | 30 | 75 | mΩ |
| I _{LEAK} | OFF-state leakage current | V _{DS} = 5.0 V | | | 1 | μA |

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾⁽²⁾)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|--|-------|-----|------|------------------|
| LED CURRENT CONTROL | | | | | | |
| V_f | LED forward voltage | | | | 4.8 | V |
| I_{LED} | DLPA2000 LED currents | $V_{IN} \geq 2.3\text{ V}$, $V_{LED} \leq 4.8\text{ V}$ $R_{LIM} = 100\text{ m}\Omega$, 0.1%, $T_A = 25^\circ\text{C}$ (see register settings) Current at minimum code 0x00Ch for SWx IDAC[9:0]. | | 25 | | mA |
| | | $V_{IN} \geq 2.3\text{ V}$, $V_{LED} \leq 4.8\text{ V}$ $R_{LIM} = 100\text{ m}\Omega$, 0.1%, $T_A = 25^\circ\text{C}$ (see register settings) Current at maximum code 0x307h for SWx_IDAC[9:0]. | | 750 | | |
| | DC current accuracy, SW4, 5, 6 | $R_{LIM} = 100\text{ m}\Omega$ | | 25 | | mA |
| | Transient LED current limit range | $ILIM[3:0] = 0000$ at $R_{LIM} = 100\text{ m}\Omega$ | | 130 | | mA |
| $ILIM[3:0] = 1111$ at $R_{LIM} = 100\text{ m}\Omega$ | | | 1500 | | | |
| t_{rise} | Current rise time | I_{LED} from 5% to 95%, $I_{LED} = 300\text{ mA}$, Transient current limit disabled Not tested in production | | | 50 | μs |
| 1.1-V REGULATOR | | | | | | |
| VCORE (BUCK) | | | | | | |
| V_{IN} | Input voltage | | 2.3 | | 6 | V |
| V_{OUT} | Nominal fixed output voltage | | | 1.1 | | V |
| | DC output voltage accuracy | $0\text{ mA} \leq I_{OUT} \leq 600\text{ mA}$ at $V_{IN} > 2.5\text{ V}$ $V_{OUT} = 1.1\text{ V}$ | -1.5% | | 1.5% | |
| d | Maximum duty cycle | | | | 100% | |
| $R_{DS(ON)}$ | Low-side MOSFET on-resistance | $V_{IN} = 3.6\text{ V}$, $T_J = 27^\circ\text{C}$ | | 185 | 380 | $\text{m}\Omega$ |
| | High-side MOSFET on-resistance | | | 240 | 480 | $\text{m}\Omega$ |
| I_{OUT} | Output current | $V_{IN} > 2.3\text{ V}$ | | 300 | 600 | mA |
| I_{LIMIT} | Switch current limit | | | 1 | | A |
| T_{SS} | Soft-start time | Time to ramp from 10% to 90% of V_{OUT} , $V_{IN} = 3.6\text{ V}$ | | 250 | | μs |
| C_{OUT} | Output capacitance | | | 10 | | μF |
| L | Nominal Inductance | | | 2.2 | | μH |
| LOAD SWITCH | | | | | | |
| V_{IN} | Input voltage range | LS_IN | 1.8 | | 3.6 | V |
| $R_{DS(ON)}$ | P-channel MOSFET on-resistance | $V_{IN} = 1.8\text{ V}$, over full temperature range | | 385 | 505 | $\text{m}\Omega$ |
| C_{OUT} | Output capacitor | Ceramic | 4.7 | 10 | 12 | μF |
| | ESR of output capacitor | Ceramic | 5 | 20 | 500 | $\text{m}\Omega$ |
| MEASUREMENT SYSTEM (AFE) | | | | | | |
| G | Amplifier gain (PGA) | AFE_GAIN[1:0] = 01 | | 1.0 | | V/V |
| | | AFE_GAIN[1:0] = 10 | | 9.5 | | |
| | | AFE_GAIN[1:0] = 11 | | 18 | | |
| V_{OFS} | Input referred offset voltage | PGA, AFE_CAL_DIS = 1 Not tested in production | -1 | | 1 | mV |
| | | Comparator Not tested in production | -1.5 | | 1.5 | |
| t_{settle} | Settling time | To 1% of final value (not tested in production) | | | 15 | μs |
| | | To 0.1% of final value (not tested in production) | | | 52 | |

Electrical Characteristics (continued)

 over operating free-air temperature range (unless otherwise noted) (see ⁽¹⁾⁽²⁾)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----------------------------|-----|-----------------------------|--------------------|
| f_{sample} | Sampling rate | Not tested in production | | | 19 | kHz |
| LOGIC LEVELS AND TIMING CHARACTERISTICS | | | | | | |
| V_{OL} | Output low-level | $I_{\text{O}} = 0.5\text{-mA}$ sink current (RESETZ, CMP_OUT) | 0 | | 0.3 | V |
| | | $I_{\text{O}} = 5\text{-mA}$ sink current (SPI_DOUT, INTZ) | 0 | | $0.3 \times V_{\text{SPI}}$ | |
| V_{OH} | Output high-level | $I_{\text{O}} = 0.5\text{-mA}$ source current (RESETZ, CMP_OUT) | 1.3 | | 2.5 | V |
| | | $I_{\text{O}} = 5\text{-mA}$ source current (SPI_DOUT) | $0.7 \times V_{\text{SPI}}$ | | V_{SPI} | |
| V_{IL} | Input low-level | PROJ_ON, LED_SEL0, LED_SEL1 | 0 | | 0.4 | V |
| | | SPI_CSZ, SPI_CLK, SPI_DIN | 0 | | $0.3 \times V_{\text{SPI}}$ | |
| V_{IH} | Input high-level | PROJ_ON, LED_SEL0, LED_SEL1 | 1.2 | | | V |
| | | SPI_CSZ, SPI_CLK, SPI_DIN | $0.7 \times V_{\text{SPI}}$ | | V_{SPI} | |
| I_{BIAS} | Input bias current | $V_{\text{IO}} = 3.3\text{ V}$, any input pin | | | 0.5 | μA |
| t_{DEGLITCH} | Deglitch time | PROJ_ON, (not tested in production) | | 1 | | ms |
| | | LED_SEL0, LED_SEL1 pins (not tested in production) | | 300 | | ns |
| INTERNAL OSCILLATOR | | | | | | |
| f_{OSC} | Oscillator frequency | | | 9 | | MHz |
| | Frequency accuracy | $T_{\text{A}} = -30$ to 85°C | -10% | | 10% | |
| THERMAL SHUTDOWN | | | | | | |
| T_{WARN} | Thermal warning (HOT threshold) | | | 120 | | $^{\circ}\text{C}$ |
| | Hysteresis | | | 10 | | |
| T_{SHUTDOWN} | Thermal shutdown (TSD threshold) | | | 150 | | $^{\circ}\text{C}$ |
| | Hysteresis | | | 15 | | |
| MOTOR DRIVER | | | | | | |
| POWER SUPPLY | | | | | | |
| V_{INM} | Operating motor supply voltage | | 2 | | 6 | V |
| I_{M} | Operating motor current | | | | 500 ⁽⁴⁾ | mA |
| H-BRIDGE FETS | | | | | | |
| $R_{\text{DS(ON)}}$ | HS + LS FET on resistance | $V_{\text{V2V5}} = 2.5\text{ V}$, $V_{\text{M}} = 3\text{ V}$, $I_{\text{O}} = 200\text{ mA}$, $T_{\text{J}} = 25^{\circ}\text{C}$ | | 1.9 | 2.1 | Ω |
| I_{OFF} | Off-state leakage current | | | | ± 200 | nA |
| MOTOR DRIVER PROTECTION CIRCUITS | | | | | | |
| I_{OCP} | Overcurrent protection trip level per A-out or B-out pin | | 0.53 | | 1.16 | A |
| t_{TSD} | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | $^{\circ}\text{C}$ |

(4) Power dissipation and thermal limits must be observed

6.7 Motor Driver Timing Requirements

The table lists the timing numbers to drive the motor voltages correctly, while Figure 2 shows the timing sequences.

| NUMBER | | MIN | MAX | UNIT |
|--------|---|-----|-----|------|
| 1 | t_1 Delay time, xPHASE high to xOUT1 low | | 300 | ns |
| 2 | t_2 Delay time, xPHASE high to xOUT2 high | | 200 | ns |
| 3 | t_3 Delay time, xPHASE low to xOUT1 high | | 200 | ns |
| 4 | t_4 Delay time, xPHASE low to xOUT1 low | | 300 | ns |
| 5 | t_5 Delay time, xENBL high to xOUTx high | | 200 | ns |
| 6 | t_6 Delay time, xENBL high to xOUTx low | | 300 | ns |
| 7 | t_7 Output enable time | | 300 | ns |
| 8 | t_8 Output disable time | | 300 | ns |
| 9 | t_9 Delay time, xINx high to xOUTx high | | 160 | ns |
| 10 | t_{10} Delay time, xINx low to xOUTx low | | 160 | ns |
| 11 | t_R Output rise time | 30 | 188 | ns |
| 12 | t_F Output fall time | 30 | 188 | ns |

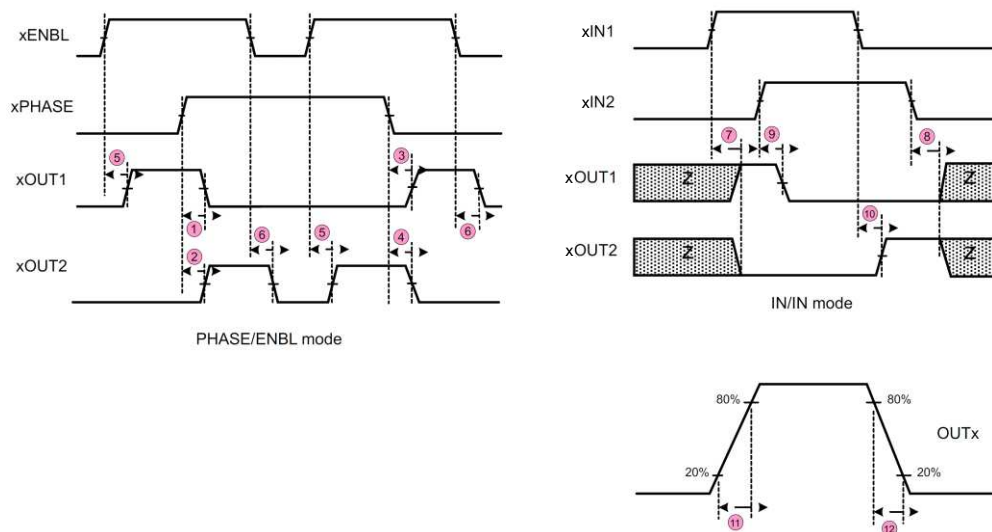


Figure 2. Bridge Control

6.8 Data Transmission Timing Requirements

VBAT = 3.6 ± 5%, T_A = 25 °C, C_L = 10 pF (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|---|-----|-----|-----|------|
| f _{CLK} | Serial clock frequency | 0 | | 36 | MHz |
| t _{CLKL} | Pulse width low, SPI_CLK, 50% level | 10 | | | ns |
| t _{CLKH} | Pulse width high, SPI_CLK, 50% level | 10 | | | ns |
| t _t | Transition time, 20% to 80% level, all signals | 0.2 | | 4 | ns |
| t _{CSCR} | SPI_CSZ falling to SPI_CLK rising, 50% level | 8 | | | ns |
| t _{CFCS} | SPI_CLK falling to SPI_CSZ rising, 50% level | | | 1 | ns |
| t _{CDS} | SPI_DIN data setup time, 50% level | 7 | | | ns |
| t _{CDH} | SPI_DIN data hold time, 50% level | 6 | | | ns |
| t _{IS} | SPI_DOUT data setup time ⁽¹⁾ , 50% level | 10 | | | ns |
| t _{IH} | SPI_DOUT data hold time ⁽¹⁾ , 50% level | 0 | | | ns |
| t _{CFDO} | SPI_CLK falling to SPI_DOUT data valid, 50% level | | | 13 | ns |
| t _{CSZ} | SPI_CSZ rising to SPI_DOUT HiZ | | | 6 | ns |

(1) The DPPxxxx processors send and receive data on the falling edge of the clock.

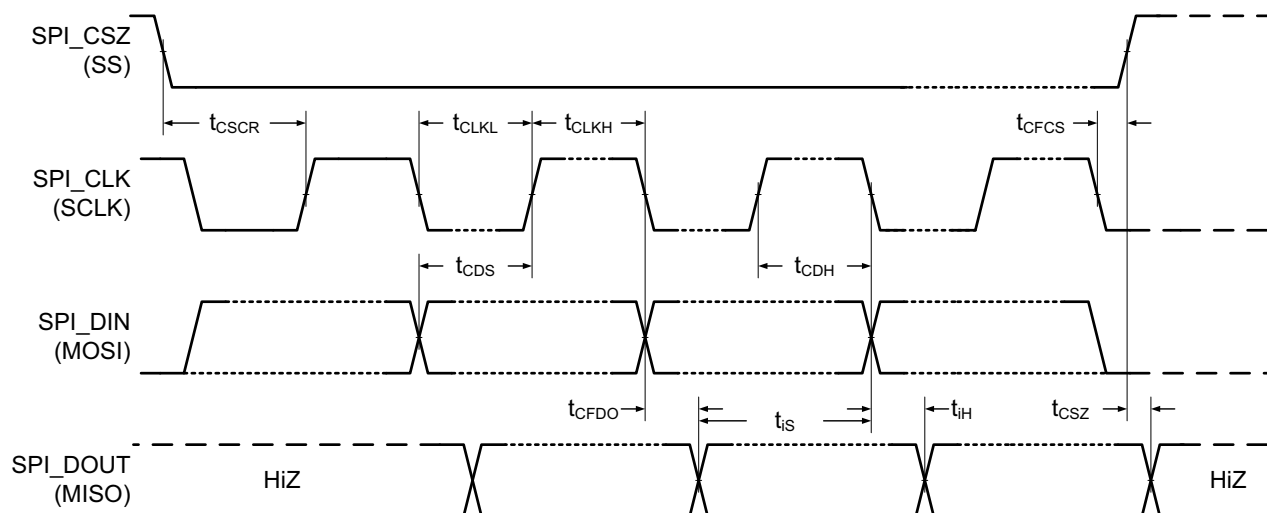
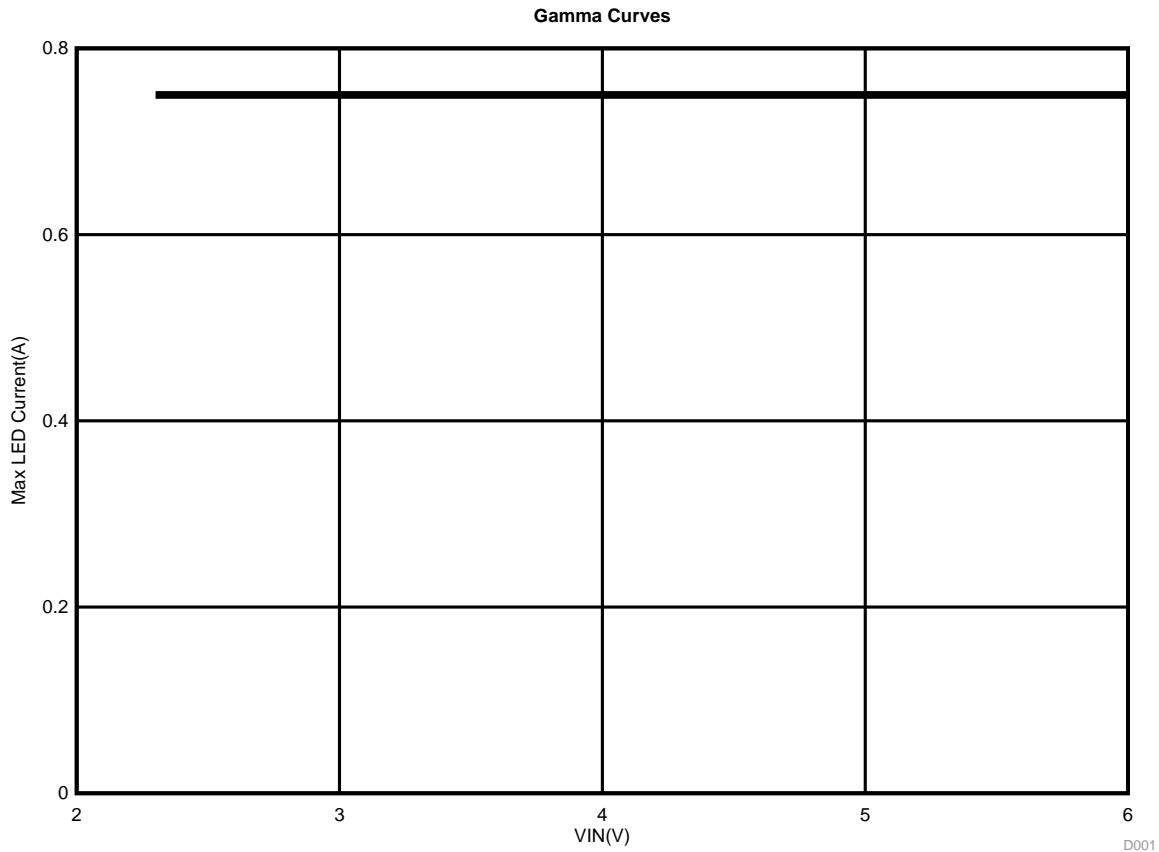


Figure 3. SPI Timing Diagram

6.9 Typical Characteristics

The maximum output current of the buck-boost is a function of input voltage (V_{IN}) and output voltage (V_{LED}). The relationship between V_{IN} , V_{LED} , and $MAX I_{LED}$ is shown in Figure 4. Note that V_{LED} is the output of the buck-boost regulator, which includes the voltage drop across the sense resistor R_{LIM} (100 m Ω typical), internal strobe control switch (75 m Ω max), and the forward voltage of the LED.



$$2.3 \text{ V} < V_{LED} < 4.8 \text{ V}$$

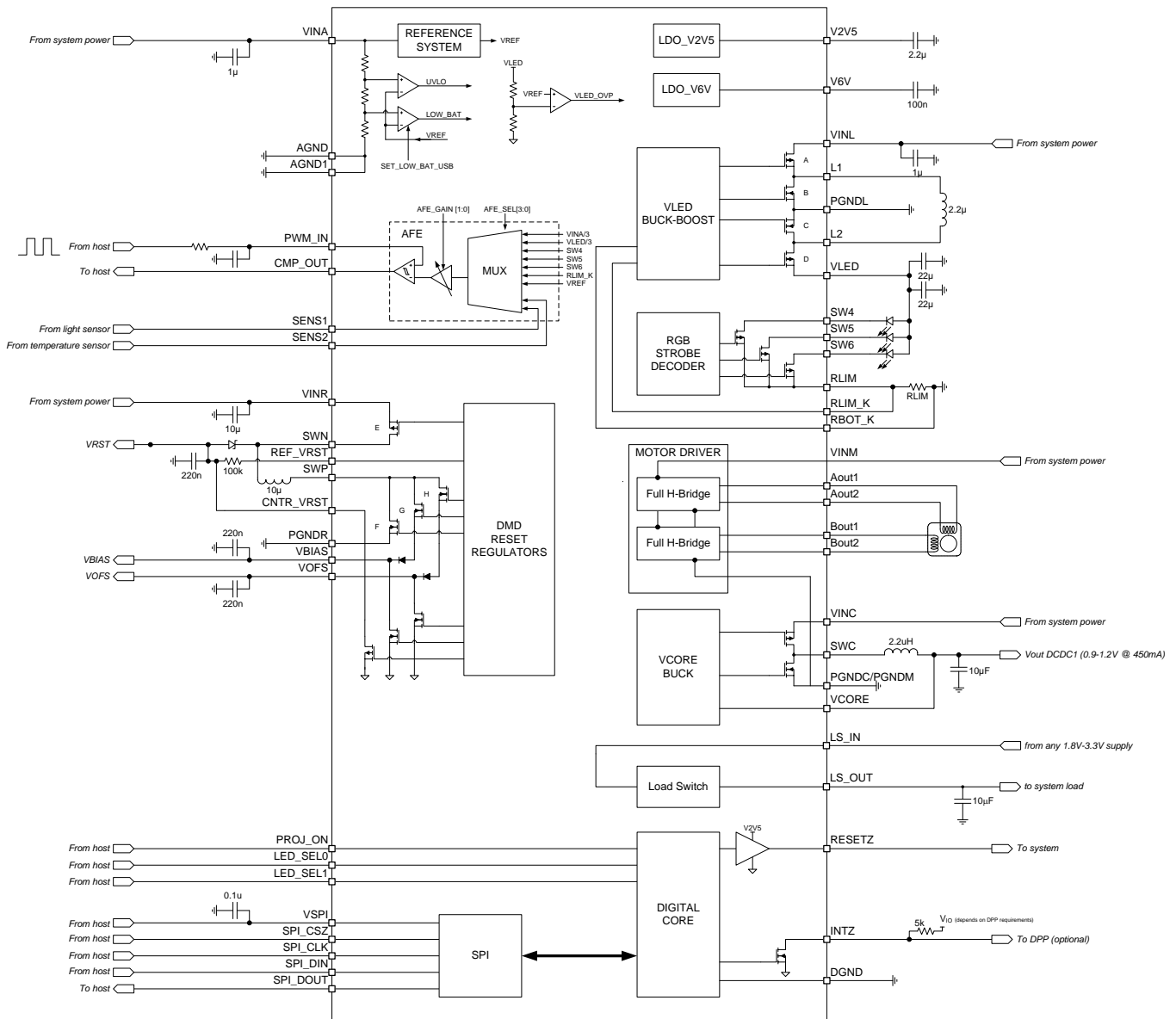
Figure 4. Maximum LED Output Current as a Function of Input Voltage (V_{IN}) and Buck-Boost Output Voltage (V_{LED})

7 Detailed Description

7.1 Overview

The DLPA2000 is a power management and LED driver IC optimized for DLP video and data display systems and meant for use in either embedded or accessory projector applications. DLPA2000 is part of the chipset comprising of either DLP2010 (0.2 WVGA) DMD and DLPC3430/DLPC3435 controller or the DLP2010NIR (0.2 WVGA NIR) DMD and DLPC150 controller. The DLPA2000 contains a complete LED driver including high efficiency power convertors. The DLPA2000 can supply up to 750 mA per LED. Integrated high-current switches are included for sequentially selecting R, G, and B LEDs. The DLPA2000 also contains three regulated DC supplies for the DMD reset circuitry: V_{BIAS} , V_{RST} and V_{OFS} , as well as a regulated DC supply of 1.1 V and a load switch for the 1.8 V to support the DLPC3430 or DLPC3435 controller. The DLPA2000 also contains a motor driver which can be used to drive the focus lens motor. The DLPA2000 has a SPI used for setting the configuration. Using SPI, currents can be set independently for each LED with 10-bit resolution. Other features included are the generation of the system reset, power sequencing, input signals for sequentially selecting the active LED, IC self-protections, and an analog MUX for routing analog information to an external ADC.

7.2 Functional Block Diagram



- Pin names refer to DLPA2000 pinout
- Pins connected to 'system power' can be locally decoupled with the capacity as indicated in the block diagram. At least adequate decoupling capacity (50 μ F or more) should be connected at the location the supply is entering the board.

7.3 Feature Description

7.3.1 DMD Regulators

DLPA2000 contains three switch-mode power supplies that power the DMD. These rails are V_{OFS} , V_{BIAS} , and V_{RST} . After pulling the PROJ_ON pin high, the DMD is first initialized followed by a power-up of the V_{OFS} line after a small delay of less than 10 ms followed by V_{BIAS} and V_{RST} with an additional delay of 145 ms. The LED driver and STROBE DECODER circuit can only be enabled after all three rails are enabled. There are two power-down sequences, the normal power-down timing initiated after pulling the PROJ_ON pin low, and a fast power-down mode where if any one of the rails encounters a fault such as an output short, all three rails are discharged simultaneously. The detailed power-up and power-down diagrams are shown in Figure 5 and Figure 6.

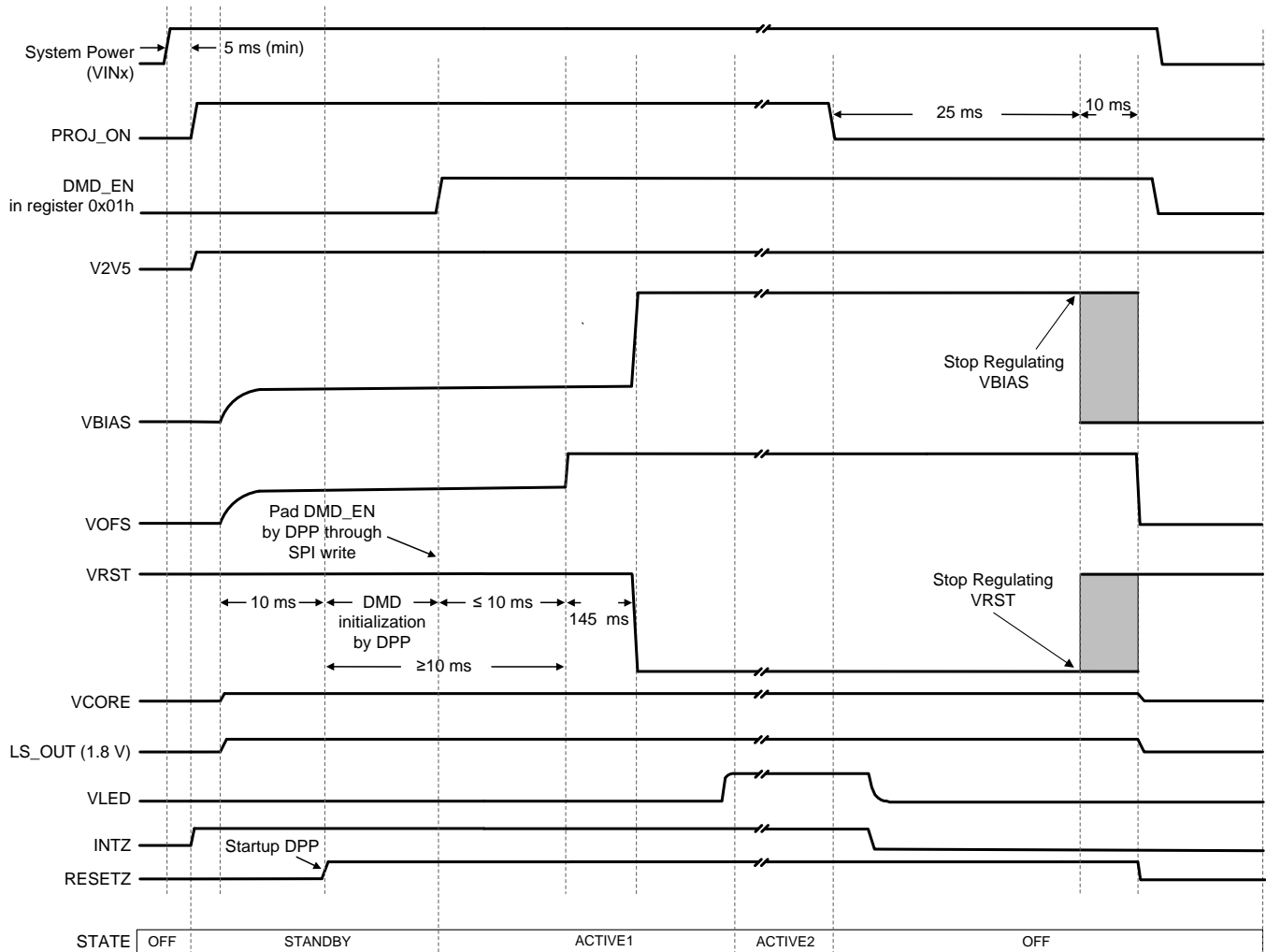
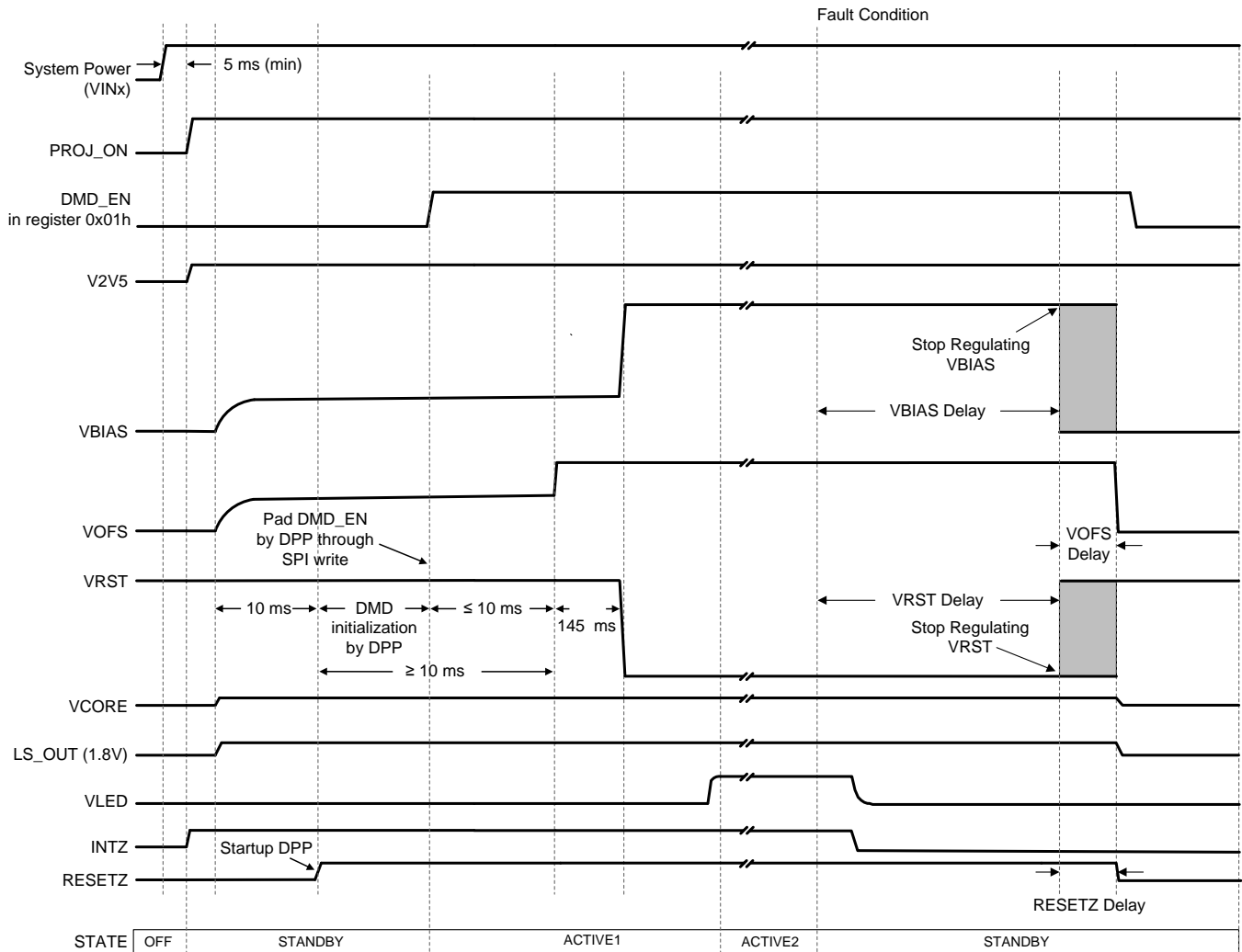


Figure 5. Power Sequence Normal Shutdown Mode

NOTE

All values are typical (unless otherwise noted).

Feature Description (continued)



A. If the FAULT condition happens and its associated interrupt is masked in the interrupt mask register (0Dh), the INTZ does not go low, but all other timing shown in the diagram is unaffected.

Figure 6. Power Sequence Fault Shutdown Mode

NOTE

All values are typical (unless otherwise noted).

7.3.2 RGB Strobe Decoder

DLPA2000 contains RGB color-sequential circuitry that is composed of three NMOS switches, the LED driver, the strobe decoder, and the LED current control. The NMOS switches are connected to the terminals of the external LED package and turn the currents through the LEDs on and off. Package connections are shown in Figure 7 and Figure 10 and the corresponding switch map is in Table 1.

The LED_SEL[1:0] signals typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. When the LED_SEL[1:0] input signals select a specific color, the NMOSFETs are controlled based on the color selected, and a 10-bit current control DAC for this color is selected that provides a control current to the RGB LEDs' feedback control network.

Feature Description (continued)

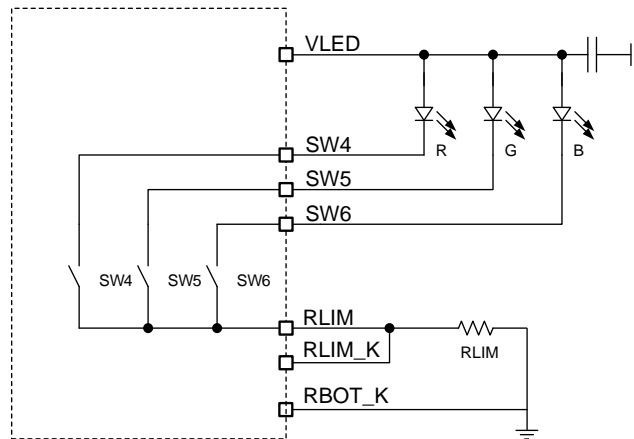


Figure 7. Switch Connection for a Common-Anode LED Assembly

Table 1. Switch Positions for Common Anode RGB LEDs (MAP = 0)

| Common Anode | | | | |
|--------------|--------|--------|--------|---------------|
| LED_SEL[1:0] | SW6 | SW5 | SW4 | IDAC INPUT |
| 0x00h | Open | Open | Open | N/A |
| 0x01h | Open | Open | Closed | SW4_IDAC[9:0] |
| 0x02h | Open | Closed | Open | SW5_IDAC[9:0] |
| 0x03h | Closed | Open | Open | SW6_IDAC[9:0] |

The switching of the three NMOS switches is controlled such that switches are returned to the open position first before the closed connections are made (break before make). The dead time between opening and closing switches is controlled through the BBM register. Switches that already are in the closed position (and are to remain in the closed state according to the SWCNTRL register) are not opened during the BBM delay time.

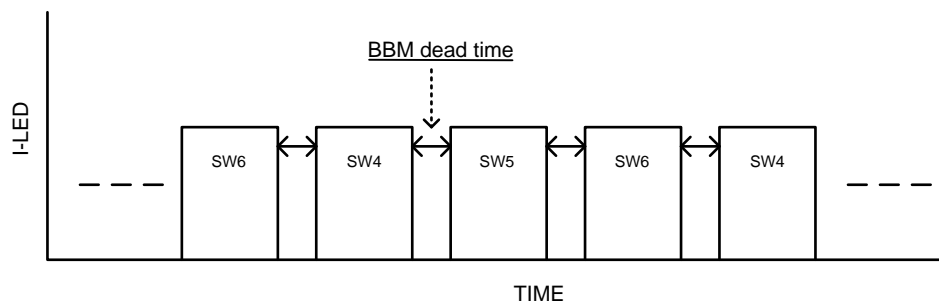


Figure 8. BBM Timing (See Register 0Bh in Figure 27)

7.3.3 LED Current Control

DLPA2000 provides time-sequential circuitry to drive three LEDs with independent current control. A system based on a common anode LED configuration is shown in Figure 10 and consists of a buck-boost converter, which provides the voltage to drive the LEDs, three switches connected to the cathodes of the LEDs, an R_{LIM} resistor used to sense the LED current, and a current DAC to control the LED current. The voltage measured at the pin V(RLIM_K) is used by the regulator loop.

The STROBE DECODER controls the switch positions as described in the previous section (RGB Strobe Decoder). With all switches in the open position, the buck-boost output assumes an output voltage of 3.5 V.

For a common-anode RGB LED configuration, the buck-boost output voltage (V_{LED}) assumes a value such that the voltage drop across the sense resistor equals:

$$(SW4_IDAC[9:0] \text{Ivalue} + I_{LED}) \times R_{LIM} \quad (1)$$

The exact value of V_{LED} depends on the current setting and the voltage drop across the LED but is limited to 5.4 V. When the STROBE decoder switches from SW4 to SW5, the buck-boost assumes a new output voltage such that the sense voltage equals:

$$(SW5_IDAC[9:0] \text{Ivalue} + I_{LED}) \times R_{LIM} \quad (2)$$

$$(SW6_IDAC[9:0] \text{Ivalue} + I_{LED}) \times R_{LIM} \quad (3)$$

The relationship between V_{IN} , V_{LED} , and $MAX I_{LED}$ is shown in [Figure 4](#).

7.3.4 Calculating Inductor Peak Current

To properly configure the DLPA2000 device, a 2.2- μ H inductor must be connected between pin L1 and pin L2. The peak current for the inductor in steady state operation can be calculated.

[Equation 4](#) shows how to calculate the peak current I_1 in step down mode operation, and [Equation 5](#) shows how to calculate the peak current I_2 in boost mode operation. V_{IN1} is the maximum input voltage, V_{IN2} is the minimum input voltage, f is the switching frequency (2.25 MHz), and L the inductor value (2.2 μ H).

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}(V_{IN1} - V_{OUT})}{2 \times V_{IN1} \times f \times L} \quad (4)$$

$$I_2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN2}} + \frac{V_{IN2}(V_{OUT} - V_{IN2})}{2 \times V_{OUT} \times f \times L} \quad (5)$$

The critical current value for selecting the right inductor is the higher value of I_1 and I_2 . Also consider that load transients and error conditions may cause higher inductor currents. This needs to be accounted for when selecting an appropriate inductor. Internally the switching current is limited to a maximum of 4 A.

7.3.5 LED Current Accuracy

The LED drive current is controlled by a current digital-to-analog converter (DAC) and can be set independently for switch SW4, SW5, and SW6. The DAC is trimmed at a current of 750 mA for the DLPA2000 at code: 0x307h. The DLPA2000 current step size is 0.95 mA.

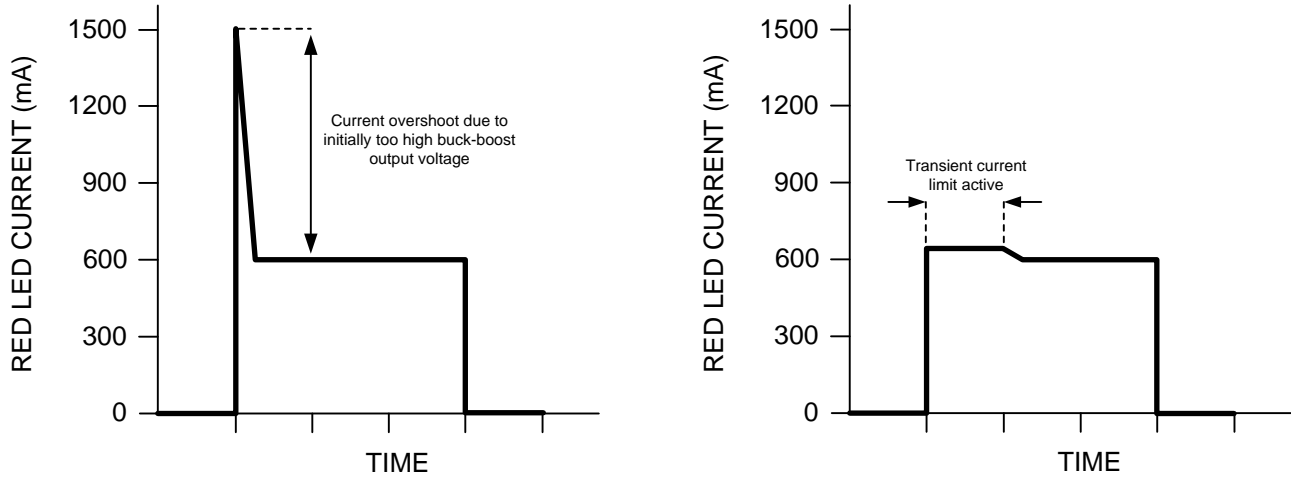
First order gain-error of the DAC can be neglected, but an offset current error must be taken into account. This offset error differs depending on the used R_{LIM} and will be ± 25 mA for the DLPA2000 for a 100-m Ω current sense resistor.

The max current of the DLPA2000 ($SWx_IDAC[9:0] = 0x307h$) is regulated to 750 mA. At the lowest setting ($SWx_IDAC[9:0] = 0x001h$) the current is regulated to 14 mA for the DLPA2000. For this current setting (0x001h), the absolute current error results into a large relative error; however, this is not a typical operating point.

Be aware that the LED current setting not only depends on the accuracy of the R_{LIM} resistor, but also strongly depends on the added resistance of PCB traces and soldering quality. Due to the low value of the current sense resistor R_{LIM} , any extra introduced resistance (for example several m Ω) will result in a noticeable different LED current.

7.3.6 Transient Current Limiting

Typically the forward voltages of the green and blue diodes are close to each other (about 3 V to 4 V). However, the forward voltage of the red diode is significantly lower (1.8 V to 2.5 V). This can lead to a current spike in the red diode when the strobe controller switches from green or blue to red because VLED is initially at a higher voltage than required to drive the RED diode. DLPA2000 provides transient current limiting for each switch to limit the current in the LEDs during the transition. The transient current limit value is controlled through the ILIM[3:0] bits in the IREG register. The same register also contains three bits to select which switch employs the transient current limiting feature. In a typical application, the transient current limit will only apply to the RED diode, and the ILIM[3:0] value will typically be set approximately 10% higher than the DC regulation current. The effect that the transient current limit has on the LED current is shown in [Figure 9](#).



Red LED current without transient current limit. The current overshoots because the buck-boost voltage starts at the (higher) level of the green or blue LED.

LED current with transient current limit.

Figure 9. RED LED Current With and Without Transient Current Limit

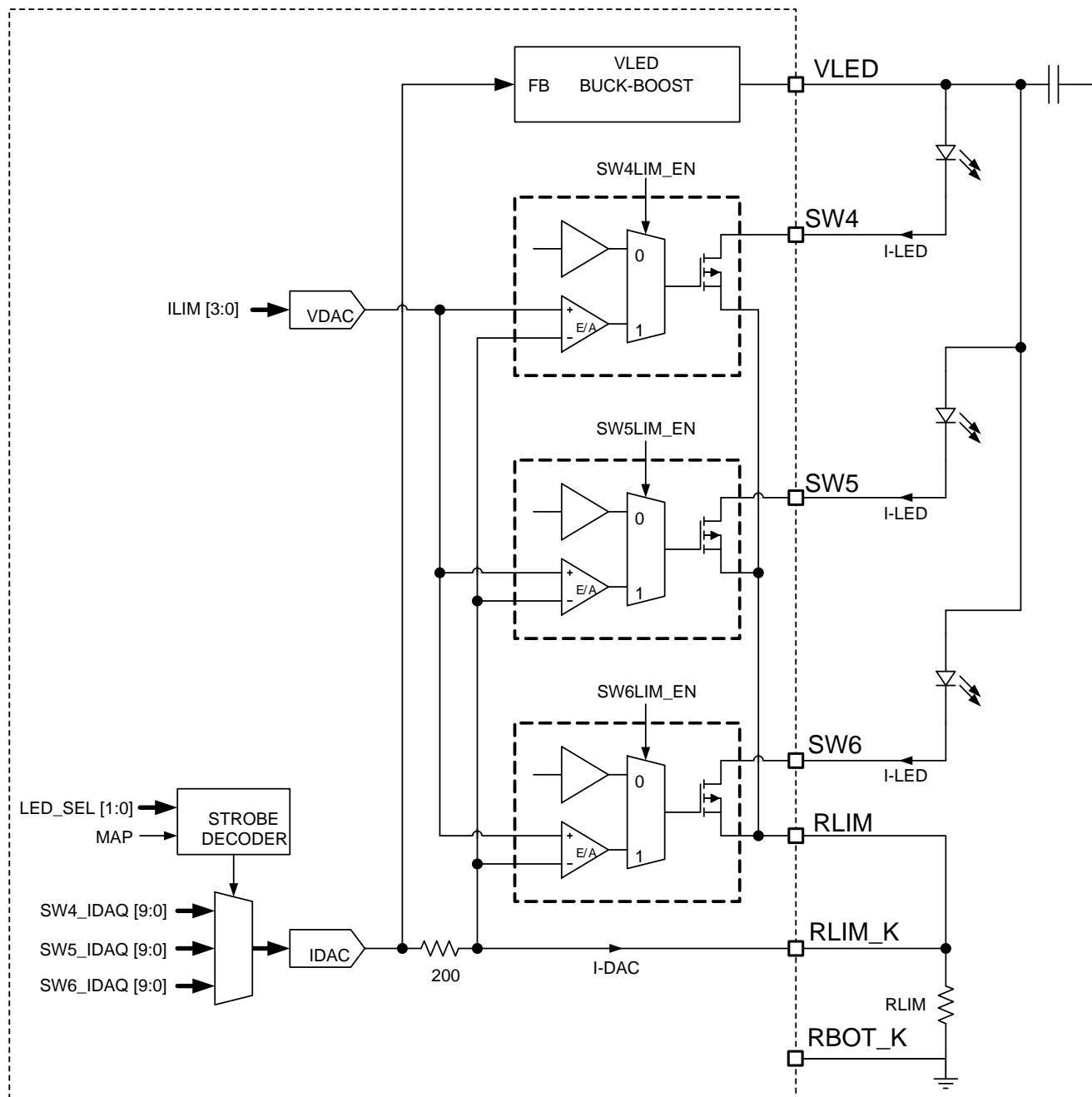


Figure 10. LED Driver Block Diagram

7.3.7 1.1-V Regulator (Buck Converter)

The buck converter creates a voltage of 1.1 V, and due to its switching nature, an output ripple with a frequency of approximately 2.25 MHz occurs on its output. This ripple is strongly dependent on the decoupling capacitor at the output in combination with the inductor. The magnitude of the ripple can be calculated with Equation 6.

$$\Delta V_{CORE} = V_{CORE} \times \frac{1 - \frac{V_{CORE}}{V_{INC}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (6)$$

The best way to minimize this ripple is to select a capacitor with a very-low ESR.

7.3.8 Motor Driver

Two control modes are available in the DLPA2000: IN/IN mode and PHASE/ENABLE mode. IN/IN mode is selected if the MODE pin is driven low or left unconnected; PHASE/ENABLE mode is selected if the MODE pin is driven to logic high. [Table 2](#) and [Table 3](#) show the logic for these modes.

The main difference between both modes is that to change the rotation direction for IN/IN mode, both xIN1 and xIN2 signals must change polarity, while for PHASE/ENABLE mode, the PHASE signal must be held high while the PHASE signal is used to change rotation direction for a DC motor. In case a stepper motor is used, the sequence of OUT1 and OUT2 determines the rotation direction.

The motor position is changed by using the internal, register-generated, control signals AIN1 and AIN2 (register 0F[123:122] in combination with BIN1 and BIN2 (register 0F[121:120]).

Table 2. IN/IN Mode (See [Figure 31](#))

| MD_MODE BIT 124 REG 0Fh | xIN1 | xIN2 | xOUT1 | xOUT2 | FUNCTION (DC MOTOR) |
|----------------------------|------|------|-------|-------|------------------------|
| 0 | 0 | 0 | Z | Z | Coast |
| 0 | 0 | 1 | L | H | Reverse |
| 0 | 1 | 0 | H | L | Forward |
| 0 | 1 | 1 | L | L | Brake |

Table 3. PHASE/ENABLE Mode (See [Figure 31](#))

| MD_MODE BIT 124 REG 0Fh | xIN1 (ENABLE) | xIN2 (PHASE) | xOUT1 | xOUT2 | FUNCTION (DC MOTOR) |
|----------------------------|------------------|-----------------|-------|-------|------------------------|
| 1 | 0 | X | L | L | Brake |
| 1 | 1 | 1 | L | H | Reverse |
| 1 | 1 | 0 | H | L | Forward |

7.3.8.1 Motor Driver Overcurrent Protection

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for a longer period of time than the overcurrent deglitch time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

7.3.9 Measurement System

The measurement system is composed of a 10:1 analog multiplexer (MUX), a programmable-gain amplifier, and a comparator. It works together with the DPP processor to provide:

- White-point correction (WPC) by independently adjusting the RGB LED currents after measuring the brightness of each color with an external light sensor
- A measurement of the:
 - Battery voltage
 - LED forward voltage
 - Exact LED current
 - Temperature as derived by measuring the voltage across an external thermistor

[Figure 11](#) shows a block diagram of the measurement system.

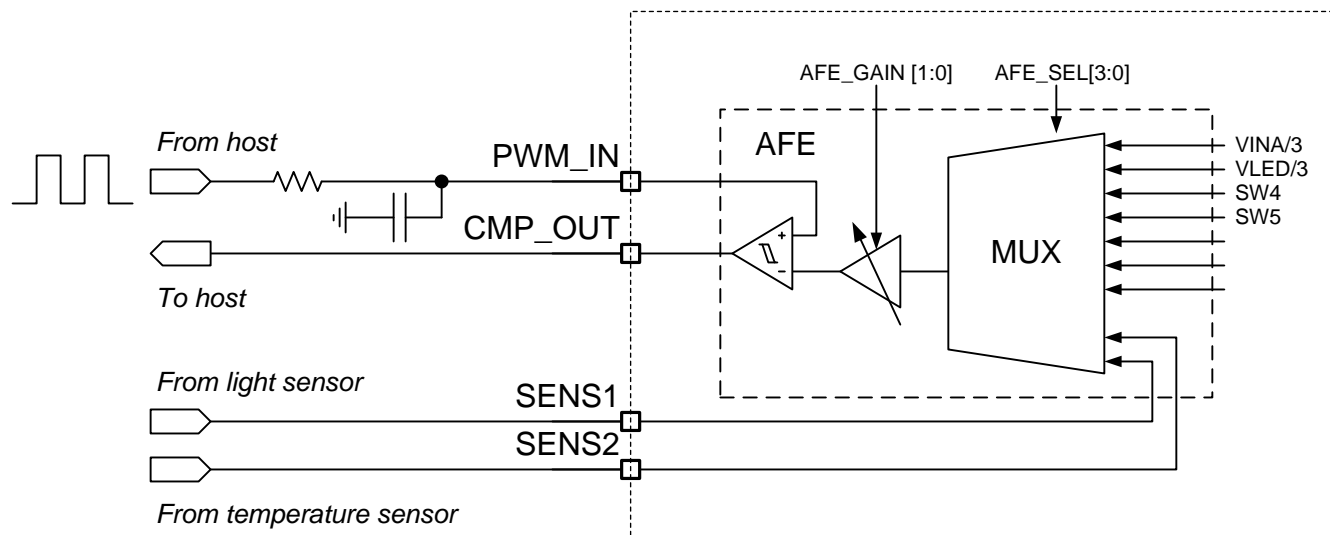


Figure 11. Block Diagram of the Measurement System

Table 4. Recommended Configuration of the AFE for Different Input Selections

| AFE_SEL[3:0] | SELECTED INPUT | RECOMMENDED GAIN SETTING AFE-GAIN[1:0] | RECOMMENDED SETTING OF AFE_CAL_DIS BIT |
|--------------|----------------|--|---|
| 0x00h | SENS2 | 0x01h (1x) | Setting has no effect on measurement. |
| 0x01h | VLED | 0x01h (1x) | Setting has no effect on measurement. |
| 0x02h | VINA | 0x01h (1x) | Setting has no effect on measurement. |
| 0x03h | SENS1 | 0x01h (1x) | Setting has no effect on measurement. |
| 0x04h | RLIM_K | 0x03h (18x) | Set to 1 if sense voltage is >100 mV. Otherwise set to 0 (default). |
| 0x05h | SW4 | 0x02h (9.5x) | Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default). |
| 0x06h | SW5 | 0x02h (9.5x) | Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default). |
| 0x07h | SW6 | 0x02h (9.5x) | Set to 1 if sense voltage is >200 mV. Otherwise set to 0 (default). |
| 0x08h | No connect | N/A | N/A. |
| 0x09h | VREF | 0x01h (1x) | Setting has no effect on measurement. |

7.3.10 Protection Circuits

DLPA2000 has several protection circuits to protect the IC and system from damage due to excessive power consumption, die temperature, or over-voltages. These circuits are described in the following sections.

7.3.10.1 Thermal Warning (HOT) and Thermal Shutdown (TSD)

DLPA2000 continuously monitors the junction temperature and issues a HOT interrupt if temperature exceeds the HOT threshold. If the temperature continues to increase above the thermal shutdown threshold, all rails are disabled and the TSD bit in the INT register is set. After the temperature drops below its threshold, the system recovers and waits for the DPP to resend the DMD_EN bit.

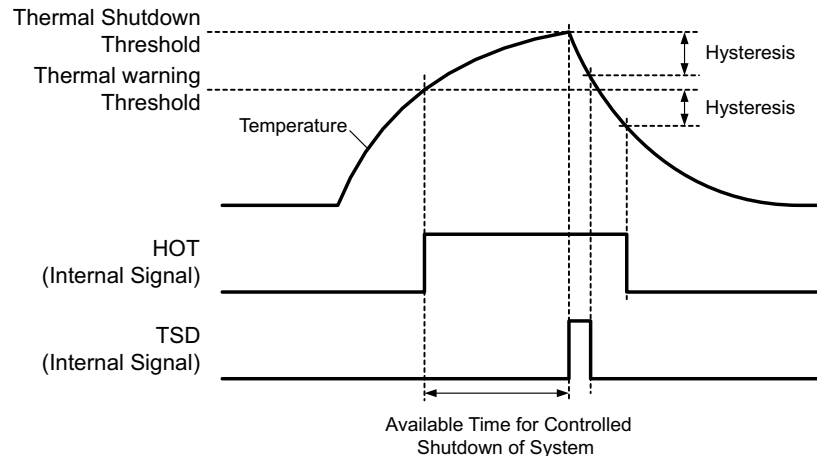


Figure 12. Definition of the Thermal Shutdown and Hot-Die Temperature Warning

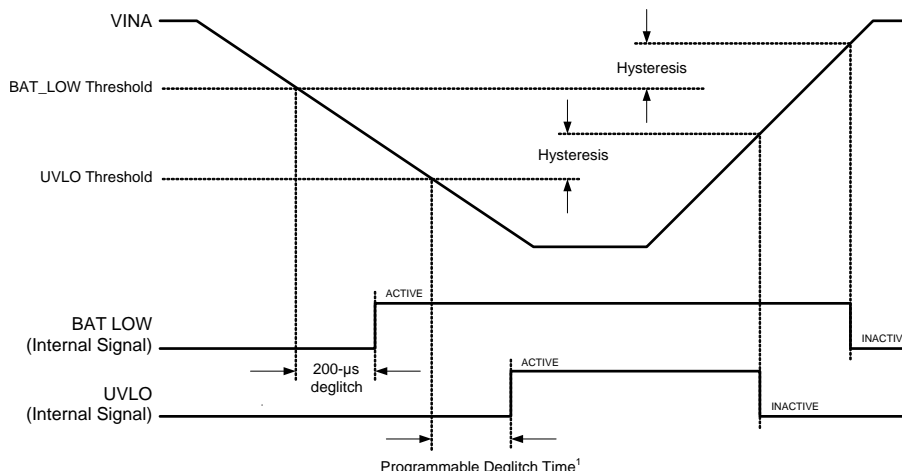
7.3.10.2 Low Battery Warning (BAT_LOW) and Undervoltage Lockout (UVLO)

If the battery voltage drops below the BAT_LOW threshold (typically 3.0 V) the BAT_LOW interrupt is issued, but normal operation continues. After the battery drops below the undervoltage threshold which has a default hardcoded value of 2.3 V (this UVLO voltage can be changed through register 09h from 2.3 V to 4.5 V), the UVLO interrupt is issued, all rails are powered down in sequence, the DMD_EN bit is reset, and the part enters STANDBY mode. The power rails cannot be re-enabled before the input voltage recovers to >2.4 V. To re-enable the rails, the PROJ_ON pin must be toggled. The undervoltage threshold is programmable from 2.3 V to 4.5 V in 31 steps.

The UVLO shutdown process will protect the DMD by allowing time for the mirrors to park, then doing a fast discharge of V_{OFS} , V_{RST} , and V_{BIAS} . This protection occurs even in the case of sudden battery removal from the projector, as long as the bulk capacitance on the battery voltage (V_{INx}) keeps this voltage above 2.3 V for as long as needed for V_{OFS} , V_{RST} , and V_{BIAS} to discharge to the required safe levels as shown in the DMD data sheet. V_{OFS} , V_{RST} , and V_{BIAS} discharge times depend on the load capacitance on each regulator. When for instance every supply is decoupled using a capacitor of 0.5 μ F, V_{INx} should stay above 2.3 V for at least 100 μ s after the battery is suddenly removed. During this time, the mirrors can be placed in a safe position and V_{OFS} , V_{RST} , and V_{BIAS} can be discharged.

NOTE

As required by the DMD data sheet, LS_OUT must stay above 1.65 V until V_{OFS} , V_{RST} , and V_{BIAS} have discharged to their required safe levels.



A. This time is programmable from 0 to 100 μ s.

Figure 13. UVLO is Asserted When the Input Supply Drops Below the UVLO Threshold

7.3.10.3 DMD Regulator Fault (DMD_FLT)

The DMD regulator is continuously monitored to check if the output rails are in regulation and if the inductor current increases as expected during a switching cycle. If either one of the output rails drops out of regulation (for example, due to a shorted output) or the inductor current does not increase as expected during a switching cycle (due to a disconnected inductor), the DMD_FLT interrupt bit is set in the INT register, the DMD_EN bit is reset, and the DMD regulator is shut down. Resetting the DMD_EN bit also causes the LED driver to power down. To restart the system, the PROJ_ON pin must be toggled. In case the interrupt is masked, it is sufficient to set the DMD_EN bit to restart the system.

7.3.10.4 V_{6V} Power-Good (V_{6V_PGF}) Fault

The LED driver regulation loop requires the V_{6V} rail for proper operation. The rail is continuously monitored and should the output drop below the power-good threshold, the V_{6V_PGF} bit is set. The V_{LED} buck-boost is then disabled and attempts to restart automatically.

7.3.10.5 V_{LED} Overvoltage (V_{LED_OVP}) Fault

If the buck-boost output voltage rises above 5.4 V, the V_{LED_OVP} interrupt is set but the buck-boost regulator is not turned off. A typical condition to cause this fault is an open LED.

7.3.10.6 V_{LED} Power Save Mode

In normal PWM operation, the efficiency of the V_{LED} buck-boost converter dramatically reduces for LED currents below 100 mA. In this case, the power save mode allows high converting efficiency at low output currents by skipping pulses in the switcher's gate driver control.

7.3.10.7 V_{1V8} PG Failure

If for any reason the voltage on the LS_OUT drops below approximately 1.3 V, then V_{OFS} , V_{BIAS} , and V_{RST} immediately go into fast shut down. Holding off power down to do mirror parking is not included since 1.3 V is too low to wait for this. Reactivating can only be done by toggling the PROJ_ON off and on again.

7.3.10.8 Interrupt Pin (INTZ)

The interrupt pin is used to signal events and fault conditions to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INTZ pin is released (returns to HiZ state) and fault bits are cleared when the INT register is read by the host.

However, if a failure persists, the corresponding INT bit remains set and the INTZ pin is pulled low again after a maximum of 32 μ s.

Interrupt events include fault conditions such as power-good faults, over-voltage, over-temperature shutdown, and UVLO. For all interrupt conditions see the interrupt register on [Figure 28](#).

The MASK register is used to mask events from generating interrupts, that is, from pulling the INTZ pin low. The MASK settings affect the INTZ pin only and have no impact on protection and monitor circuits themselves. When an interrupt is masked, the event causing the interrupt still sets the corresponding bit in the INT register. However, it does not pull the INTZ pin low.

7.3.10.9 SPI

DLPA2000 provides a 4-wire SPI port that supports high-speed serial data transfers up to 33.3 MHz. Support includes register and data buffer write and read operations. The SPI_CSZ input serves as the active low chip select for the SPI port. The SPI_CSZ input must be forced low in order to write or read registers and data buffers. When SPI_CSZ is forced high, the data at the SPI_DIN input is ignored, and the SPI_DOUT output is forced to a high-impedance state. The SPI_DIN input serves as the serial data input for the port; the SPI_DOUT output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data is latched at the SPI_DIN input on the rising edge of SPI_CLK, while data is clocked out of the SPI_DOUT output on the falling edge of SPI_CLK. [Figure 14](#) shows the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in [Figure 14](#), the auto-increment mode is invoked by simply holding the SPI_CSZ input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

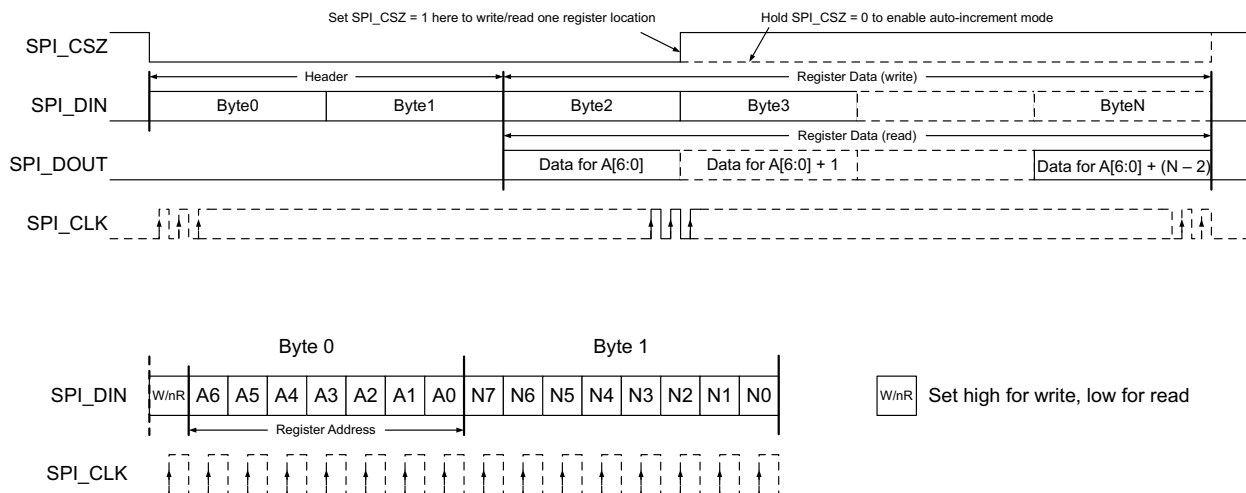


Figure 14. SPI Protocol

7.3.11 Password Protected Registers

Register addresses 0x11h through 0x27h can be read-accessed the same way as any other register, but are protected against accidental write operations through the PASSWORD register (address 0x10h). To write to a protected register, follow these steps:

1. Write data 0xBAh to register address 0x10h.
2. Write data 0xBEh to register address 0x10h.

Both writes must be consecutive, that is, there must be no other read or write operation in between sending the two bytes. After the password has been successfully written, registers 0x11h through 0x27h are unlocked and can be write accessed using the regular SPI protocol. They remain unlocked until any byte other than 0xBAh is written to the PASSWORD register or the part is power cycled.

To check if the registers are unlocked, read back the PASSWORD register. If the data returned is 0x00h, the registers are locked. If the PASSWORD register returns 0x01h, the registers are unlocked.

7.4 Device Functional Modes

Table 5. Modes of Operation

| MODE | DESCRIPTION |
|---------|--|
| OFF | This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values, and the IC does not respond to SPI commands. RESETZ pin is pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is low. |
| STANDBY | The DMD regulators and LED power (V_{LED}) are turned off, but the IC does respond to the SPI. The device enters STANDBY mode whenever PROJ_ON is set high or DMD_EN ⁽¹⁾ bit is set to 0 using the SPI interface after PROJ_ON is already high. The device also enters STANDBY mode when a fault condition is detected ⁽²⁾ . (See Protection Circuits). |
| ACTIVE1 | The DMD supplies are enabled but LED power (V_{LED}) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and V_{LED_EN} ⁽³⁾ bit is set to 0. |
| ACTIVE2 | DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and V_{LED_EN} bits must both be set to 1. |

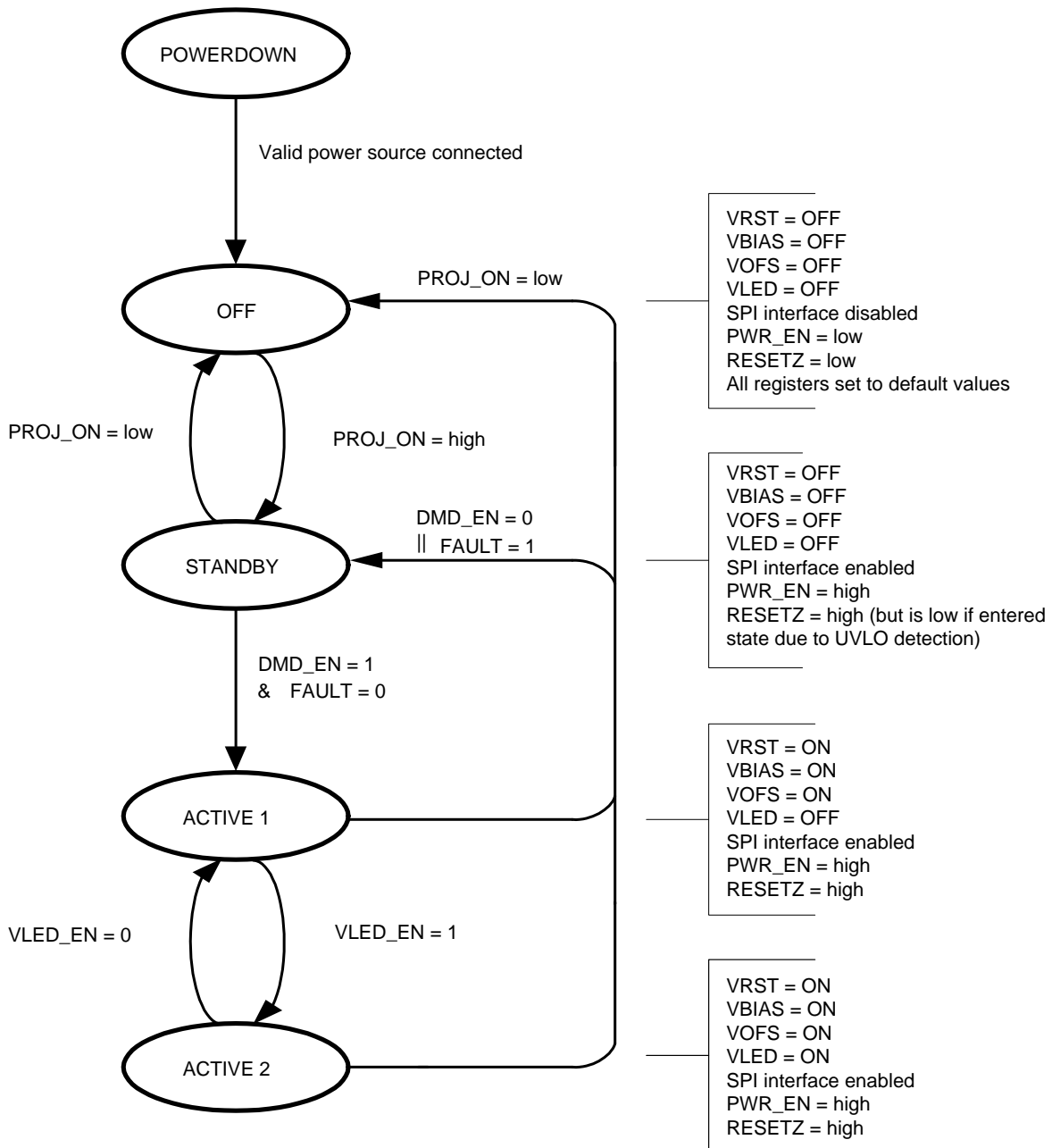
(1) Settings can be done through Reg01h [9] and Reg2E [119].

(2) Power-good faults, over-voltage, overtemperature shutdown, and undervoltage lockout.

(3) Settings can be done through Reg47h [60], bit is named $V_{LED_EN_SET}$.

Table 6. Device State as a Function of Control-Pin Status

| PROJ_ON PIN | STATE |
|-------------|--|
| LOW | OFF |
| HIGH | STANDBY ACTIVE1 ACTIVE2 (Device state depends on DMD_EN and V_{LED_EN} bits and whether there are any fault conditions.) |



- A. || = OR, & = AND.
- B. FAULT = Undervoltage on any supply (except LS_OUT), thermal shutdown, or UVLO detection.
- C. UVLO detection, per the diagram, causes the DLPA2000 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ_ON should be set low.
- D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DPP ASIC software automatically sets it to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.
- E. PWR_EN is a signal internal to the PAD200x. This signal turns on the VCORE regulator and the load switch that drives pin LS_OUT.

Figure 15. State Diagram

7.5 Register Maps

Table 7. Register Description

| REGISTER | ADDRESS (HEX) | NAME | TABLE | DESCRIPTION | DEFAULT |
|---|---------------|------------|---------------------|---|---------|
| USER CONFIGURATION DEFINITIONS | | | | | |
| R | 0x00 | CHIP ID | Figure 16 | Chip revision register; DLPA2000 | B3 |
| R/W | 0x01 | CHIPENABLE | Figure 17 | Enable register | 0F |
| R/W | 0x02 | IREG | Figure 18 | Transient-current limit settings | 30 |
| R/W | 0x03 | SW4MSB | Figure 19 | Regulation current MSB, SW4 | 0 |
| R/W | 0x04 | SW4LSB | Table 12, Table 13 | Regulation current LSB, SW4 | 0 |
| R/W | 0x05 | SW5MSB | Figure 21 | Regulation current MSB, SW5 | 0 |
| R/W | 0x06 | SW5LSB | Figure 22, Table 16 | Regulation current LSB, SW5 | 0 |
| R/W | 0x07 | SW6MSB | Figure 23 | Regulation current MSB, SW6 | 0 |
| R/W | 0x08 | SW6LSB | Figure 24, Table 19 | Regulation current LSB, SW6 | 0 |
| R/W | 0x09 | SWCNTRL | Figure 25 | Switch ON/OFF control (direct mode) | 0 |
| R/W | 0x0A | AFE | Figure 26 | AFE (MUX) control | 0 |
| R/W | 0x0B | BBM | Figure 27, Table 22 | Break before make timing | 0 |
| R | 0x0C | INT | Figure 28, Table 23 | Interrupt register | 0 |
| R/W | 0x0D | INT MASK | Figure 29, Table 24 | Interrupt mask register | DFh |
| R/W | 0x0E | TIMING | Figure 30, Table 26 | Timing register V_{OFS} , V_{BIAS} , V_{RST} , and RESETZ | 7 |
| R/W | 0x0F | MOTOR CTRL | Figure 31, Table 27 | Motor control register | 0 |
| USER PROTECTED DEFINITION | | | | | |
| R/W | 0x10 | PASSWORD | Figure 32 | Password register | 0 |
| R/W | 0x11 | SYSTEM | Figure 33 | System configuration register | 0 |
| USER EEPROM SCRATCH PAD DEFINITION | | | | | |
| R/W | 0x20 | BYTE0 | Figure 34 | User EEPROM, Byte0 | 0 |
| R/W | 0x21 | BYTE1 | Figure 35 | User EEPROM, Byte1 | 0 |
| R/W | 0x22 | BYTE2 | Figure 36 | User EEPROM, Byte2 | 0 |
| R/W | 0x23 | BYTE3 | Figure 37 | User EEPROM, Byte3 | 0 |
| R/W | 0x24 | BYTE4 | Figure 38 | User EEPROM, Byte4 | 0 |
| R/W | 0x25 | BYTE5 | Figure 39 | User EEPROM, Byte5 | 0 |
| R/W | 0x26 | BYTE6 | Figure 40 | User EEPROM, Byte6 | 0 |
| R/W | 0x27 | BYTE7 | Figure 41 | User EEPROM, Byte7 | 0 |

7.5.1 Chip Revision Register

Figure 16. Chip Revision Register, Address = 00h, HEX = B3

| | | | | | | | |
|---------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHIP ID [7:0] | | | | | | | |
| R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 8. Chip Revision Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|---------|------|-------|-------------|
| 7:4 | CHIP ID | R | 1011 | CHIPID<3:0> |
| 3:0 | | R | 0011 | REVID<3:0> |

7.5.2 Enable Register

Figure 17. Enable Register, Address = 01h, HEX = 0F

| | | | | | | | |
|-------------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHIPENABLE [15:8] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Enable Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|------------|------|-------|---|
| 15:12 | CHIPENABLE | R/W | 0000 | USER_GPO<3:0> |
| 11 | | R/W | 1 | VLED_POWER_SAVE_MODE_DIS Power save mode is used to improve efficiency at light load. |
| 10 | | R/W | 1 | FAST_SHUTDOWN_EN Applicable only during a fault condition. Shutdown timing is defined by register 0Eh (see Figure 7). |
| 9 | | R/W | 1 | DMD_EN |
| 8 | | R/W | 1 | VLED_EN |

7.5.3 Transient-Current Limit Settings

Figure 18. Transient-Current Limit Settings, Address = 02h, HEX = 30

| | | | | | | | |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IREG [23:16] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 10. Transient-Current Limit Settings Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION | |
|-------|-----------|------|-------|--|--------|
| 23 | RSVD | R/W | 0 | Not used | |
| 22:19 | IREG | R/W | 0110 | IREG_ILIM<3:0> | |
| | | | | $R_{LIM} = 100 \text{ m}\Omega$ | |
| | | | | 0000 | 130 mA |
| | | | | 0001 | 150 mA |
| | | | | 0010 | 172 mA |
| | | | | 0011 | 192 mA |
| | | | | 0100 | 220 mA |
| | | | | 0101 | 275 mA |
| | | | | 0110 | 330 mA |
| | | | | 0111 | 440 mA |
| | | | | 1000 | 550 mA |
| | | | | 1001 | 660 mA |
| | | | | 1010 | 770 mA |
| 18 | SW6LIM_EN | R/W | 0 | SW6LIM_EN Transient current-limit enable for SW6 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled | |

Table 10. Transient-Current Limit Settings Field Descriptions (continued)

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-----------|------|-------|--|
| 17 | SW5LIM_EN | R/W | 0 | SW5LIM_EN Transient current-limit enable for SW5 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled |
| 16 | SW4LIM_EN | R/W | 0 | SW4LIM_EN Transient current-limit enable for SW4 0 – Transient current-limit is disabled 1 – Transient current-limit is enabled |

7.5.4 Regulation Current MSB, SW4

Figure 19. Regulation Current MSB, SW4, Address = 03h, HEX = 00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| SW4MSB [31:24] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 11. Regulation Current MSB, SW4 Field Descriptions⁽¹⁾

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|--------|------|-------|---------------|
| 31:26 | SW4MSB | R/W | 0000 | TBD |
| 25:24 | | R/W | 0000 | SW4_IDAC<9:8> |

(1) The DLPA2000 can use up to code 0x0FFh for SW4_IDAC[9:0].

7.5.5 Regulation Current LSB, SW4

Figure 20. Regulation Current LSB, SW4, Address = 04h, HEX = 00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| SW4LSB [39:32] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 12. Regulation Current LSB, SW4 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|--------|------|----------|---------------|
| 39:32 | SW4LSB | R/W | 00000000 | SW4_IDAC<7:0> |

Table 13. Regulation Current LSB, SW4 Bit Definitions

| DLPA2000 ⁽¹⁾⁽²⁾ | | | | | |
|----------------------------|-------------|---------------|-------------|---------------|-------------|
| SW4_IDAC[9:0] | LED CURRENT | SW4_IDAC[9:0] | LED CURRENT | SW4_IDAC[9:0] | LED CURRENT |
| 0x000h | 0 mA | 0x100h | 257 mA | 0x200h | 500 mA |
| 0x00Ch | 25 mA | 0x101h | 258 mA | 0x201h | 501 mA |
| 0x00Dh | 26 mA | 0x102h | 259 mA | 0x202h | 502 mA |
| ... | ... | ... | ... | ... | ... |
| 0x0FEh | 255 mA | 0x1FEh | 498 mA | 0x306h | 749 mA |
| 0x0FFh | 256 mA | 0x1FFh | 499 mA | 0x307h | 750 mA |

(1) Values shown are for a typical DLPA2000 unit at T = 25°C. Typical step size is 0.95 mA for R_{LIM} = 100 mΩ.

(2) The DLPA2000 can use up to code 0x307h for SW4_IDAC[9:0].

7.5.6 Regulation Current MSB, SW5
Figure 21. Regulation Current MSB, SW5, Address = 05h, HEX = 00

| | | | | | | | |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW5MSB [47:40] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 14. Regulation Current MSB, SW5 Field Descriptions⁽¹⁾

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|--------|------|-------|---------------|
| 47:42 | SW5MSB | R/W | 0000 | TBD |
| 41:40 | | R/W | 0000 | SW5_IDAC<9:8> |

(1) The DLPA2000 can use up to code 0x0FFh for SW5_IDAC[9:0].

7.5.7 Regulation Current LSB, SW5
Figure 22. Regulation Current LSB, SW5, Address = 06h, HEX = 00

| | | | | | | | |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW5LSB [55:48] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 15. Regulation Current LSB, SW5 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|--------|------|----------|---------------|
| 55:48 | SW5LSB | R/W | 00000000 | SW5_IDAC<7:0> |

Table 16. Regulation Current LSB, SW5 Bit Definitions

| DLPA2000 ⁽¹⁾⁽²⁾ | | | | | |
|----------------------------|-------------|---------------|-------------|---------------|-------------|
| SW5_IDAC[9:0] | LED CURRENT | SW5_IDAC[9:0] | LED CURRENT | SW5_IDAC[9:0] | LED CURRENT |
| 0x000h | 0 mA | 0x100h | 257 mA | 0x200h | 500 mA |
| 0x00Ch | 25 mA | 0x101h | 258 mA | 0x201h | 501 mA |
| 0x00Dh | 26 mA | 0x102h | 259 mA | 0x202h | 502 mA |
| ... | ... | ... | ... | ... | ... |
| 0x0FEh | 255 mA | 0x1FEh | 498 mA | 0x306h | 749 mA |
| 0x0FFh | 256 mA | 0x1FFh | 499 mA | 0x307h | 750 mA |

 (1) Values shown are for a typical DLPA2000 unit at T = 25°C. Typical step size is 0.95 mA for R_{LIM} = 100 mΩ.

(2) The DLPA2000 can use up to code 0x307h for SW5_IDAC[9:0].

7.5.8 Regulation Current MSB, SW6

Figure 23. Regulation Current MSB, SW6, Address = 07h, HEX = 00

| | | | | | | | |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW6MSB [63:56] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 17. Regulation Current MSB, SW6 Field Descriptions⁽¹⁾

| BIT | FIELD | Type | Reset | Description |
|-------|--------|------|-------|---------------|
| 63:58 | SW6MSB | R/W | 0000 | TBD |
| 57:56 | | R/W | 0000 | SW6_IDAC<9:8> |

(1) The DLPA2000 can use up to code 0x0FFh for SW6_IDAC[9:0].

7.5.9 Regulation Current LSB, SW6

Figure 24. Regulation Current LSB, SW6, Address = 08h, HEX = 00

| | | | | | | | |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SW6LSB [71:64] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 18. Regulation Current LSB, SW6 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|--------|------|----------|---------------|
| 71:64 | SW6LSB | R/W | 00000000 | SW6_IDAC<7:0> |

Table 19. Regulation Current LSB, SW6 Bit Definitions

| DLPA2000 ⁽¹⁾⁽²⁾ | | | | | |
|----------------------------|-------------|---------------|-------------|---------------|-------------|
| SW6_IDAC[9:0] | LED CURRENT | SW6_IDAC[9:0] | LED CURRENT | SW6_IDAC[9:0] | LED CURRENT |
| 0x000h | 0 mA | 0x100h | 257 mA | 0x200h | 500 mA |
| 0x00Ch | 25 mA | 0x101h | 258 mA | 0x201h | 501 mA |
| 0x00Dh | 26 mA | 0x102h | 259 mA | 0x202h | 502 mA |
| ... | ... | ... | ... | ... | ... |
| 0x0FEh | 255 mA | 0x1FEh | 498 mA | 0x306h | 749 mA |
| 0x0FFh | 256 mA | 0x1FFh | 499 mA | 0x307h | 750 mA |

(1) Values shown are for a typical DLPA2000 unit at T = 25°C. Typical step size is 0.95 mA for R_{LIM} = 100 mΩ.

(2) The DLPA2000 can use up to code 0x307h for SW6_IDAC[9:0].

7.5.10 Switch On/Off Control (Direct Mode)

Figure 25. Switch On/Off Control (Direct Mode), Address = 09h, HEX = 00

| | | | | | | | |
|-----------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SWCNTRL [79:72] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 20. Switch On/Off Control (Direct Mode) Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION | | | |
|-------|---------|------|-------|---|---|--|--|
| 79 | SWCNTRL | R/W | 0 | SW6 (controls switch 6 if direct mode (see reg 11h) is enabled) | 00000 00001 11110 11111 | 2.3 V (minimum value – default value) 2.37 V Step approximately 70 mV 4.43 V 4.5 V (maximum value) | |
| 78 | | R/W | 0 | SW5 (controls switch 5 if direct mode (see reg 11h) is enabled) | | | |
| 77 | | R/W | 0 | SW4 (controls switch 4 if direct mode (see reg 11h) is enabled) | | | |
| 76:72 | | R/W | 00000 | UVLO_TRIM<4:0> | | | |

7.5.11 AFE (MUX) Control

Figure 26. AFE (MUX) Control, Address = 0Ah, HEX = 00

| | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AFE [87:80] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 21. AFE (MUX) Control Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|-------|---------------|
| 87 | AFE | R/W | 00 | AFE_EN |
| 86 | | R/W | 00 | AFE_CAL_DIS |
| 85:84 | | R/W | 00 | AFE_GAIN<1:0> |
| 83:80 | | R/W | 00 | AFE_SEL<3:0> |

7.5.12 Break Before Make (BBM) Timing

Figure 27. BBM Timing, Address = 0Bh, HEX = 00

| | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BBM [95:88] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 22. BBM Timing Field Descriptions⁽¹⁾

| BIT | FIELD | TYPE | RESET | DESCRIPTION | | | |
|-------|-------|------|----------|----------------|-----------------|-----------------|-----------------|
| 95:88 | BBM | R/W | 00000000 | BBM_DELAY<7:0> | | | |
| | | | | 0x00 – 0 ns | 0x40 – 7326 ns | 0x80 – 14430 ns | 0xC0 – 21534 ns |
| | | | | 0x01 – 333 ns | 0x41 – 7437 ns | 0x81 – 14541 ns | 0xC1 – 21645 ns |
| | | | | 0x02 – 444 ns | 0x42 – 7548 ns | 0x82 – 14652 ns | 0xC2 – 21756 ns |
| | | | | ... | ... | ... | ... |
| | | | | 0x3E – 7104 ns | 0x7E – 14208 ns | 0xBE – 21312 ns | 0xFE – 28416 ns |
| | | | | 0x3F – 7215 ns | 0x7F – 14319 ns | 0xBF – 21423 ns | 0xFF – 28527 ns |

(1) It takes 333 to 444 ns to turn off the switches from the time a change occurs on LED_SEL[1:0].

7.5.13 Interrupt Register

Figure 28. Interrupt Register, Address = 0Ch, HEX = 00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|
| INT [103:96] | | | | | | | |
| R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 23. Interrupt Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-------|------|-------|---|
| 103 | INT | R | 0 | V_{LED_OVP} $V_{LED_buck_boost}$ overvoltage fault interrupt (normal operation resumes) 0 – No fault 1 – Buck_boost output is above OVP threshold |
| 102 | | R | 0 | IREG_PG_FAULT V_{6V} power-good fault interrupt (normal operation resumes) 0 – No fault 1 – V_{6V} is not in regulation |
| 101 | | R | 0 | PROJ_ON_INT Proj_On interrupt (part enters OFF mode) 0 – Pin is pulled high, normal mode 1 – Pin is pulled low, alerts the DPP that the DMD regulator is about to shut down. |
| 100 | | R | 0 | DMD_FAULT DMD regulator fault (part enters STANDBY mode and DMD_EN bit is cleared) 0 – No fault 1 – The inductor current is not increasing at the correct rate, likely to be caused by an open inductor. Or, one of the regulator outputs has dropped below the power-good threshold, likely to be caused by a short. |
| 99 | | R | 0 | UVLO UVLO interrupt (sensed at V_{INA} pin), DMD bit is cleared. 0 – Battery voltage is above the UVLO threshold. 1 – Battery voltage has dropped below the UVLO threshold. |
| 98 | | R | 0 | BAT_LOW_WARN Low battery warning interrupt (sensed at V_{INA} pin, normal operation resumes) 0 – Battery voltage is above the low-battery threshold 1 – Battery voltage has dropped below the low-battery threshold |
| 97 | | R | 0 | TS_WARN Thermal warning interrupt (normal operation resumes) 0 – Die temperature is in normal operating range 1 – Die temperature is above the HOT threshold Or, part has not cooled down enough to recover from HOT. |
| 96 | | R | 0 | TS_WARN Thermal Warning Interrupt (normal operation resumes) 0 – Die temperature is in normal operating range 1 – Die temperature is above the HOT threshold Or, part has not cooled down enough to recover from HOT. |

7.5.14 Interrupt Mask Register
Figure 29. Interrupt Mask Register, Address = 0Dh, HEX = DF

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|-----|-----|-----|-----|-----|
| INT MASK [111:104] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 24. Interrupt Mask Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|----------|------|-------|---|
| 111 | INT MASK | R/W | 1 | V _{LED} BUCK_BOOST Overvoltage fault interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked |
| 110 | | R/W | 1 | I _{REG_PG_FAULT_MASK} 0 – Interrupt is not masked 1 – Interrupt is masked |
| 109 | | R/W | 0 | PROJ_ON interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked |
| 108 | | R/W | 1 | DMD_REGULATOR fault mask 0 – Interrupt is not masked 1 – Interrupt is masked |
| 107 | | R/W | 1 | UVLO_MASK 0 – Interrupt is not masked 1 – Interrupt is masked |
| 106 | | R/W | 1 | Low battery warning mask (sensed at V _{INA} pin) 0 – Interrupt is not masked 1 – Interrupt is masked |
| 105 | | R/W | 1 | Thermal shutdown interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked |
| 104 | | R/W | 1 | Thermal warning interrupt mask 0 – Interrupt is not masked 1 – Interrupt is masked |

7.5.15 Timing Register V_{OFS} , V_{BIAS} , V_{RST} , and RESETZ

Figure 30. Timing Register V_{OFS} , V_{BIAS} , V_{RST} , and RESETZ, Address = 0Eh, HEX = 07

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| TIMING [119:112] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 25. Timing Register VOFS, VBIAS, VRST, and RESETZ Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---------|--------|------|-------|---|
| 119:116 | TIMING | R/W | 0000 | $V_{OFS}/RESETZ_DELAY<3:0>$ (for values see minimum and maximum delay) |
| 115:112 | | R/W | 0111 | $V_{BIAS}/V_{RST_DELAY<3:0>}$ (for values see minimum and maximum delay) |

Table 26. Timing Register V_{OFS} , V_{BIAS} , V_{RST} , and RESETZ Bit Definitions

| FIELD NAME | BIT | BIT DEFINITION | | |
|------------|-----------|----------------|--------------------------|--------------------------|
| | | | Minimum Delay (μ s) | Maximum Delay (μ s) |
| TIMING | [119:112] | 0000 | 4.0 | 4.4 |
| | | 0001 | 8.0 | 8.9 |
| | | 0010 | 16.0 | 17.8 |
| | | 0011 | 32.0 | 35.5 |
| | | 0100 | 64.0 | 71.1 |
| | | 0101 | 128.0 | 142.2 |
| | | 0110 | 256.0 | 284.4 |
| | | 0111 | 512.0 | 569.0 |
| | | 1000 | 6.2 | 7.1 |
| | | 1001 | 12.4 | 14.2 |
| | | 1010 | 24.9 | 28.4 |
| | | 1011 | 49.8 | 56.9 |
| | | 1100 | 99.5 | 113.8 |
| | | 1101 | 199.1 | 227.6 |
| | | 1110 | 398.3 | 455.2 |
| | | 1111 | 1024.2 | 1138.0 |

7.5.16 Motor Control Register

Figure 31. Motor Control Register, Address = 0Fh, HEX = 00⁽¹⁾

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|-----|-----|-----|-----|-----|-----|-----|
| MOTOR CTRL [127:120] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

 (1) V_{INM} can be left floating if the motor controller is not used.

Table 27. Motor Control Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|------------|------|-------|-------------|
| 127 | MOTOR CTRL | R/W | 0 | TBD |
| 126 | | R/W | 0 | TBD |
| 125 | | R/W | 0 | MD_EN |
| 124 | | R/W | 0 | MD_MODE |
| 123 | | R/W | 0 | MD_AIN1 |
| 122 | | R/W | 0 | MD_AIN2 |
| 121 | | R/W | 0 | MD_BIN1 |
| 120 | | R/W | 0 | MD_BIN2 |

7.5.17 Password Register

Figure 32. Password Register, Address = 10h, HEX = 00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----|-----|-----|-----|-----|-----|-----|
| PASSWORD [135:128] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Password Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---------|----------|------|----------|---|
| 135:128 | PASSWORD | R/W | 00000000 | USER PASSWORD (0xBAh + 0xBEh) disable (0x00h). Once set, register 11h can be written. |

7.5.18 System Configuration Register

Figure 33. System Configuration Register, Address = 11h, HEX = 00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| SYSTEM [143:136] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 29. System Configuration Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---------|--------|------|-------|--|
| 143:139 | SYSTEM | R/W | 00000 | TBD |
| 138 | | R/W | 0 | EEPROM_PROGRAM Program scratch pad values to EEPROM |
| 137 | | R/W | 0 | DIRECT_MODE Allows direct control of switches through SW CONTROL REGISTER |
| 136 | | R/W | 0 | TBD |

7.5.19 User EEPROM, BYTE0

Figure 34. User EEPROM, BYTE0, Address = 20h, HEX = 00

| | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE0 [7:0] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 30. User EEPROM, BYTE0 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-------|------|----------|-------------|
| 7:0 | BYTE0 | R/W | 00000000 | USER BYTE 0 |

7.5.20 User EEPROM, BYTE1

Figure 35. User EEPROM, BYTE1, Address = 21h, HEX = 00

| | | | | | | | |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE1 [15:8] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 31. User EEPROM, BYTE1 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|------|-------|------|----------|-------------|
| 15:8 | BYTE1 | R/W | 00000000 | USER BYTE 1 |

7.5.21 User EEPROM, BYTE2

Figure 36. User EEPROM, BYTE2, Address = 22h, HEX = 00

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE2 [23:16] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 32. User EEPROM, BYTE2 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 23:16 | BYTE2 | R/W | 00000000 | USER BYTE 2 |

7.5.22 User EEPROM, BYTE3

Figure 37. User EEPROM, BYTE3, Address = 23h, HEX = 00

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE3 [31:24] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 33. User EEPROM, BYTE3 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 31:24 | BYTE3 | R/W | 00000000 | USER BYTE 3 |

7.5.23 User EEPROM, BYTE4
Figure 38. User EEPROM, BYTE4, Address = 24h, HEX = 00

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE4 [39:32] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 34. User EEPROM, BYTE4 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 39:32 | BYTE4 | R/W | 00000000 | USER BYTE 4 |

7.5.24 User EEPROM, BYTE5
Figure 39. User EEPROM, BYTE5, Address = 25h, HEX = 00

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE5 [47:40] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 35. User EEPROM, BYTE5 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 47:40 | BYTE5 | R/W | 00000000 | USER BYTE 5 |

7.5.25 User EEPROM, BYTE6
Figure 40. User EEPROM, BYTE6, Address = 26h, HEX = 00

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE6 [55:48] | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 36. User EEPROM, BYTE6 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 55:48 | BYTE6 | R/W | 00000000 | USER BYTE 6 |

7.5.26 User EEPROM, BYTE7
Figure 41. User EEPROM, BYTE7, Address = 27h, HEX = 00

| | | | | | | | |
|---------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE7 [63:56] | | | | | | | |
| R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Table 37. User EEPROM, BYTE7 Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-------|-------|------|----------|-------------|
| 63:56 | BYTE7 | R | 00000000 | USER BYTE 7 |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A DLPC343x controller can be used with a DLP2010 (0.2 WVGA) DMD or DLP3010 (0.3 720p) DMD to provide a compact, reliable, high-efficiency display solution for many different video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions with the primary direction being into collection optics within a projection lens. The projection lens sends the light to the destination needed for the application. Each application is derived primarily from the optical architecture of the system and the format of the pixel data being input into the DLPC343x.

In display applications using the DLP2010 DMD or DLP3010 DMD, the DLPA2000 provides all needed analog functions including the analog power supplies and the RGB LED driver to provide a robust and efficient display solution. Display applications of interest include pico-projectors embedded in display devices like smart phones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery-powered mobile accessories, interactive displays, low latency gaming displays, and digital signage.

Alternately, a DLPC150 controller can be used with a DLP2010 or DLP2010NIR DMD. Applications of interest when using the DLPC150 controller include machine vision systems, spectrometers, skin analysis, medical systems, material identification, chemical sensing, infrared projection, and compressive sensing. In a spectroscopy application the DLPC150 controller and DLP2010NIR DMD are often combined with a single element detector to replace expensive InGaAs array-based detector designs. In this application the DMD acts as a wavelength selector reflecting specific wavelengths of light into the single point detector.

8.2 Typical Projector Application

A common application when using DLPA2000 with DLP2010 DMD and DLPC3430 controller is for creating a pico-projector embedded in a handheld product. For example, a pico-projector may be embedded in a smart phone, a tablet, a camera, or camcorder. The DLPC3430 in the pico-projector embedded module typically receives images from a host processor within the product as shown in Figure 42. DLPA2000 provides power supply sequencing and controls the LED currents as required by the application.

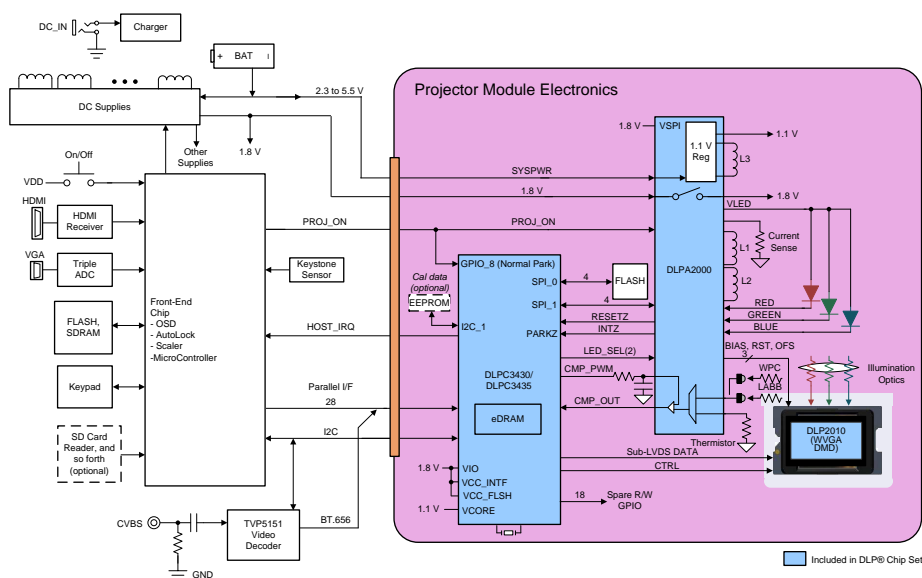


Figure 42. Typical Embedded Setup Using DLPA2000

Typical Projector Application (continued)

8.2.1 Design Requirements

A pico-projector is created by using a DLP chipset comprised of DLP2010 (0.2 WVGA) DMD, DLPC3430, or DLPC3435 controller and DLPA2000 PMIC/LED driver. The DLPC3430 or DLPC3435 does the digital image processing, the DLPA2000 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips may be needed. At a minimum, a flash part is needed to store the software and firmware to control the DLPC3430 or DLPC3435.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

When connecting the DLPC3430 or DLPC3435 to the host processing to receive images, a parallel interface is used. While using the parallel interface, I²C should be connected to the host processor for sending commands to the DLPC3430 or DLPC3435.

The only power supplies needed external to the projector are the battery (SYSPWR) and a regulated 1.8-V supply. The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPA2000 will not draw current on the 1.8-V supply.

8.2.2 Detailed Design Procedure

For connecting together the DLP2010, DLPC3430 or DLPC3435, and DLPA2000, see the reference design schematic. When a circuit board layout is created from this schematic, a very small circuit board is possible. An example small board layout is included in the reference design database. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

A miniature stepper motor can optionally be added to the optical engine for creating a motorized focus. Direct control and driving of the motor can be done by the DLPA2000, and software commands sent over I²C to the DLPC3430 or DLPC3435 are available to move the motor to the desired position.

Typical Projector Application (continued)

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in [Figure 43](#). For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

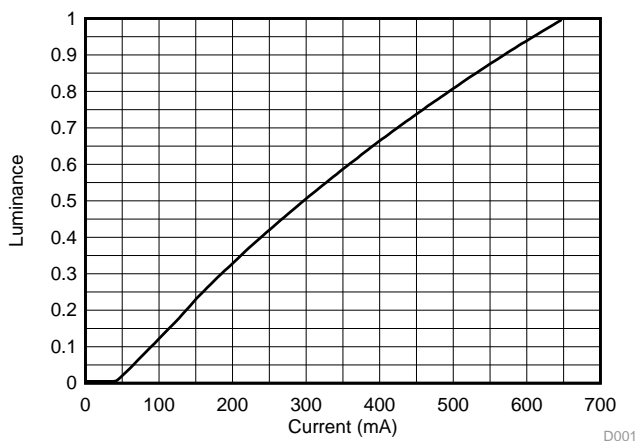


Figure 43. Luminance vs Current

8.3 Typical Mobile Sensing Application

A typical embedded system application using the DLPC150 controller and the DLPC2010NIR is shown in [Figure 44](#). In this configuration, the DLPC150 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. The DLPC150 controller processes the digital input image and converts the data into the format needed by the DLP2010NIR. The DLP2010NIR steers light by setting specific micromirrors to the *on* position, directing light to the detector, while unwanted micromirrors are set to the *off* position, directing light away from the detector. The microprocessor sends binary images to the DLP2010NIR to steer specific wavelengths of light into the detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light.

Typical Mobile Sensing Application (continued)

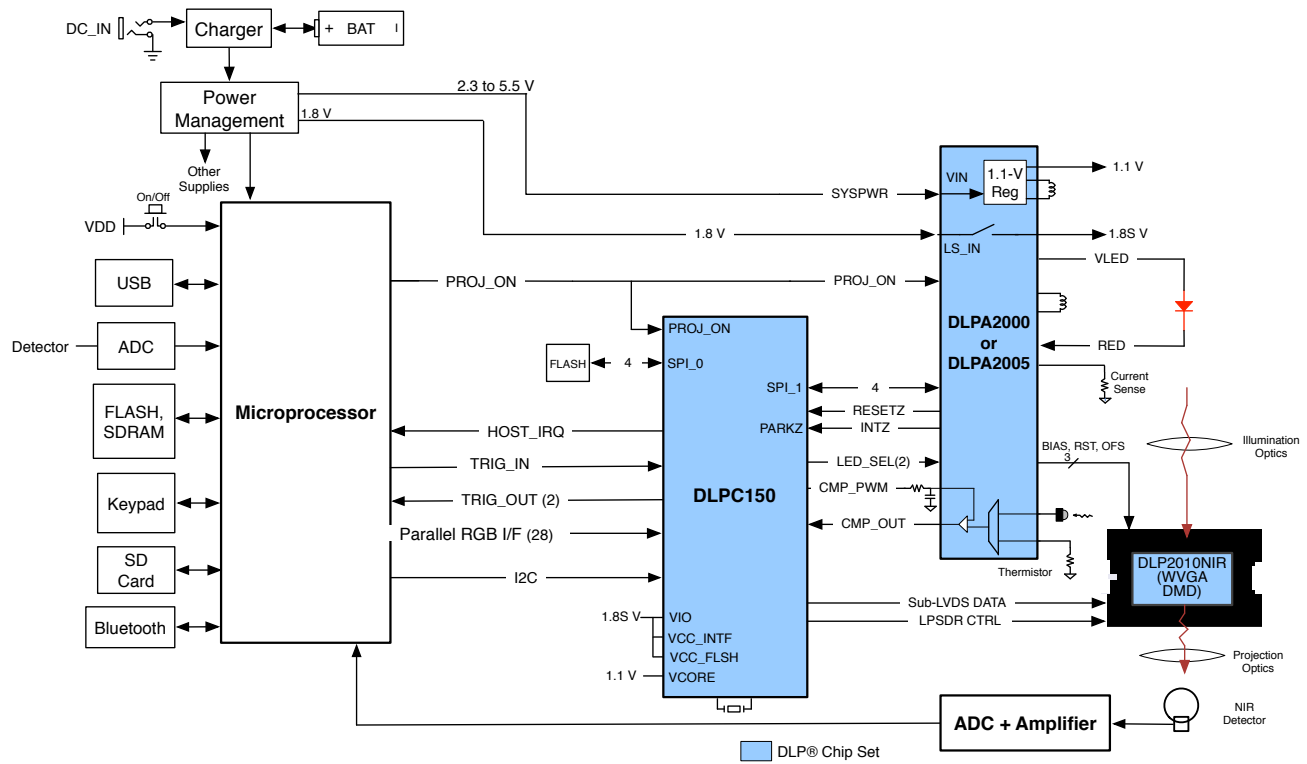


Figure 44. Typical Application Diagram

8.3.1 Design Requirements

All applications using the DLP 0.2-inch WVGA chipset require the:

- DLPC150 controller, and
- DLPA2000 PMIC, and
- DLP2010 or DLP2010NIR DMD

components for operation. The system also requires an external parallel flash memory device loaded with the DLPC150 configuration and support firmware. DLPC150 does the digital image processing and formats the data for the DMD. DLPA2000 PMIC provides the needed analog functions for the DLPC150 and DLP2010 or DLP2010NIR. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC150 system interfaces:
 - Control interface
 - Trigger interface
 - Input data interface
 - Illumination interface
- DLPC150 support circuitry and interfaces:
 - Reference clock
 - PLL
 - Program memory flash interface
- DMD interfaces:
 - DLPC150 to DMD digital data
 - DLPC150 to DMD control interface
 - DLPC150 to DMD micromirror reset control interface

Typical Mobile Sensing Application (continued)

8.3.2 Detailed Design Procedure

8.3.2.1 Dlp150 System Interfaces

The 0.2-inch WVGA chipset supports a 16-bit or 24-bit parallel RGB interface for image data transfers from another device. There are two primary output interfaces: Illumination driver control interface and sync outputs.

8.3.2.1.1 Control Interface

The 0.2-inch WVGA chipset supports I²C commands through the control interface. The control interface allows another master processor to send commands to the DLPC150 controller to query system status or perform realtime operations, such as LED driver current settings.

8.3.3 Application Curve

In a reflective spectroscopy application, a broadband light source illuminates a sample and the reflected light spectrum is dispersed onto the DLP2010NIR. A microprocessor in conjunction with the DLPC150 controls individual DLP2010NIR micromirrors to reflect specific wavelengths of light to a single point detector. The microprocessor uses an analog-to-digital converter to sample the signal received by the detector into a digital value. By sequentially selecting different wavelengths of light and capturing the values at the detector, the microprocessor can then plot a spectral response to the light. This systems allows the measurement of the collected light and derive the wavelengths absorbed by the sample. This process leads to the absorption spectrum shown in [Figure 45](#).

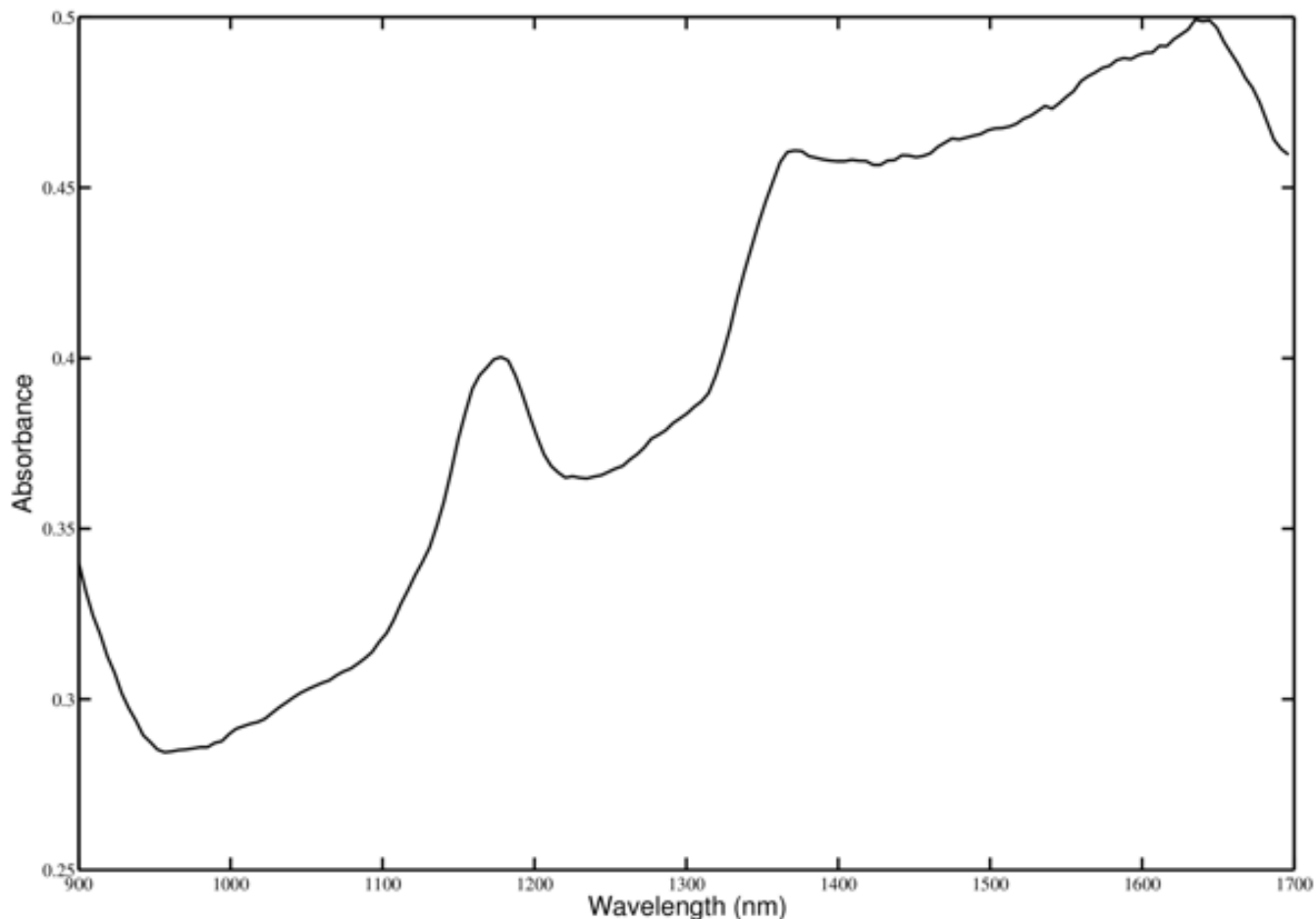


Figure 45. Sample DLPC150 Based Spectrometer Output

9 Power Supply Recommendations

The DLPA2000 is designed to operate from a 2.3-V to 6-V input voltage supply or battery. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the V_{IN} terminal, or supply peak current limitations, additional bulk capacitance may be required. In the case ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping. The amount of bulk capacitance required should be evaluated such that the input voltage can remain in specification long enough for a proper fast shutdown to occur for the V_{OFS} , V_{RST} , and V_{BIAS} supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply or battery supply is suddenly removed from the system.

10 Layout

10.1 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

[Figure 46](#) shows an example layout that has critical parts placed as close as possible to the pins they are connected to. Here are recommendations for the following components:

- R1 is R_{LIM} and is connected via a wide trace and as short as possible to the DLPA2000 and the ground.
- L1 is the big inductor for the V_{LED} that is connected via two wide traces to the pins.
- C3/C4 are the decoupling capacitors for the V_{LED} and they are as close as possible placed to the part and directly connected to ground.
- L3/C20 are components used for the V_{CORE} BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin.
- L2 This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2000 using wide PCB traces.

10.2 Layout Example

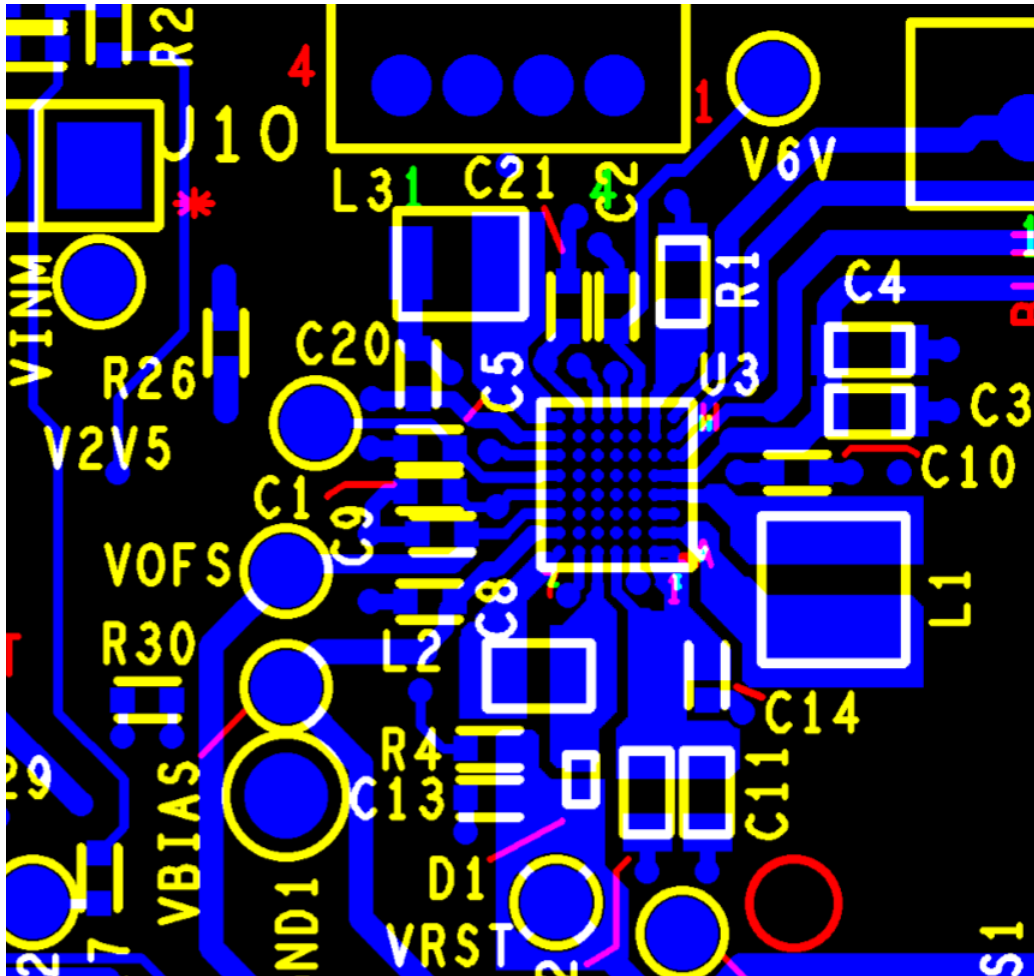


Figure 46. Example Layout of DLPA2000

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

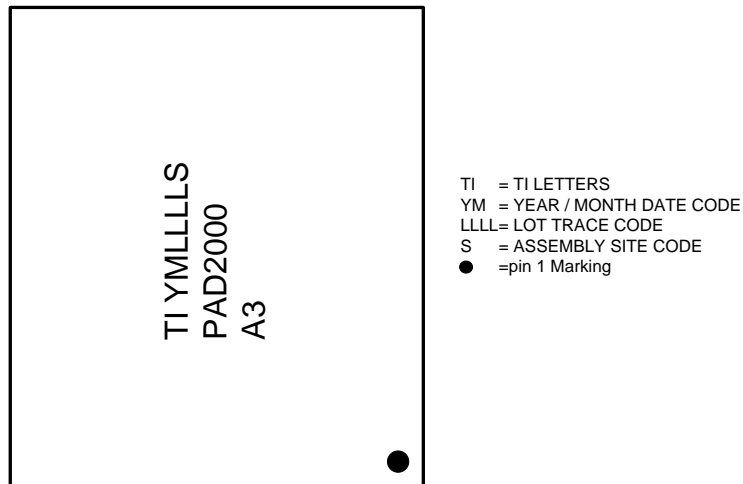


Figure 47. DLPA2000 Package Marking(Top View)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 38. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DLPA2000 | Click here | Click here | Click here | Click here | Click here |
| DLPC3430 | Click here | Click here | Click here | Click here | Click here |
| DLPC3435 | Click here | Click here | Click here | Click here | Click here |
| DLP2010 | Click here | Click here | Click here | Click here | Click here |

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

DLP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

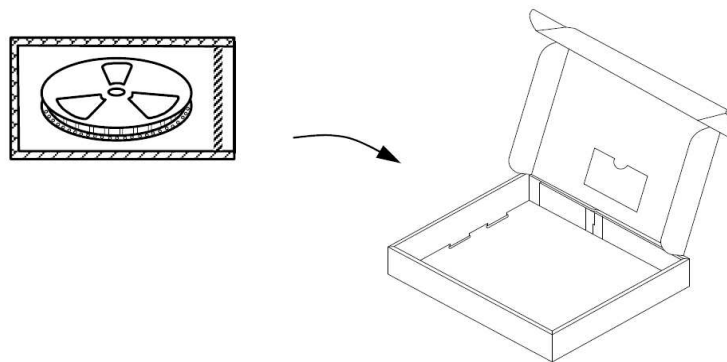
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

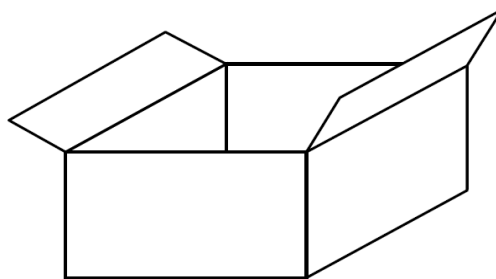
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

- Insertion of device –The device is located such as symbolization in upper side and lead pins in lower side.
- Cover tape – The cover tape does not cover the index hole and does not shift to outside from carrier tape.
- Tape Structure –The carrier tape is made of plastic and the structure is shown in above schematic. The device is put on embossed area of carrier tape, and covered by cover tape made of plastic.
- ESD Countermeasure Plastic – material used in both carrier tape and cover tape are static dissipative.
- Material – Polycarbonate, Polystyrene or and approved equivalent (Static Dissipative / Antistatic).
- Packing method – The reel is packed into Moisture Barrier bag and fastened by heat-sealing after fixed the end of leader tape by tape. The QFN device packing includes desiccant, humidity indicator.
- Reel Box – Each Moisture Barrier bag is packed into reel box.



Reel box (carton)

- Reel Box Material – Corrugated Fiberboard
- Shipping Box –The filler such as cushion is added if space exists inside. The size of shipping box will be changed per packing quantity of reel box.



Shipping box (carton)

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DLPA2000DYFFR | ACTIVE | DSBGA | YFF | 56 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -10 to 85 | PAD2000 A3 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DLPA2000DYFFR | DSBGA | YFF | 56 | 3000 | 330.0 | 12.4 | 3.4 | 3.75 | 0.82 | 8.0 | 12.0 | Q1 |

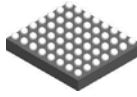
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DLPA2000DYFFR | DSBGA | YFF | 56 | 3000 | 335.0 | 335.0 | 25.0 |

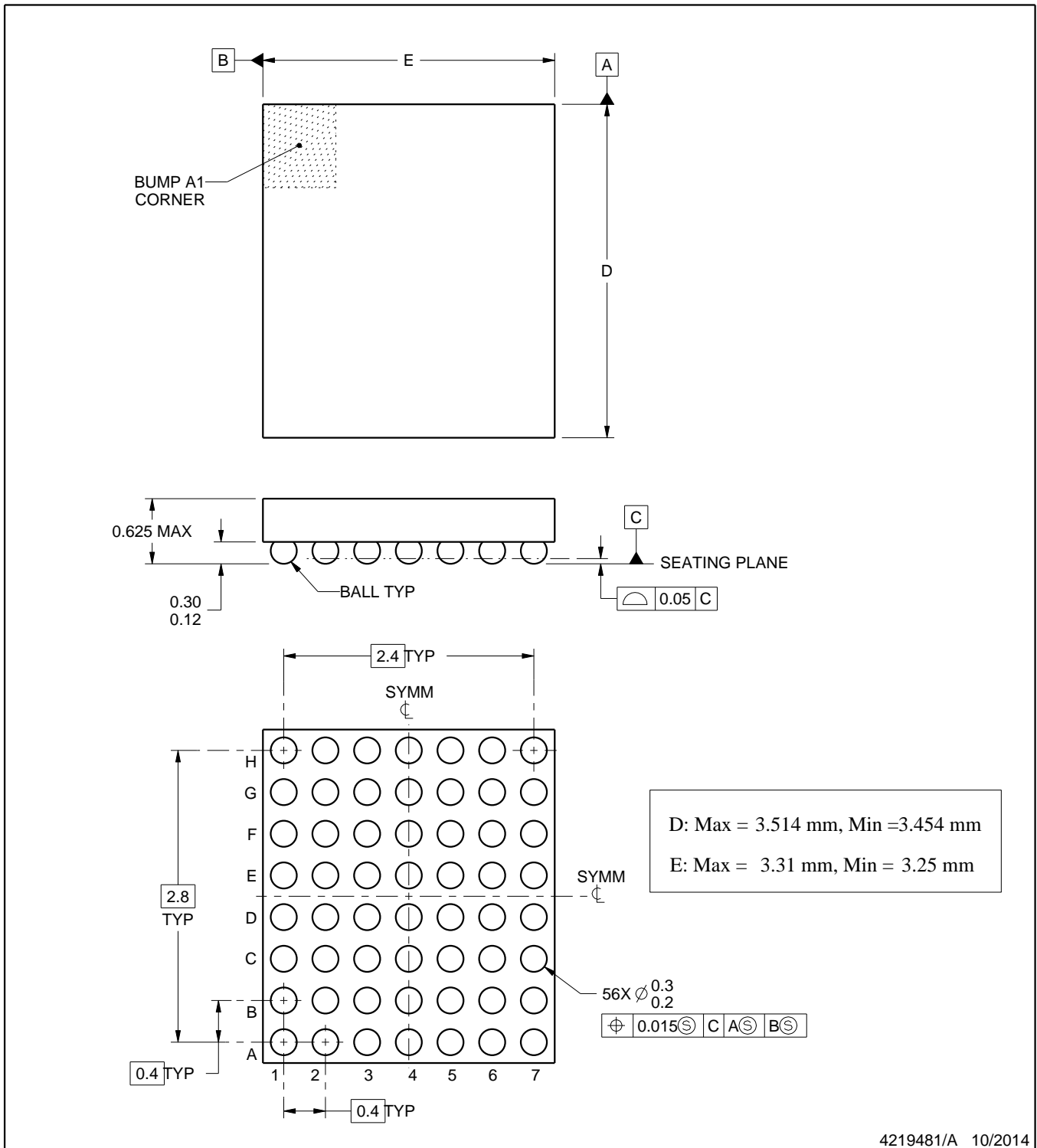
YFF0056



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

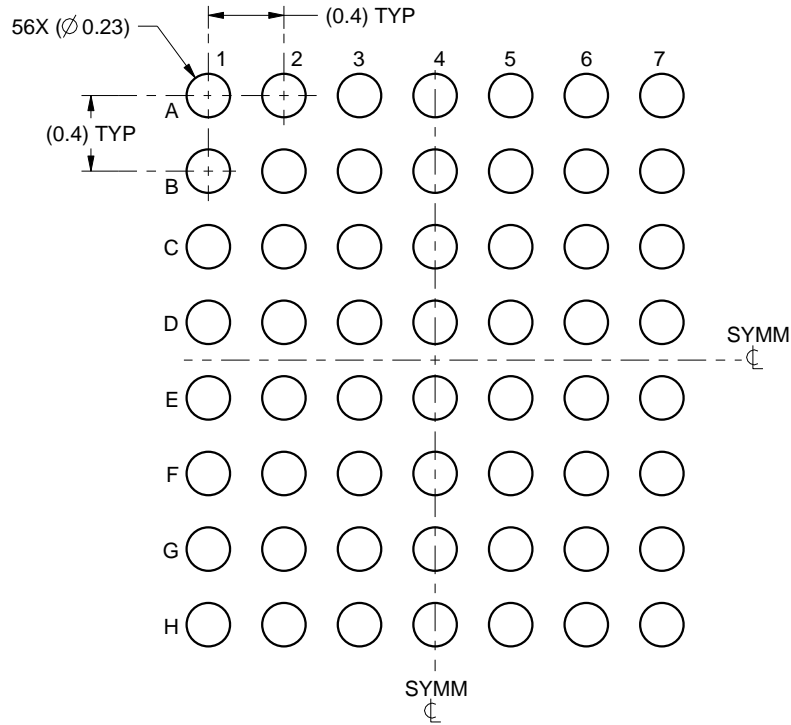
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

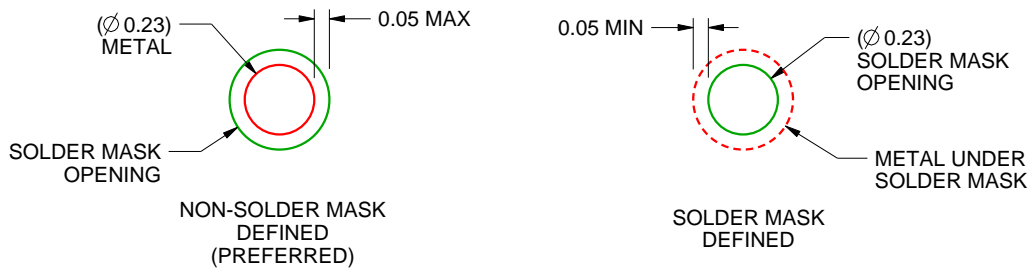
YFF0056

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

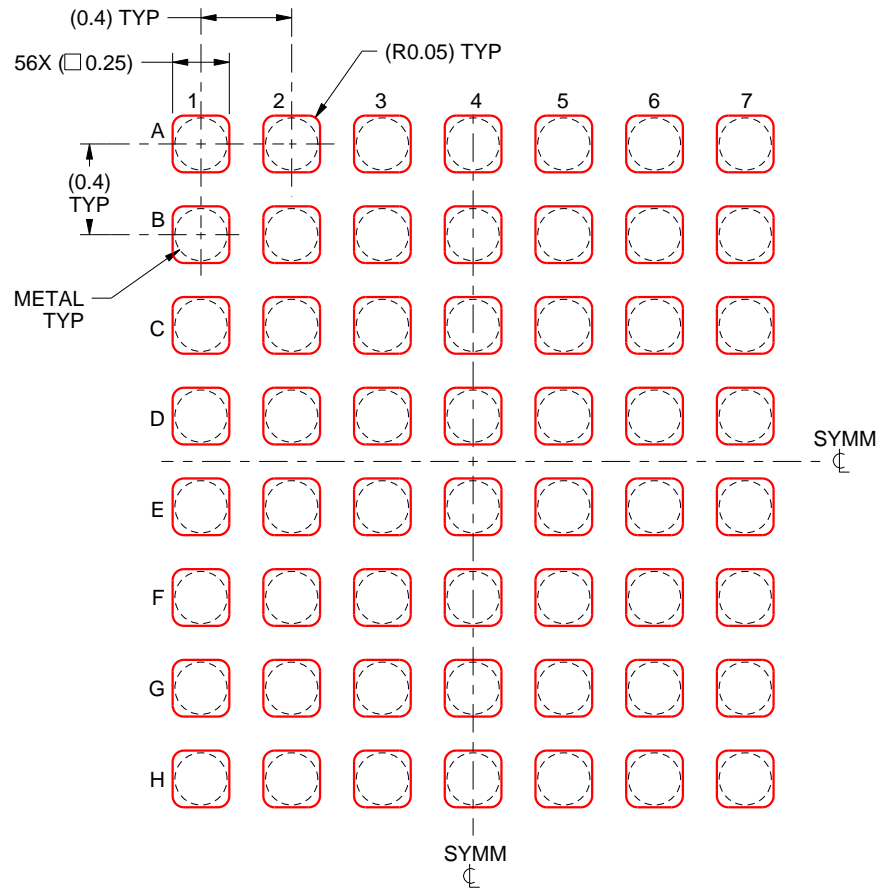
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YFF0056

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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