DLP3020-Q1 0.3-Inch WVGA DMD for Automotive Interior Display

1 Features

- Automotive qualified
- 0.3-inch diagonal micromirror array
  - 7.6-µm micromirror pitch
  - ±12° micromirror tilt angle (relative to flat state)
  - Side illumination for optimized efficiency
- WVGA (864 × 480) resolution
- Polarization independent spatial light modulator
  - Compatible with LED or laser light sources
  - Image viewable with polarized glasses
- Low-power consumption: 105-mW (typical)
- Operating temperature range: –40°C to 105°C
- Hermetic package with 7.0°C/W thermal efficiency
- JTAG boundary scan to allow in-system validation
- Compatible with the DLPC120-Q1 automotive DMD controller
- 78-MHz DDR DMD interface
- Same micromirror array as DLP3030-Q1 with a reduced package size

2 Applications

- Wide field of view and augmented reality head-up display (HUD)
- Digital cluster, navigation, and infotainment windshield displays
- Interior projection display and lighting

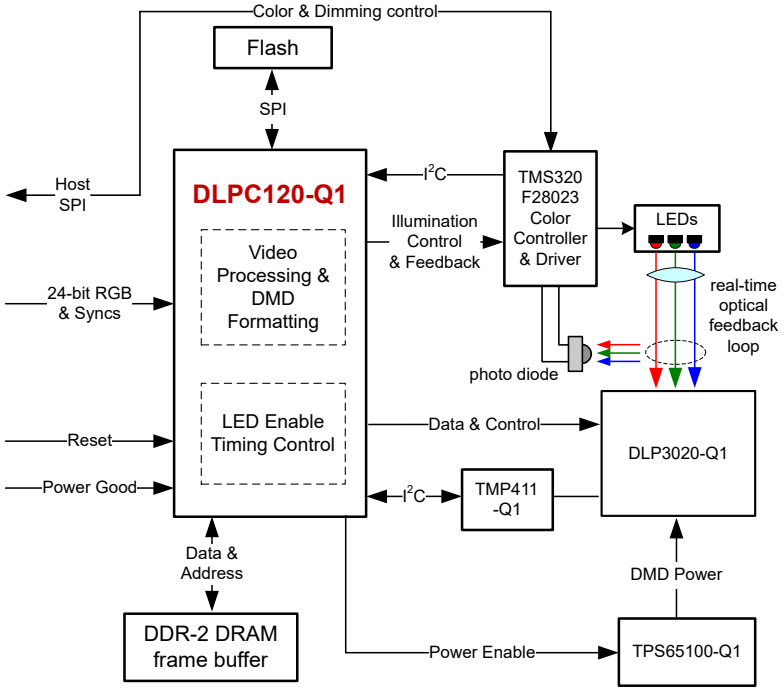
3 Description

The DLP3020-Q1 Automotive DMD is primarily targeted for automotive head-up display (HUD) applications with large field of view or augmented reality capability requiring long focal distances. This chipset can be coupled with LEDs or lasers to create deep saturated colors with over 125% NTSC color gamut with support for 24-bit RGB video input. In addition, the chipset enables high brightness (15,000-cd/m2 typical) HUD systems with wide dynamic range, and fast switching speeds that do not vary with temperature. As used in the TI reference design, very high dynamic range over 5000:1 can be achieved to meet the operating range of an automotive HUD system for bright daylight and dark night time driving conditions. This device has the same micromirror array as DLP3030-Q1 with a smaller package, allowing overall volume reduction on optical system design.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
DLP3020-Q1	FQR (64)	8.55 mm × 16.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DLP3020-Q1 System Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial Release

5 Pin Configuration and Functions

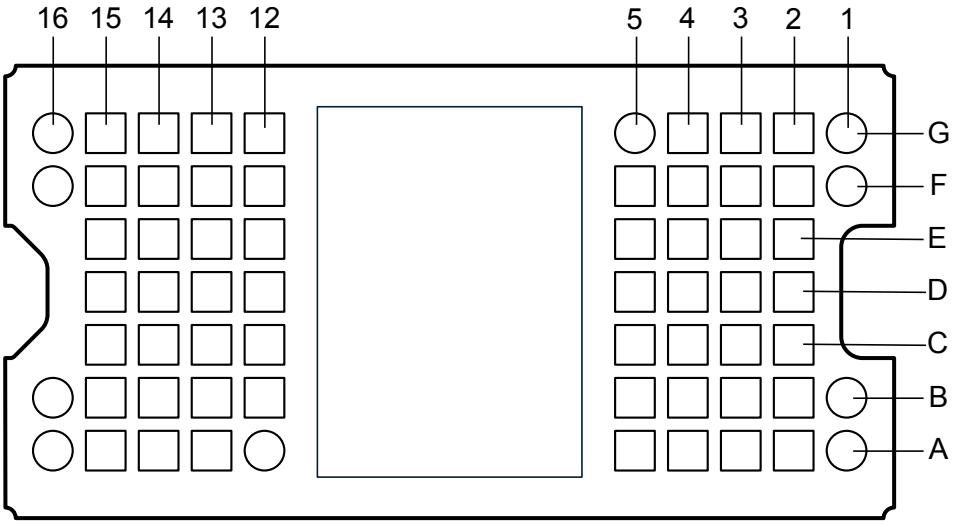


Figure 5-1. FQR Package, 64-Pin LGA (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DATA(0)	A2	LVCMOS input	Data bus. Synchronous to rising edge and falling edge of DCLK.
DATA(1)	A4		
DATA(2)	B2		
DATA(3)	B3		
DATA(4)	B5		
DATA(5)	C2		
DATA(6)	C3		
DATA(7)	B4		
DATA(8)	C5		
DATA(9)	D2		
DATA(10)	D3		
DATA(11)	D4		
DATA(12)	D5		
DATA(13)	E2		
DATA(14)	F5		
DCLK	F4		Data clock.
LOADB	F3		Parallel latch load enable. Synchronous to rising edge and falling edge of DCLK.
SCTRL	E4		Serial control (sync). Synchronous to rising edge and falling edge of DCLK.
TRC	F2		Toggle rate control. Synchronous to rising edge and falling edge of DCLK.
DAD_BUS	B15		Reset control serial bus. Synchronous to rising edge of SAC_CLK.
RESET_OEZ	C15		Active low. Output enable signal for internal reset driver circuitry.
RESET_STROBE	B13		Rising edge on RESET_STROBE latches in the control signals.
SAC_BUS	A15		Stepped address control serial bus. Synchronous to rising edge of SAC_CLK.
SAC_CLK	A14		Stepped address control clock.
TCK	F15		JTAG clock.
TDI	E13		JTAG data input. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.
TDO	G15	LVCMOS output	JTAG data output. Synchronous to falling edge of TCK. Tri-state fail-safe output buffer.
TMS	G14	LVCMOS input	JTAG mode select. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.
TEMP_MINUS	G13	Analog input	Calibrated temperature diode used to assist accurate temperature measurements of DMD die.
TEMP_PLUS	G2		
V_{BIAS}	D15	Power	Power supply for positive bias level of mirror reset signal.
V_{CC}	A5, B12, C14, D12, F13, G3		Power supply for low voltage CMOS logic. Power supply for normal high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal during power down.
V_{OFFSET}	E14	Power	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal.
V_{REF}	E15		Power supply for low voltage CMOS DDR interface.
V_{RESET}	D14		Power supply for negative reset level of mirror reset signal.
V_{SS}	A3, A13, B14, C4, C12, C13, D13, E3, E5, E12, F12, F14, G4, G12		Common return for all power.

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
RESERVED	A1, A12, A16,B1, B16, F1, F16, G1, G5, G16	Reserved	Do not connect.

6 Specifications

6.1 Absolute Maximum Ratings

See (2)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(1)				
V_{REF}	LVCMOS logic supply voltage	–0.5	4	V
V_{CC}	LVCMOS logic supply voltage	–0.5	4	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage	–0.5	8.75	V
V_{BIAS}	Mirror electrode voltage	–0.5	17	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta(3)		8.75	V
V_{RESET}	Mirror electrode voltage	–11	0.5	V
Input voltage: other inputs		–0.5	V_{REF} + 0.3	V
f_{DCLK}	Clock frequency	60	82	MHz
I_{TEMP_DIODE}	Temperature diode current		500	µA
ENVIRONMENTAL				
T_{ARRAY}	Operating DMD array temperature(4)	–40	105	°C

(1) All voltage values are with respect to the ground pins (V_{SS}).
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Unless otherwise indicated, these are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(3) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than or equal to 8.75 V.
(4) See Section 7.6.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system. The device is not designed to be exposed to corrosive environments.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	–40	125	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All Pins	±2000	V
	Charged-device model (CDM) per AEC Q100-011	All Pins	±750	
		Corner Pins(2)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Corner pins are A1, G1, A16, and G16.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE						
V_{REF}	LVCMOS interface power supply voltage		1.65	1.8	1.95	V
V_{CC}	LVCMOS logic power supply voltage		2.25	2.5	2.75	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage		8.25	8.5	8.75	V
V_{BIAS}	Mirror electrode voltage		15.5	16	16.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (2)				8.75	V
V_{RESET}	Mirror electrode voltage		–9.5	–10	–10.5	V
V_P VT+	Positive going threshold voltage		0.4 × V_{REF}		0.7 × V_{REF}	V
V_N VT–	Negative going threshold voltage		0.3 × V_{REF}		0.6 × V_{REF}	V
V_H ΔVT	Hysteresis voltage (Vp – Vn)		0.1 × V_{REF}		0.4 × V_{REF}	V
I_{OH_TDO}	High level output current @ Voh = 2.25 V, TDO, Vcc = 2.25 V				–2	mA
I_{OL_TDO}	Low level output current @ Vol = 0.4 V, TDO, Vcc = 2.25 V				2	mA
TEMPERATURE DIODE						
I_{TEMP_DIODE}	Max current source into temperature diode (4)				120	µA
ENVIRONMENTAL						
T_{ARRAY} (5)	Operating DMD array temperature - steady state (1)		–40		105	°C
ILL_{UV} (3)	Illumination, wavelength < 395 nm				2.0	mW/cm^2
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in Figure 6-1 (6)	T_{ARRAY} ≤ 75°C			26	mW/mm^2
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in Figure 6-1 (6)	T_{ARRAY} > 75°C			20	mW/mm^2

(1) DMD active array temperature can be calculated as shown in Section 7.6 and assumes uniform illumination across the array.
(2) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than or equal to 8.75 V.
(3) The maximum operation conditions for DMD array temperature and illumination UV shall not be implemented simultaneously.
(4) Temperature diode is to assist in the calculation of the DMD array temperature during operation.
(5) Operating profile information for device micromirror landed duty-cycle and temperature may be provided if requested.
(6) The active area of the DLP3020-Q1 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation. Overfill illumination in excess of this specification may also impact thermal performance.

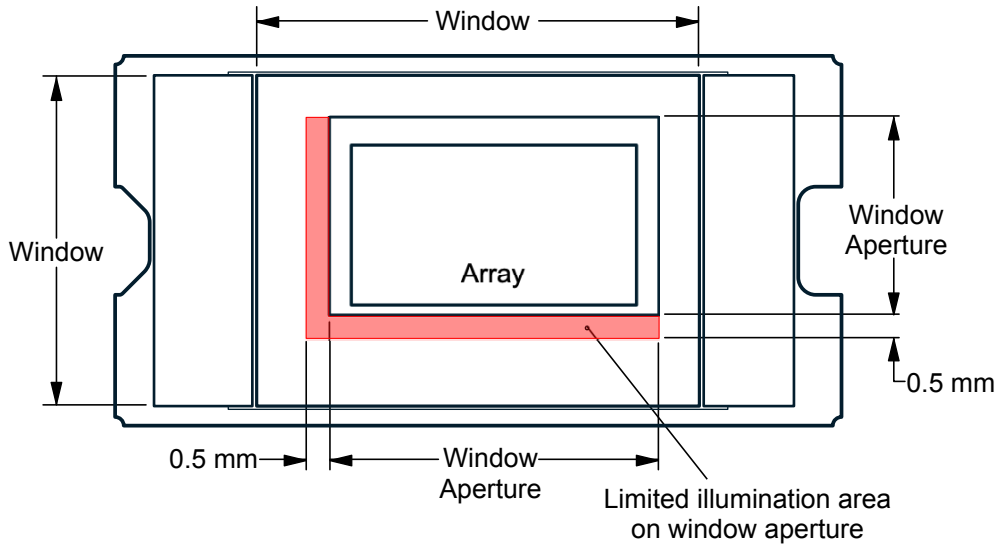


Figure 6-1. Illumination Overfill Diagram

6.5 Thermal Information

THERMAL METRIC[1]		DLP3020-Q1 FQR (LGA) 64 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)[1]	7.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in Section 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[2]

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	VCC = 2.25 V I_{OH} = –8 mA	1.7			V
V_{OH2}	High level output voltage[6]	VREF = 1.8 V I_{OH} = –2 mA	1.44			V
V_{OL}	Low level output voltage	VCC = 2.75 V I_{OL} = 8 mA			0.4	V
V_{OL2}	Low level output voltage[6]	VREF = 1.8 V I_{OL} = 2 mA			0.36	V
I_{OZ}	Output high impedance current	VREF = 1.95 V V_{OL} = 0 V	–10			µA
		VREF = 1.95 V V_{OH} = VREF			10	
I_{IL}	Low level input current[3]	VREF = 1.95 V V_I = 0 V	–5			µA
I_{IH}	High level input current[3]	VREF = 1.95 V V_I = VREF			6	µA
I_{IL2}	Low level input current[4]	VREF = 1.95 V V_I = 0 V	–785			µA
I_{IH2}	High level input current[4]	VREF = 1.95 V V_I = VREF			6	µA
I_{IL3}	Low level input current[5]	VREF = 1.95 V V_I = 0 V	–5			µA
I_{IH3}	High level input current[5]	VREF = 1.95 V V_I = VREF			785	µA
CURRENT						
I_{REF}	Current at V_{REF} = 1.95 V	f_{DCLK} = 80 MHz			2.80	mA
I_{cc}	Current at V_{CC} = 2.75 V	f_{DCLK} = 80 MHz			59.90	mA
I_{OFFSET}	Current at V_{OFFSET} = 8.75 V				2.93	mA
I_{BIAS}	Current at V_{BIAS} = 16.5 V				2.30	mA
I_{RESET}	Current at V_{RESET} = –10.5 V				–2.00	mA

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
POWER						
P_{REF}	Power at V_{REF} = 1.95 V	f_{DCLK} = 80 MHz			5.46	mW
P_{CC}	Power at V_{CC} = 2.75 V	f_{DCLK} = 80 MHz			164.73	mW
P_{OFFSET}	Power at V_{OFFSET} = 8.75 V				25.64	mW
P_{BIAS}	Power at V_{BIAS} = 16.5 V				37.95	mW
P_{RESET}	Power at V_{RESET} = –10.5 V				21.00	mW
P_{TOTAL}	Total power at nominal conditions	f_{DCLK} = 80 MHz			254.77	mW
CAPACITANCE						
C_{IN}	Input pin capacitance	f = 1 MHz			20	pF
C_A	Analog pin capacitance (TEMP_PLUS and TEMP_MINUS pins)	f = 1 MHz			65	pF
C_o	Output pin capacitance	f = 1 MHz			20	pF

(1) All voltage values are with respect to the ground pins (V_{SS}).
(2) Device electrical characteristics are over Section 6.4 unless otherwise noted.
(3) Specification is for LVCMOS input pins, which do not have pull up or pull down resistors. See Section 5.
(4) Specification is for LVCMOS input pins which do have pull up resistors (JTAG: TDI, TMS). See Section 5.
(5) Specification is for LVCMOS input pins which do have pull down resistors. See Section 5.
(6) Specification is for LVCMOS JTAG output pin TDO.

6.7 Timing Requirements

Over Section 6.4 unless otherwise noted.

		MIN	NOM	MAX	UNIT
DMD MIRROR AND SRAM CONTROL LOGIC SIGNALS					
t_{SU}	Setup time SAC_BUS low before SAC_CLK↑	1.0			ns
t_H	Hold time SAC_BUS low after SAC_CLK↑	1.0			ns
t_{SU}	Setup time DAD_BUS high before SAC_CLK↑	1.0			ns
t_H	Hold time DAD_BUS after SAC_CLK↑	1.0			ns
t_C	Cycle time SAC_CLK	12.5		16.67	ns
t_W	Pulse width 50% to 50% reference points: SAC_CLK high or low	5.0			ns
t_R	Rise time 20% to 80% reference points: SAC_CLK			2.5	ns
t_F	Fall time 80% to 20% reference points: SAC_CLK			2.5	ns
DMD DATA PATH AND LOGIC CONTROL SIGNALS					
t_{SU}	Setup time DATA(14:0) before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time DATA(14:0) after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time SCTRL before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time SCTRL after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time TRC before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time TRC after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time LOADB low before DCLK↑	1.0			ns
t_H	Hold time LOADB low after DCLK↓	1.0			ns
t_{SU}	Setup time RESET_STROBE high before DCLK↑	1.0			ns
t_H	Hold time RESET_STROBE after DCLK↑	3.5			ns
t_C	Cycle time DCLK	12.5		16.67	ns
t_W	Pulse width 50% to 50% reference points: DCLK high or low	5.0			ns
$t_W(L)$	Pulse width 50% to 50% reference points: LOADB low	7.0			ns
$t_W(H)$	Pulse width 50% to 50% reference points: RESET_STROBE high	7.0			ns
t_R	Rise time 20% to 80% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
t_F	Fall time 80% to 20% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
JTAG BOUNDARY SCAN CONTROL LOGIC SIGNALS					
f_{TCK}	Clock frequency TCK			10	MHz
t_C	Cycle time TCK	100			ns
t_W	Pulse width 50% to 50% reference points: TCK high or low	10			ns
t_{SU}	Setup time TDI valid before TCK↑	5			ns
t_H	Hold time TDI valid after TCK↑	25			ns
t_{SU}	Setup time TMS valid before TCK↑	5			ns
t_H	Hold time TMS valid after TCK↑	25			ns
t_R	Rise time 20% to 80% reference points: TCK, TDI, TMS			2.5	ns
t_R	Fall time 80% to 20% reference points: TCK, TDI, TMS			2.5	ns

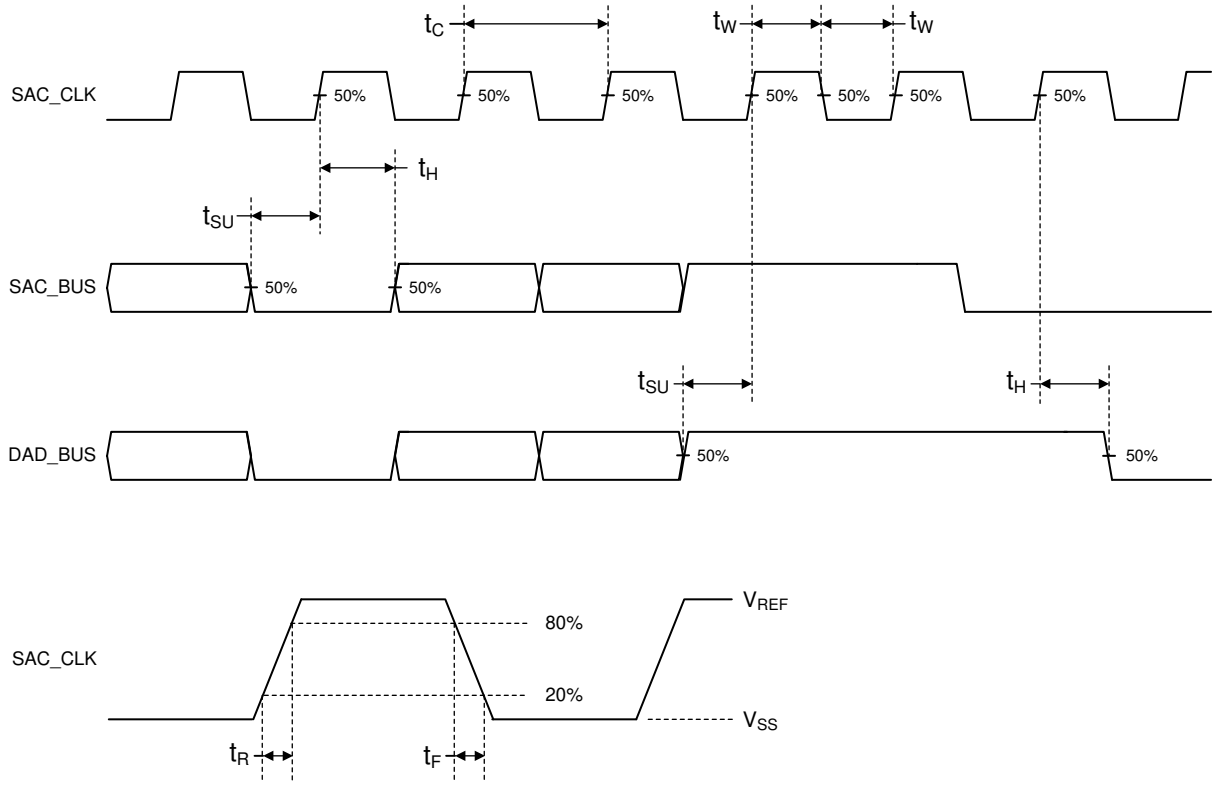


Figure 6-2. DMD Mirror and SRAM Control Logic Timing Requirements

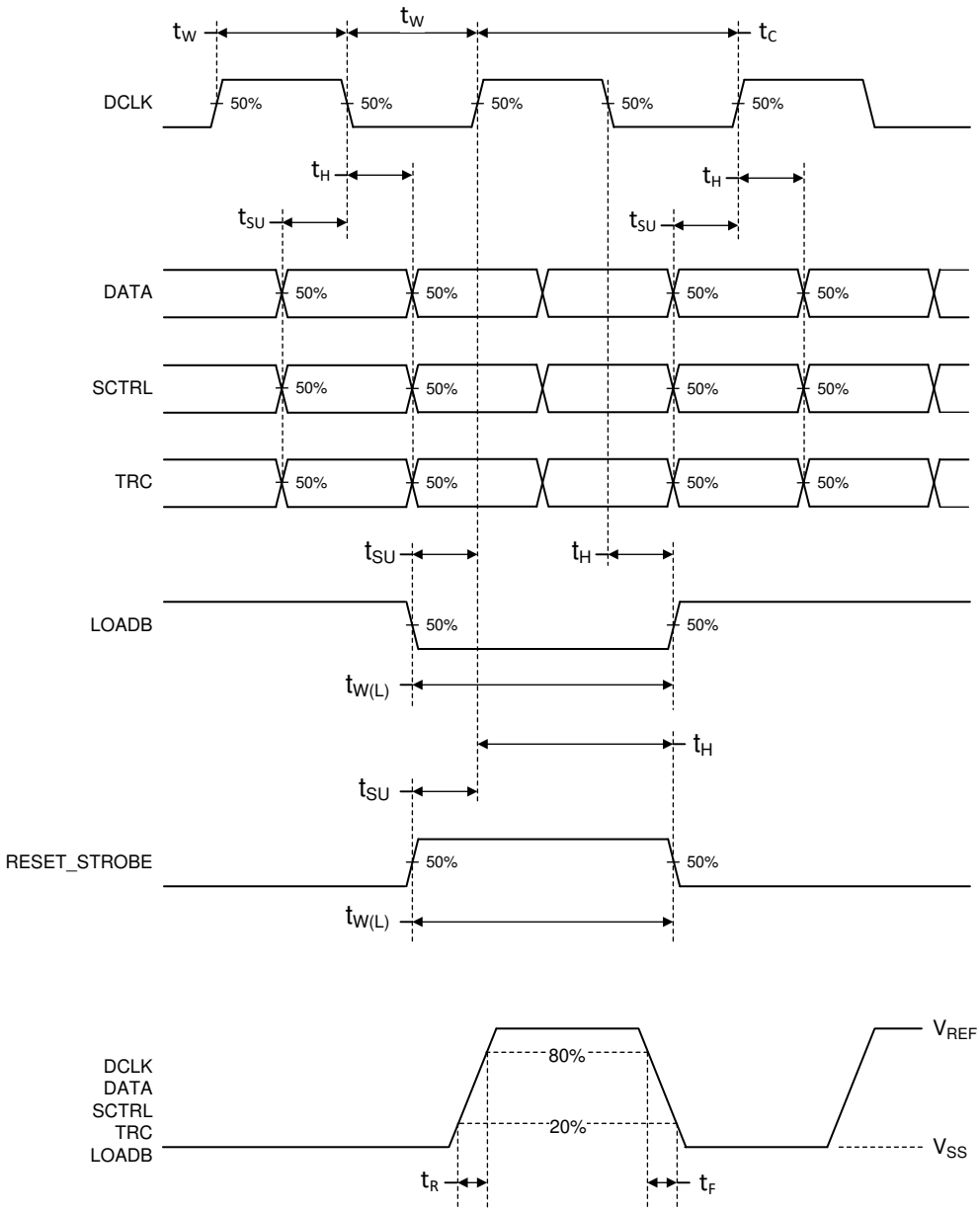


Figure 6-3. DMD Data Path and Control Logic Timing Requirements

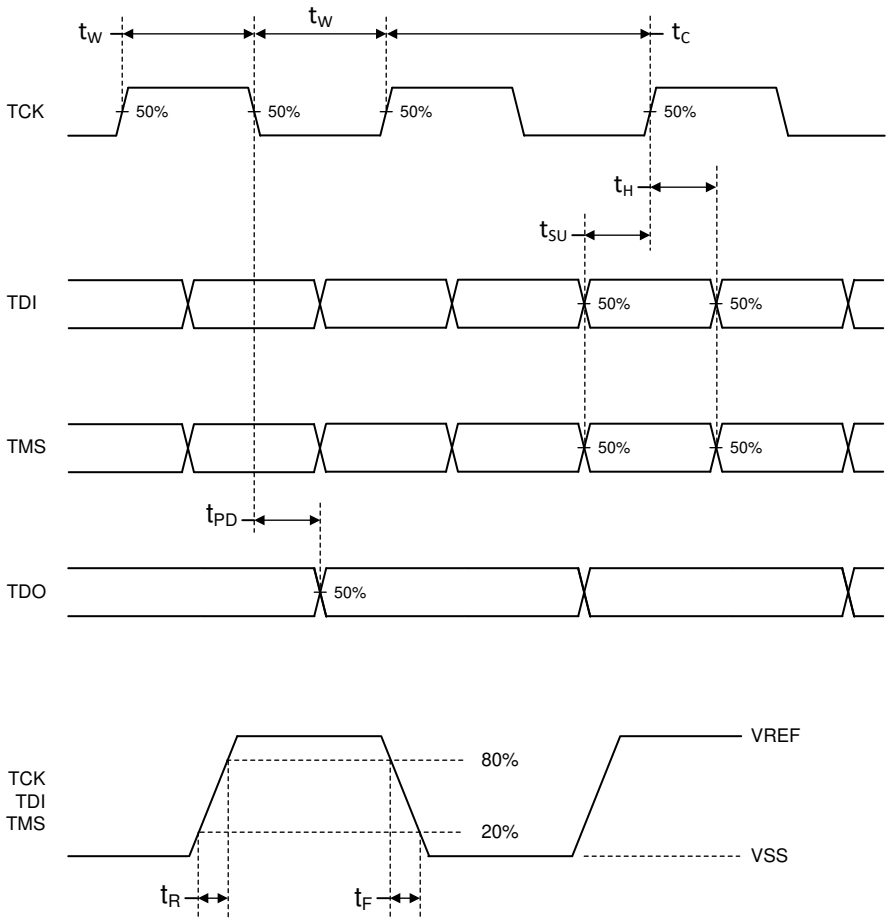


Figure 6-4. JTAG Boundary Scan Control Logic Timing Requirements

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q (see Figure 6-4)	C_L = 11 pF, from (Input) falling edge of TCK to (Output) TDO, see Figure 6-4	3		25	ns

(1) Device electrical characteristics are over *Recommended Operating Characteristics* unless otherwise noted.

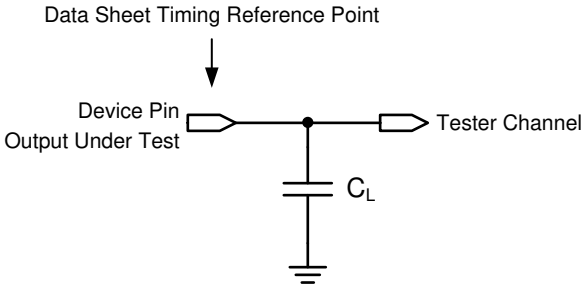


Figure 6-5. Test Load Circuit for Output Propagation Measurement

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Uniformly distributed within the Thermal Interface Area shown in Figure 6-6			70	N
Uniformly distributed within the Electrical Interface Area shown in Figure 6-6			100	N

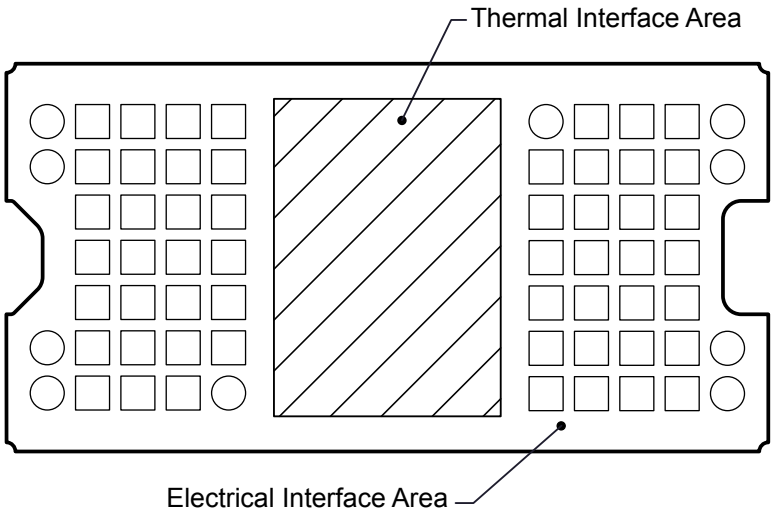


Figure 6-6. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

PARAMETER		VALUE	UNIT
N Number of active columns	See Figure 6-7	684	micromirrors
M Number of active rows	See Figure 6-7	608	micromirrors
ε Micromirror (pixel) pitch – diagonal	See Figure 6-8	7.6	µm
P Micromirror (pixel) pitch – horizontal and vertical	See Figure 6-8	10.8	µm
Micromirror active array width	P × M + P / 2; see Figure 6-7	6.5718	mm
Micromirror active array height	(P × N) / 2 + P / 2; see Figure 6-7	3.699	mm
Micromirror active border	Pond of micromirror (POM)(1)	10	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

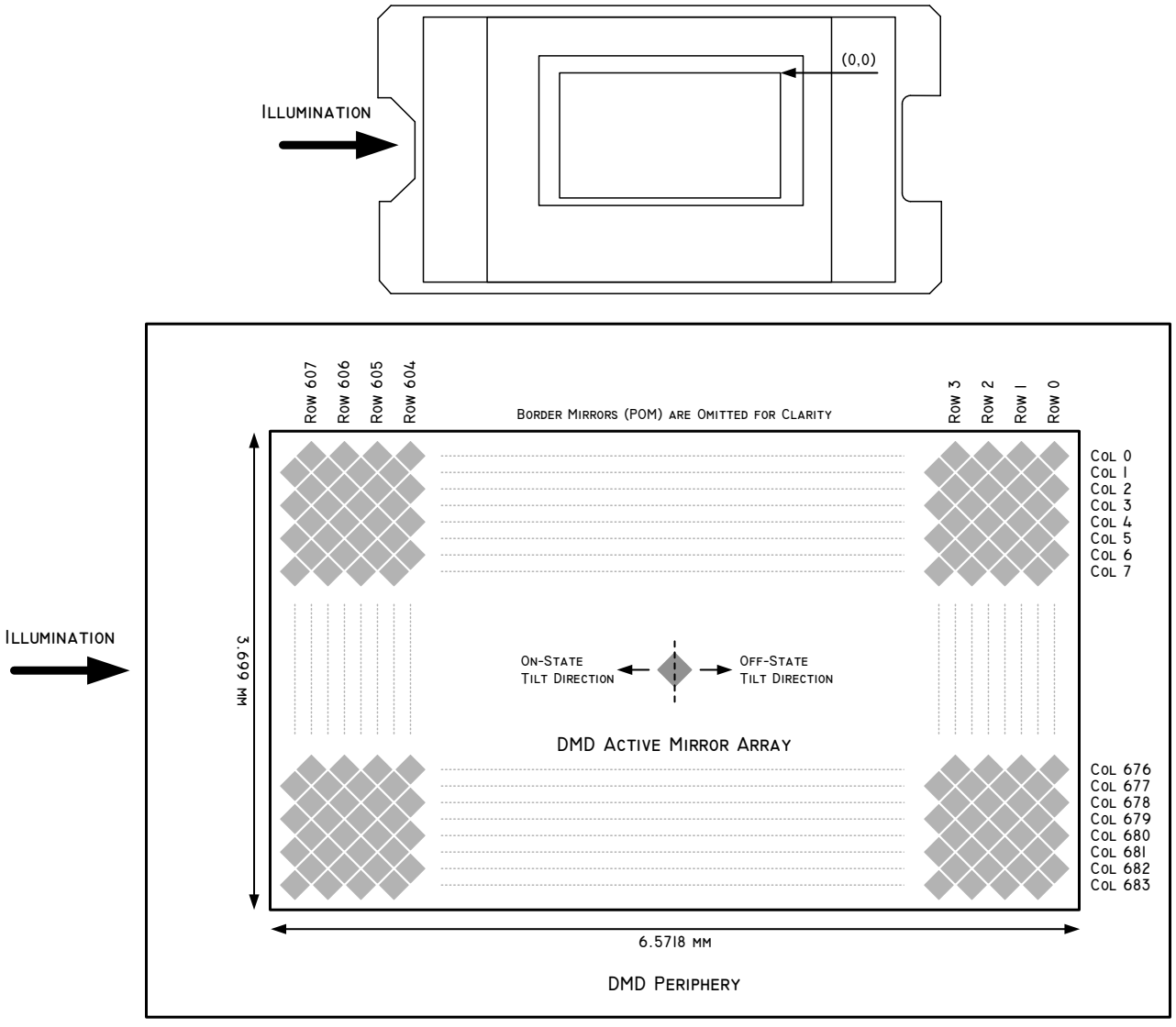


Figure 6-7. Micromirror Array Physical Characteristics

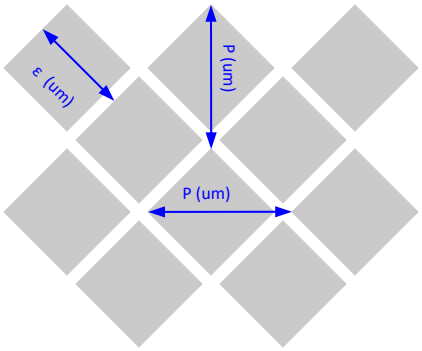


Figure 6-8. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

Table 6-1. Optical Parameters

PARAMETER	MIN	NOM	MAX	UNIT
Micromirror tilt angle, landed (on-state or off-state)(1)		12		°
Micromirror tilt angle tolerance(1)	–1		1	°
DMD efficiency, 420 nm–680 nm(2)		66%		

(1) For some applications, it is critical to account for the micromirror tilt angle variation in the overall optical system design. With some optical system designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some optical system designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.

(2) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic mirror duty cycle and do not include system optical efficiency or overfill loss. Note that this number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in *DMD Optical Efficiency for Visible Wavelengths*.

6.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(1)				See (1)	

(1) See the package mechanical ICD for details regarding the size and location of the window aperture.

6.13 Chipset Component Usage Specification

The DLP3020-Q1 DMD is a component of a DLP® chipset including a DLP products controller. Reliable function and operation of the DMD requires that it be used in conjunction with a DLP products controller.

Note

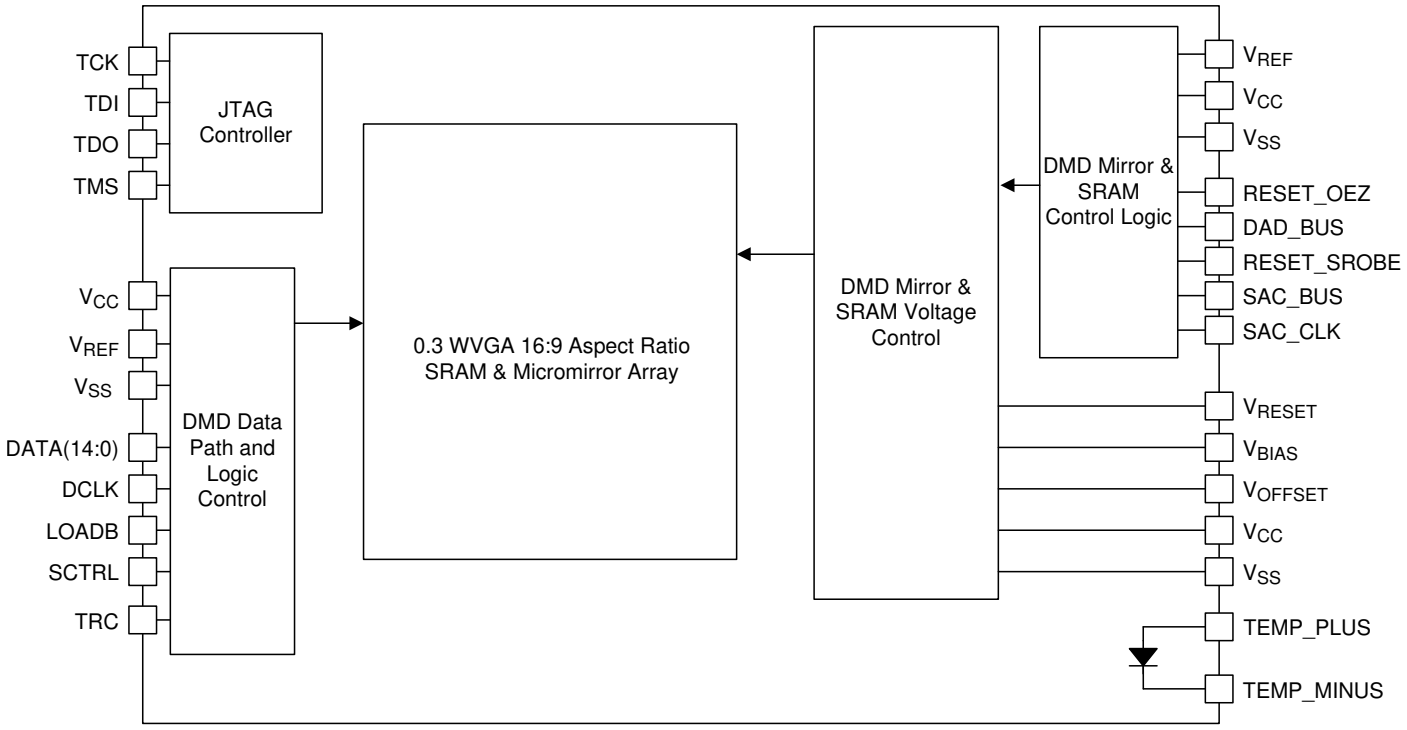
TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously

7 Detailed Description

7.1 Overview

The DLP3020-Q1 DMD has a resolution of 608 × 684 mirrors configured in a diamond format that results in an aspect ratio of 16:9 which creates an effective resolution of 864 × 480 square pixels. By configuring the pixels in a diamond format, the illumination input to the DMD enters from the side allowing for smaller mechanical packaging of the optical system.

7.2 Functional Block Diagram



7.3 Feature Description

To ensure reliable operation, the DLP3020-Q1 DMD must be used with a DLP products controller.

7.3.1 Micromirror Array

The DLP3020-Q1 DMD consists of a two-dimensional array of 1-bit CMOS memory cells that determine the state of the each of the 608 × 684 micromirrors in the array. Refer to Section 6.10 for a calculation of how the 608 × 684 micromirror array represents a 16:9 dimensional aspect ratio to the user. Each micromirror is either “ON” (tilted +12°) or “OFF” (tilted –12°). Combined with appropriate projection optical system the DMD can be used to create sharp, colorful, and vivid digital images.

7.3.2 Double Data Rate (DDR) Interface

Each DMD micromirror and its associated SRAM memory cell is loaded with data from the DLP controller via the DDR interface (DATA(14:0), DCLK, LOADB, SCRTL, and TRC). These signals are low voltage CMOS nominally operating at 1.8-V level to reduce power and switching noise. This high speed data input to the DMD allows for a maximum update rate of the entire micromirror array to be nearly 5 kHz, enabling the creation of seamless digital images using Pulse Width Modulation (PWM).

7.3.3 Micromirror Switching Control

Once data is loaded onto the DMD, the mirrors switch position (+12° or –12°) based on the timing signal sent to the DMD Mirror and SRAM control logic. The DMD mirrors will be switched from OFF to ON or ON to OFF, or stay in the same position based on control signals DAD_BUS, RESET_STROBE, SAC_BUS, and SAC_CLK, which are coordinated with the data loading by the DLP controller. In general, the DLP controller loads the DMD SRAM memory cells over the DDR interface, and then commands to the micromirrors to switch position.

At power down, the DMD Mirrors are commanded by the DLP controller to move to a near flat (0°) position as shown in Section 9. The flat state position of the DMD mirrors are referred to as the “Parked” state. To maintain long-term DMD reliability, the DMD must be properly “Parked” prior to every power down of the DMD power supplies.

7.3.4 DMD Voltage Supplies

The micromirrors switching requires unique voltage levels to control the mechanical switching. These voltages levels are nominally 16 V, 8.5 V, and –10 V (V_{BIAS}, V_{OFFSET}, and V_{RESET}). The specification values for V_{BIAS}, V_{OFFSET}, and V_{RESET} are shown in Section 6.4.

7.3.5 Logic Reset

Reset of the DMD is required and controlled by the DLP products controller.

7.3.6 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411-Q1 temperature monitoring device. The DLP products controller may monitor the DMD array temperature via the TMP411-Q1 and temperature sense diode.

Figure 7-1 shows the typical connection between the DLP products controller, TMP411-Q1, and the DLP3020-Q1 DMD. The signals to the temperature sense diode are sensitive to system noise, and care should be taken in the routing and implementation of this circuit. See the *TMP411-Q1 data sheet* for detailed PCB layout recommendations.

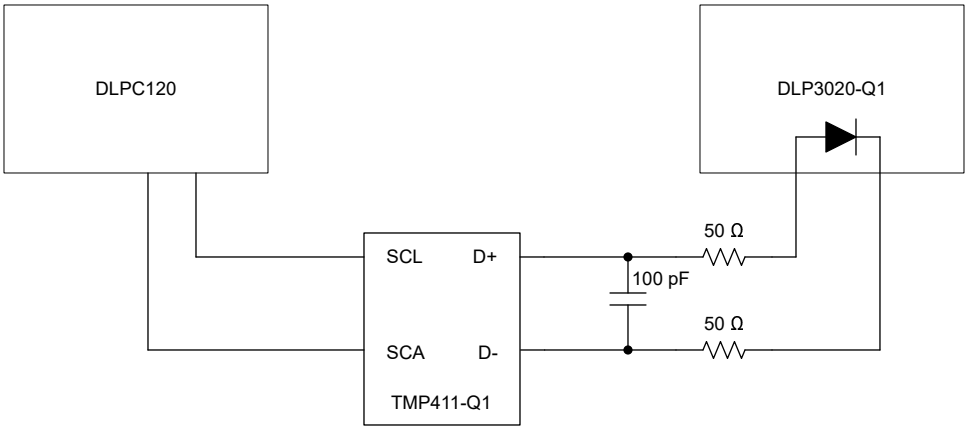


Figure 7-1. Temperature Sense Diode Typical Circuit Configuration

It is recommended that the host controller manage parking of the DMD based on the allowable temperature specifications and temperature measurements.

7.3.6.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Two different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in the base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the *TMP411-Q1 data sheet* for detailed information about temperature diode theory and measurement. Figure 7-2 and Figure 7-3 illustrate the relationship between the current and voltage through the diode.

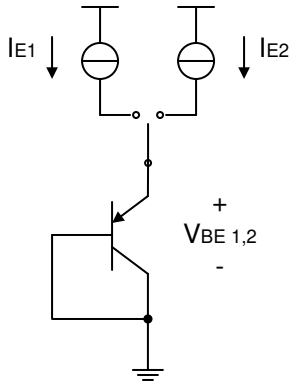


Figure 7-2. Temperature Measurement Theory

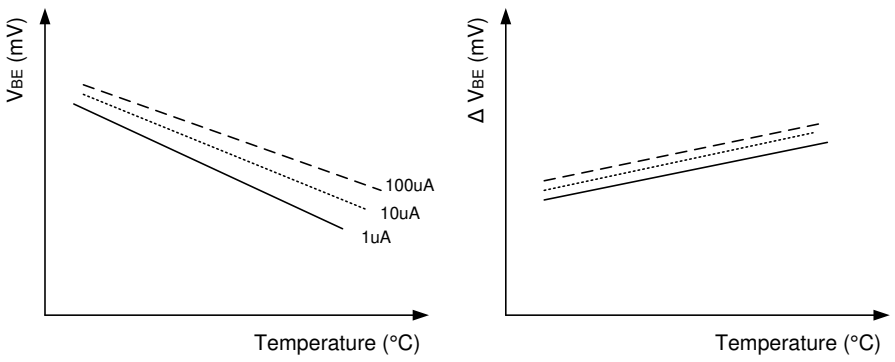


Figure 7-3. Example of Delta VBE vs Temperature

7.3.7 DMD JTAG Interface

The DMD uses 4 standard JTAG signals for sending and receiving boundary scan test data. TCK is the test clock used to drive an IEEE 1149.1 TAP state machine and logic. TMS directs the next state of the TAP state machine. TDI is the scan data input and TDO is the scan data output.

The DMD does not support IEEE 1149.1 signals TRST (Test Logic Reset) and RTCK (Returned Test Clock). Boundary scan cells on the DMD are Observe-Only. To initiate the JTAG boundary scan operation on the DMD, a minimum of 6 TCK clock cycles are required after TMS is set to logic high.

Refer to Figure 7-4 for a JTAG system board routing example.

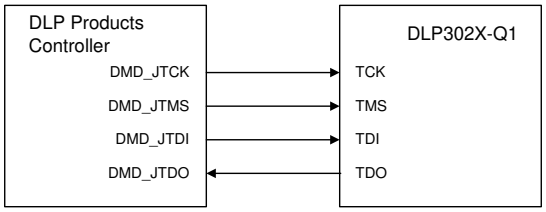


Figure 7-4. System Interface Connection to DLP Products Controller

The DMD Device ID can be read via the JTAG interface. The ID and 32-bit shift order is shown in Figure 7-5.

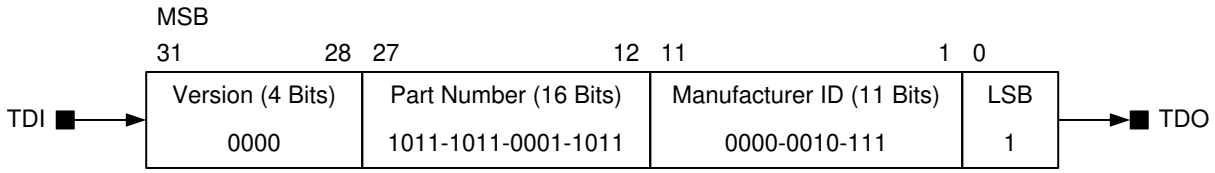


Figure 7-5. DMD Device ID and 32-bit Shift Order

Refer to Figure 7-6 for a JTAG boundary scan block diagram for the DMD. These show the pins and the scan order that are observed during the JTAG boundary scan.

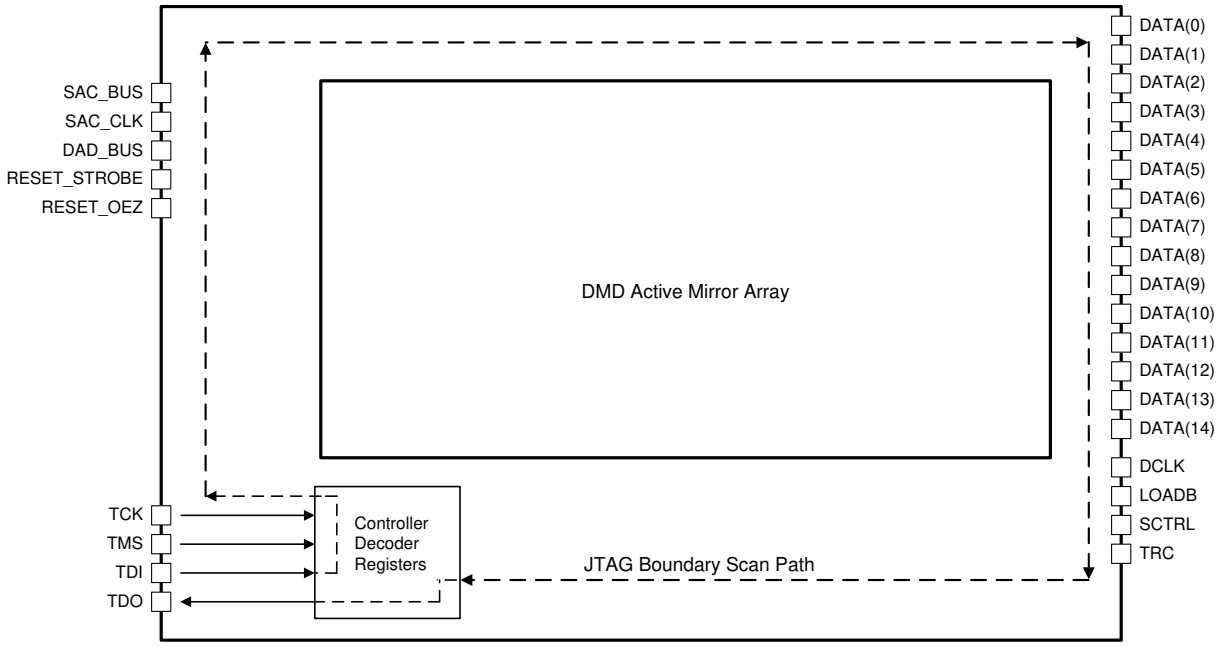


Figure 7-6. JTAG Boundary Scan Path

Refer to Figure 7-7 for a functional block diagram of the JTAG control logic.

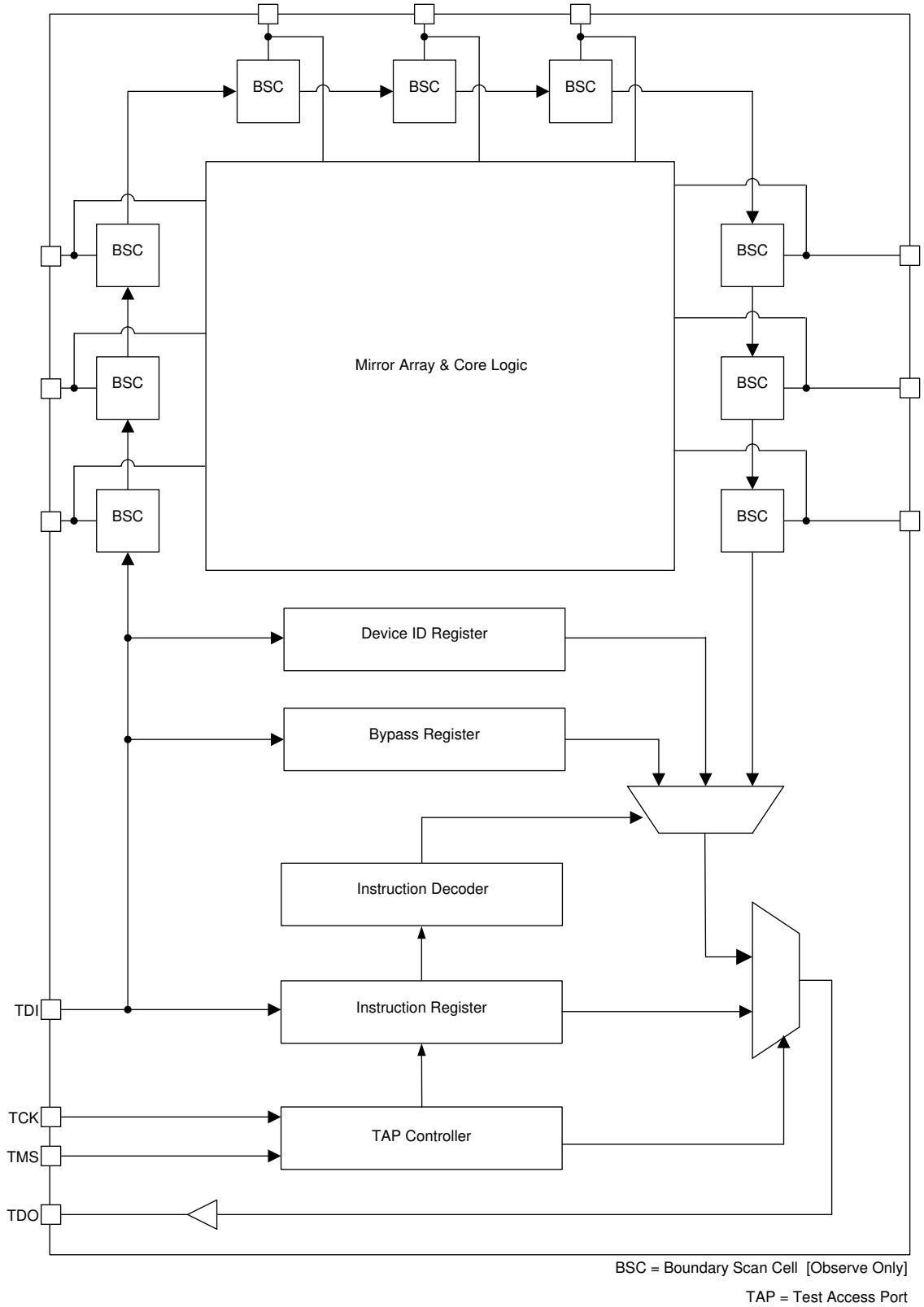


Figure 7-7. JTAG Functional Block Diagram

7.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block flat-state and stray light from passing through the projection lens. The mirror tilt angle defines DMD capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast ratio can be reduced and objectionable artifacts in the image border and/or active area could occur.

7.4.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the image border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill and Alignment

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible. Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Refer to Section 6.4 for a specification on this maximum allowable heat load due to illumination overfill.

7.5 DMD Image Performance Specification

PARAMETER (1)	MIN	NOM	MAX	UNIT
Bright Pixels - Viewed on a linear gray 10 screen			0	micromirrors
Dark Pixels - Viewed on a white screen			4	micromirrors
Optical performance	See *System Optical Considerations*			

(1) Any artifact that is not specifically called out in this table is acceptable. Viewing distance must be > 60 in. Screen size should be similar to application image size. All values referenced are in linear gamma. Non-linear gamma curves may be running by default, and it should be ensured with a TI applications engineer that the equivalent linear gamma value as specified is used to judge artifacts.

7.6 Micromirror Array Temperature Calculation

Active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in Figure 7-8) is provided by the following equations.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = computed DMD array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (TP1 location in Figure 7-8) (°C)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = DMD package thermal resistance from array to TP1 (°C/watt) (see Section 6.5)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (watts)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (watts)
- $Q_{ILLUMINATION}$ = ($C_{L2W} \times S_L$)
- C_{L2W} = conversion constant for screen lumens to power on the DMD (watts/lumen)
- S_L = measured screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown previous are valid for a 1-Chip DMD system with total projection efficiency from DMD to the screen of 87%.

The constant C_{L2W} is based on the DMD array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculation:

- S_L = 50 lm
- C_{L2W} = 0.00293 W/lm
- $Q_{ELECTRICAL}$ = 0.162 W
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = 7.0°C/W
- $T_{CERAMIC}$ = 55°C

$$Q_{ARRAY} = 0.162\ W + (0.00293 \times 50\ lm) = 0.309\ W \quad (3)$$

$$T_{ARRAY} = 55°C + (0.309\ W \times 7.0°C/W) = 57.2°C \quad (4)$$

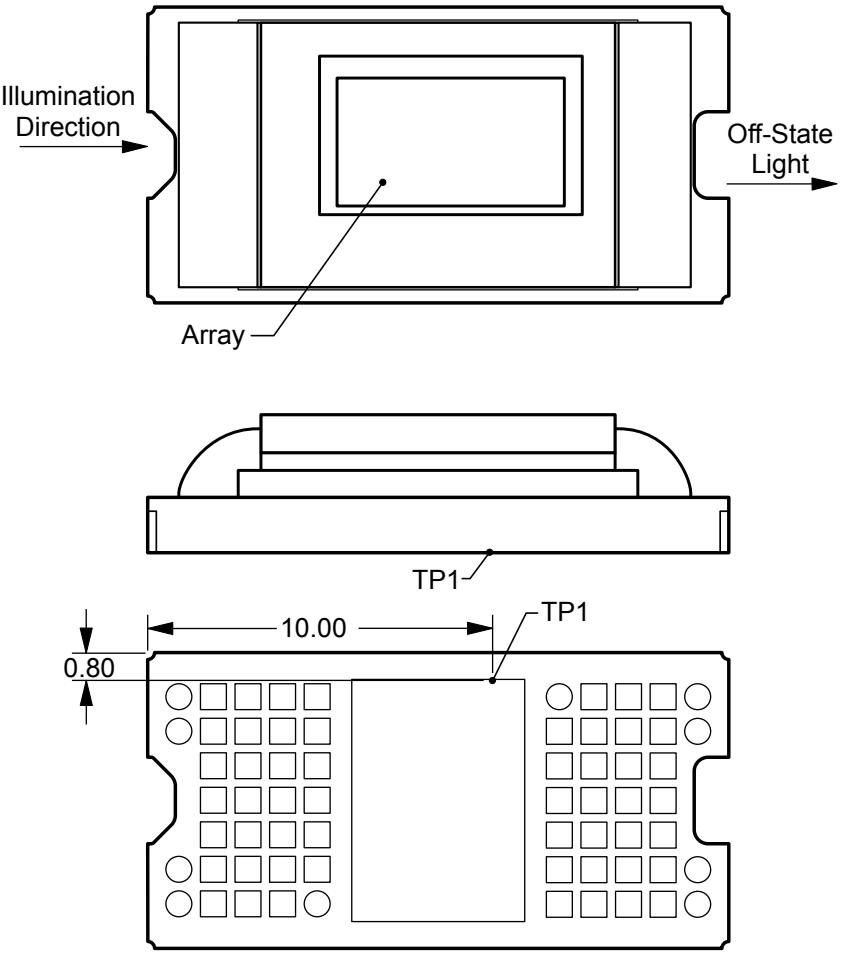


Figure 7-8. Thermocouple Location

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, assuming a fully-saturated white pixel, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DLP3020-Q1 DMD was designed to be used in automotive applications such as head-up display (HUD).

The information shown in this section describes the HUD application based on the TI reference design. Contact TI application engineer for information on this design.

8.2 Typical Application

The DLP3020-Q1 DMD combined with the DLPC120-Q1 are the primary devices that make up the reference design for a HUD system as shown in the block diagram Figure 8-1.

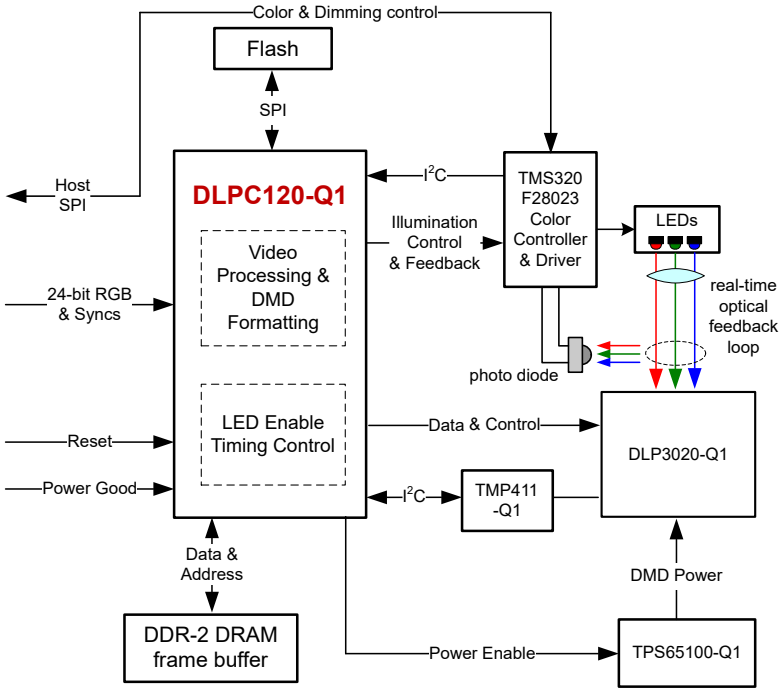


Figure 8-1. HUD Reference Design Block Diagram

The DLPC120-Q1 accepts input video over the parallel RGB data interface up to 8 bits per color from a video graphics processor. The DLPC120-Q1 then processes the video data (864 × 480 manhattan orientation) by scaling the image to match the DMD resolution (608 × 684 diamond pixel), applies de-gamma correction, bezel adjustment, and then formats the data into DMD bit plane information and stores the data into the DDR2 DRAM.

The DMD bit planes are read from DDR2 DRAM, and are then displayed on the DMD using pulse width modulation (PWM) timing. The DLPC120-Q1 synchronizes the DMD bit plane data with the RGB enable timing for the LED color controller and Driver circuit. Finally, the DMD accepts the bit plane formatted data from the DLPC120-Q1 and displays the data according to the timing controlled by the DLPC120-Q1.

Due to the mechanical nature of the micromirrors, the latency of the DLP3020-Q1 and DLPC120-Q1 chipset is fixed across all temperature and operating conditions. The observed video latency is one frame, or 16.67 ms at

an input frame rate of 60 Hz. However, please note that the use of the DLPC120-Q1 bezel adjustment feature, if enabled by the host controller, requires an additional frame of processing.

The DLPC120-Q1 is configured at power up by data stored in the flash file which stores configuration data, DMD and sequence timing information, LED drive information, and other information related to the system functions.

See the DLPC120-Q1 programmer's guide for information about the this flash configuration data.

The HUD reference design from TI includes the TMS320F28023 microcontroller (Piccolo) which is used to control the color point by adjusting the RGB flux levels, and drives each RGB LED. This circuit also manages the dimming function for the HUD system. The dimming level of a HUD system requires very large dynamic range of over 5000:1. For example, on a bright day, the HUD system may require a brightness level as high as 15,000 cd/m^2 and conversely at night time the minimum brightness level desired may only be 3 cd/m^2.

8.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation, the automotive DMD reliability lifetime estimates Application Report may be provided. See the TI Application team for more information.

9 Power Supply Recommendations

9.1 Power Supply Sequencing Requirements

- V_{BIAS}, V_{CC}, V_{OFFSET}, V_{REF}, V_{RESET}, V_{SS} are required to operate the DMD.

CAUTION

- For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power up and power down procedures may affect device reliability.
- The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power up and power down operations. Failure to meet any of the following requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 9-1. V_{SS} must also be connected.

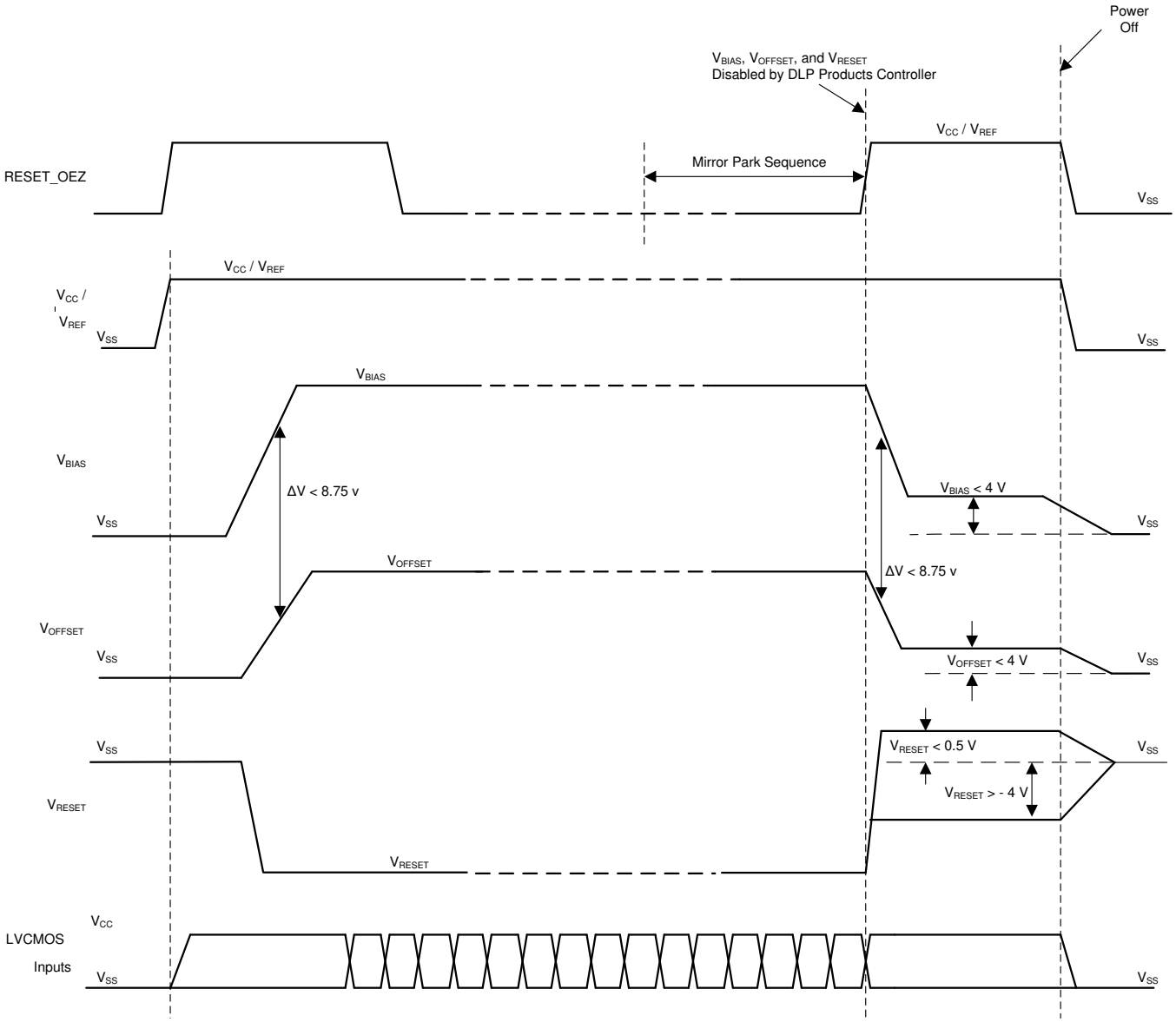
DMD Power Supply Power Up Procedure:

- During power up, V_{CC} and V_{REF} must always start and settle before V_{OFFSET}, V_{BIAS} and V_{RESET} voltages are applied to the DMD.
- During power up, V_{BIAS} does not have to start after V_{OFFSET}. However, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (refer to Note 1 for Figure 9-1).
- During power up, the DMD's LVCMOS input pins shall not be driven high until after V_{CC} and V_{REF} have settled at operating voltage.
- During power up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power up are flexible, provided that the transient voltage levels follow the requirements listed previously in Section 6.4 and in Figure 9-1.

DMD Power Supply Power Down Procedure

- V_{CC} and V_{REF} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power down it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (refer to Note 1 for Figure 9-1).
- During power down, the DMD's LVCMOS input pins must be less than V_{REF} + 0.3 V.
- During power down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power down are flexible, provided that the transient voltage levels follow the requirements listed previously in Section 6.4 and in Figure 9-1.

9.1.1 Power Up and Power Down



Note 1: ±8.75-V delta, ΔV, shall be considered the max operating delta between V_{BIAS} and V_{OFFSET}. Customers may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power up and to remove V_{BIAS} prior to V_{OFFSET} during power down.

Figure 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

10 Layout

10.1 Layout Guidelines

For specific DMD PCB guidelines, use the following:

- V_{CC} should have at least 1 × 2.2-µF and 4 × 0.1-µF capacitors evenly distributed among the V_{CC} pins.
- A 0.1-µF, X7R rated capacitor should be placed near every pin for the V_{REF}, V_{BIAS}, V_{RSET}, and V_{OFF}.

10.2 Temperature Diode Pins

The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411-Q1 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411-Q1 are sensitive to noise. See the *TMP411-Q1 data sheet* for specific routing recommendations.

Avoid routing the temperature diodes signals near other traces to reduce coupling of noise onto these signals.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

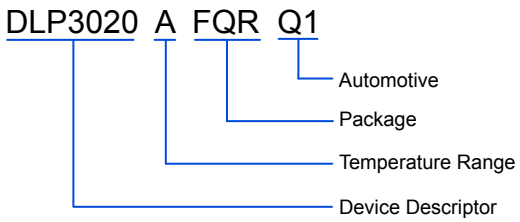


Figure 11-1. Part Number Description

11.1.2 Device Markings

The device marking is shown in Figure 11-2. The marking will include both human-readable information and a 2-dimensional matrix code.

The human-readable information is described in Figure 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number and lot trace code.

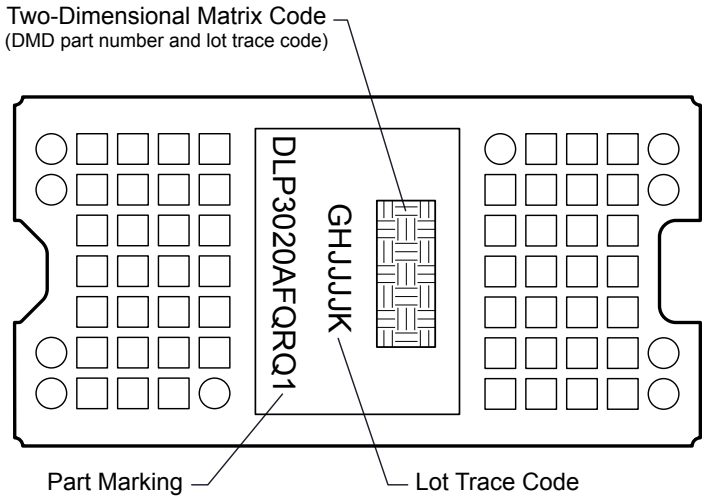


Figure 11-2. DMD Marking

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- DLPC120-Q1 product folder for the DLPC120-Q1 data sheet and other documentation
- Texas instruments, *TMS320F2802x Microcontrollers* (Piccolo™) data sheet
- Texas Instruments, *TMP411-Q1 ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction* data sheet
- Texas Instruments, *DMD Optical Efficiency for Visible Wavelengths* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Device Handling

The DMD is an optical device so precautions should be taken to avoid damaging the glass window. Please see the DMD Handling application note for instructions on how to properly handle the DMD.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3020AFQRQ1	ACTIVE	CLGA	FQR	54	126	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

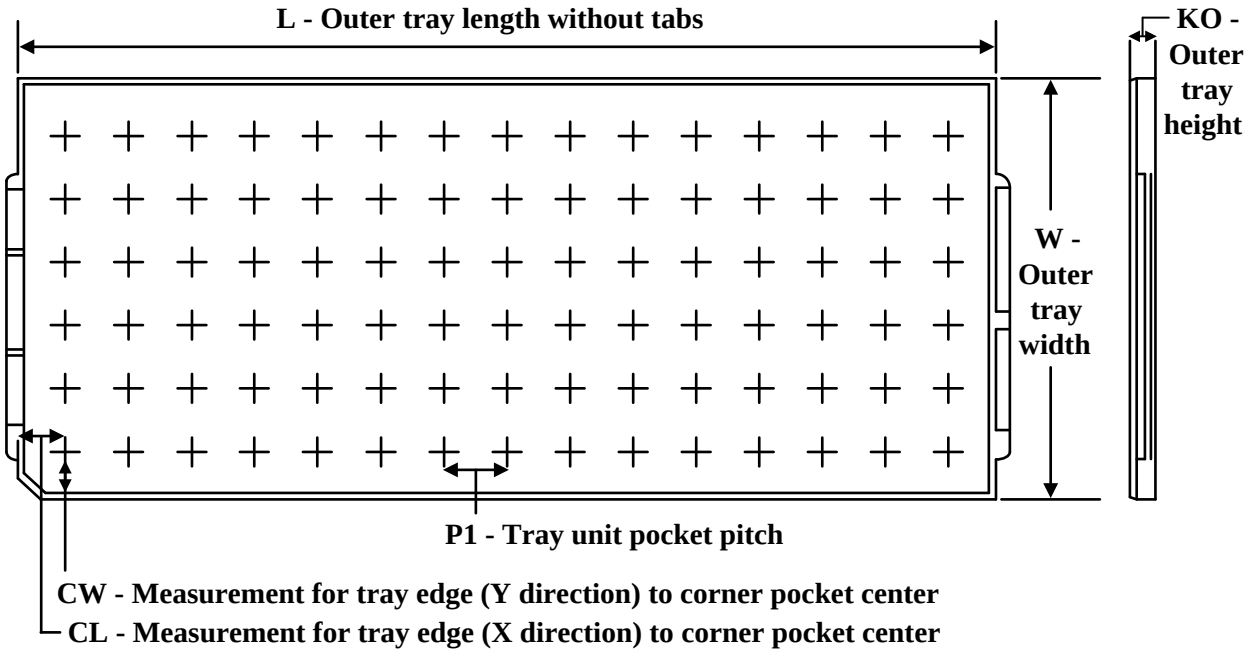
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

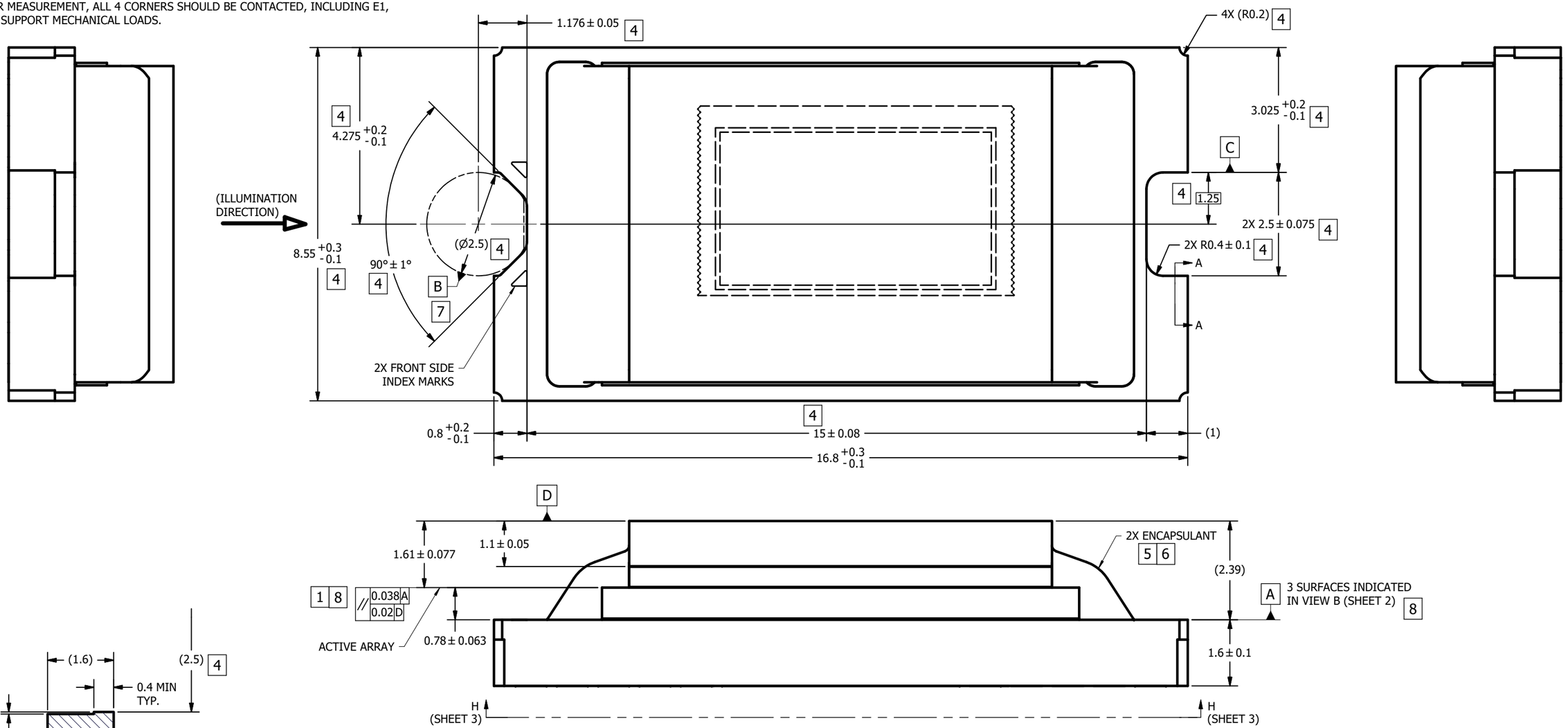
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP3020AFQRQ1	FQR	CLGA	54	126	9 x 14	150	315	135.9	12190	21.9	15.15	16.95

REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2181963: INITIAL RELEASE	6/25/2019	BMH
B	ECO 2184085: ADD FRONT AND BACK SIDE INDEX MARKS	11/8/2019	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.



SECTION A-A
NOTCH OFFSETS

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	6/25/2019
ENGINEER	B. HASKETT	6/24/2019
QA/CE	S. HUDGENS	6/24/2019
CM	M. LOPEZ	6/30/2019
	B. RAY	6/24/2019
APPROVED	J. GRIMMETT	6/26/2019

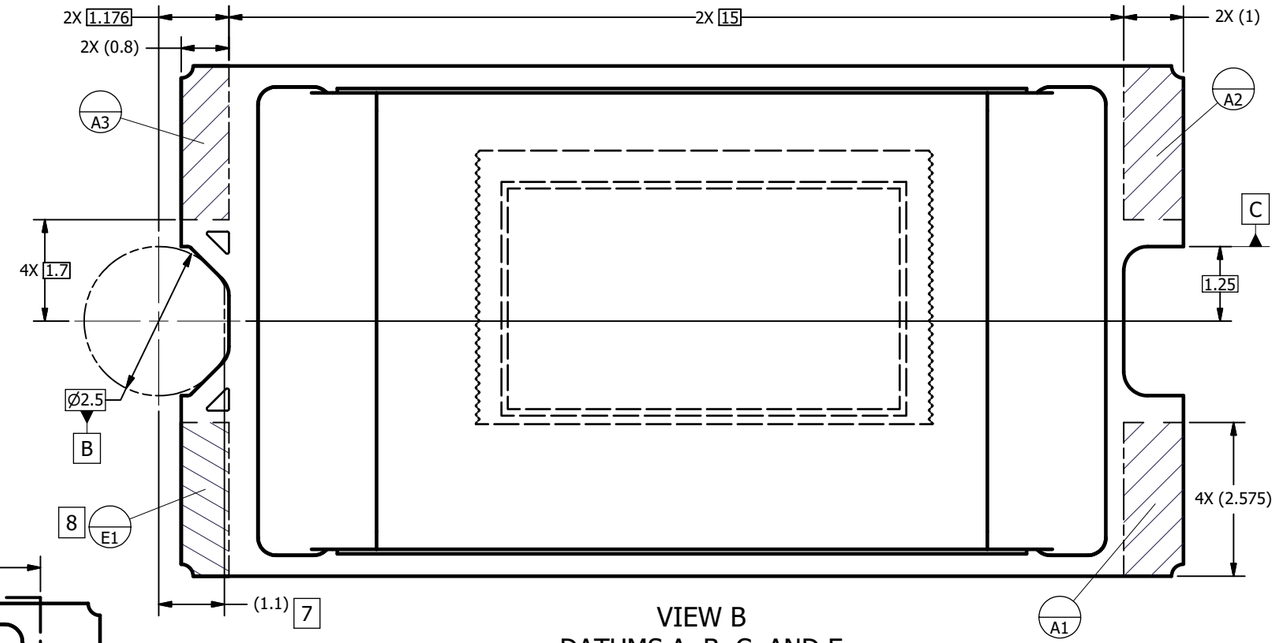
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .3 WVGA SERIES 247 (FQR PACKAGE)

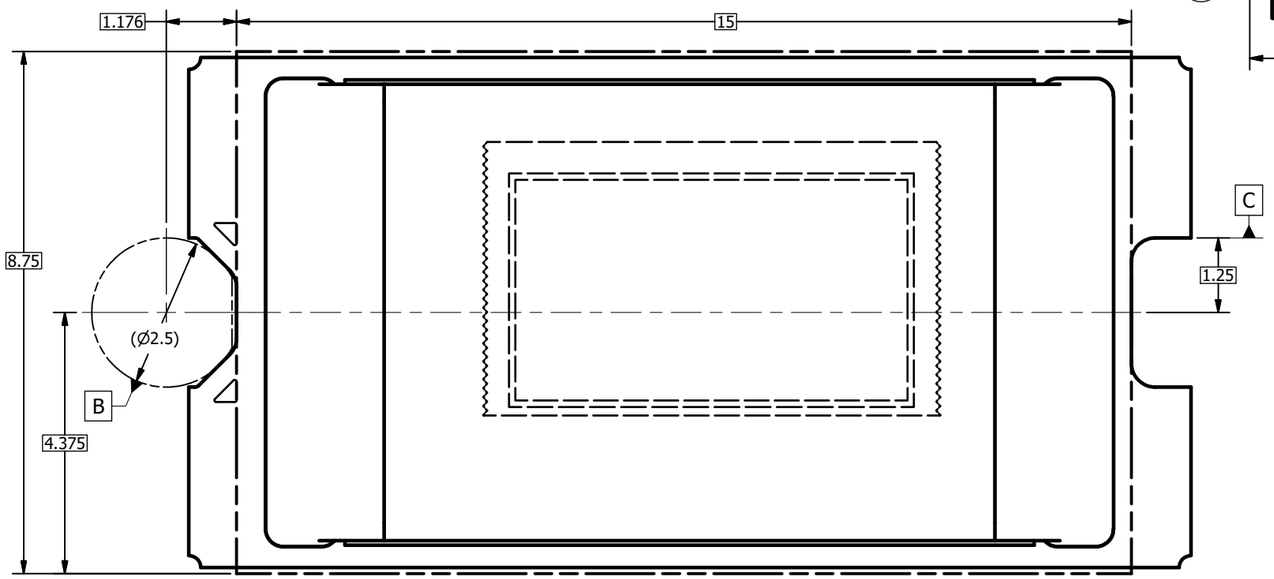
SIZE	DWG NO	REV
D	2516663	B

SCALE 20:1 SHEET 1 OF 3

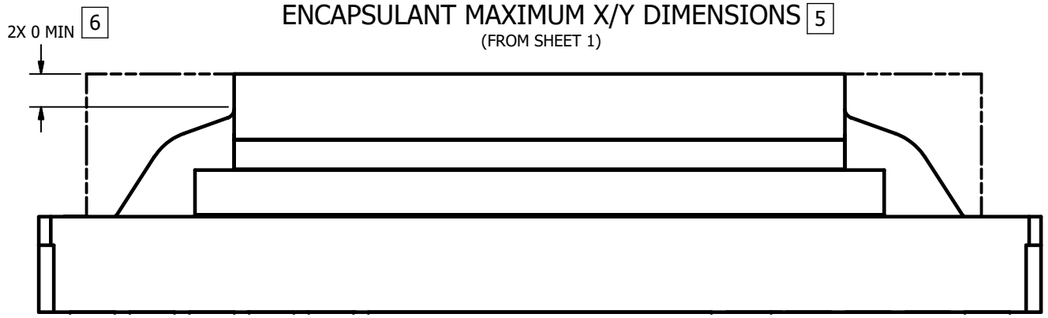
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



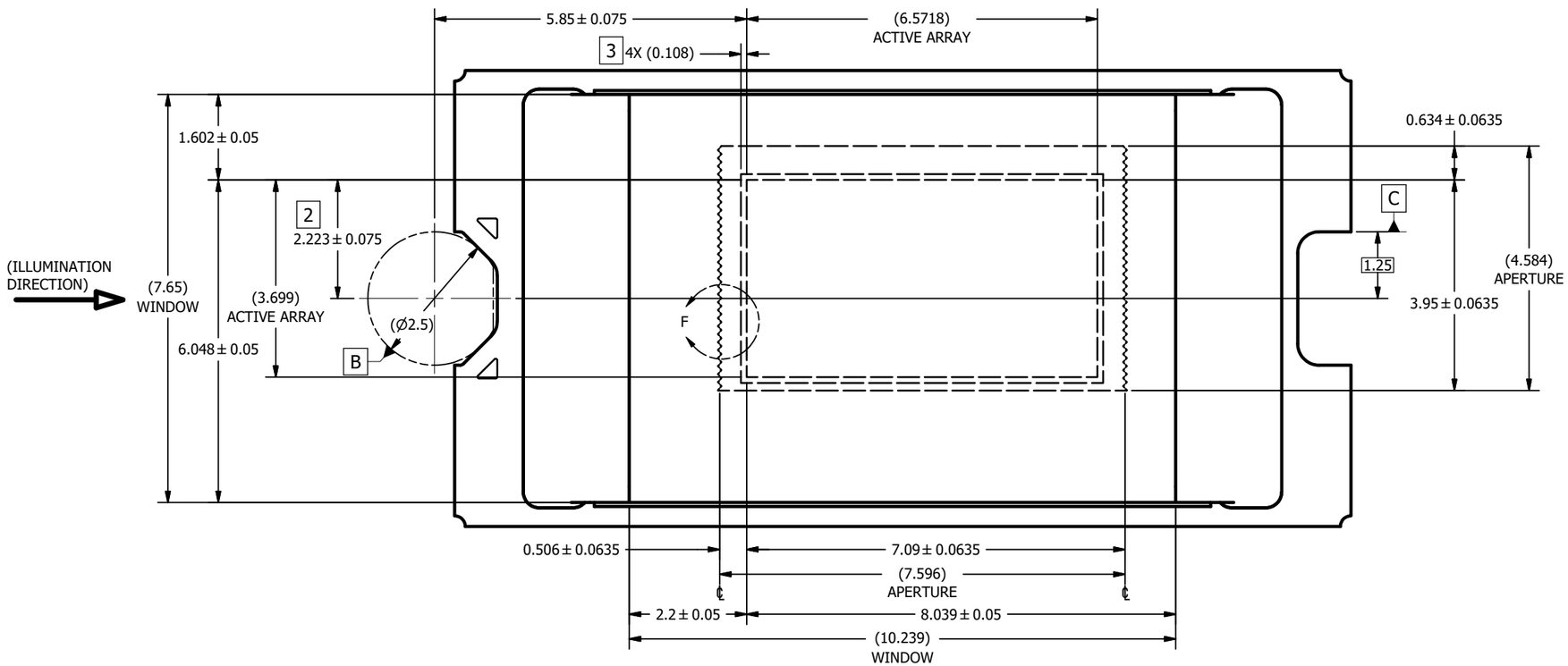
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)



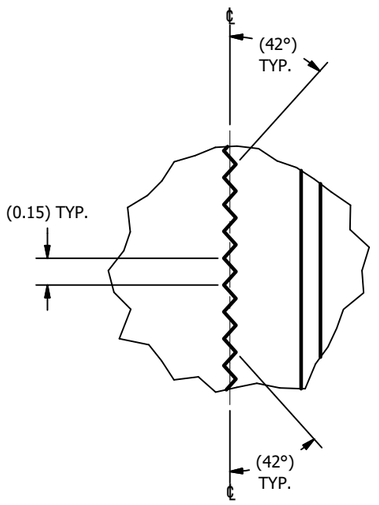
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 6/25/2019	SIZE D	DWG NO 2516663 REV B
			SCALE	SHEET 2 OF 3

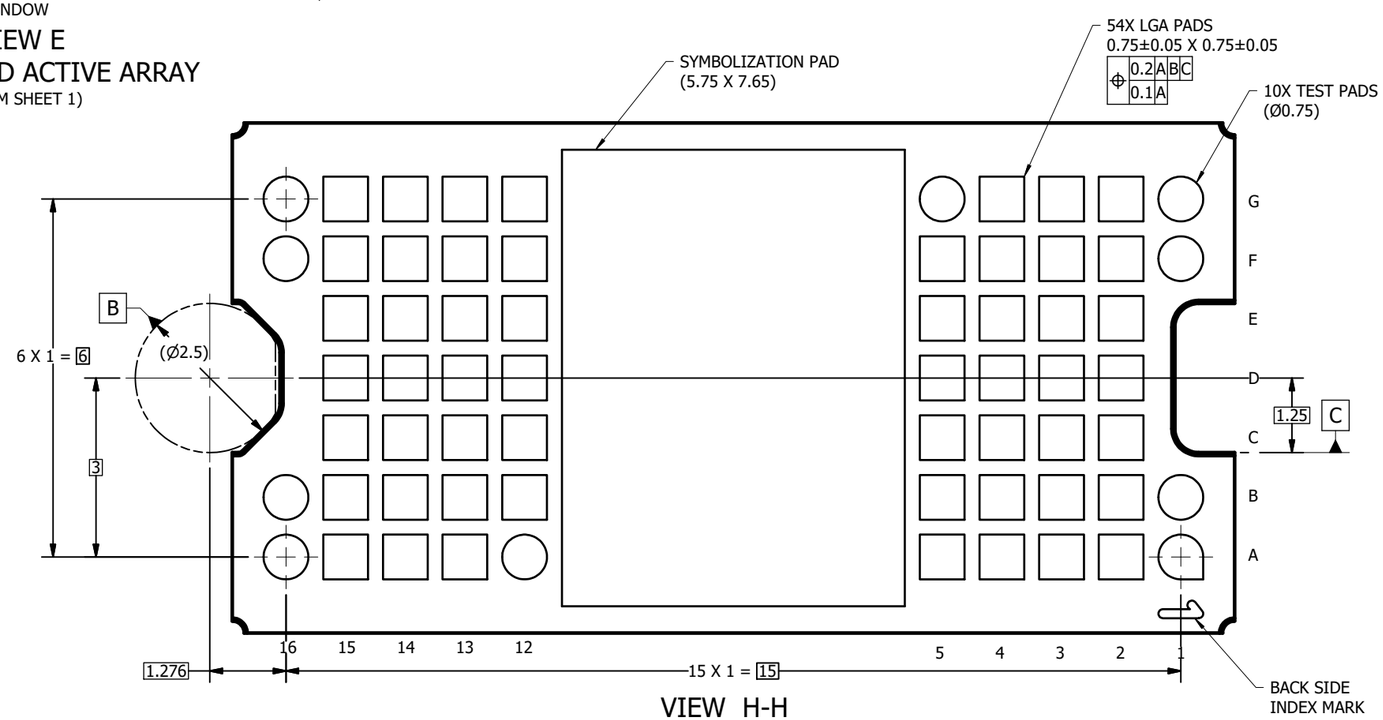
INV11-2006a



VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT AND RIGHT EDGES
(WINDOW OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 6/25/2019	SIZE D	DWG NO 2516663	REV B
			SCALE	SHEET 3 OF 3	

INV11-2006a

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