DAC7811 12-Bit, Serial Input, Multiplying Digital-to-Analog Converter

1 Features

- 2.7-V to 5.5-V Supply Operation
- 50-MHz Serial Interface
- 10-MHz Multiplying Bandwidth
- ±15-V Reference Input
- Low Glitch Energy: 5 nV-s
- Extended Temperature Range: –40°C to +125°C
- 10-Pin VSSOP Package
- 12-Bit Monotonic
- 4-Quadrant Multiplication
- Power-On Reset With Brownout Detection
- Daisy-Chain Mode
- Readback Function
- Industry-Standard Pin Configuration

2 Applications

- Portable Battery-Powered Instruments
- Waveform Generators
- Analog Processing
- Programmable Amplifiers and Attenuators
- Digitally Controlled Calibration
- Programmable Filters and Oscillators
- Composite Video
- Ultrasound

3 Description

The DAC7811 is a CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.7-V to 5.5-V power supply, making it suitable for battery-powered and many other applications.

This DAC uses a double-buffered 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE, and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple devices are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7811 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10 MHz. The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

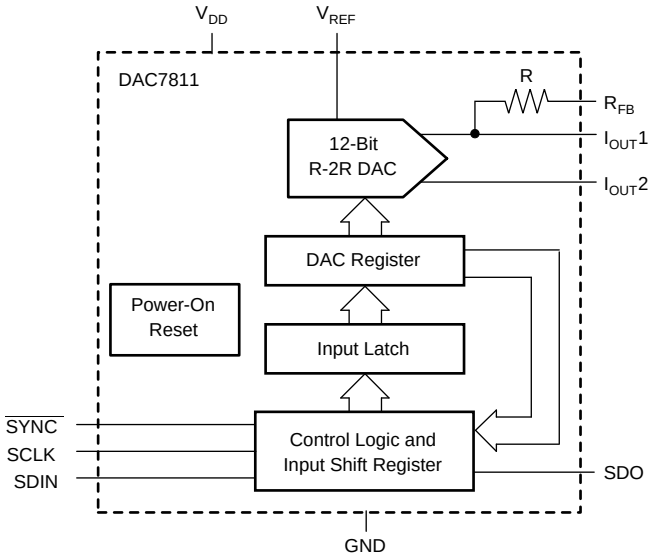
The DAC7811 is available in a 10-lead VSSOP package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC7811	VSSOP (10)	3.00 mm 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2016) to Revision E — **Page**

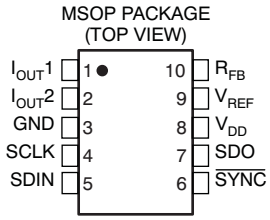
- Changed Figure 28 SDO pin timing to remove Hi-Z ... 14

Changes from Revision C (July 2007) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$I_{OUT}1$	O	DAC Current Output
2	$I_{OUT}2$	O	DAC Analog Ground. This pin is normally tied to the analog ground of the system.
3	GND	G	Ground pin.
4	SCLK	I	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK.
5	SDIN	I	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to the rising edge.
6	$\overline{SYNC}$	I	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks (power-on default is falling clock edge). In stand-alone mode, the serial interface counts the clocks and data is latched to the shift register on the 16th active clock edge.
7	SDO	O	Serial Data Output. This allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data will always be clocked out on the alternate edge to loading data to the shift register. Writing the Readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge.
8	V_{DD}	I	Positive Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
9	V_{REF}	I	DAC Reference Voltage Input
10	R_{FB}	O	DAC Feedback Resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{DD} to GND	–0.3	7	V
Digital input voltage to GND	–0.3	V_{DD} + 0.3	V
$I_{OUT}1$, $I_{OUT}2$ to GND	–0.3	V_{DD} + 0.3	V
Operating temperature	–40	125	°C
Junction temperature, (T_J max)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage to GND		2.7		5.5	V
V_{REF}	Reference voltage		–15		15	V
V_{IL}	Input low voltage	V_{DD} = 2.7 V			0.6	V
		V_{DD} = 5 V			0.8	V
V_{IH}	Input high voltage	V_{DD} = 2.7 V	2.1			V
		V_{DD} = 5 V	2.4			V
T_A	Operating ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DAC7811 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = 10 V; T_A = full operating temperature. All specifications –40°C to 125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
Resolution			12			Bits
Relative accuracy					±1	LSB
Differential nonlinearity					±1	LSB
Output leakage current		Data = 0000h, T_A = 25°C			±5	nA
Output leakage current		Data = 0000h, $T_A = T_{MAX}$			±25	nA
Full-scale gain error		All ones loaded to DAC register		±5	±10	mV
Full-scale tempco(1)				±5		ppm/°C
Output capacitance(1)		Code dependent		5		pF
REFERENCE INPUT						
Input resistance			8	10	12	kΩ
R_{FB} resistance			8	10	12	kΩ
LOGIC INPUTS AND OUTPUT(1)						
I_{IL}	Input leakage current				10	µA
C_{IL}	Input capacitance				10	pF
INTERFACE TIMING (see Figure 28)						
f_{CLK}					50	MHz
t_C	Clock period		20			ns
t_{CH}	Clock pulse width high		8			ns
t_{CC}	Clock pulse width low		8			ns
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK active edge setup time		13			ns
t_{CST}	SCLK active edge to $\overline{SYNC}$ rising edge hold time		5			ns
t_{DS}	Data setup time		5			ns
t_{DH}	Data hold time		3			ns
t_{SH}	$\overline{SYNC}$ high time		30			ns
t_{DDS}	$\overline{SYNC}$ inactive edge to SDO valid	V_{DD} = 2.7 V		25	35	ns
		V_{DD} = 5 V		20	30	ns
POWER REQUIREMENTS						
I_{DD} (normal operation)		Logic inputs = 0 V			5	µA
V_{DD} = 4.5 V to 5.5 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		0.8	5	µA
V_{DD} = 2.7 V to 3.6 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		0.4	2.5	µA
AC CHARACTERISTICS(1)						
Output voltage settling time					0.2	µs
Reference multiplying BW		V_{REF} = 7 V_{PP}, Data = FFFh		10		MHz
DAC glitch impulse		V_{REF} = 0 V to 10 V, Data = 7FFh to 800h to 7FFh		5		nV-s
Feedthrough error V_{OUT}/V_{REF}		Data = 000h, V_{REF} = 100 kHz		–60		dB
Digital feedthrough				2		nV-s
Total harmonic distortion				–105		dB
Output spot noise voltage				18		nV/√Hz

(1) Specified by design and characterization; not production tested.

6.6 Typical Characteristics: V_{DD} = 5 V

At T_A = 25°C, unless otherwise noted.

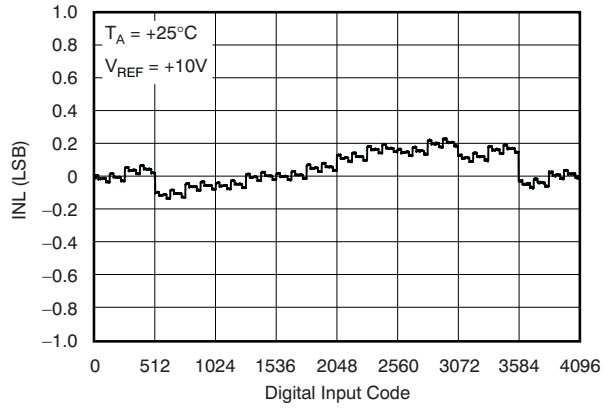


Figure 1. Linearity Error vs Digital Input Code

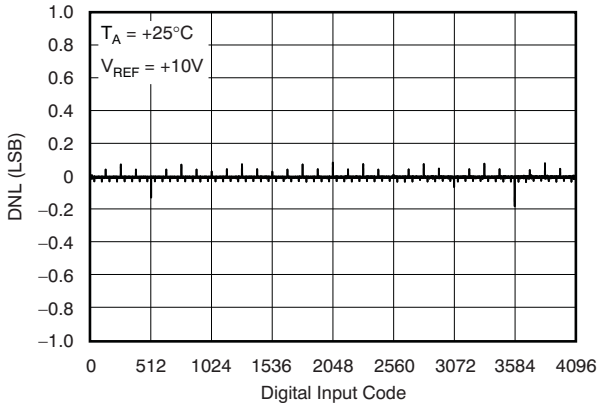


Figure 2. Differential Linearity Error vs Digital Input Code

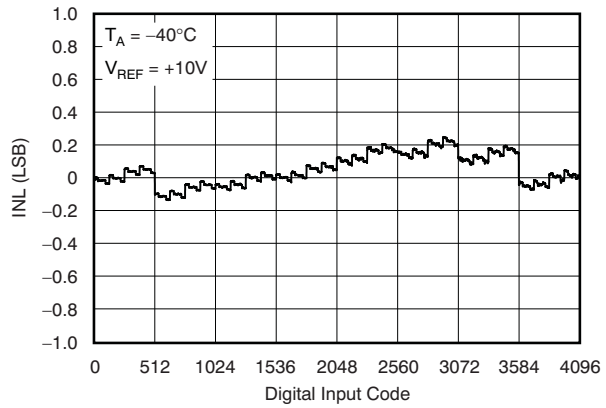


Figure 3. Linearity Error vs Digital Input Code

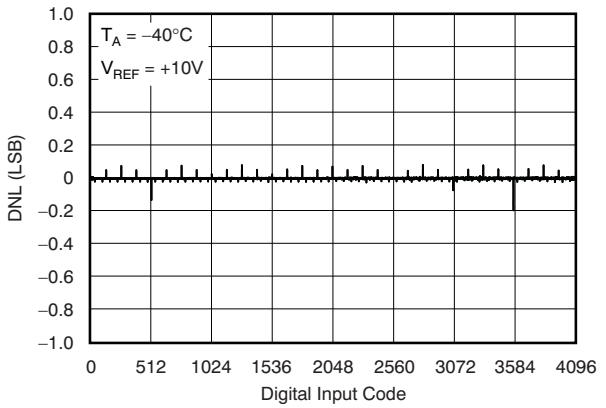


Figure 4. Differential Linearity Error vs Digital Input Code

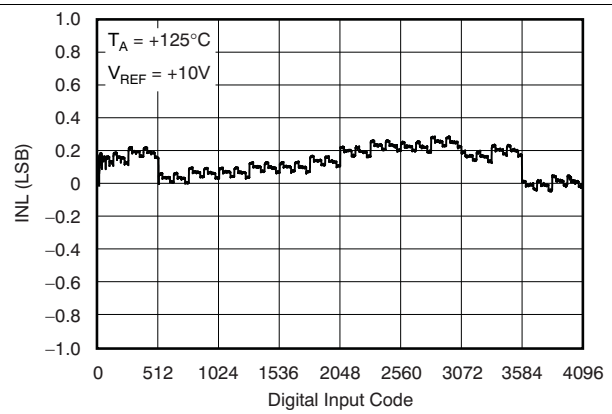


Figure 5. Linearity Error vs Digital Input Code

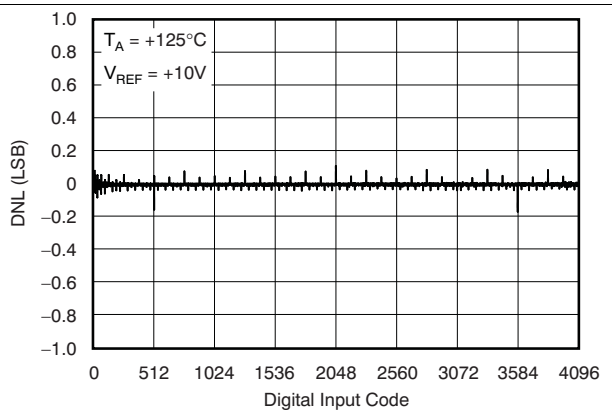


Figure 6. Differential Linearity Error vs Digital Input Code

Typical Characteristics: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted.

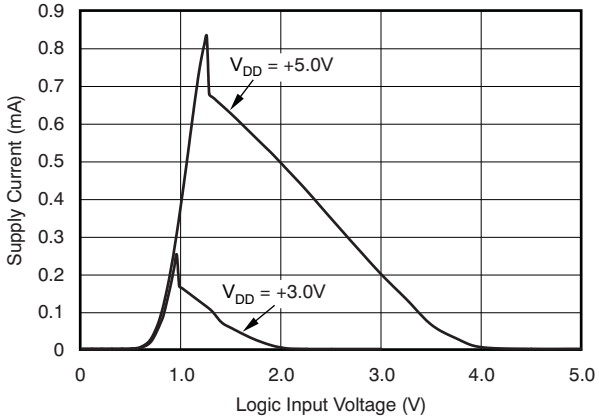


Figure 7. Supply Current vs Logic Input Voltage

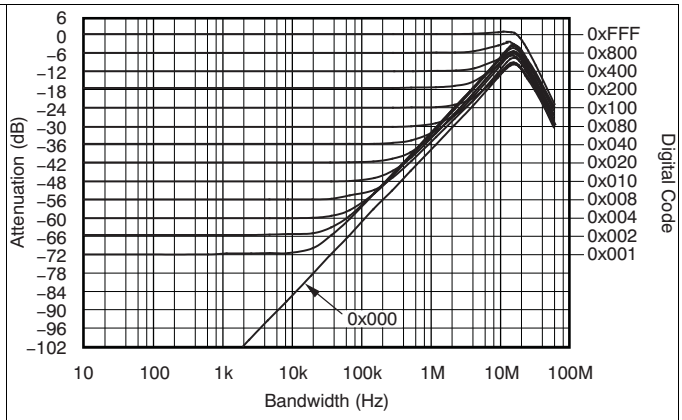


Figure 8. Reference Multiplying Bandwidth

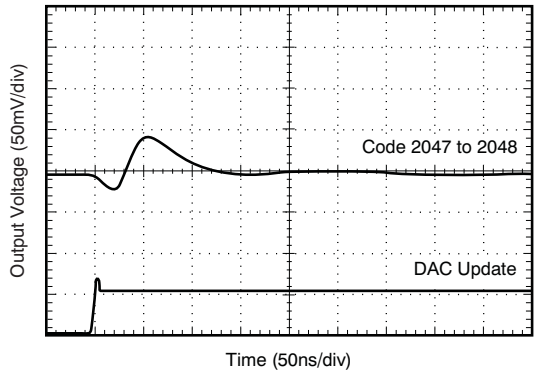


Figure 9. Midscale DAC Glitch

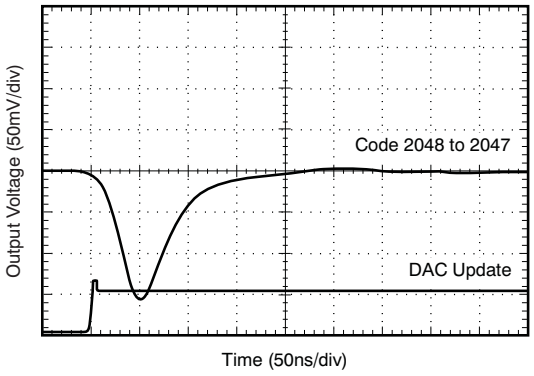


Figure 10. Midscale DAC Glitch

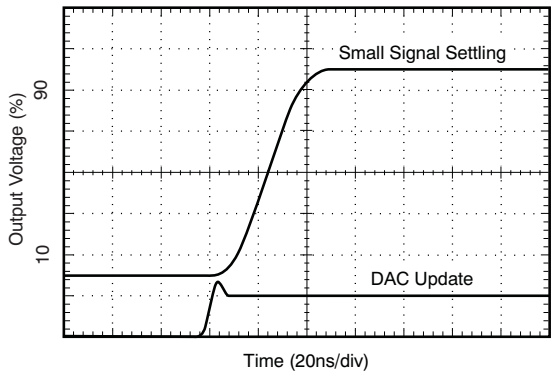


Figure 11. DAC Settling Time

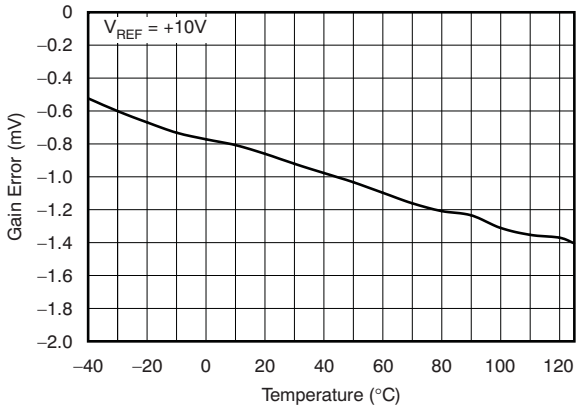


Figure 12. Gain Error vs Temperature

Typical Characteristics: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted.

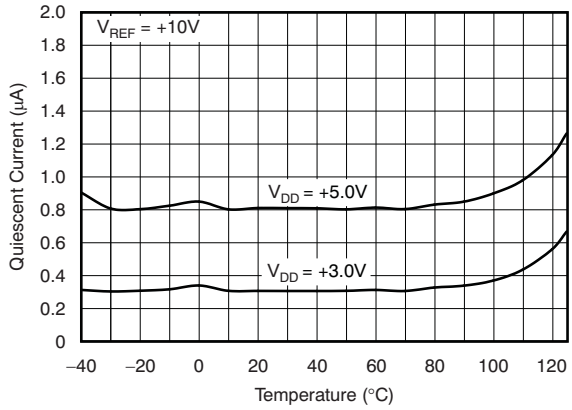


Figure 13. Supply Current vs Temperature

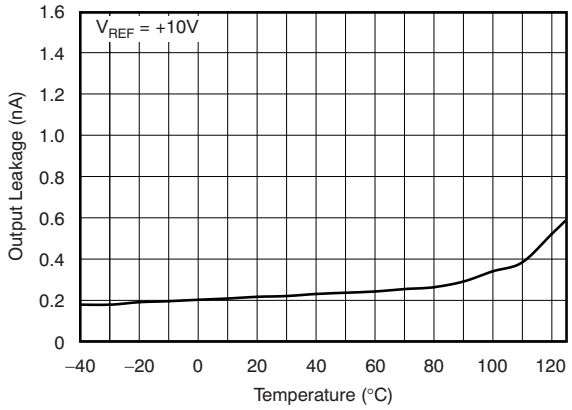


Figure 14. Output Leakage vs Temperature

6.7 Typical Characteristics: V_{DD} = 2.7 V

At T_A = 25°C, unless otherwise noted.

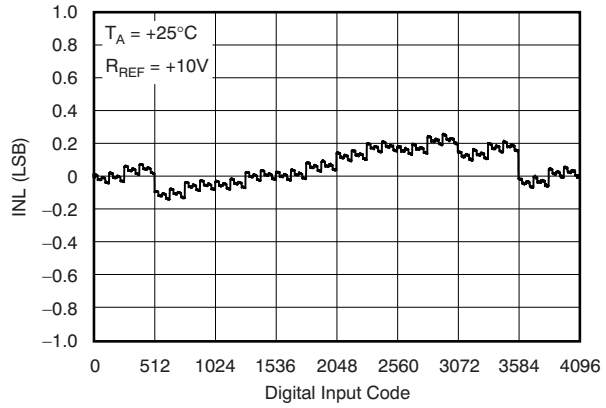


Figure 15. Linearity Error vs Digital Input Code

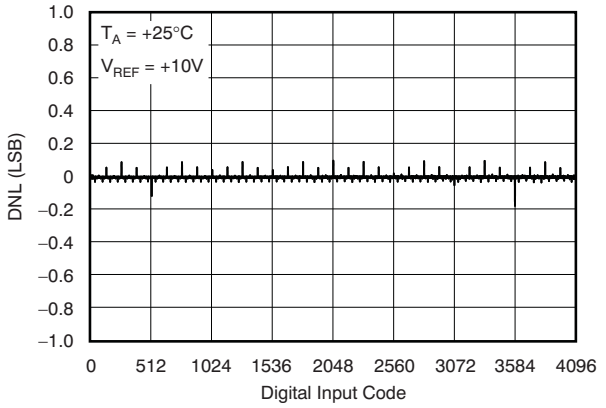


Figure 16. Differential Linearity Error vs Digital Input Code

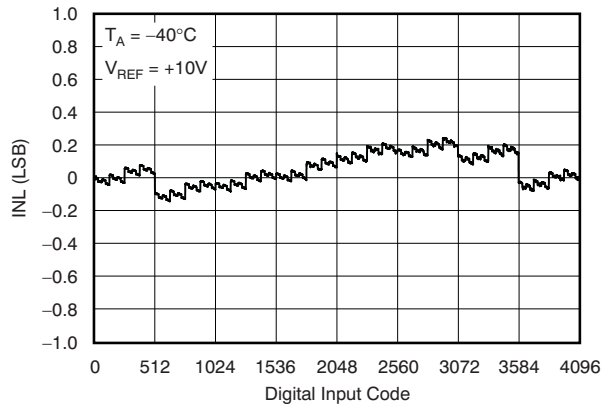


Figure 17. Linearity Error vs Digital Input Code

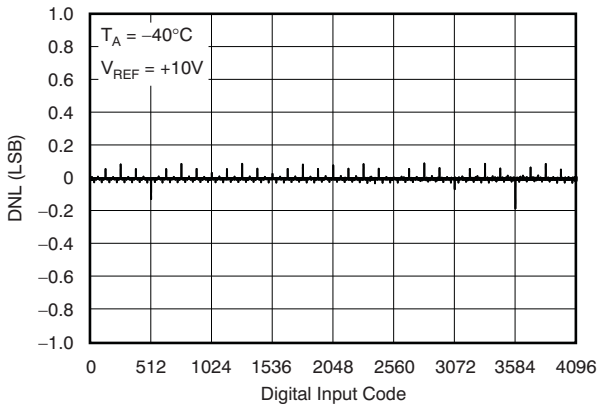


Figure 18. Differential Linearity Error vs Digital Input Code

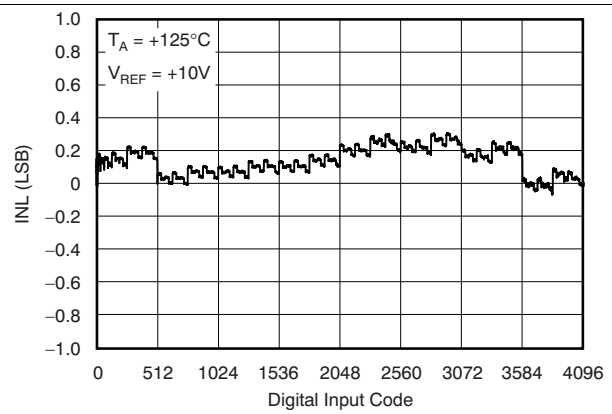


Figure 19. Linearity Error vs Digital Input Code

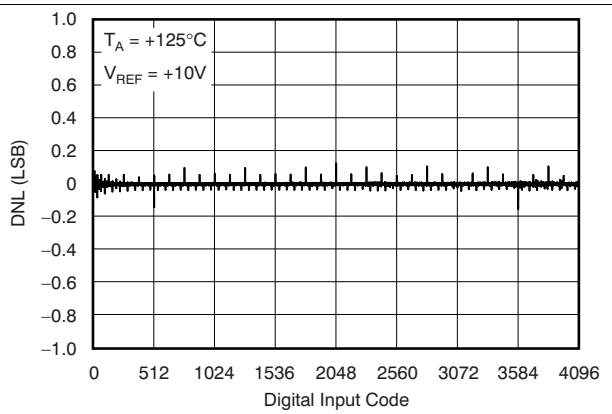


Figure 20. Differential Linearity Error vs Digital Input Code

Typical Characteristics: V_{DD} = 2.7 V (continued)

At T_A = 25°C, unless otherwise noted.

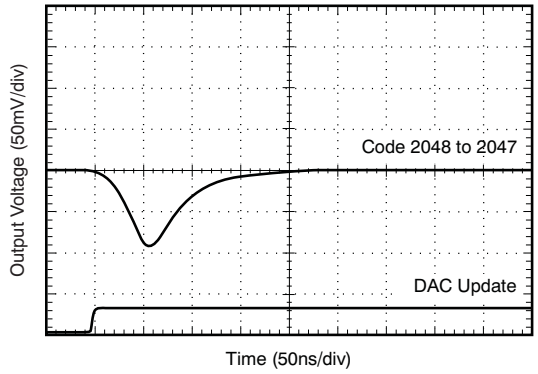


Figure 21. Midscale DAC Glitch

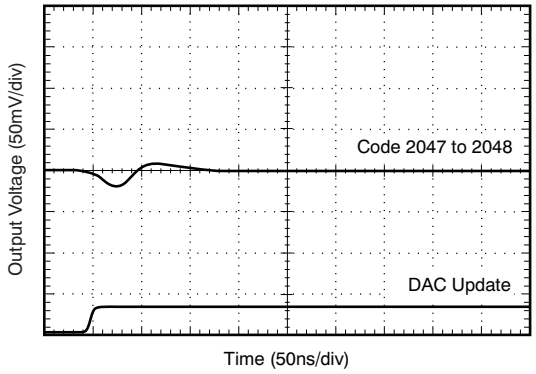


Figure 22. Midscale DAC Glitch

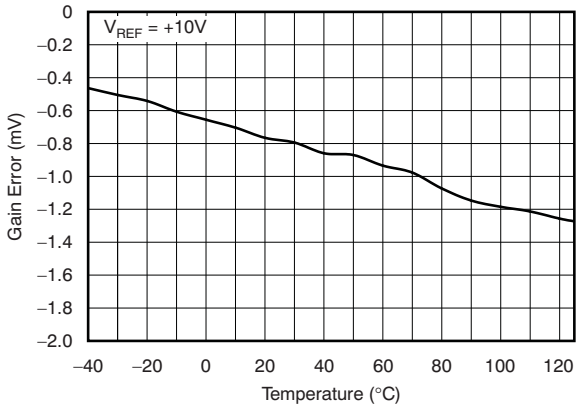


Figure 23. Gain Error vs Temperature

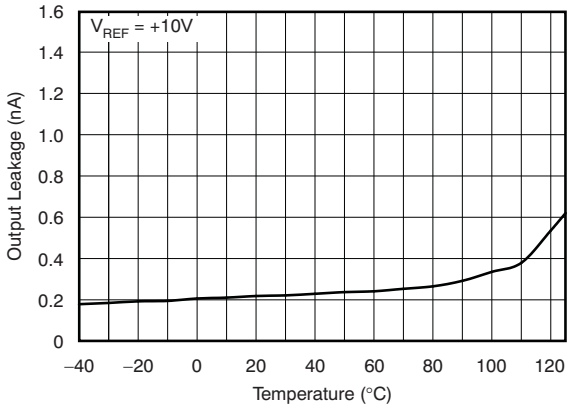


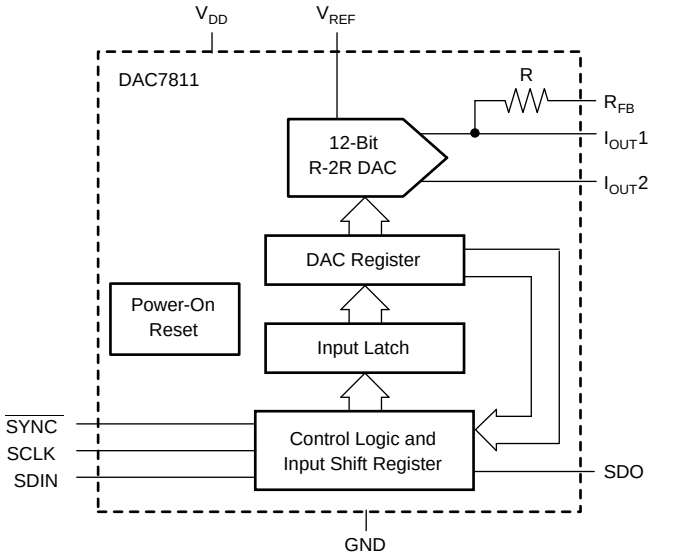
Figure 24. Output Leakage vs Temperature

7 Detailed Description

7.1 Overview

The DAC7811 is a CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.7-V to 5.5-V power supply, making it suitable for battery-powered and many other applications. This DAC uses a double-buffered 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE, and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple devices are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeroes and the DAC outputs are at zero scale.

7.2 Functional Block Diagram



7.3 Feature Description

The DAC7811 is a single channel, current output, 12-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 25, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to $I_{OUT}1$ or the $I_{OUT}2$ terminal. The $I_{OUT}1$ terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 10kΩ ±20%. The external reference voltage can vary over a range of –15V to +15V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC7811 R_{FB} resistor, output voltage ranges of $–V_{REF}$ to V_{REF} can be generated.

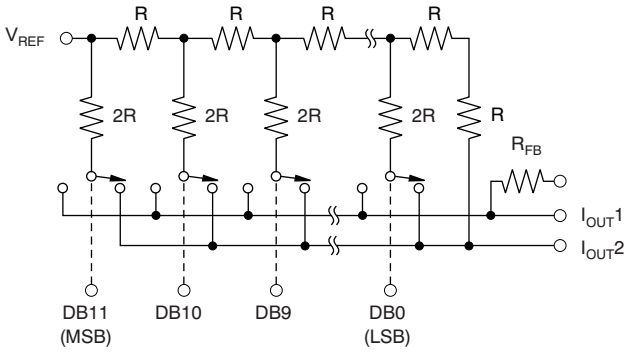


Figure 25. Equivalent R-2R DAC Circuit

Feature Description (continued)

When using an external I/V converter and the DAC7811 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \left(\frac{CODE}{4096} \right) \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the $I_{OUT}1$ terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC $I_{OUT}1$ terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7811 due to offset modulation versus DAC code.

For best linearity performance of the DAC7811, a low offset voltage op amp (such as the OPA277) is recommended (see Figure 26). This circuit allows V_{REF} swinging from –10 V to 10 V.

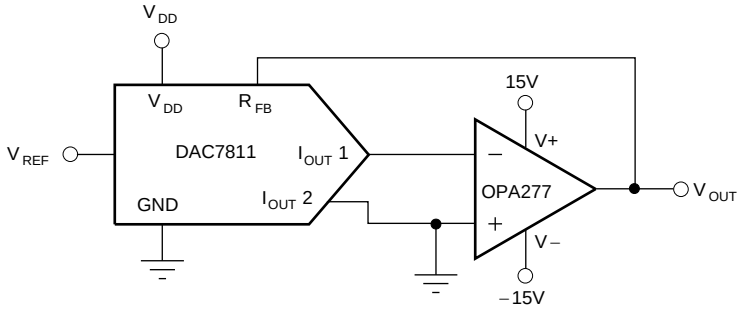


Figure 26. Voltage Output Configuration

7.4 Device Functional Modes

7.4.1 Serial Interface

The DAC7811 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and SDIN), which is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most Digital Signal Processor (DSP) devices. See the Serial Write Operation timing diagram (Figure 28) for an example of a typical write sequence. The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line are clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC7811 compatible with high-speed DSPs. The SDIN and SCLK input buffers are gated off while $\overline{SYNC}$ is high which minimizes the power dissipation of the digital interface. After $\overline{SYNC}$ goes low, the digital interface will respond to the SDIN and SCLK input signals and data can now be shifted into the device. If an inactive clock edge occurs after $\overline{SYNC}$ goes low, but before the first active clock edge, it will be ignored. If the SDO pin is being used then $\overline{SYNC}$ must remain low until after the inactive clock edge that follows the 16th active clock edge.

7.4.2 Input Shift Register

The input shift register is 16 bits wide, as shown in Figure 27. The four MSBs are the control bits C3–C0; these bits determine which function will be executed at the rising edge of $\overline{SYNC}$ in daisy-chain mode or the 16th active clock edge in stand-alone mode. The remaining 12 bits are the data bits. On a load and update command (C3–C0 = 0001) these 12 data bits will be transferred to the DAC register; otherwise, they have no effect. Table 1 shows serial shift register and DAC register operation with CLK and $\overline{SYNC}$ pin settings.

Device Functional Modes (continued)

4 CONTROL BITS				12 DATA BITS											
B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
C3	C2	C1	C0	DB11											DB0

Figure 27. Contents of the 16-Bit Input Shift Register

Table 1. Control Logic Truth Table(1)

CLK	$\overline{\text{SYNC}}$	SERIAL SHIFT REGISTER	DAC REGISTER
X	H	No effect	Latched
↓–	L	Shift register data advanced one bit	Latched
X	↑+	In daisy-chain mode, the function as determined by C3-C0 is executed.	In daisy-chain mode, the contents may change as determined by C3-C0.

(1) ↓– Negative logic transition, default CLK mode;↑+ Positive logic transition; **X** = Do not care.

7.4.3 $\overline{\text{SYNC}}$ Interrupt (Stand-Alone Mode)

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs.

7.4.4 Daisy-Chain

The DAC7811 powers up in the daisy-chain mode which must be used when two or more devices are connected in tandem. The SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices while the SDO output of the first device connects to the SDIN input of the following device, and so forth. In this configuration 16 SCLK cycles for each DAC7811 in the chain are required. Please refer to the timing diagram of Figure 28.

For *n* devices in a daisy-chain configuration, 16*n* SCLK cycles are required to shift in the entire input data stream. After 16*n* active SCLK edges are received following a falling $\overline{\text{SYNC}}$, the data stream becomes complete, and $\overline{\text{SYNC}}$ can brought high to update *n* devices simultaneously.

When $\overline{\text{SYNC}}$ is brought high, each device will execute the function defined by the four DAC control bits C3-C0 in its input shift register. For example, C3-C0 must be **0001** for each DAC in the chain that is to be updated with new data, and C3-C0 must be **0000** for each DAC in the chain whose contents are to remain unchanged.

A continuous stream containing the exact number of SCLK cycles may be sent first while the $\overline{\text{SYNC}}$ signal is held low, and then raise $\overline{\text{SYNC}}$ at a later time. Nothing happens until the rising edge of $\overline{\text{SYNC}}$, and then each DAC7811 in the chain will execute the function defined by the four DAC control bits C3-C0 in its input shift register.

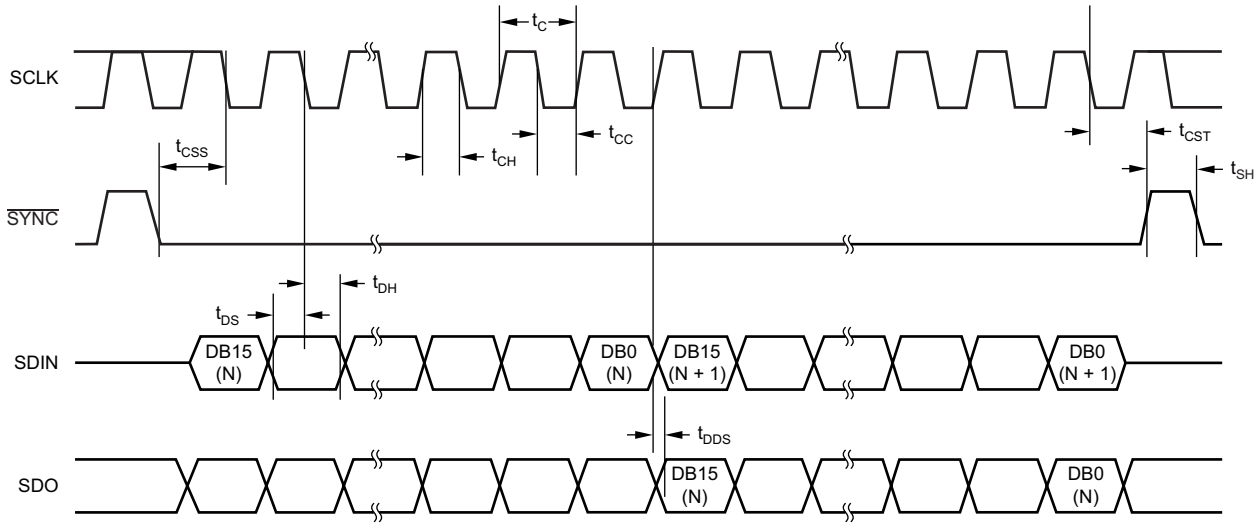


Figure 28. DAC7811 Timing Diagram

7.4.5 Control Bits C3 to C0

Control Bits C3 to C0 allow control of various functions of the DAC; see Table 2. Default settings of the DAC on powering up are as follows: Data clocked into shift register on falling clock edges; daisy-chain mode is enabled. The device powers on with zero-scale loaded into the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features as part of an initialization sequence; for example, daisy-chaining may be disabled if not in use, active clock edge may be changed to rising edge, and DAC output may be cleared to either zero or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

Table 2. Serial Input Register Data Format, Data Loaded MSB First

C3	C2	C1	C0	FUNCTION IMPLEMENTED
0	0	0	0	No operation (power-on default)
0	0	0	1	Load and update
0	0	1	0	Initiate readback
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Daisy-chain disable
1	0	1	0	Clock data to shift register on rising edge
1	0	1	1	Clear DAC output to zero
1	1	0	0	Clear DAC output to midscale
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The 2.7-V to 5.5-V supply operation makes the DAC7811 a viable candidate for battery operated applications, such as waveform generators, programmable amplifiers, and any mobile platforms that may require analog outputs and processing. Additionally, the large signal multiplying bandwidth of the DAC7811 makes it an excellent choice for programmable filters and oscillators.

8.1.1 Unipolar Operation Using DAC7811

To generate a positive voltage output, a negative reference is input to the DAC7811. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, VOUT and GND of the reference are level-shifted to a virtual ground and a –2.5-V input to the DAC7811 with an op amp.

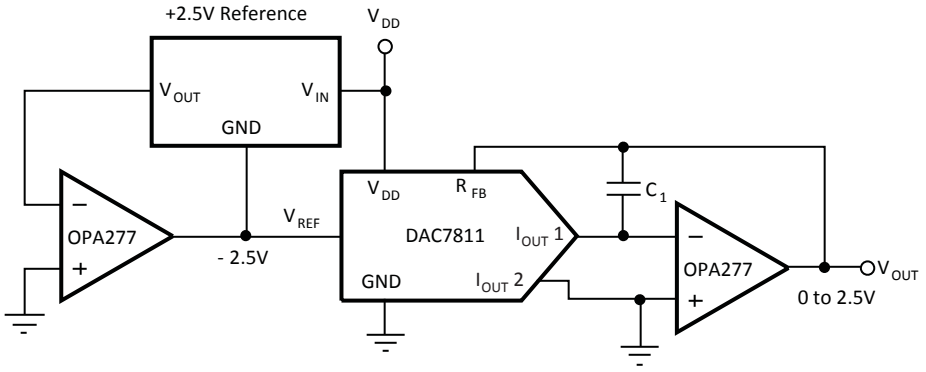


Figure 29. Positive Voltage Output Circuit

8.1.2 Bipolar Operation Using the DAC7811

The DAC7811, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output IOUT is the inverse of the input reference voltage at VREF.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 30, external op amp U3 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U3. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produces output voltages of VOUT = –2.5 V to VOUT = +2.5 V

$$V_{OUT} = \left[\left(\frac{D}{2^{11}}\right) - 1\right] \times V_{REF} \quad (2)$$

External resistance mismatching is the significant error in Figure 30.

Application Information (continued)

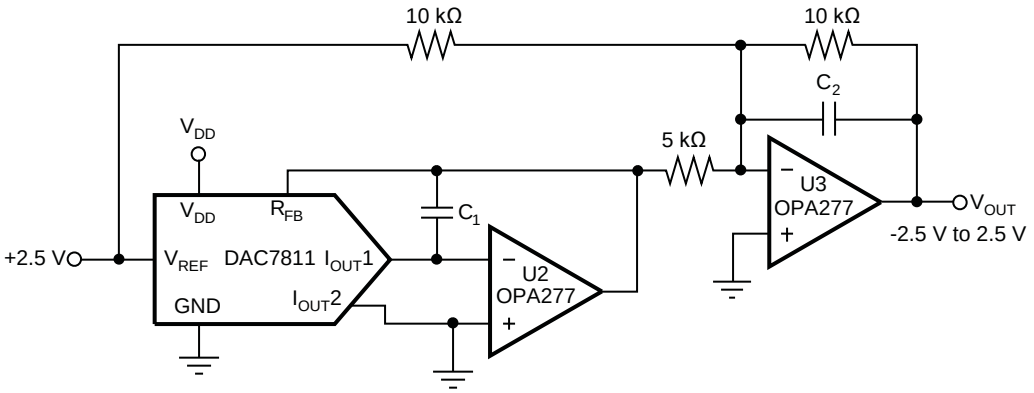


Figure 30. Bipolar Output Circuit

8.1.3 Stability Circuit

For a current-to-voltage design (see Figure 31), the DAC7811 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design practices. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in Figure 31.

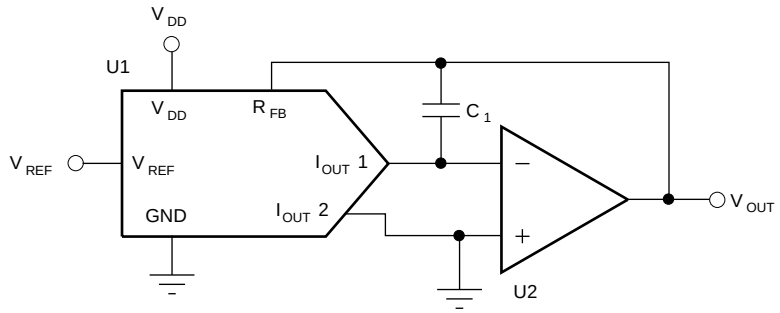


Figure 31. Gain Peaking Prevention Circuit With Compensation Capacitor

8.1.4 Amplifier Selection

There are many choices and many differences in selecting the proper operational amplifier for a multiplying DAC (MDAC). Making the analog signal out of the MDAC is one critical aspect. However, there are also other issues to take into account such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy. Table 3 and Table 4 suggest some suitable operational amplifiers for low power, fast settling, and high-speed applications. A greater selection of operational amplifiers can be found at www.ti.com/amplifier.

Application Information (continued)

Table 3. Suitable Precision Operational Amplifiers from Texas Instruments

PRODUCT	TOTAL SUPPLY VOLTAGE (V) (min)	TOTAL SUPPLY VOLTAGE (V) (max)	I_Q PER CHANNEL (max) (mA)	GBW (typ) (MHz)	SLEW RATE (typ) (V/µs)	OFFSET DRIFT (typ) (µV/°C)	I_{IB} (max) (pA)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
LOW POWER										
OPA703	4	12	0.2	1	0.6	4	10	70	SOT5-23, PDIP-8, SOIC-8	12V, CMOS, Rail-to-Rail I/O, Operational Amplifier
OPA735	2.7	12	0.75	1.6	1.5	0.01	200	115	SOT5-23, SOIC-8	0.05µV/°C (max), Single-Supply CMOS Zero-Drift Series Operational Amplifier
OPA344	2.7	5.5	0.25	1	1	2.5	10	80	SOT5-23, PDIP-8, SOIC-8	Low Power, Single-Supply, Rail-To-Rail Operational Amplifiers MicroAmplifier Series
OPA348	2.1	5.5	0.065	1	0.5	2	10	70	SC5-70, SOT5-23, SOIC-8	1MHz, 45µA, Rail-to-Rail I/O, Single Op Amp
OPA277	4	36	0.825	1	0.8	0.1	1000	130	PDIP-8, SOIC-8, SON-8	High Precision Operational Amplifiers
FAST SETTLING										
OPA350	2.7	5.5	7.5	38	22	4	10	76	MSOP-8, PDIP-8, SOIC-8	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series
OPA727	4	12	6.5	20	30	0.6	500	86	MSOP-8, SON-8	e-trim 20MHz, High Precision CMOS Operational Amplifier
OPA227	5	36	3.8	8	2.3	0.1	10000	120	PDIP-8, SOIC-8	High Precision, Low Noise Operational Amplifiers

Table 4. Suitable High Speed Operational Amplifiers from Texas Instruments (Multiple Channel Options)

PRODUCT	SUPPLY VOLTAGE (V)	GBW PRODUCT (MHz)	VOLTAGE NOISE $nV/\sqrt{Hz}$	GBW (typ) (MHz)	SLEW RATE (V/µs)	V_{OS} (typ) (µV)	V_{OS} (max) (µV)	CMRR (min) (dB)	PACKAGE/ LEAD	DESCRIPTION
SINGLE CHANNEL										
THS4281	±2.7 to ±15	38	12.5	35	500	3500	500	1000	SOT5-23, MSOP-8, SOIC-8	Very Low-Power High Speed Rail-To-Rail Input/Output Voltage Feedback Operational Amplifier
THS4031	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	CDIP-8, MSOP-8, SOIC-8	100-MHz Low Noise Voltage-Feedback Amplifier
THS4631	±4.5 to ±16.5	210	7	900	260	2000	50pA	2	SOIC-8, MSOP-8	High Speed FET-Input Operational Amplifier
OPA656	±4 to ±6	230	7	290	250	2600	2pA	5pA	SOIC-8, SOT5-23	Wideband, Unity Gain Stable FET-Input Operational Amplifier
OPA820	±2.5 to ±6	280	2.5	240	200	1200	900	23,000	SOIC-8, SOT5-23	Unity Gain Stable, Low Noise, Voltage Feedback Operational Amplifier
DUAL CHANNEL										
THS4032	±4.5 to ±16.5	200	1.6	100	500	3000	3000	8000	SOIC-8, MSOP-8	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
OPA2822	±2 to ±6.3	220	2	170	200	1200	9600	12000	SOIC-8, MSOP-8	SpeedPlus Dual Wideband, Low-Noise Operational Amplifier

8.1.5 Programmable Current Source Circuit

A DAC7811 can be integrated into the circuit in Figure 32 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times \frac{D}{4096} \quad (3)$$

The value of R3 in Equation 3 can be reduced to increase the output current drive of U3. U3 can drive ±20mA in both directions with voltage compliance limited up to 15V by the U3 voltage supply. Elimination of the circuit compensation capacitor C_1 in the circuit is not suggested as a result of the change in the output impedance Z_O, according to Equation 4:

$$Z_O = \frac{R1'R3(R1+R2)}{R1(R2'+R3') - R1'(R2+R3)} \quad (4)$$

As shown in Equation 4, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C_1 into the circuit, possible oscillation problems are eliminated. The value of C_1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

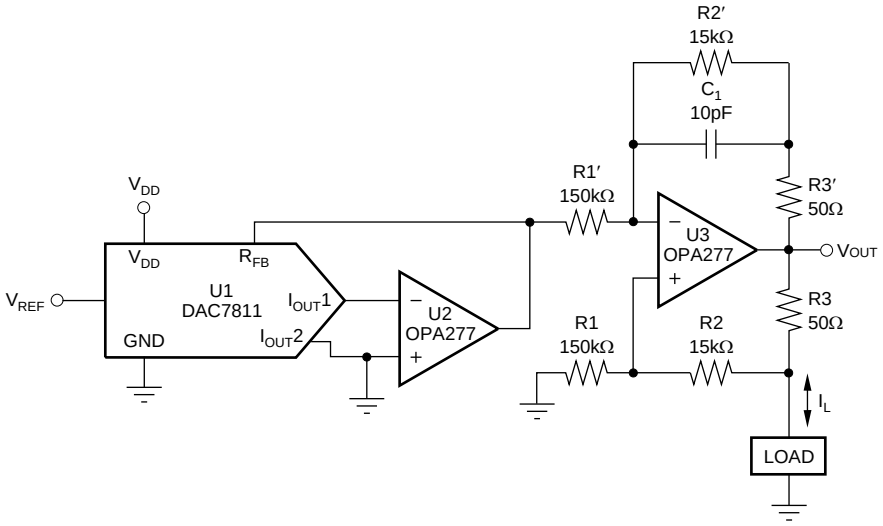


Figure 32. Programmable Bidirectional Current Source Circuit

8.2 Typical Application

8.2.1 Single Supply Unipolar Multiplying DAC

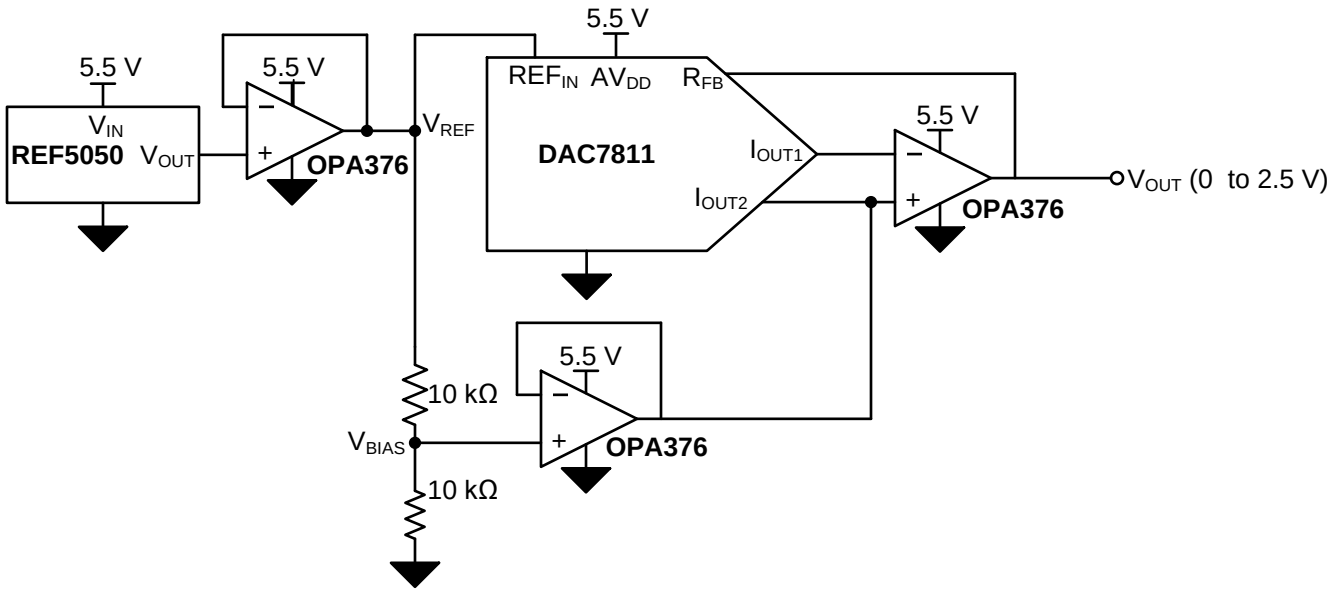


Figure 33. Complete Circuit Schematic

8.2.1.1 Design Requirements

This multiplying DAC (MDAC) circuit outputs unipolar voltages from 0 V to 2.5 V. This design does not require dual supplies to realize a unipolar, positive output voltage. This design removes the need for a negative supply rail by applying a bias voltage the output transimpedance stage.

8.2.1.2 Detailed Design Procedure

The DAC7811 output current is converted into a voltage by including an op-amp in a transimpedance configuration at the DAC7811 current output terminal. The transimpedance stage creates an output voltage with opposite polarity to that of VREF and subsequently requires dual supplies. This circuit removes the need of dual power supplies and uses a single supply to power the circuit.

The transfer function from digital code to output voltage is shown in Equation 5.

$$V_{OUT}(Code) = V_{BIAS} - \frac{\left(V_{REF} - V_{BIAS}\right)}{2^{bits}} \times Code \tag{5}$$

More information regarding this design can be found in *Single-Supply Unipolar Multiplying DAC Reference Design* (TIDU300).

8.2.1.3 Application Curve

The Absolute error (TUE) in %FSR is shown the following graph, Figure 34. The plot below represents data ranging from code 30 to 4050. The figure shows the absolute error (TUE) has a maximum value of about 0.05% FSR.

Typical Application (continued)

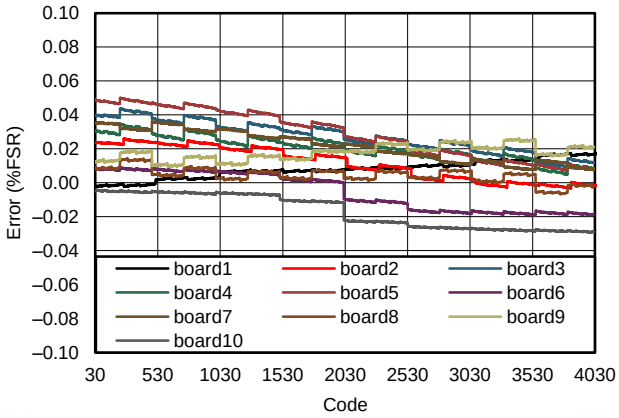


Figure 34. Absolute Error (TUE) in %FSR

9 Power Supply Recommendations

The DAC7811 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to VDD should be well regulated and low noise. Switching power supplies and DC-DC converters often have high frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, a strong recommendation is to include a 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor. The required supply current vs Logic Input voltage or temperature is displayed in *Typical Characteristics*. The power supply must meet the aforementioned current requirements.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- All Power Supply pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 to 0.22-µF ceramic with a X7R or NP0 dielectric.
- Power supplies and VREF bypass capacitors should be placed close to terminals or planes to minimize inductance and optimize performance.
- A high-quality ceramic type NP0 or X7R is recommended for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections should have proper placement with respect to the digital pins and analog pins of the DAC9881 device. The separation of analog and digital blocks will allow for better design and practice as it will ensure less coupling into neighboring blocks, and will minimize the interaction between analog and digital return currents.

10.2 Layout Example

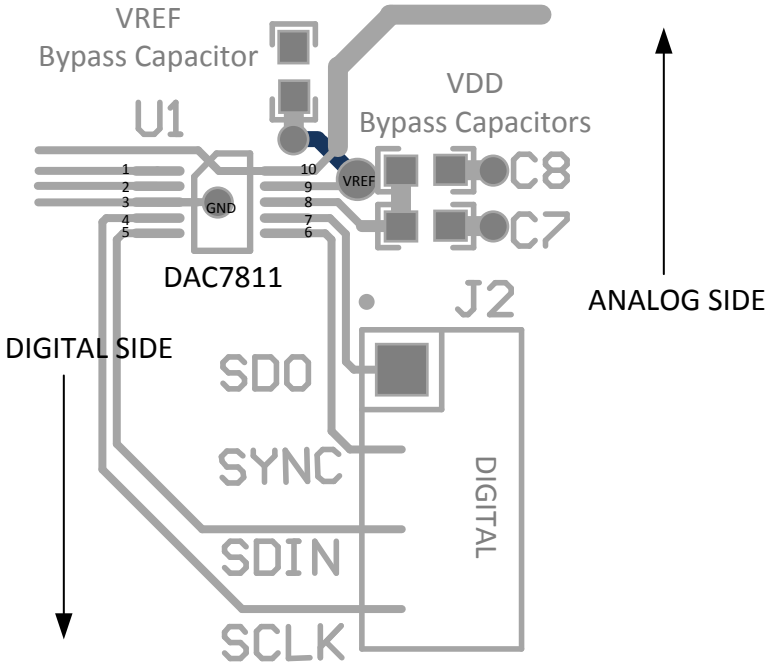


Figure 35. DAC7811 Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *TI Designs – Precision: Verified Design Voltage Mode Multiplying DAC Reference Design* (TIDUAF0)
- *TI Designs – Precision: Verified Design Single Supply Unipolar Multiplying DAC Reference Design* (TIDU300)
- *Interfacing the DAC7811 to the MSP430F449* (SLAA372)
- *DAC7811EVM* (SLAU163)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
QSPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7811IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811	Samples
DAC7811IDGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811	Samples
DAC7811IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	7811	Samples
DAC7811IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	7811	Samples
DAC7811IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	7811	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

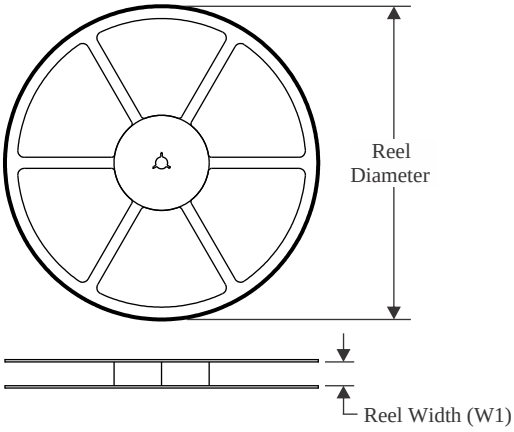
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

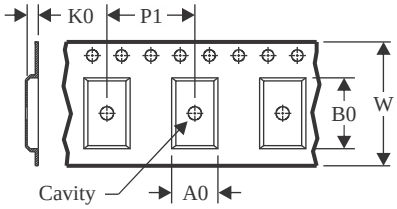
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

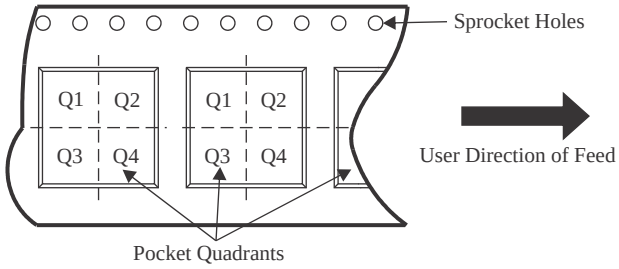


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

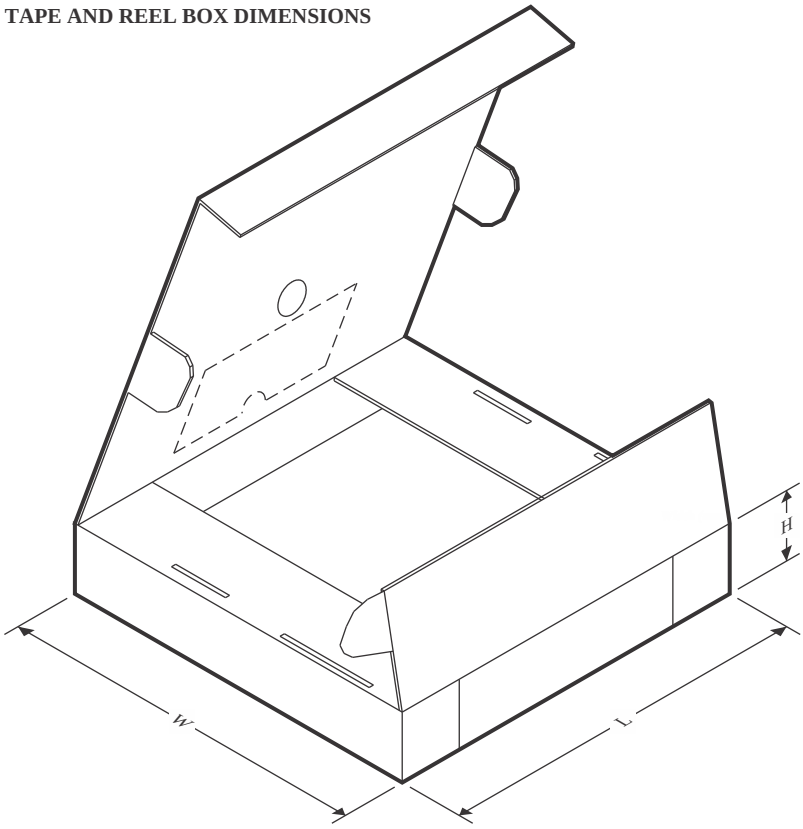
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7811IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7811IDGSRG4	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7811IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

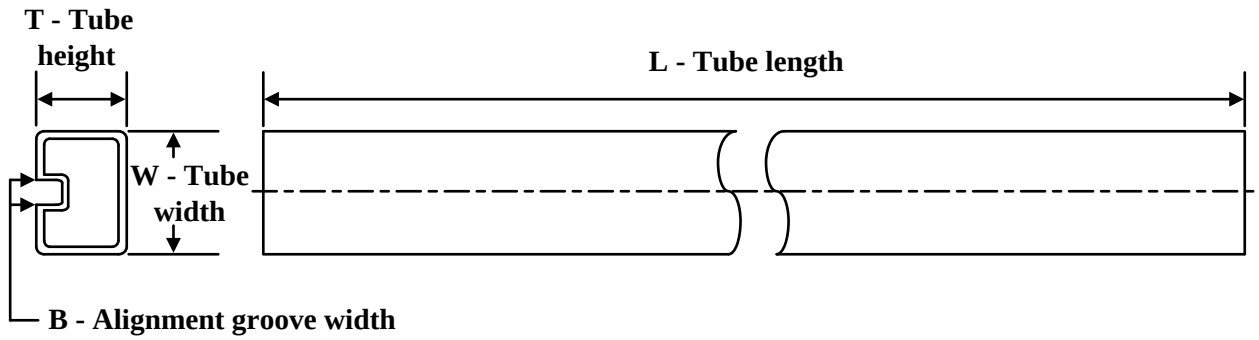
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7811IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
DAC7811IDGSRG4	VSSOP	DGS	10	2500	366.0	364.0	50.0
DAC7811IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0

TUBE



*All dimensions are nominal

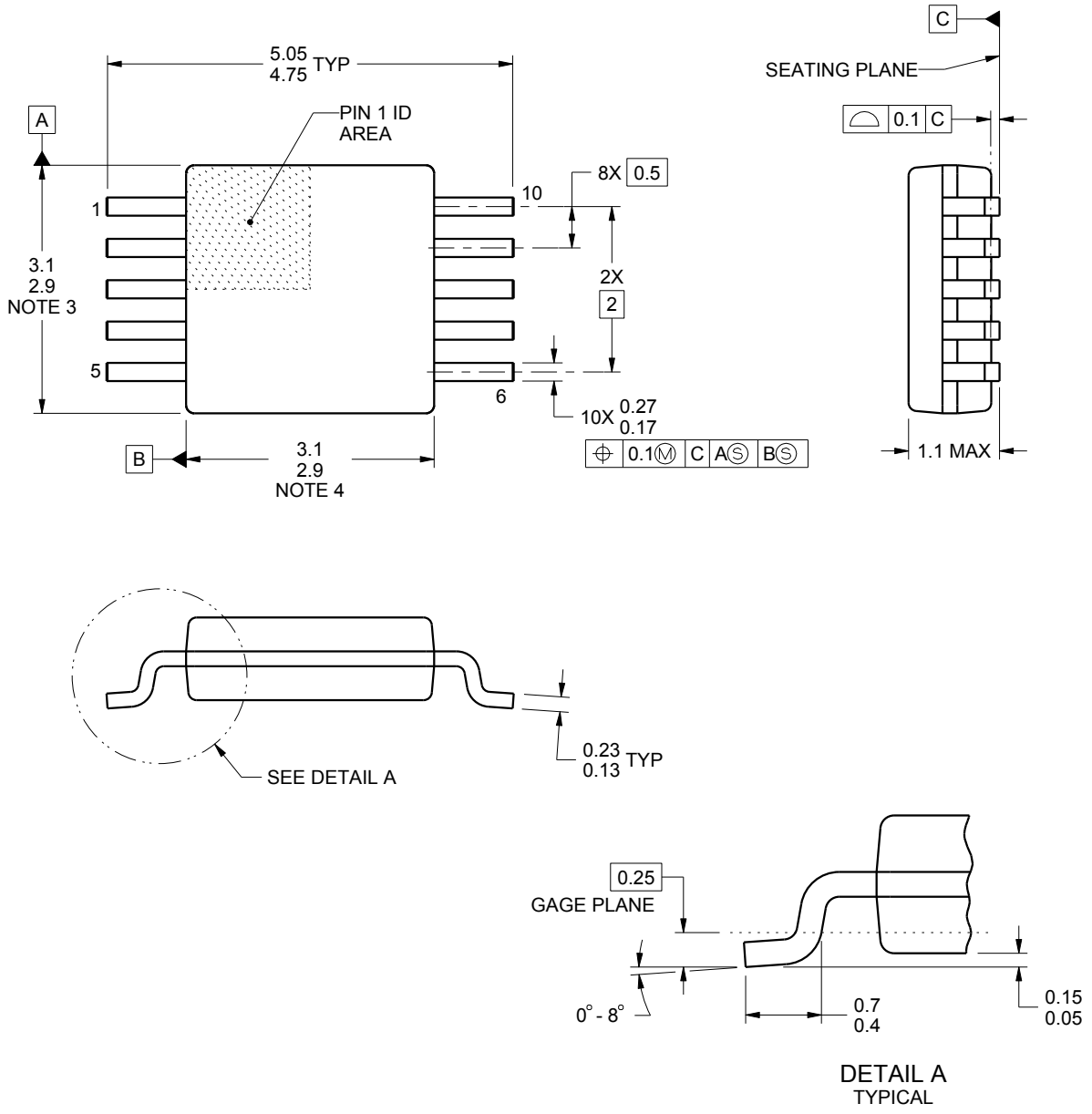
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7811IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88
DAC7811IDGSG4	DGS	VSSOP	10	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

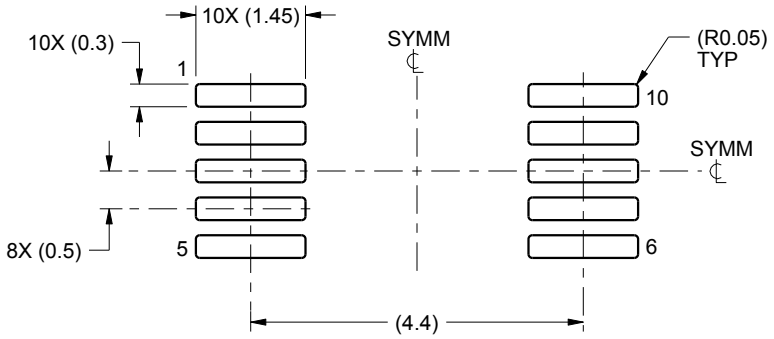
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

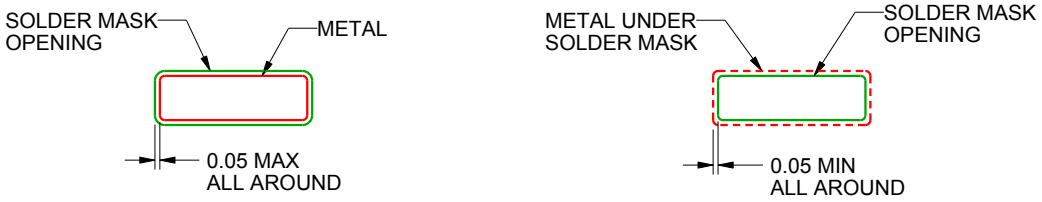


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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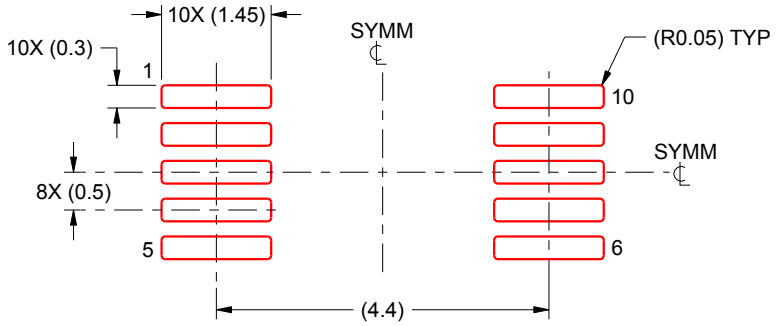
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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