CSD25310Q2 20V P-Channel NexFET™ Power MOSFETs

1 Features

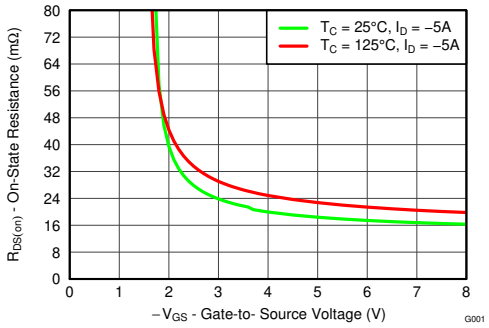
- Ultra-low Q_g and Q_{gd}
- Low on resistance
- Low thermal resistance
- Pb-free
- RoHS compliant
- Halogen free
- SON 2mm × 2mm plastic package

2 Applications

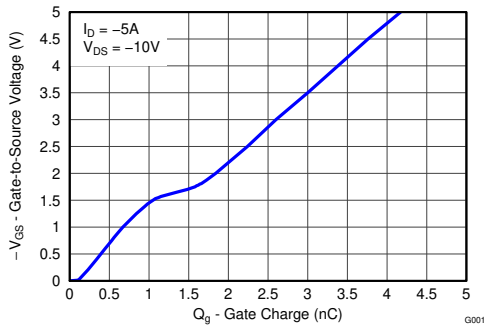
- Battery management
- Load management
- Battery protection

3 Description

This 19.9mΩ, –20V P-Channel device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Its low on resistance coupled with an extremely small footprint in a SON 2mm × 2mm plastic package make the device ideal for battery operated space constrained operations.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Product Summary

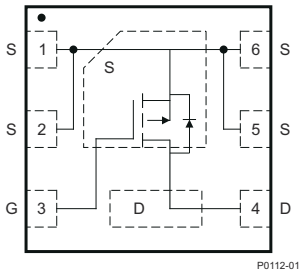
T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5V)	3.6		nC
Q_{gd}	Gate Charge Gate to Drain	0.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8V	59.0	mΩ
		V_{GS} = –2.5V	27.0	mΩ
		V_{GS} = –4.5V	19.9	mΩ
$V_{GS(th)}$	Threshold Voltage	-0.85		V

Ordering Information

Device	Media	Qty	Package	Ship
CSD25310Q2	7-Inch Reel	3000	SON 2mm x 2mm Plastic Package	Tape and Reel
CSD25310Q2T	7-Inch Reel	250		

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current (Package Limit)	–20	A
	Continuous Drain Current(1)	–9.6	A
I_{DM}	Pulsed Drain Current(2)	48	A
P_D	Power Dissipation 1. $R_{\theta JA}$ = 43°C/W on 1 in² Cu (2 oz.) on .060-inch thick FR4 PCB.	2.9	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C



Top View

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

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4 Specifications

4.1 Electrical Characteristics

T_A = 25°C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0V, I_D = –250µA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0V, V_{DS} = –16V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = –8V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = –250µA	–0.55	–0.85	–1.10	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8V, I_{DS} = –5A		59.0	89.0	mΩ
		V_{GS} = –2.5V, I_{DS} = –5A		27.0	32.5	mΩ
		V_{GS} = –4.5V, I_{DS} = –5A		19.9	23.9	mΩ
g_{fs}	Transconductance	V_{DS} = –16V, I_{DS} = –5A		34		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 1MHz		504	655	pF
C_{OSS}	Output Capacitance			281	365	pF
C_{RSS}	Reverse Transfer Capacitance			16.7	21.7	pF
R_g	Series Gate Resistance			1.9		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –10V, I_{DS} = –5A		3.6	4.7	nC
Q_{gd}	Gate Charge Gate to Drain			0.5		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	V_{DS} = –10V, V_{GS} = 0V		5.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10V, V_{GS} = –4.5V, I_{DS} = –5A R_G = 2Ω		8		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			15		ns
t_f	Fall Time			5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = –5A, V_{GS} = 0V		–0.8	–1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = –10V, I_F = –5A, di/dt = 200A/µs		9.2		nC
t_{rr}	Reverse Recovery Time			13		ns

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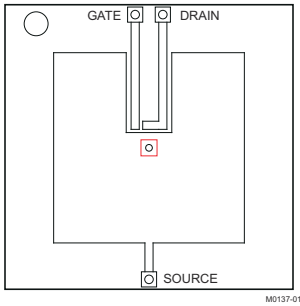
4.2 Thermal Information

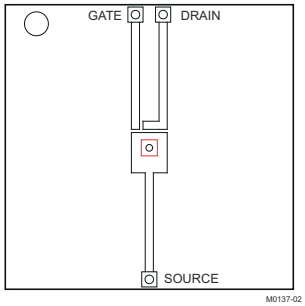
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			4.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			55	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81cm × 3.81cm), 0.06 inch (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 55 when mounted on 1 inch^2 (6.45cm^2) of 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 215 when mounted on minimum pad area of 2oz. (0.071mm thick) Cu.

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4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

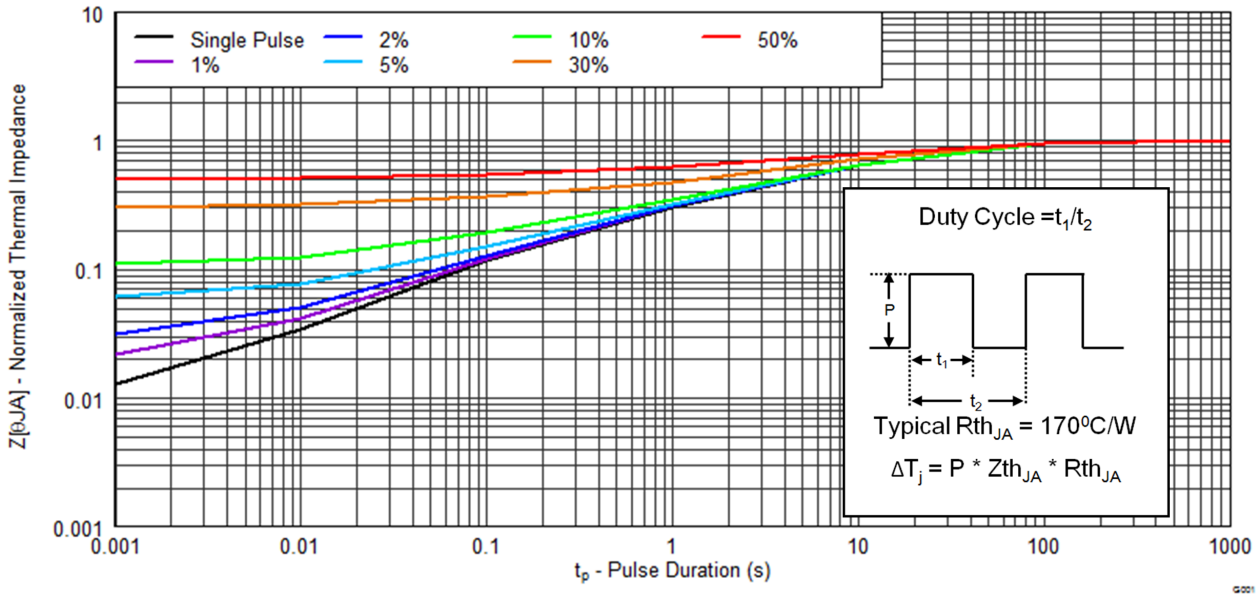

Figure 4-1. Transient Thermal Impedance

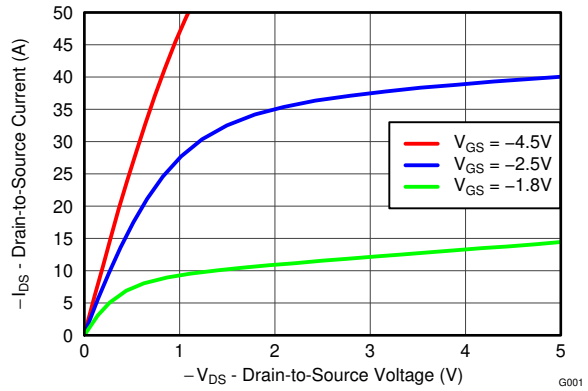

Figure 4-2. Saturation Characteristics

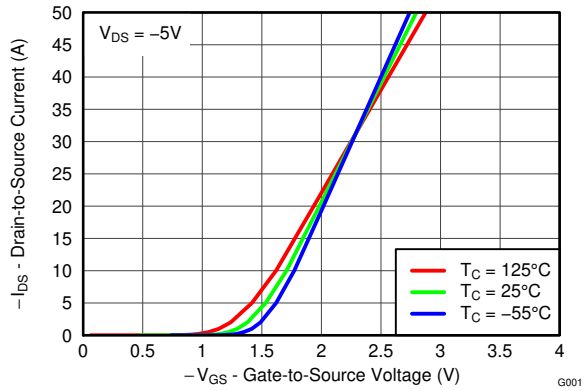

Figure 4-3. Transfer Characteristics

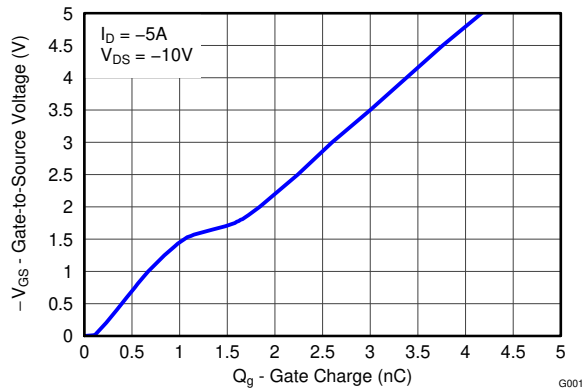

Figure 4-4. Gate Charge

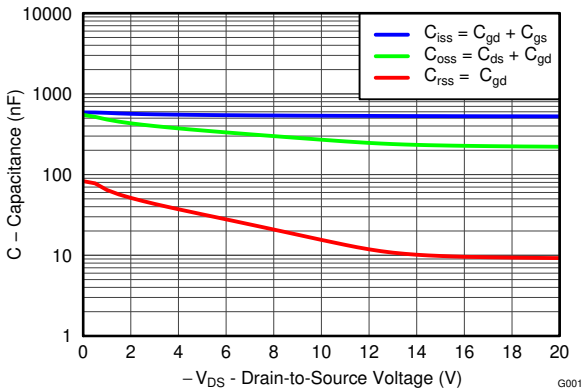

Figure 4-5. Capacitance

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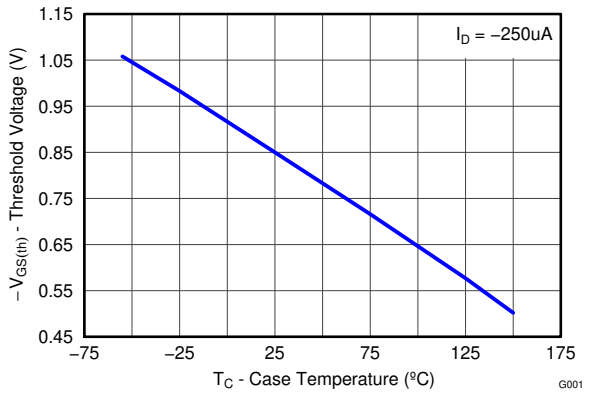

Figure 4-6. Threshold Voltage vs Temperature

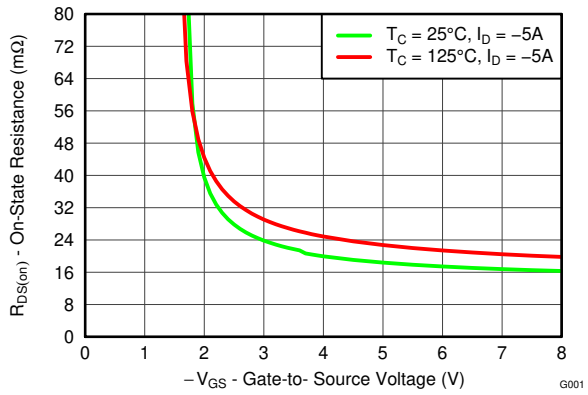

Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

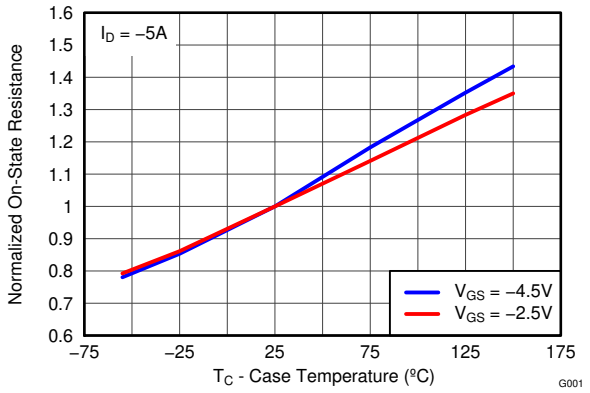

Figure 4-8. Normalized On-State Resistance vs Temperature

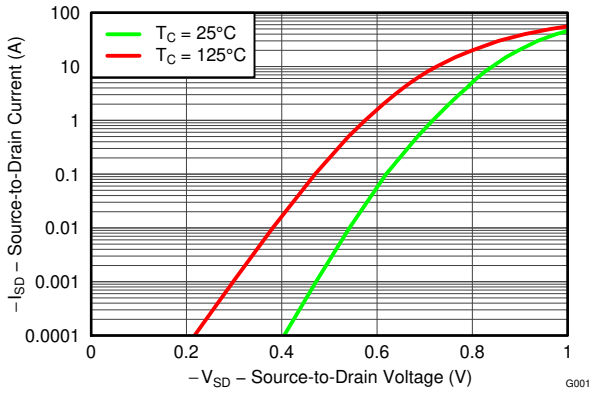

Figure 4-9. Typical Diode Forward Voltage

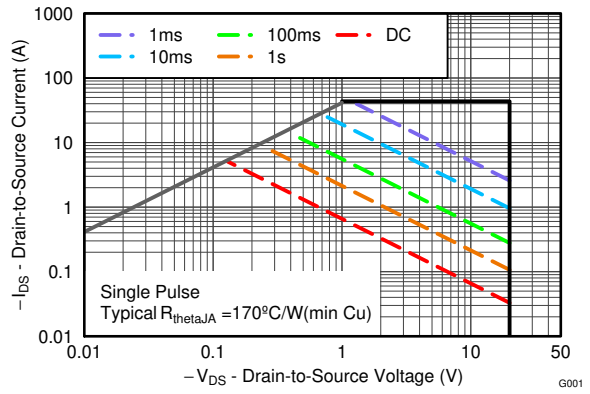

Figure 4-10. Maximum Safe Operating Area

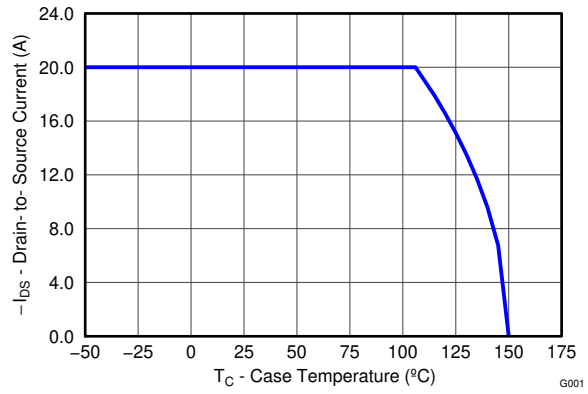

Figure 4-11. Maximum Drain Current vs Temperature

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5 Device and Documentation Support

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 Receiving Notification of Documentation Updates

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5.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision B (March 2022) to Revision C (February 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision A (June 2014) to Revision B (March 2022)	Page
• Updated drain and source connection images	4

Changes from Revision * (January 2014) to Revision A (June 2014)	Page
• Revised "Pb-Free Terminal Plating" to Only State "Pb-Free"	1
• Added small reel option to the Ordering Information Table	1

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25310Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530	Samples
CSD25310Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2530	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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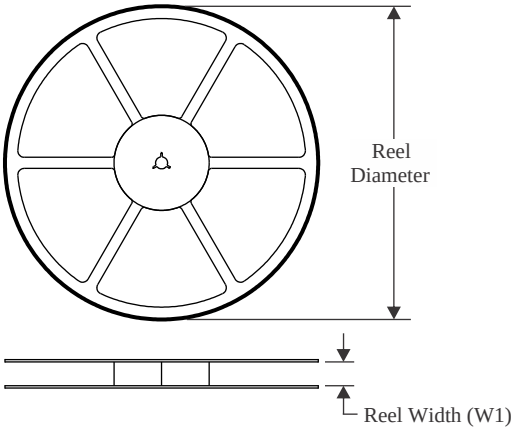
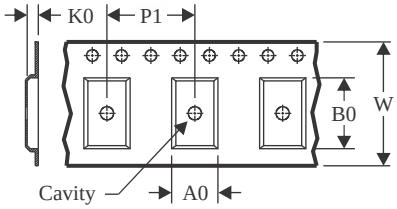
TAPE AND REEL INFORMATION

REEL DIMENSIONS

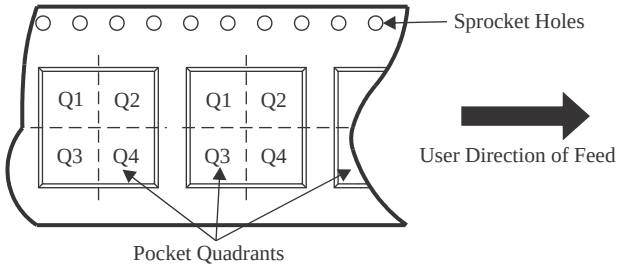


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

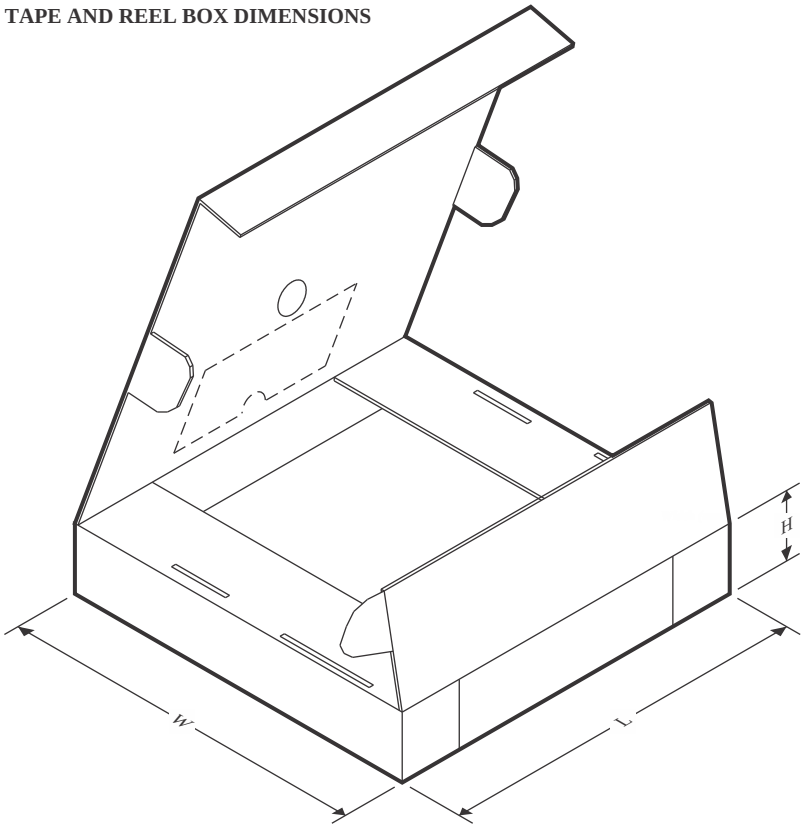
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25310Q2	WSON	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD25310Q2T	WSON	DQK	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25310Q2	WSON	DQK	6	3000	189.0	185.0	36.0
CSD25310Q2T	WSON	DQK	6	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

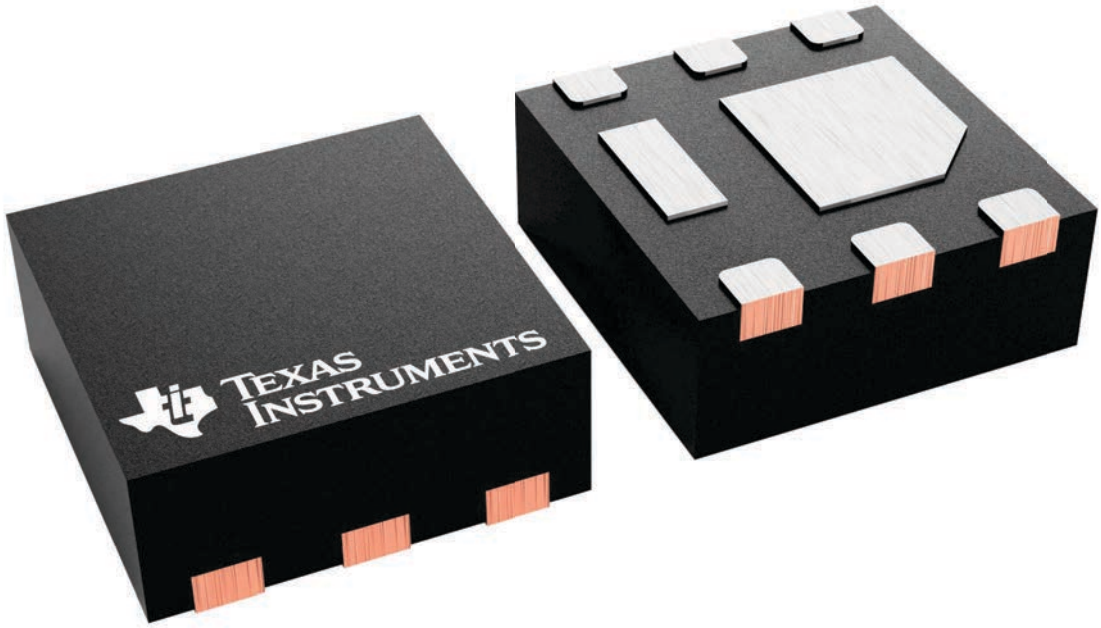
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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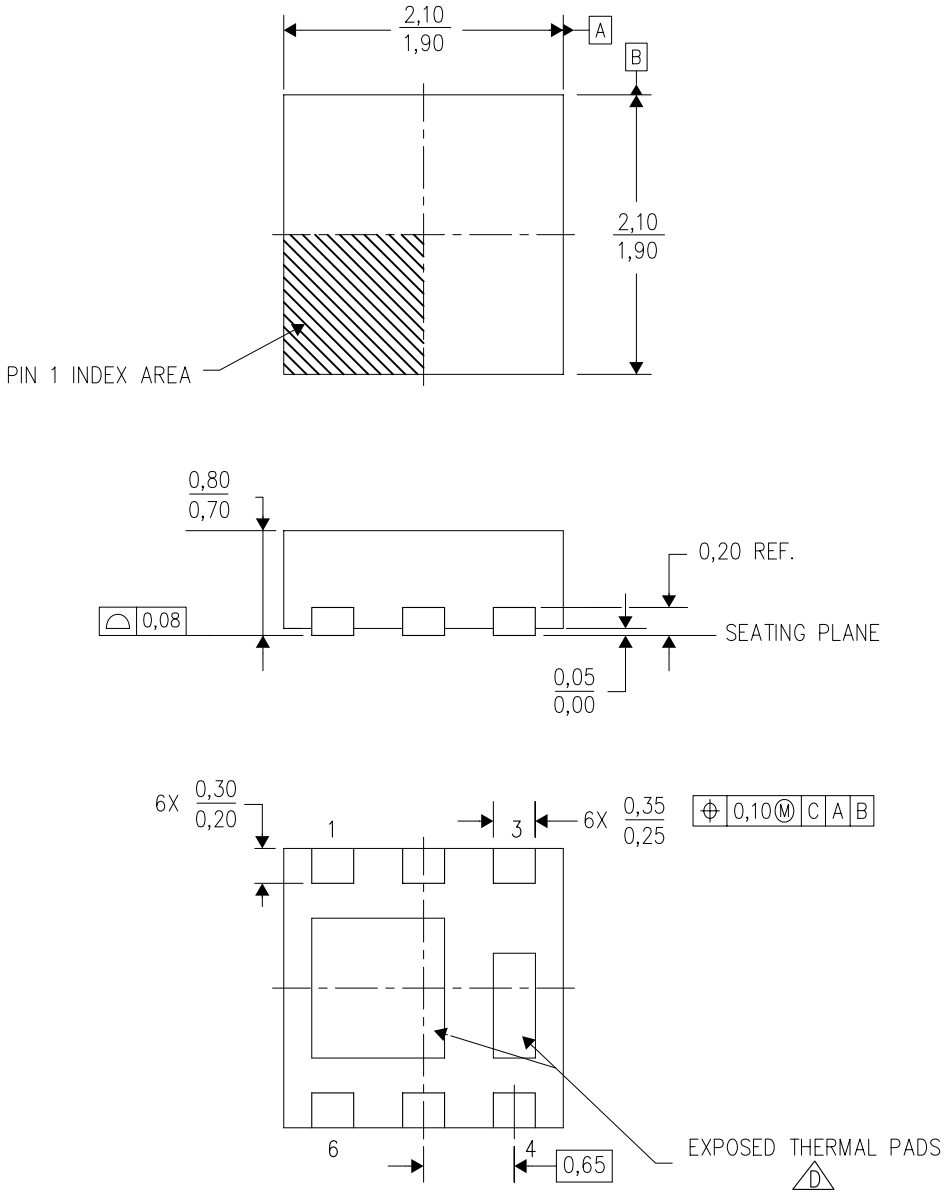
DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210192/B 01/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL PAD MECHANICAL DATA

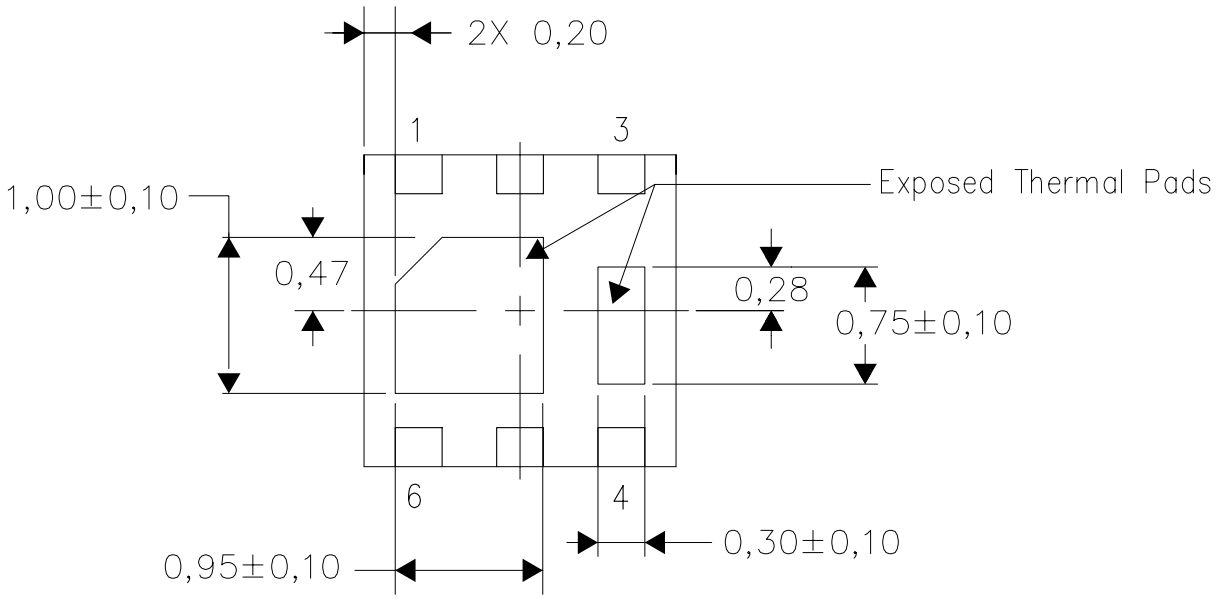
DQK (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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