

# CSD22206W –8-V P-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-Low Resistance
- Small Footprint 1.5 mm × 1.5 mm
- Lead Free
- Gate ESD Protection
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

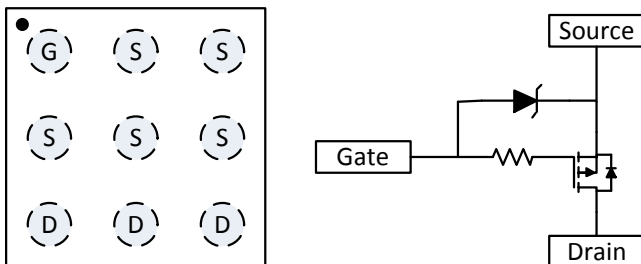
## 2 Applications

- Load Switch Applications
- Battery Management
- Battery Protection

## 3 Description

This –8-V, 4.7-mΩ, 1.5-mm × 1.5-mm device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View and Circuit Configuration



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	–8		V
$Q_g$	Gate Charge Total (–4.5 V)	11.2		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	1.8		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -2.5\text{ V}$	6.8	mΩ
		$V_{GS} = -4.5\text{ V}$	4.7	
$V_{GS(th)}$	Threshold Voltage	–0.7		V

## Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD22206W	3000	7-Inch Reel	1.50-mm × 1.50-mm Wafer BGA Package	Tape and Reel
CSD22206WT	250			

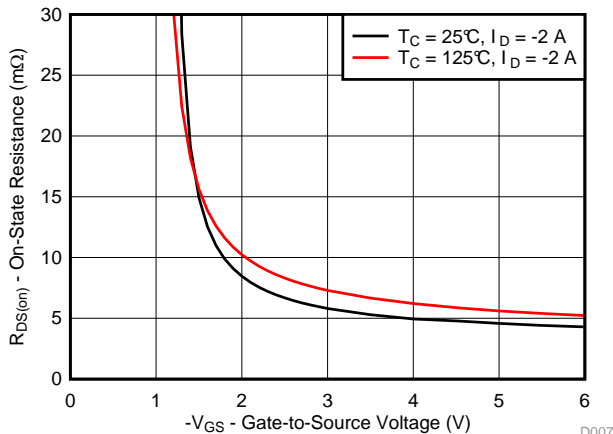
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–8	V
$V_{GS}$	Gate-to-Source Voltage	–6	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	–5	A
	Pulsed Drain Current <sup>(2)</sup>	–108	A
$P_D$	Power Dissipation	1.7	W
$T_J$ , $T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

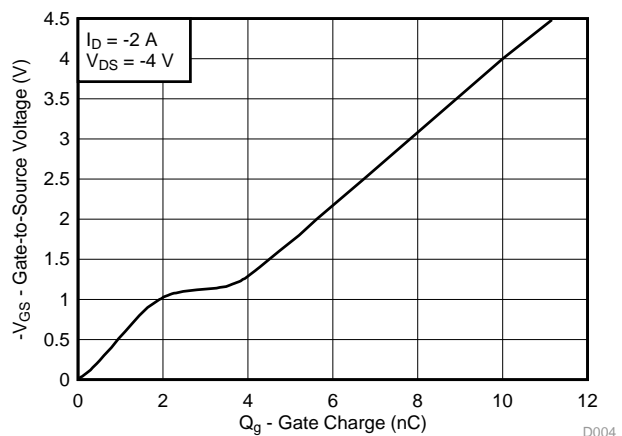
(1) Device operating at a temperature of 105°C.

(2) Typ  $R_{\theta JA} = 75^\circ\text{C/W}$ , mounted on FR4 material with maximum Cu mounting area, pulse width  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

DATE	REVISION	NOTES
May 2017	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = -250\ \mu\text{A}$	-8			V
$BV_{GSS}$	Gate-to-source voltage	$V_{DS} = 0\text{ V}, I_G = -250\ \mu\text{A}$	-6			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = -6.4\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = -6\text{ V}$			-100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	-0.4	-0.7	-1.05	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = -2.5\text{ V}, I_{DS} = -2\text{ A}$		6.8	9.1	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_{DS} = -2\text{ A}$		4.7	5.7	
$g_{fs}$	Transconductance	$V_{DS} = -0.8\text{ V}, I_{DS} = -2\text{ A}$		20		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -4\text{ V},$ $f = 1\text{ MHz}$		1750	2275	pF
$C_{OSS}$	Output capacitance			960	1250	pF
$C_{RSS}$	Reverse transfer capacitance			340	440	pF
$R_G$	Series gate resistance			30		$\Omega$
$Q_g$	Gate charge total (-4.5 V)	$V_{DS} = -4\text{ V},$ $I_D = -2\text{ A}$		11.2	14.6	nC
$Q_{gd}$	Gate charge gate-to-drain			1.8		nC
$Q_{gs}$	Gate charge gate-to-source			2.1		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			1.3		nC
$Q_{OSS}$	Output charge		$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}$		7.2	
$t_{d(on)}$	Turnon delay time	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V},$ $I_{DS} = -2\text{ A}, R_G = 0\ \Omega$		37		ns
$t_r$	Rise time			17		ns
$t_{d(off)}$	Turnoff delay time			118		ns
$t_f$	Fall time			45		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{DS} = -2\text{ A}, V_{GS} = 0\text{ V}$	-0.69	-1.0		
$Q_{rr}$	Reverse recovery charge	$V_{DS} = -4\text{ V}, I_F = -1\text{ A},$ $di/dt = 200\text{ A}/\mu\text{s}$		24		nC
$t_{rr}$	Reverse recovery time			59		ns

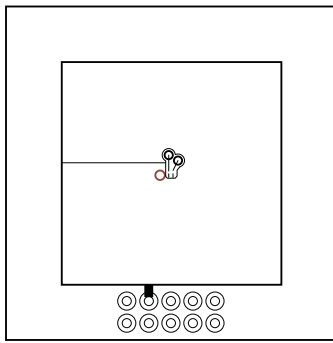
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	75	$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>	230	

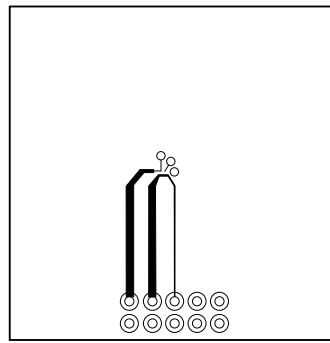
(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



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Typ  $R_{\theta JA} = 75^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
of 2-oz Cu.

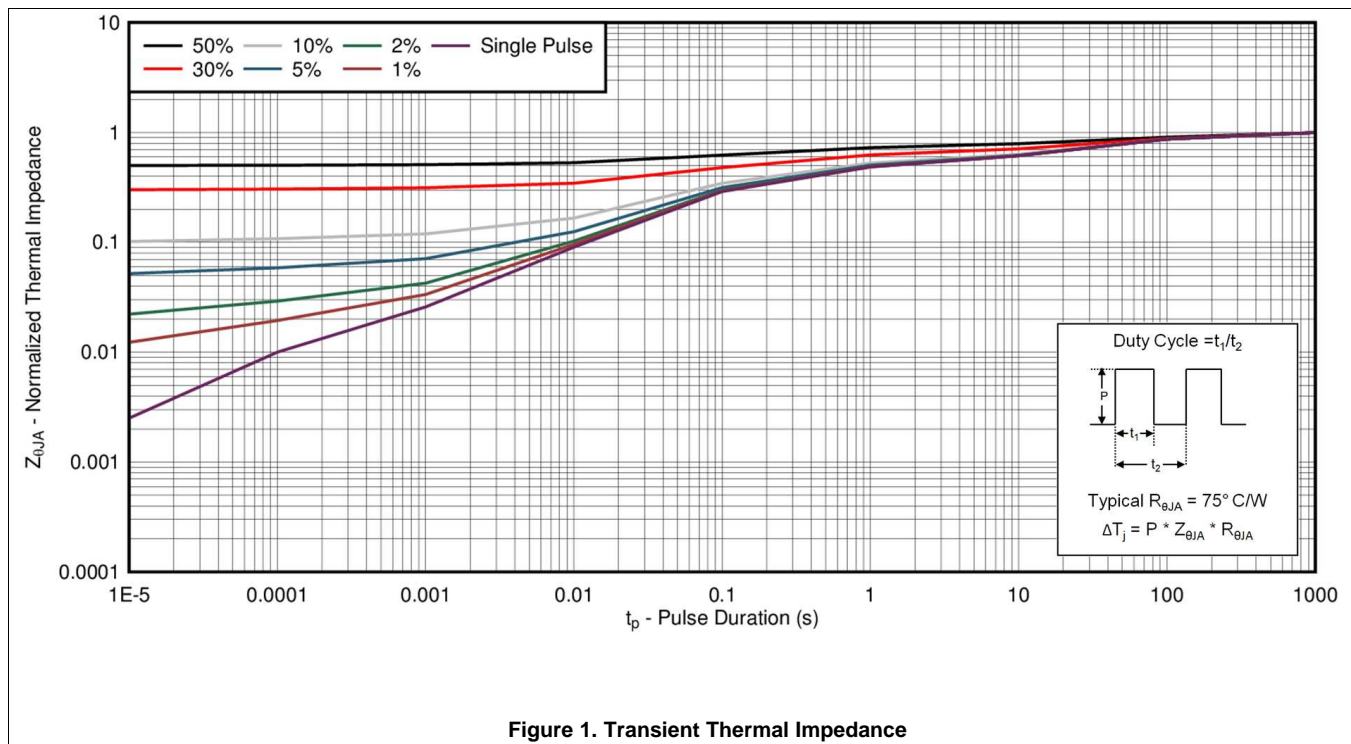


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Typ  $R_{\theta JA} = 230^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)

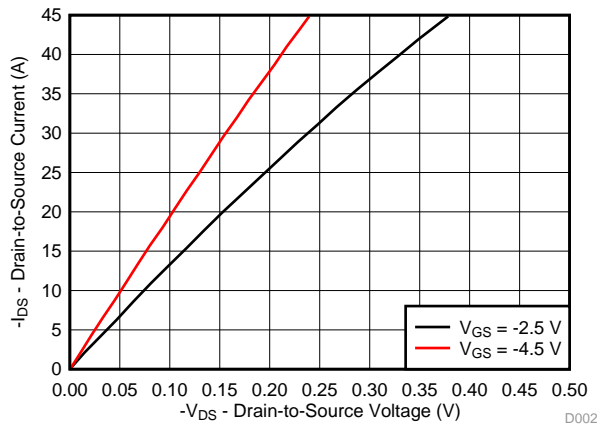


Figure 2. Saturation Characteristics

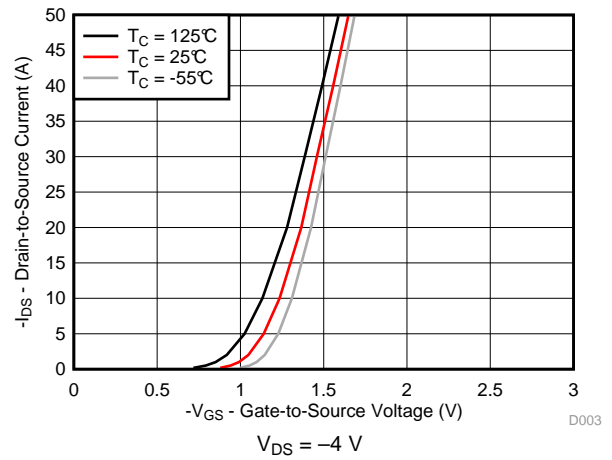


Figure 3. Transfer Characteristics

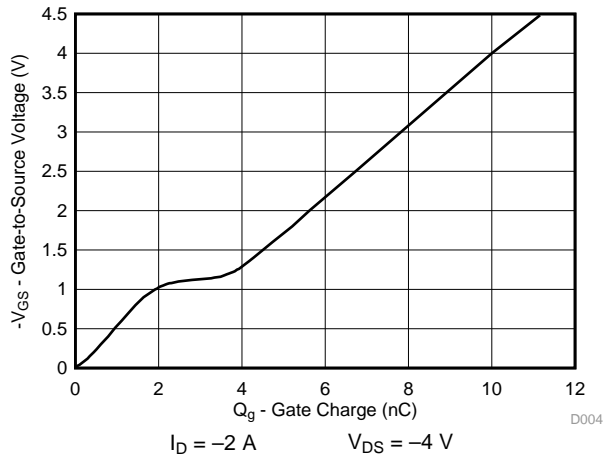


Figure 4. Gate Charge

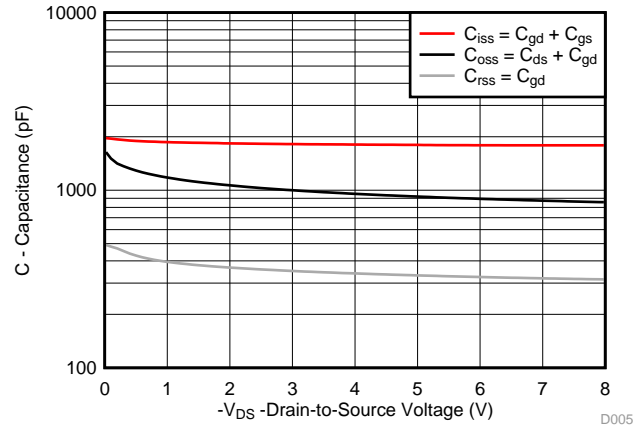


Figure 5. Capacitance

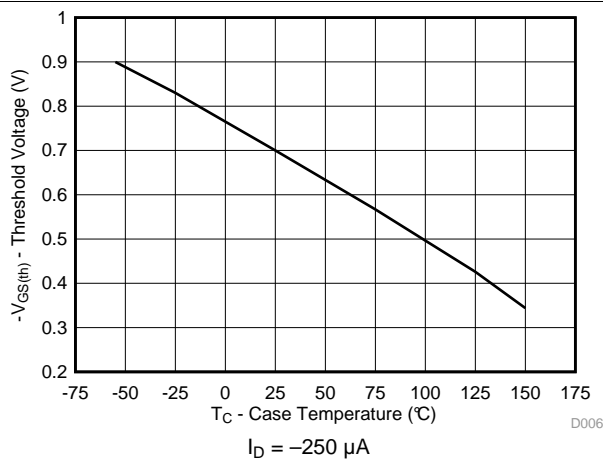


Figure 6. Threshold Voltage vs Temperature

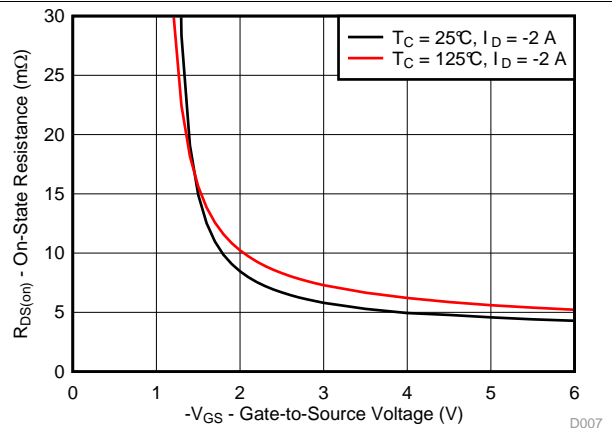
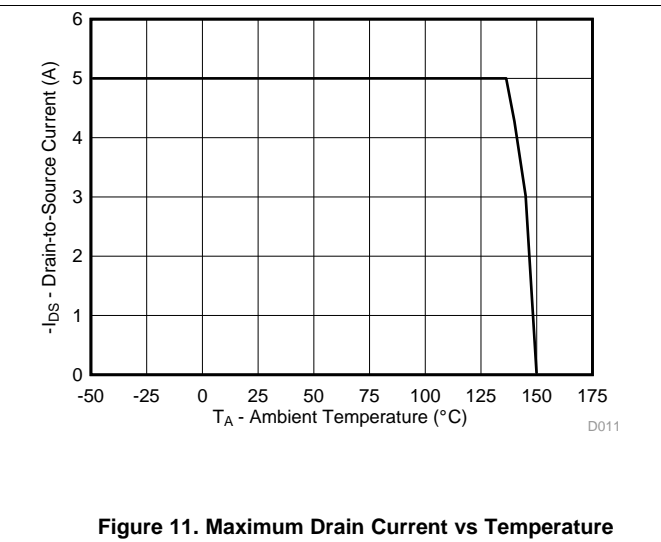
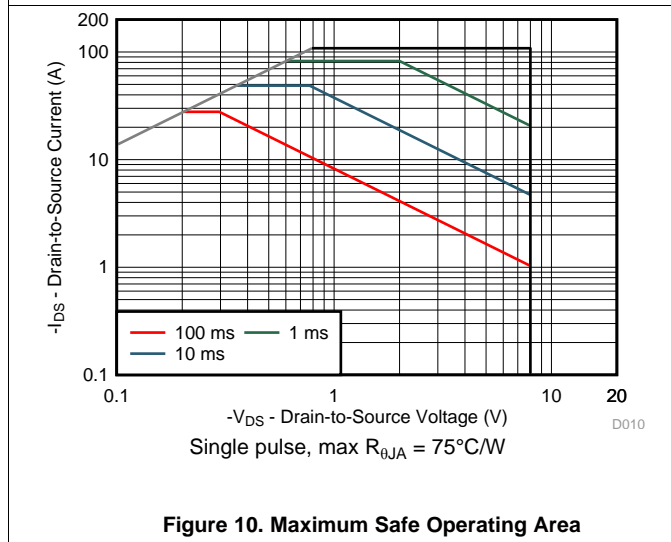
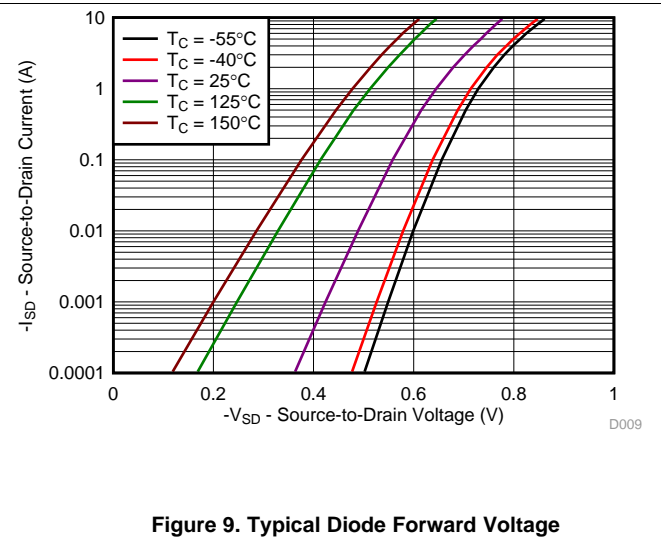
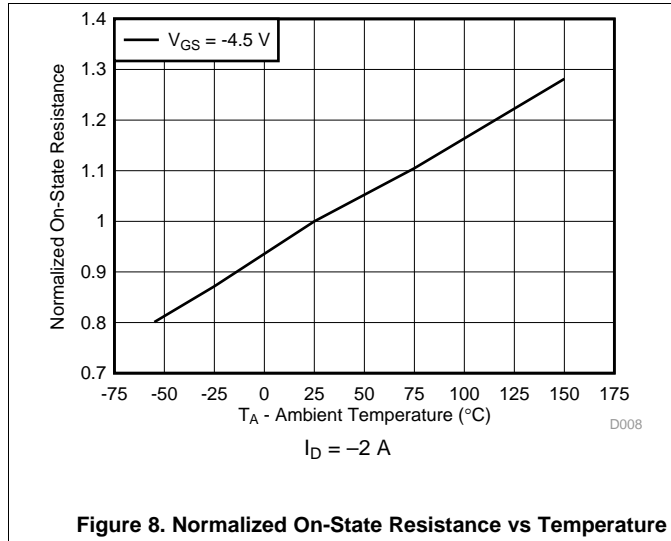


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

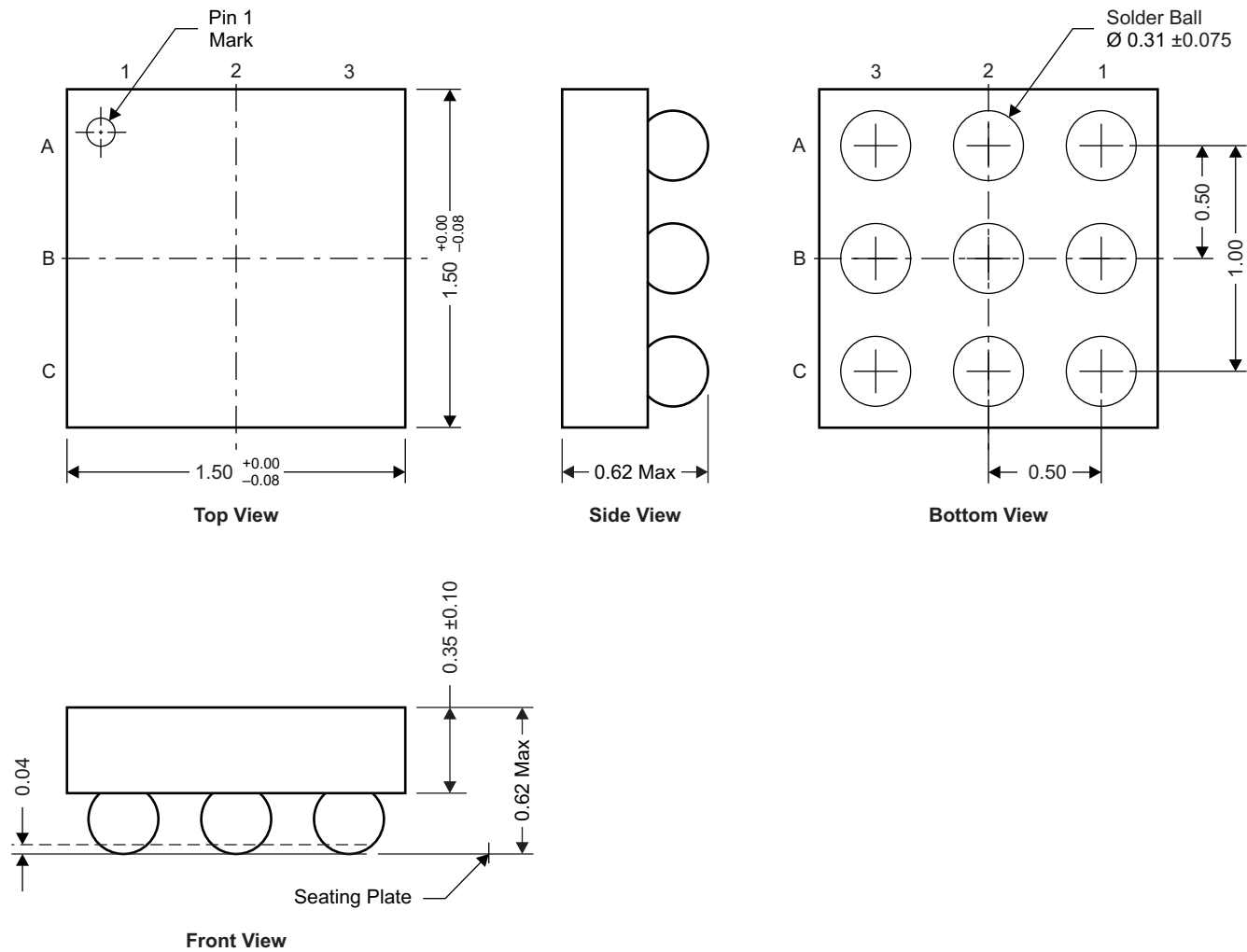
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 CSD22206W Package Dimensions



NOTE: All dimensions are in mm (unless otherwise specified).

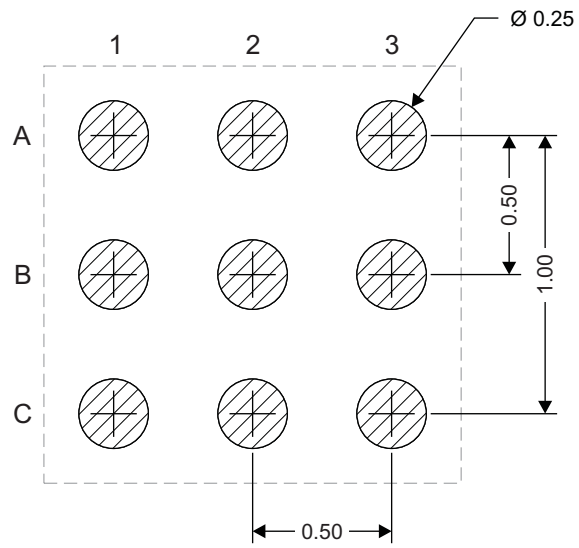
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Table 1. Pinout

POSITION	DESIGNATION
A1	Gate
A2, A3, B1, B2, B3	Source
C1, C2, C3	Drain



## 7.2 Recommended Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22206W	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206	<a href="#">Samples</a>
CSD22206WT	ACTIVE	DSBGA	YZF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22206W	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
CSD22206WT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22206W	DSBGA	YZF	9	3000	182.0	182.0	20.0
CSD22206WT	DSBGA	YZF	9	250	182.0	182.0	20.0

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