CSD18504Q5A 40V N-Channel NexFET™ Power MOSFET

1 Features

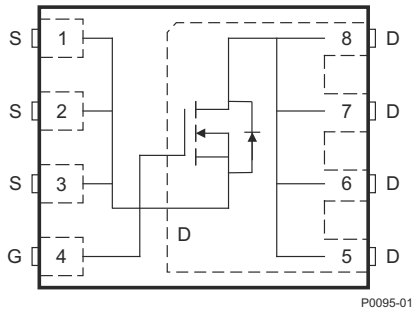
- Optimized for 5V gate drive
- Resistance rated at V_{GS} = 2.5V
- Ultra low Qg and Qgd
- Low thermal resistance
- Avalanche rated
- Pb free terminal plating
- RoHS compliant
- Halogen free
- SON 5mm x 6mm plastic package

2 Applications

- Point-of-load synchronous buck converter for applications in networking, telecom and computing systems
- Optimized for control or synchronous FET applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.



Top View

Product Summary

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	6.8		nC
Q_{gd}	Gate Charge Gate to Drain	1.2		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 2.5V	6.1	mΩ
		V_{GS} = 4.5V	4.3	mΩ
		V_{GS} = 8V	3.8	mΩ
V_{th}	Threshold Voltage	0.85		V

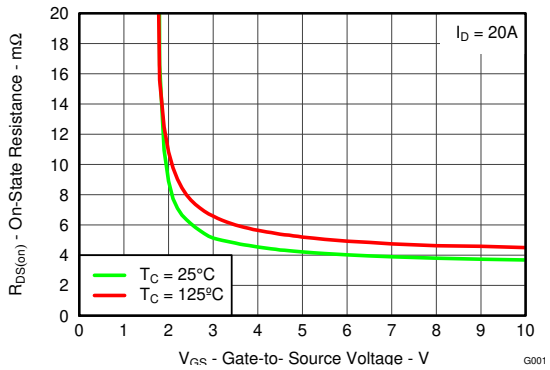
Ordering Information

Device	Package	Media	Qty	Ship
CSD16342Q5A	SON 5 × 6 Plastic Package	13-inch reel	2500	Tape and Reel

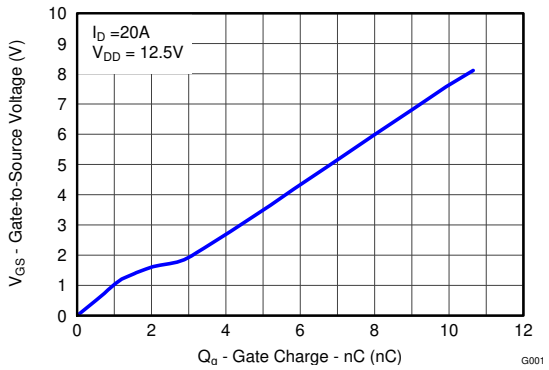
Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current(1)	21	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	131	A
P_D	Power Dissipation(1)	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 40A, L = 0.1mH, R_G = 25Ω	80	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
(2) Pulse width ≤300µs, duty cycle ≤2%



$R_{DS(ON)}$ vs V_{GS}



Gate Charge

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

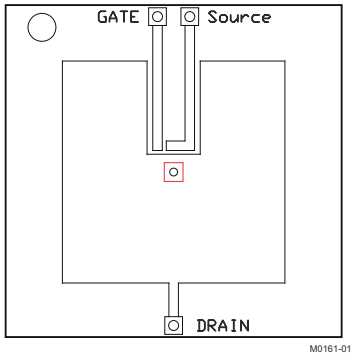
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/-8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	0.6	0.85	1.1	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 2.5V, I_{DS} = 20A		6.1	7.8	mΩ
		V_{GS} = 4.5V, I_{DS} = 20A		4.3	5.5	mΩ
		V_{GS} = 8V, I_{DS} = 20A		3.8	4.7	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 20A		91		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		1050	1350	pF
C_{OSS}	Output Capacitance			730	950	pF
C_{RSS}	Reverse Transfer Capacitance			53	69	pF
R_g	Series Gate Resistance			1.5	3	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 20A		6.8	7.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.9		nC
Q_{gs}	Gate Charge Gate to Source			1.9		nC
Qg(th)	Gate Charge at Vth			1.2		nC
Q_{OSS}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		13.7		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 20A , R_G = 2Ω		5.2		ns
t_r	Rise Time			16.6		ns
$t_{d(off)}$	Turn Off Delay Time			13.4		ns
t_f	Fall Time			3.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 20A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13V, I_F = 20A, di/dt = 300A/µs		14.5		nC
t_{rr}	Reverse Recovery Time			20		ns

4.2 Thermal Characteristics

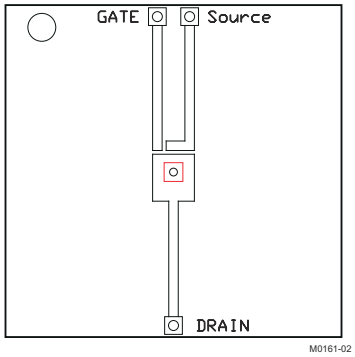
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.2	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81cm × 3.81cm), 0.06-inch (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 of 2oz. Cu.



Max $R_{\theta JA}$ = 123°C/W when mounted on minimum pad area of 2oz. Cu.

5 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

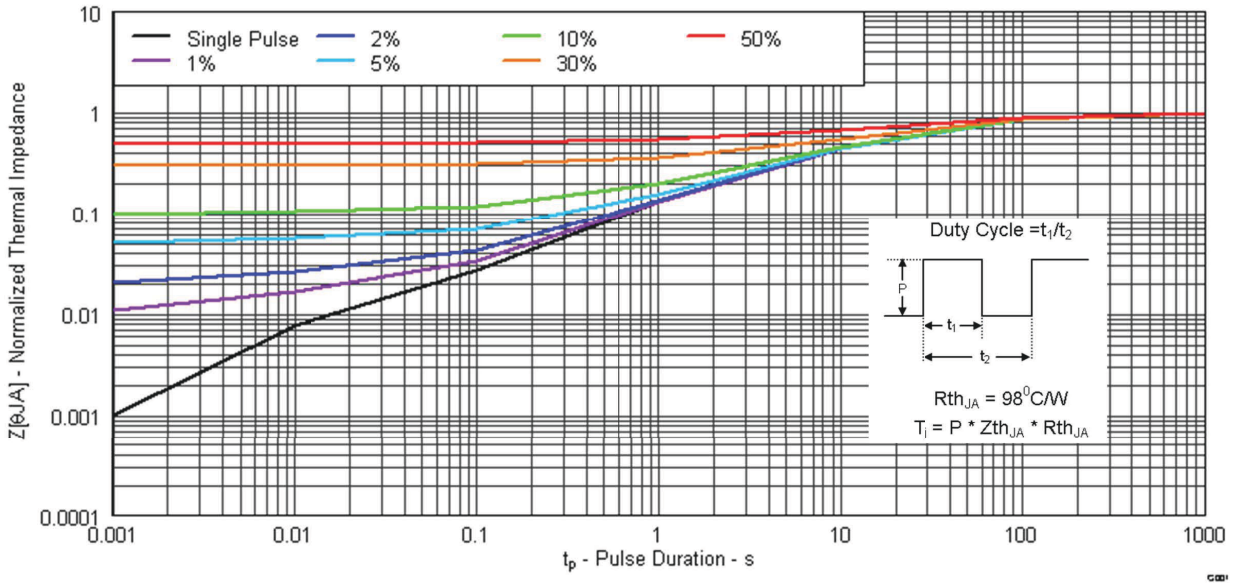


Figure 5-1. Transient Thermal Impedance

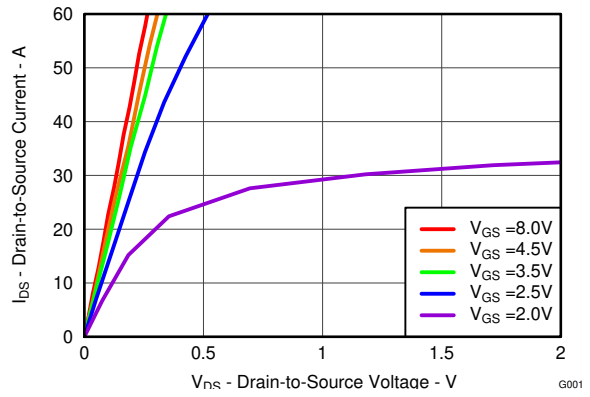


Figure 5-2. Saturation Characteristics

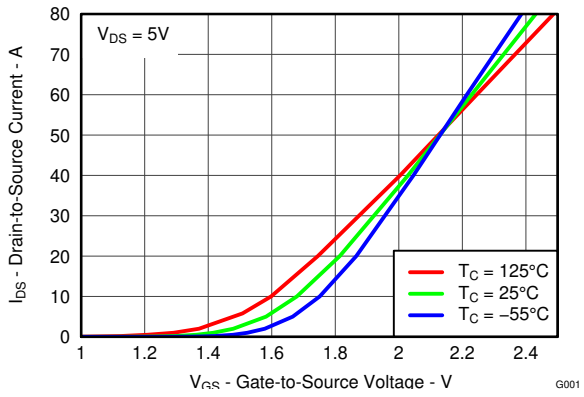


Figure 5-3. Transfer Characteristics

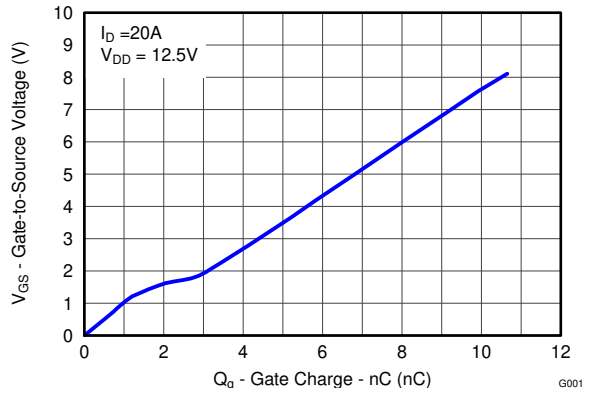


Figure 5-4. Gate Charge

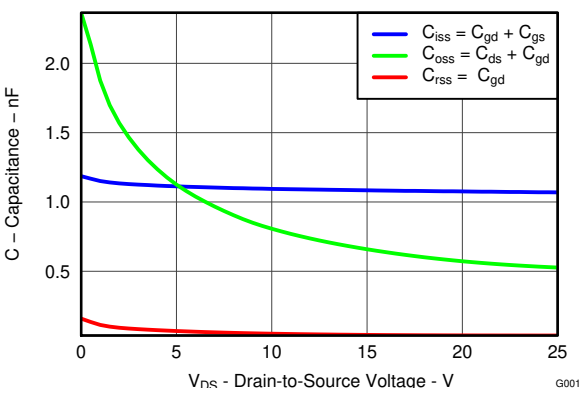


Figure 5-5. Capacitance

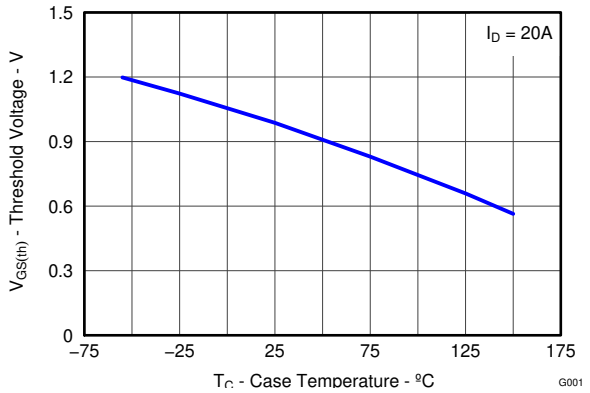


Figure 5-6. Threshold Voltage vs. Temperature

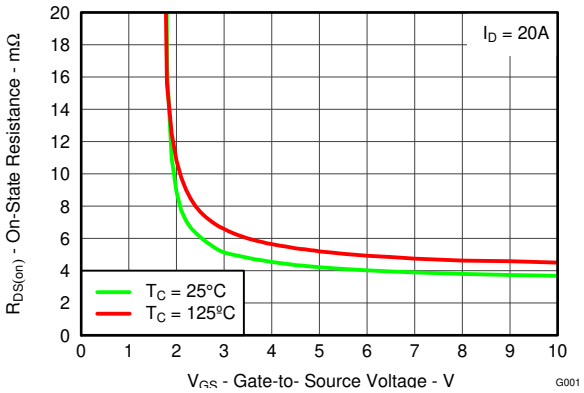


Figure 5-7. On Resistance vs. Gate Voltage

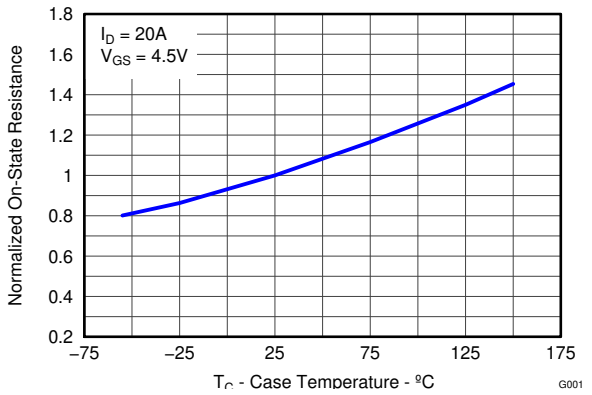


Figure 5-8. Normalized On Resistance vs. Temperature

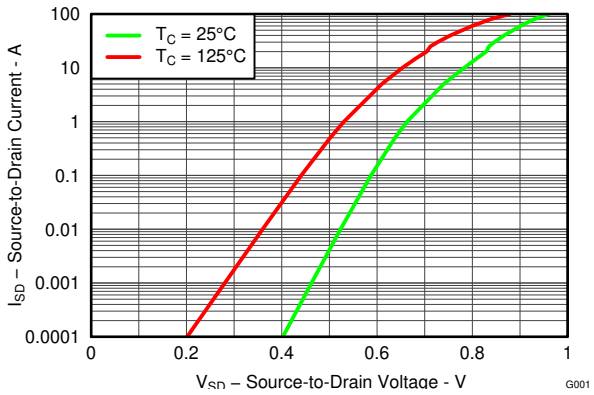


Figure 5-9. Typical Diode Forward Voltage

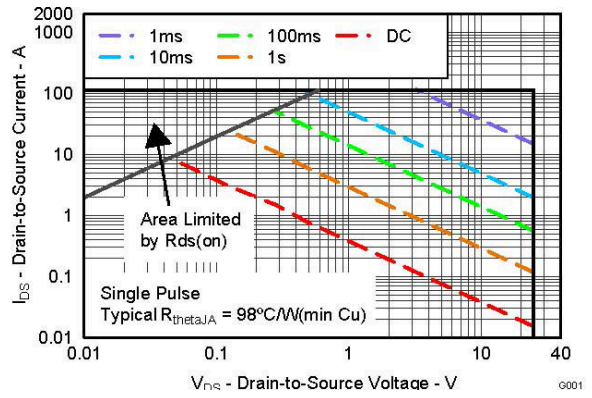


Figure 5-10. Maximum Safe Operating Area

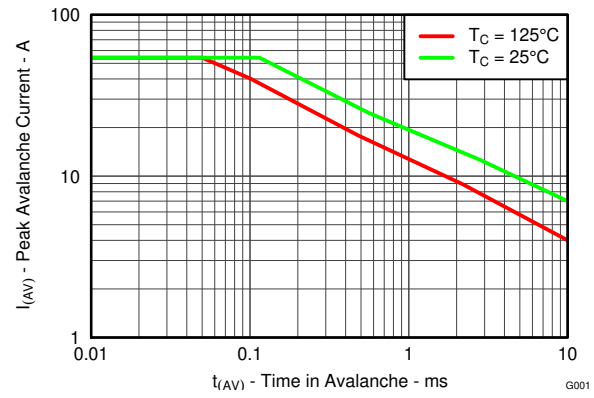


Figure 5-11. Single Pulse Unclamped Inductive Switching

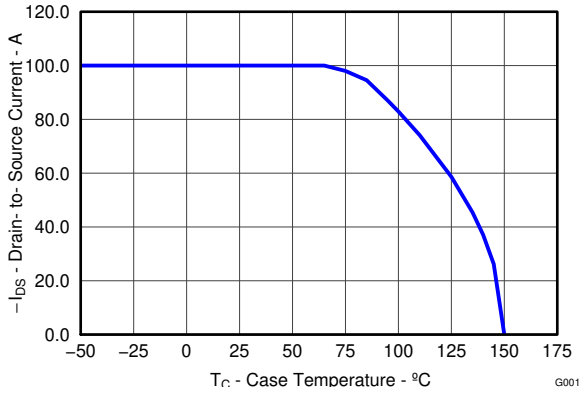


Figure 5-12. Maximum Drain Current vs. Temperature

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2012) to Revision B (January 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2012) to Revision A (March 2012)	Page
• Changed the device status from: Product Preview to Production Data	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16342Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16342	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

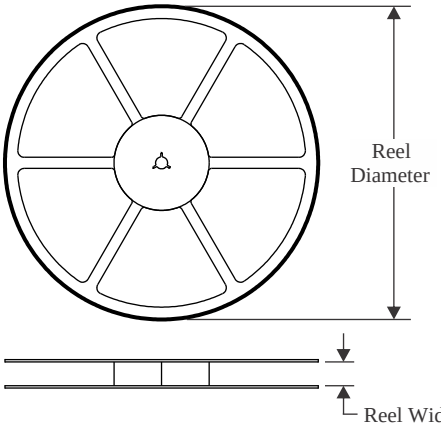
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

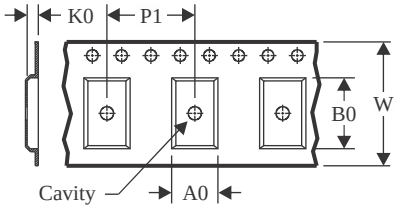
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

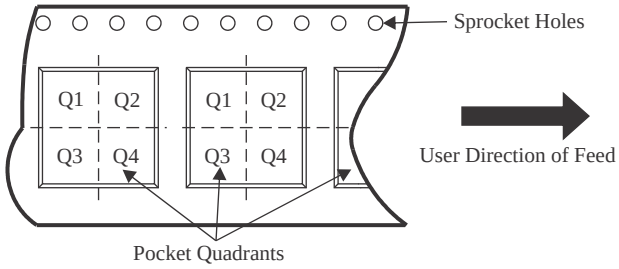


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

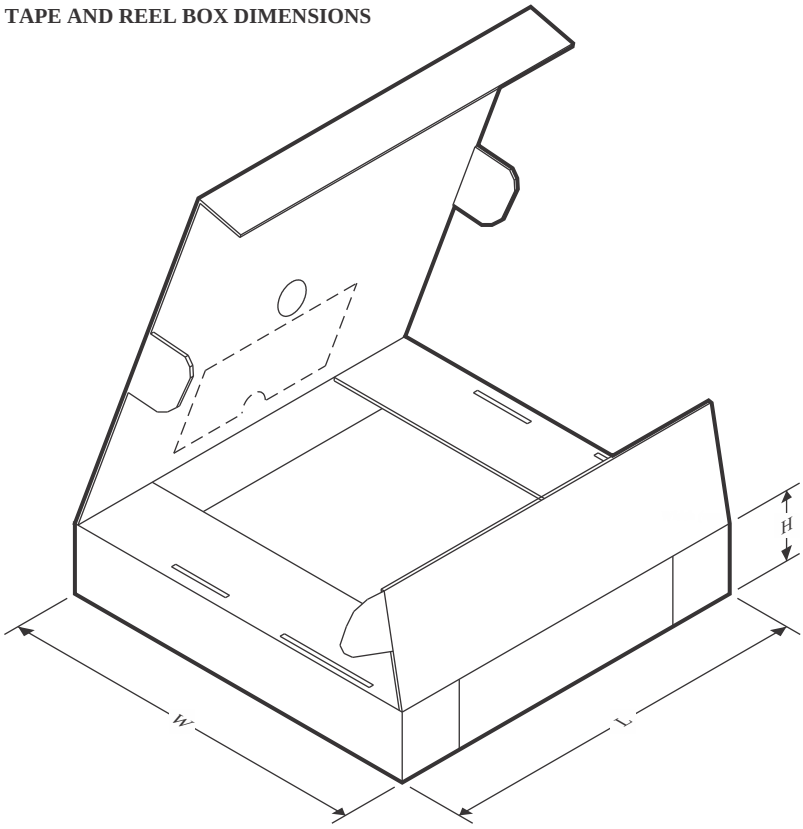
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

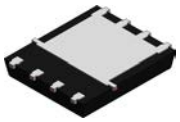
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16342Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16342Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

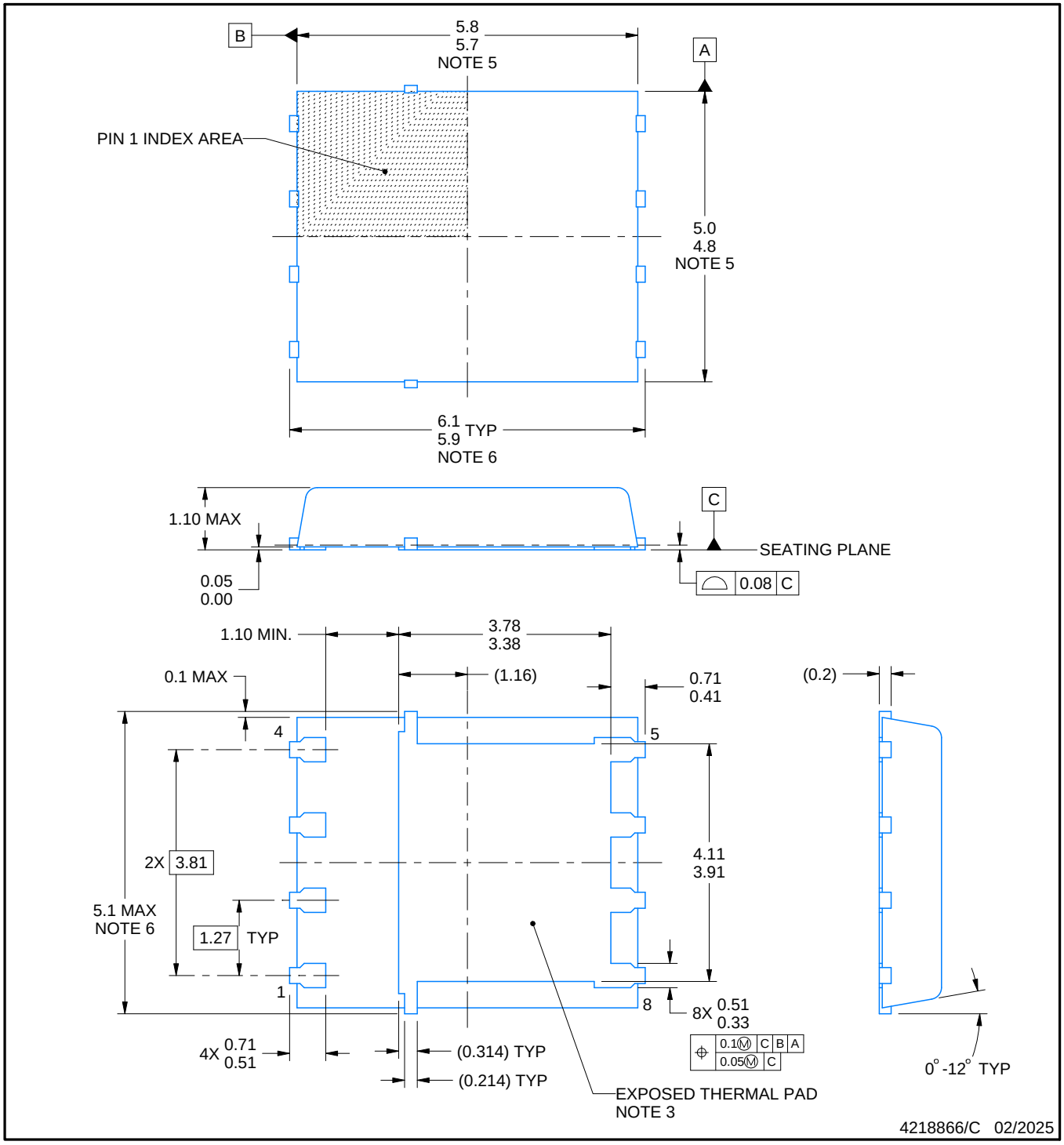


PACKAGE OUTLINE

DQJ0008A

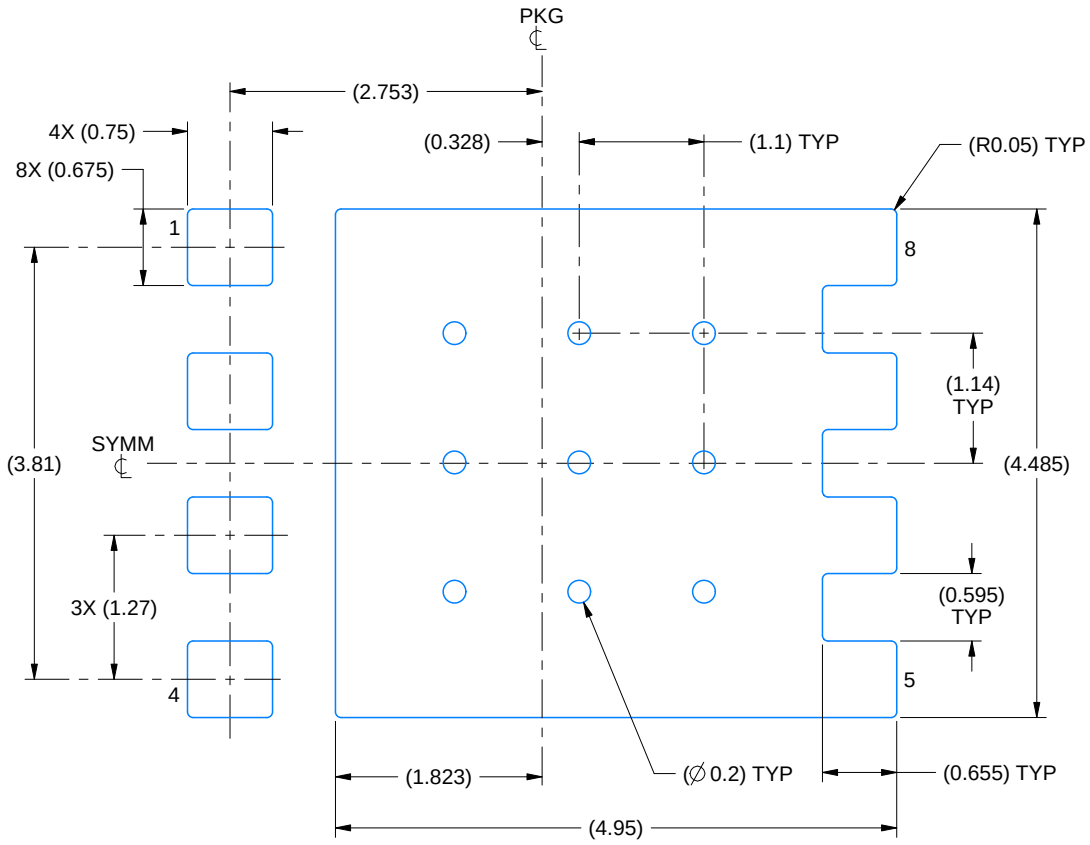
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

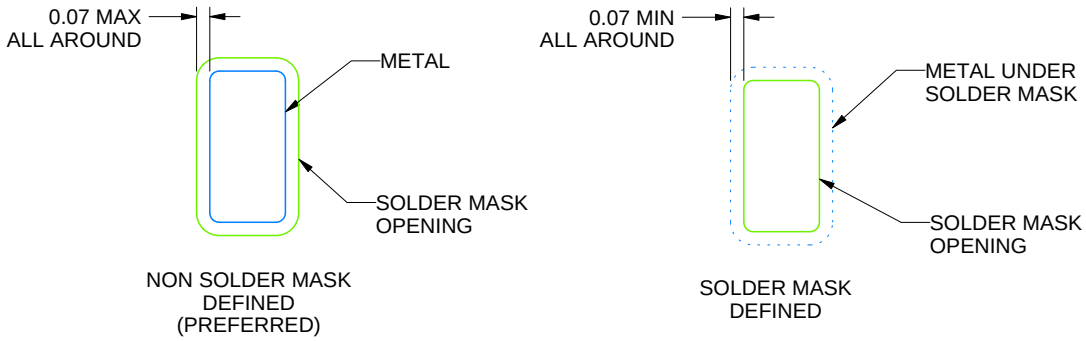


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

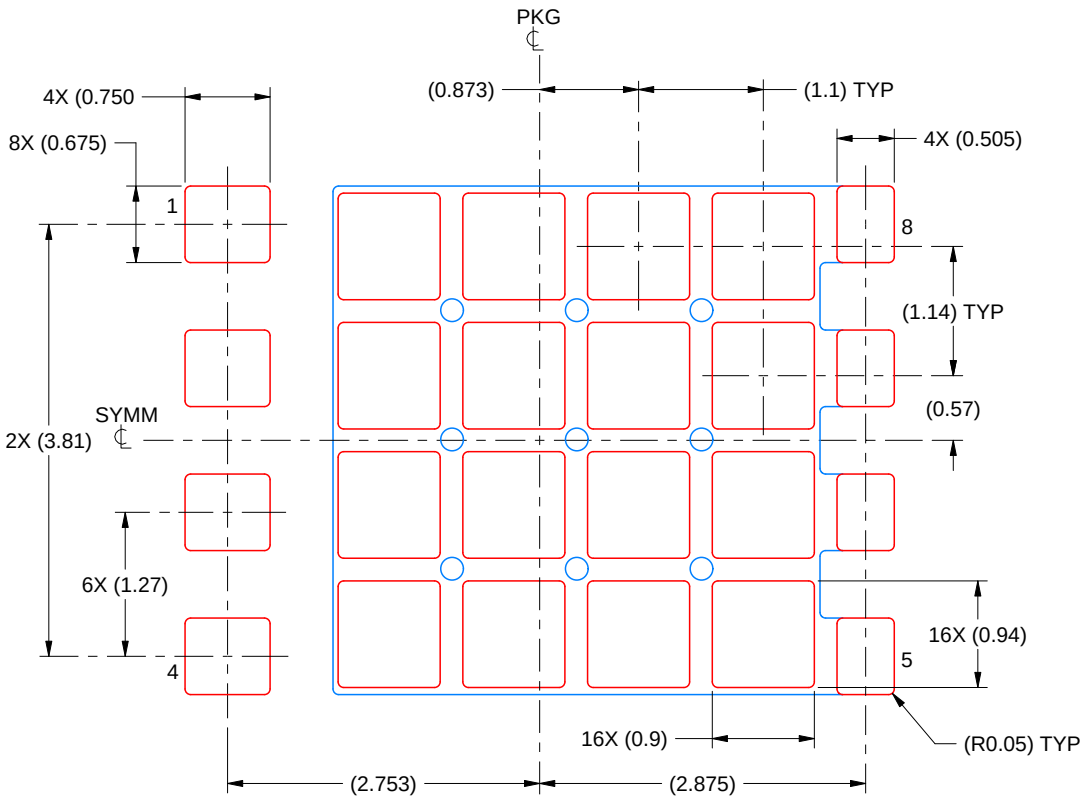


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265