CDC6Cx Low Power LVCMOS Output BAW Oscillator

1 Features

- LVCMOS output Oscillator supporting frequency range from 250kHz to 200MHz
- ±50ppm total frequency stability inclusive of all factors and including 10 years aging
- Supply Voltage supports 1.8V to 3.3V ±10%.
- Very low power consumption: 4.57mA typical and 7.4mA maximum for 25MHz
- Stand by current 2µA typical helps for battery powered applications
- Low jitter: < 1ps RMS jitter for F_{out} ≥ 10MHz
- Smallest industry standard package: 1.60mm × 1.2mm (DLY), 2.00mm × 1.60mm (DLX), 2.50mm × 2.00mm (DLF), 3.20mm × 2.5mm (DLE)
- Operating temperature range of -40°C to +105°C
- Integrated LDO for robust supply noise immunity
- Start up time < 3ms
  - Contact TI for different start-up times.
- Orderable options for slow rise and fall time for EMI reduction

Standard frequencies (MHz): 2.048, 4, 5.12, 8, 10, 12, 12.288, 16, 19.2, 20, 23.5008, 24, 24.576, 25, 26,26.2144, 27, 28.125, 29.9925, 30, 32.768, 33. 33, 33.333, 38.4, 40, 48, 49.152, 50, 66.666, 76.8, 100, 125, 156.25, and more

- Contact TI representative for any frequency and samples needed.

2 Applications

- Crystal oscillator replacement
- Data centers, Server, Storage
- Ethernet, SAS, SATA, USB, WIFI
- Wireless Communication
- Professional audio/video
- Factory Automation and Control
- Personal Electronics, Wearable devices, IoT
- FPGA, MCU, Processor and ASIC clocking

3 Description

Texas Instruments' high-precision Bulk-Acoustic Wave (BAW) micro-resonator technology is integrated directly into a package allowing for low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

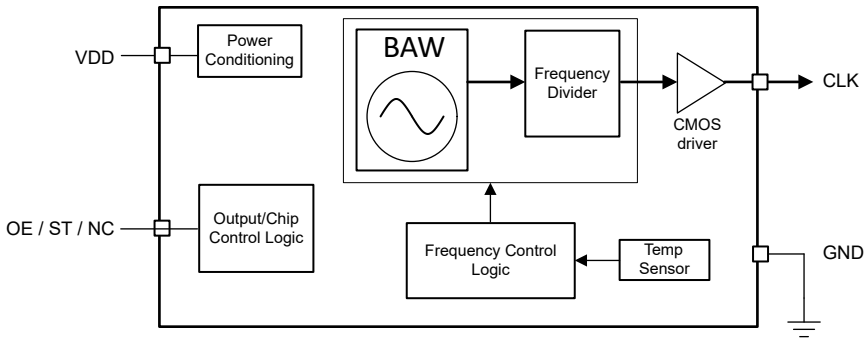
The CDC6Cx device is a low jitter, low power, fixed-frequency oscillator which incorporates the BAW as the resonator source. The device is factory-programmed per specific frequency and function pin. With a Frequency control logic and output frequency divider, the CDC6Cx is capable of producing any frequency within the specified range providing a single device family for all frequency needs.

The high-performance clocking, mechanical stability, lower power consumption and small package options for this device are designed for reference clock and core clocks in Industrial, Telecom, Data and Enterprise Network and Personal Electronics end equipments.

Packaging Information

PART NUMBER	OUTPUT TYPE	PACKAGE(1)	PACKAGE SIZE(2)
CDC6C	LVCMOS	VSON (DLE-4)	3.20mm × 2.50mm
		VSON (DLF-4)	2.50mm × 2.00mm
		VSON (DLX-4)	2.00mm × 1.60mm
		VSON (DLY-4)	1.60mm × 1.20mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



CDC6Cx Simplified Block Diagram

Table of Contents

4 Device Comparison

Use CDC6C OPN Decoder to understand the device nomenclature of the CDC6Cx orderable options. CDC6C OPN Decoder provides a quick summary of how to decode the frequency, package information and a list of the CDC6Cx orderable part numbers (OPNs) with associated configurations, packaging information, and device top marking.

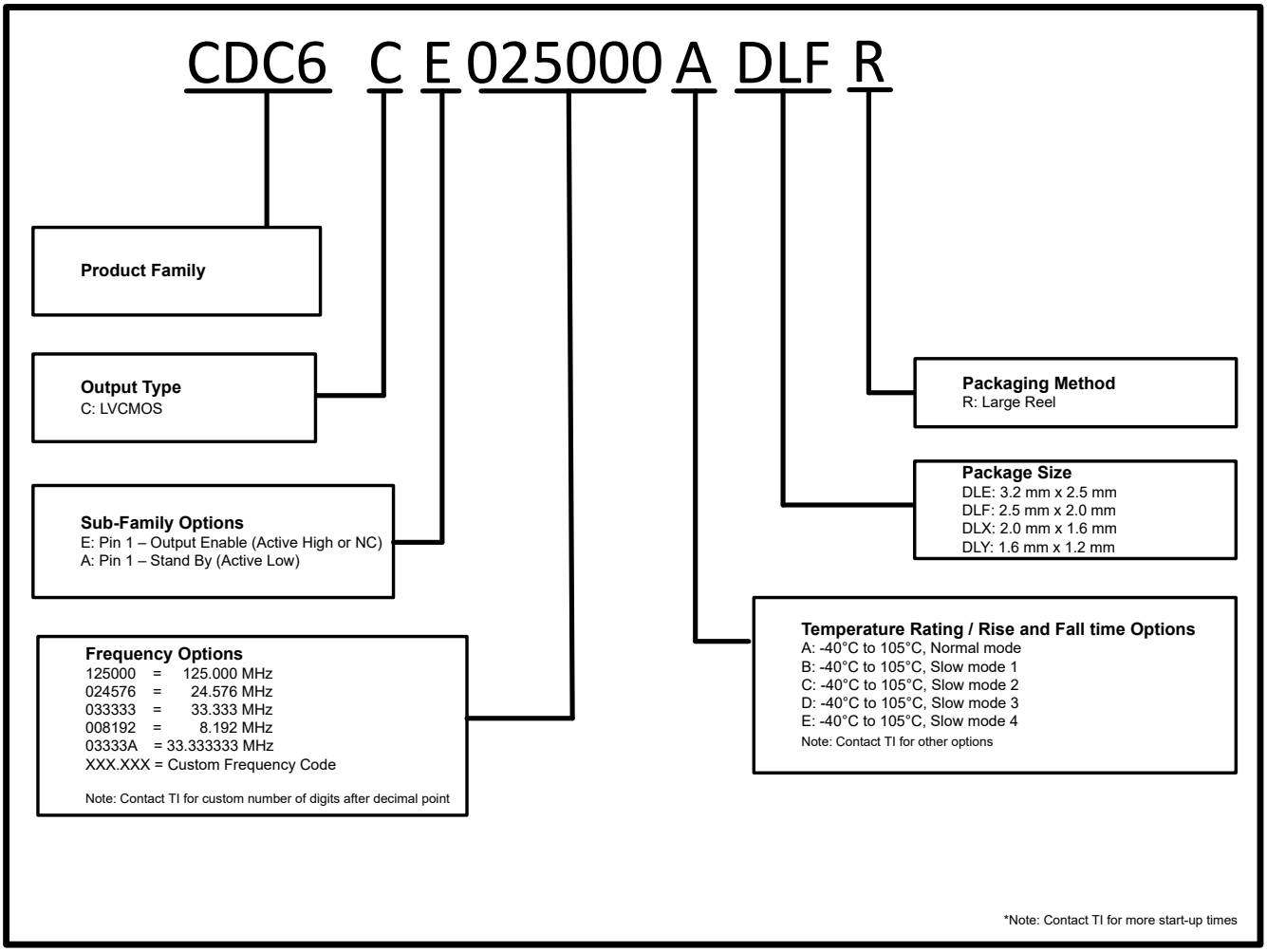


Figure 4-1. Part Number Guide: CDC6Cx

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

5 Pin Configuration and Functions

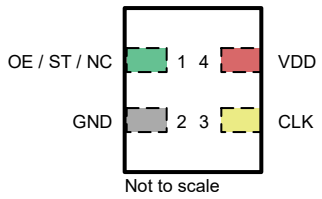


Figure 5-1. CDC6Cx 4-Pin VSON (Top View)

Table 5-1. CDC6Cx Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
OE / ST / NC	1	I / NC	Output Enable (OE) or Stand By (ST) pin on No Connect (NC). See Function Pin Descriptions for CDC6C for more details
GND	2	G	Device ground
CLK	3	O	LVCMOS output clock
VDD	4	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage(2)	–0.3	3.63	V
EN	Logic Input Voltage	–0.3	3.63	V
CLK	Clock Output Voltage	–0.3	3.63	V
T_J	Junction Temperature		130	℃
T_{STG}	Storage Temperature		150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For all devices with Recommended Operating Voltage of 1.8V ±10%, 2.5V ±10% and 3.3V ±10%

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HBM Classification Level 1C, all pins(3) (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, CDM Classification Level C1, all pins(3) (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) For Industrial Grade device

6.3 Environmental Compliance

		VALUE	UNIT
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007, Condition A	20	g
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Moisture Sensitivity Level (MSL)		MSL1	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage(1)	1.62	1.8, 2.5, 3.3	3.63	V
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature			130	°C
t_{RAMP}	VDD power-up ramp time(2)	0.1		100	ms

(1) For all devices with Recommended Operating Voltage of 1.8V ±10%, 2.5V ±10% and 3.3V ±10%
(2) VDD power-up ramp time is defined as minimum time taken for power supply to exceed 95% of nominal VDD. Monotonic power supply ramp is assumed.

6.5 Thermal Information

THERMAL METRIC(1)		CDC6C				UNIT
		DLE	DLF	DLX	DLY	
		4	4	4	4	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.8	151.7	180.3	189.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	99.3	116.2	137.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	64.4	85.5	85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.1	9.2	8.5	6.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.2	63.5	83.7	83.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Electrical Characteristics

Over Recommended Operating Conditions (VDD = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10% ; Typical values are at 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD}	Device Current Consumption (excluding load current)	-40°C to 85°C, F_{out} = 20 MHz, Vdd = 1.8V±10%		4.22	6.7	mA
		-40°C to 85°C, F_{out} = 20 MHz, Vdd = 3.3V±10%		4.41	6.7	mA
		-40°C to 105°C, F_{out} = 20 MHz, Vdd = 1.8V±10%		4.22	7.3	mA
		-40°C to 105°C, F_{out} = 20 MHz, Vdd = 3.3V±10%		4.41	7.3	mA
I_{DD}	Device Current Consumption (excluding load current)	-40°C to 85°C, F_{out} = 25 MHz, Vdd = 1.8V±10%		4.32	6.8	mA
		-40°C to 85°C, F_{out} = 25 MHz, Vdd = 3.3V±10%		4.57	6.9	mA
		-40°C to 105°C, F_{out} = 25 MHz, Vdd = 1.8V±10%		4.32	7.4	mA
		-40°C to 105°C, F_{out} = 25 MHz, Vdd = 3.3V±10%		4.57	7.5	mA
I_{DD}	Device Current Consumption (excluding load current)	-40°C to 85°C, F_{out} = 50 MHz, Vdd = 1.8V±10%		4.84	7.1	mA
		-40°C to 85°C, F_{out} = 50 MHz, Vdd = 3.3V±10%		5.33	7.2	mA
		-40°C to 105°C, F_{out} = 50 MHz, Vdd = 1.8V±10%		4.84	7.6	mA
		-40°C to 105°C, F_{out} = 50 MHz, Vdd = 3.3V±10%		5.33	7.8	mA
I_{DD}	Device Current Consumption (excluding load current)	-40°C to 85°C, F_{out} = 100 MHz, Vdd = 1.8V±10%		5.86	7.6	mA
		-40°C to 85°C, F_{out} = 100 MHz, Vdd = 3.3V±10%		6.77	9.0	mA
		-40°C to 105°C, F_{out} = 100 MHz, Vdd = 1.8V±10%		5.86	8.2	mA
		-40°C to 105°C, F_{out} = 100 MHz, Vdd = 3.3V±10%		6.77	9.0	mA
I_{DD}	Device Current Consumption (excluding load current)	-40°C to 85°C, F_{out} = 150 MHz, Vdd = 1.8V±10%		7.14	9.5	mA
		-40°C to 85°C, F_{out} = 150 MHz, Vdd = 3.3V±10%		8.72	11.0	mA
		-40°C to 105°C, F_{out} = 150 MHz, Vdd = 1.8V±10%		7.14	9.5	mA
		-40°C to 105°C, F_{out} = 150 MHz, Vdd = 3.3V±10%		8.72	11.0	mA
I_{DD_stdby}	Device Stand By Current	-40°C to 85°C, ST = GND, Vdd=1.8V±10%		1.5		µA
		-40°C to 85°C, ST = GND, Vdd=3.3V±10%		2.7		µA
		-40°C to 105°C, ST = GND, Vdd=1.8V±10%		1.5		µA
		-40°C to 105°C, ST = GND, Vdd=3.3V±10%		2.7		µA
I_{DD-OD}	Device current with output Disabled	-40°C to 85°C, F_{out} = 25 MHz, Vdd = 1.8V±10%		3.75	6.4	mA
		-40°C to 85°C, F_{out} = 25 MHz, Vdd = 3.3V±10%		3.76	6.5	mA
		-40°C to 105°C, F_{out} = 25 MHz, Vdd = 1.8V±10%		3.75	7	mA
		-40°C to 105°C, F_{out} = 25 MHz, Vdd = 3.3V±10%		3.76	7.1	mA
Output Characteristics						
F_{out}	Output Frequency		0.25		200	MHz

Over Recommended Operating Conditions (VDD = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10% ; Typical values are at 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output Low Voltage	I_{OL} = 3.6mA, VDD = 1.8V			0.36	V
		I_{OL} = 5.0mA, VDD = 2.5V			0.5	V
		I_{OL} = 6.6mA, VDD = 3.3V			0.66	V
V_{OH}	Output High Voltage	I_{OH} = 3.6mA, VDD = 1.8V	VDD x0.88			V
		I_{OH} = 5.0mA, VDD = 2.5V	VDD x 0.85			V
		I_{OH} = 6.6mA, VDD = 3.3V	VDD x 0.85			V
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 2 pF, normal mode		0.28	0.65	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 2 pF, slow mode 1		0.42	0.75	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 5 pF, normal mode		0.33	0.8	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 5 pF, slow mode 2		1.11	2.0	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 10 pF, normal mode		0.44	1.7	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 10 pF, slow mode 3		1.85	3.1	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 15 pF, normal mode		0.87	2.2	ns
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 15 pF, slow mode 4		2.7	4.0	ns
ODC	Output Duty Cycle		45	50	55	%
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	Fout = 50 MHz		–155		dBc/Hz
C_L	Maximum capacitive load	Fout < 50 MHz			30	pF
C_L	Maximum capacitive load	Fout > 50 MHz			15	pF
$R_{out-high}$	Output Impedance		37.5	50	62.5	Ω
Function Pin Characteristics (OE/ST)						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.3			V
I_{IL}	Input Low Current	EN = GND	–40			µA
I_{IH}	Input High Current	EN = VDD			40	µA
C_{IN}	Input Capacitance(1)			2		pF
Frequency Tolerance						
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 105℃, variation over supply voltage range, and 10 years aging at 25℃.			±50	ppm
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 105℃, variation over supply voltage range, and 1st year aging at 25℃.			±45	ppm
PSRR Characteristics						
PSRR	Spur induced by 50 mV power supply ripple at 50MHz output, VDD = 2.5V/3.3 V, No power supply decoupling capacitor	Sine wave at 50 kHz		-80		dBc
		Sine wave at 100 kHz		-75		dBc
		Sine wave at 500 kHz		-63		dBc
		Sine wave at 1 MHz		-59		dBc
Power-On Characteristics						
t_{START_UP}	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification. OE / ST = High; Tested with a power supply ramp time of 200 µs		1.5	3	ms
t_{RESUME}	Chip Resume Time	Time elapsed from ST = V_{IH} until output is enabled and output is within specification			3	ms

Over Recommended Operating Conditions (VDD = 1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10% ; Typical values are at 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ST-DIS}	Chip Disable Time	Time elapsed from ST = V_{IL} until chip is in standby mode; for Fout>100 MHz			250	ns
t_{OE-EN}	Output Enable Time	Time elapsed from OE = V_{IH} until output is enabled and output is within specification; for Fout>100 MHz			250	ns
t_{OE-DIS}	Output Disable Time	Time elapsed from OE = V_{IL} until output is disabled; for Fout>100 MHz			250	ns
Clock Output Jitter						
R_J	Random Phase Jitter	F_{out} = 12.288 MHz, Integration BW: 12 kHz - 5 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 19.2 MHz, Integration BW: 12 kHz - 5 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 24 MHz, Integration BW: 12 kHz - 5 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 25 MHz, Integration BW: 12 kHz - 5 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 48 MHz, Integration BW: 12 kHz - 20 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 50 MHz, Integration BW: 12 kHz - 20 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 100 MHz, Integration BW: 12 kHz - 20 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 125 MHz, Integration BW: 12 kHz - 20 MHz, Max Temp = 105		400	1000	fs
R_J	Random Phase Jitter	F_{out} = 156.25 MHz, Integration BW: 12 kHz - 20 MHz, Max Temp = 105		400	1000	fs
SPN_{100k}	Spot Phase Noise @ 1 kHz Offset	F_{out} = 100 MHz		-86		dBc/Hz
SPN_{100k}	Spot Phase Noise @ 10 kHz Offset	F_{out} = 100 MHz		-120		dBc/Hz
SPN_{100k}	Spot Phase Noise @ 100 kHz Offset	F_{out} = 100 MHz		-138		dBc/Hz
SPN_{1M}	Spot Phase Noise @ 1 MHz Offset	F_{out} = 100 MHz		-143		dBc/Hz
$R_{JITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz; Integration BW: 12 kHz - 20 MHz		3		ps
$R_{JITT,PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		26		ps

(1) Proven by Design. Not characterised

6.7 Timing Diagrams

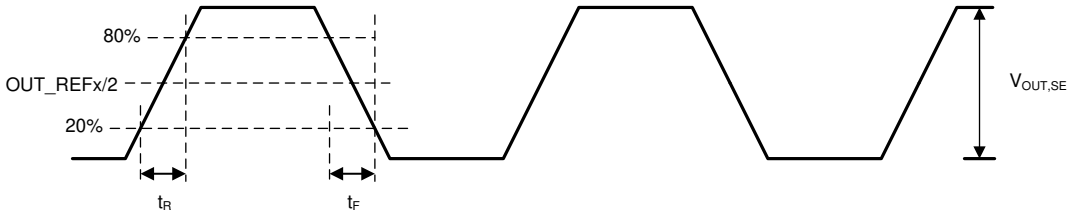


Figure 6-1. Single-Ended Output Voltage and Rise/Fall Time

6.8 Typical Characteristics

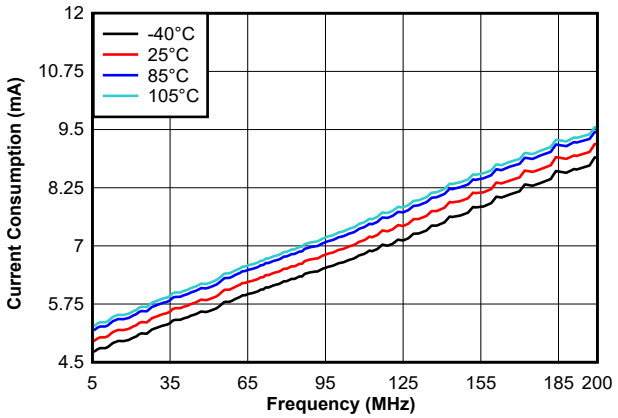


Figure 6-2. Current Consumption vs. Frequency and Temperature at 1.8V Supply

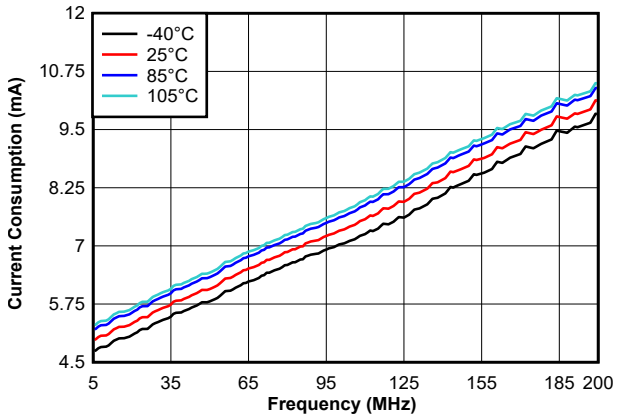


Figure 6-3. Current Consumption vs. Frequency and Temperature at 2.5V Supply

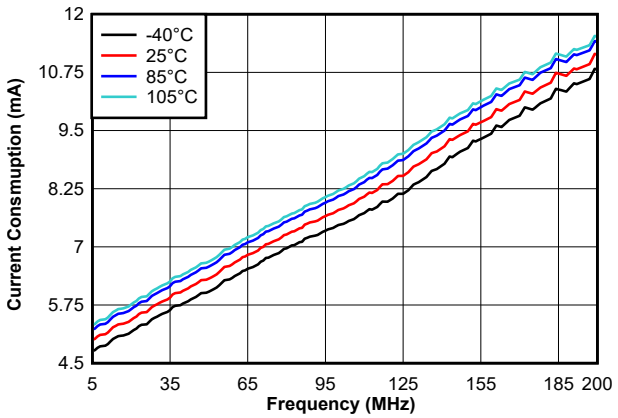


Figure 6-4. Current Consumption vs. Frequency and Temperature at 3.3V Supply

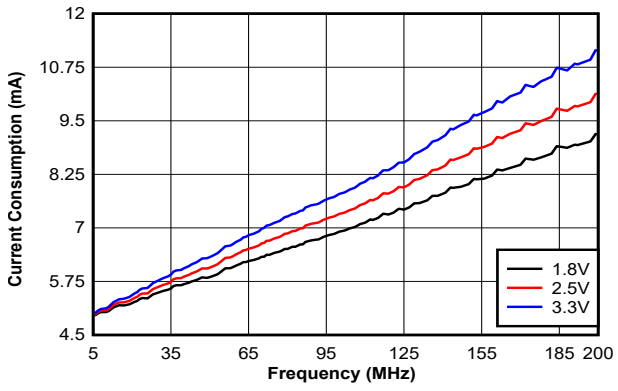


Figure 6-5. Current Consumption vs. Frequency and Supply Voltage at 25°C

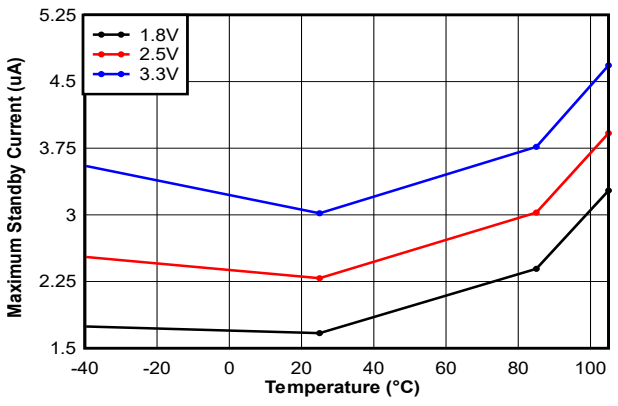


Figure 6-6. Maximum Standby Current vs. Temperature and Supply Voltage

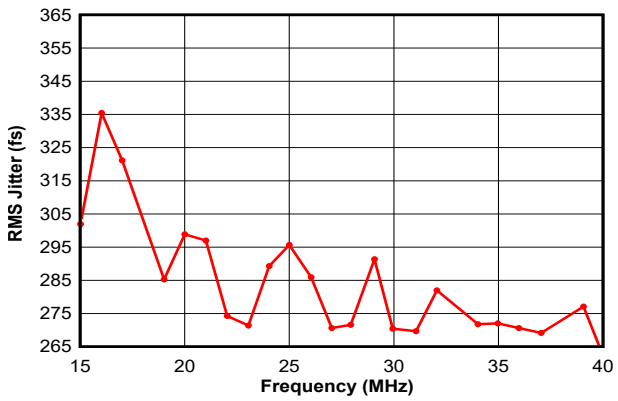


Figure 6-7. Typical RMS Jitter vs. Frequency at 3.3V Supply and 25°C (BW 12kHz to 5MHz)

6.8 Typical Characteristics (continued)

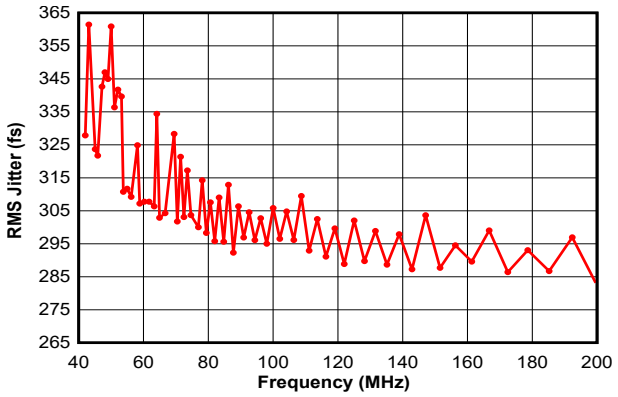


Figure 6-8. Typical RMS Jitter vs. Frequency at 3.3V Supply and 25°C (BW 12kHz to 20MHz)

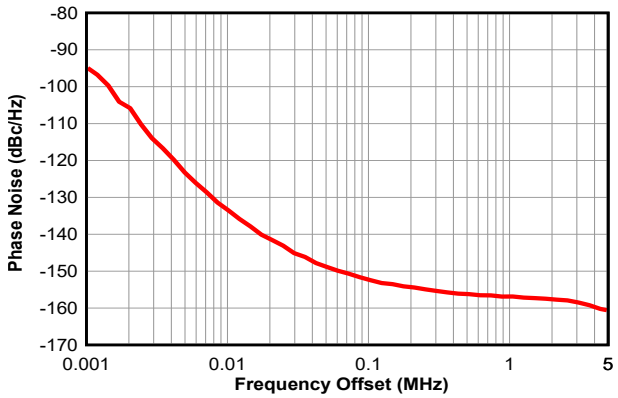


Figure 6-9. Phase Noise Curve at 25MHz, 25°C, and 3.3V Supply

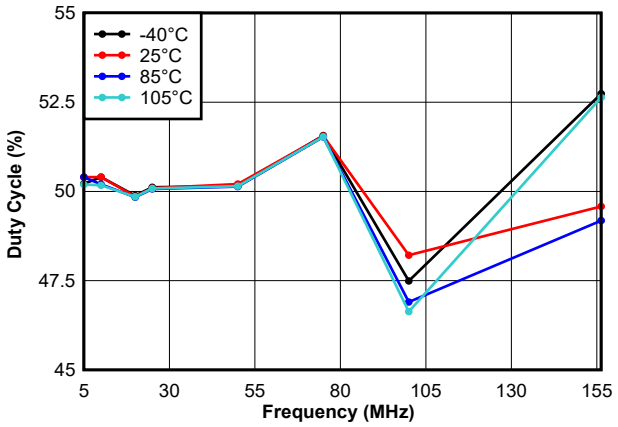


Figure 6-10. Duty Cycle vs. Frequency and Temperature at 3.3V Supply, No Capacitative Load, Normal Mode Device

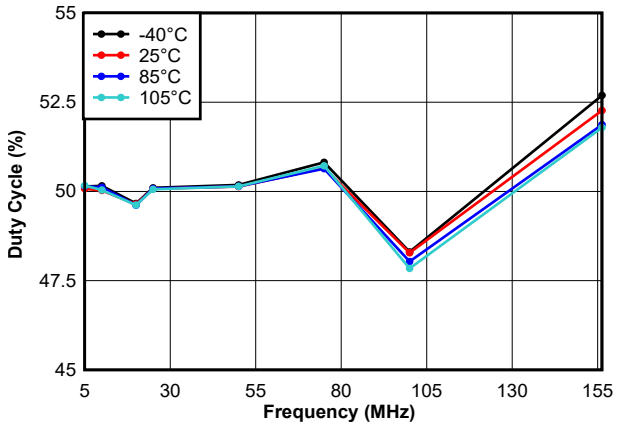


Figure 6-11. Duty Cycle vs. Frequency and Temperature at 2.5V Supply, No Capacitative Load, Normal Mode Device

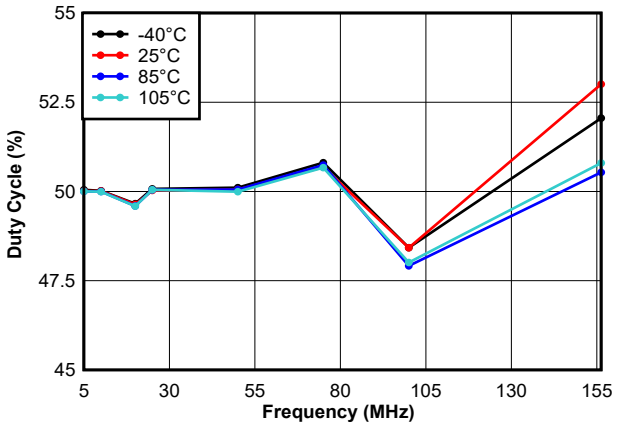


Figure 6-12. Duty Cycle vs. Frequency and Temperature at 1.8V Supply, No Capacitative Load, Normal Mode Device

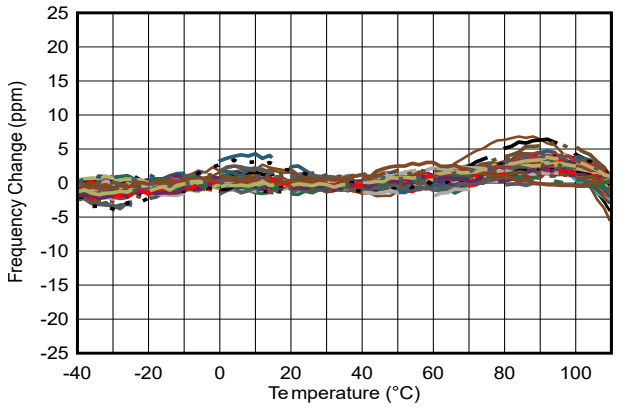
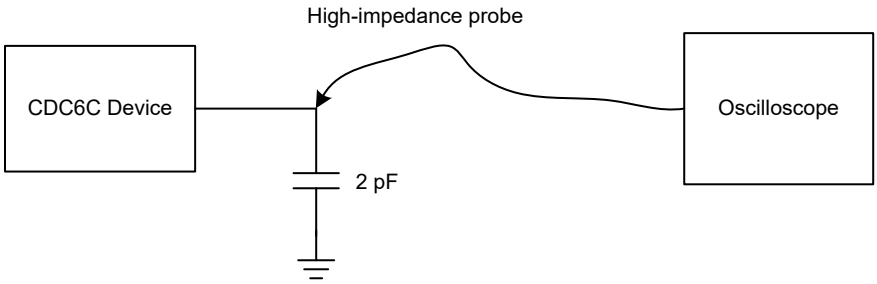


Figure 6-13. Frequency Change vs. Temperature at 25MHz and 3.3V Supply, 80 devices

7 Parameter Measurement Information

7.1 Device Output Configurations



Load capacitor modified based on measurement condition.

Figure 7-1. CDC6Cx Output Test Configuration

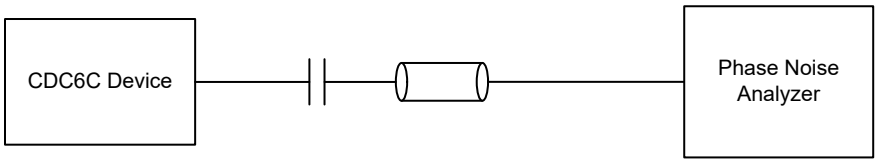


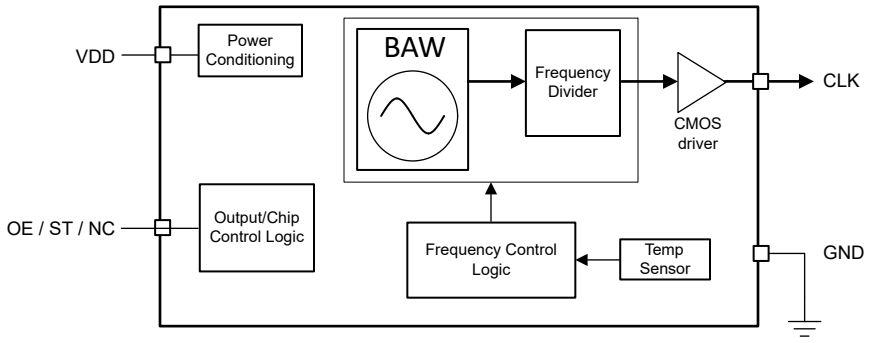
Figure 7-2. CDC6Cx Output Phase Noise Test Configuration

8 Detailed Description

8.1 Overview

The CDC6Cx is a fixed-frequency, BAW based oscillator that supports a CMOS output format within the range of 250kHz to 200MHz.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5 GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by absorption of surface contaminants and can be directly placed in a non-hermetic plastic package with the oscillator IC in small standard oscillator footprints.

8.3.2 Device Block-Level Description

The device contains a BAW oscillator, frequency divider and CMOS driver which together generates a pre programmed output frequency. Temperature variations of oscillation frequency are continuously monitored by internal precision temperature sensor and provided as input to the Frequency Control Logic Block. Using this Frequency Control Logic block, frequency corrections are performed internally for maintaining the output frequency within ±50ppm across temperature range and aging. The device contains an internal LDO which reduces the power supply noise, resulting in low noise clock output.

8.3.3 Function Pin

Pin 1 on the CDC6Cx is the function pin which have multiple functions based on the orderable part number. The function can be used as Output Enable (OE), Stand By (ST) or No Connect (NC). Options for both Active High and Active Low are available for OE and ST. Contact TI for Active Low options. Table 8-1 lists the functions of pin 1.

Table 8-1. Function Pin Descriptions for CDC6Cx

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
E (Pin 1)	Output Enable (Active High / NC)	**HIGH or No Connect** : Output active at Specified Frequency **LOW** : Output disabled, high impedance; current consumption is given by I_{DD-PD}

Table 8-1. Function Pin Descriptions for CDC6Cx (continued)

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
A (Pin 1)	Standby (Active Low)	**LOW** : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ **HIGH or No Connect**: Output active at Specified Frequency

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of the Section 6.6 table. The return to the output clock active time corresponds to the same as the initial start-up time.

The Function Pin is driven internally with resistance >100 kΩ.

8.3.4 Clock Output Interfacing and Termination

Below are the recommended output interfacing and termination circuits.

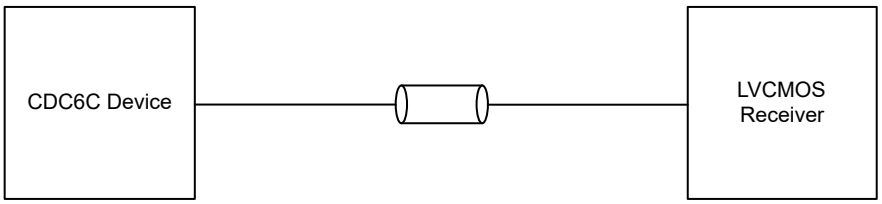


Figure 8-1. CDC6Cx Output to LVCMOS Receiver

8.3.5 Temperature Stability

Figure 8-2 shows the CDC6Cx frequency change across temperature. The figure illustrates the frequency change of 80 different devices at different temperatures across the temperature range of –40°C to 105°C. This demonstrates the typical temperature stability of the device, remaining below ±10ppm.

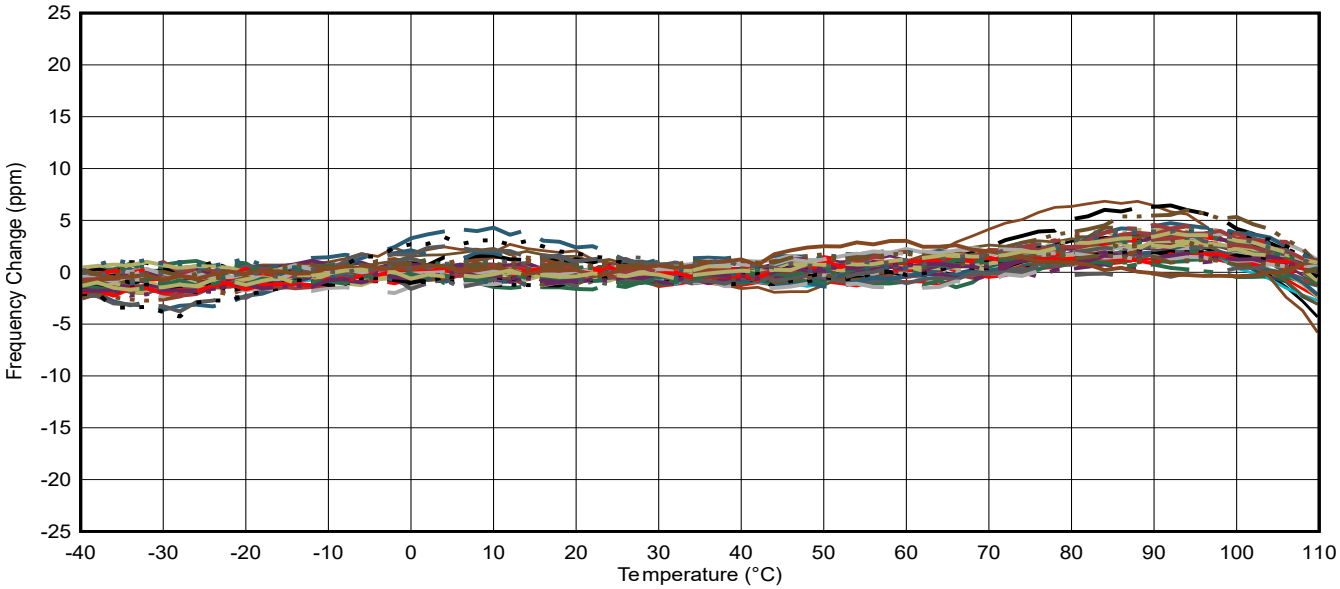


Figure 8-2. Typical Frequency Change From 25MHz Over Temperature Over 80 devices

8.3.6 Mechanical Robustness

For reference oscillators, vibration and shock are common causes for increased phase noise and jitter, frequency shift and spikes, or even physical damages to the resonator and package. Compared to quartz

crystals, the BAW resonator is more immune to vibration and shock due to the orders of magnitude smaller mass and higher frequency—that is force applied to the device from acceleration is much smaller due to smaller mass.

Figure 8-3 shows the CDC6Cx BAW oscillator vibration performance. TI followed MIL-STD-883 Method 2026 Conditions C (10g) and Method 2007 Condition A (20g) for testing. In this test, the CDC6Cx oscillator is mounted on an EVM and subjected to a 10g acceleration force, ranging from 50Hz to 2kHz in the x, y, and z-axis. Phase noise trace with spur due to vibration is captured using Keysight E5052B and frequency deviation is calculated from the spur power. Then the frequency deviation is converted to ppb by noting the carrier frequency and normalized to ppb/g. Finally, the RMS sum of ppb/g along all three axes is reported as the Vibration sensitivity in ppb/g. CDC6Cx performance under vibration is approximately 2ppb/g while most quartz oscillators best case is 3ppb/g and worse can be above 10ppb/g.

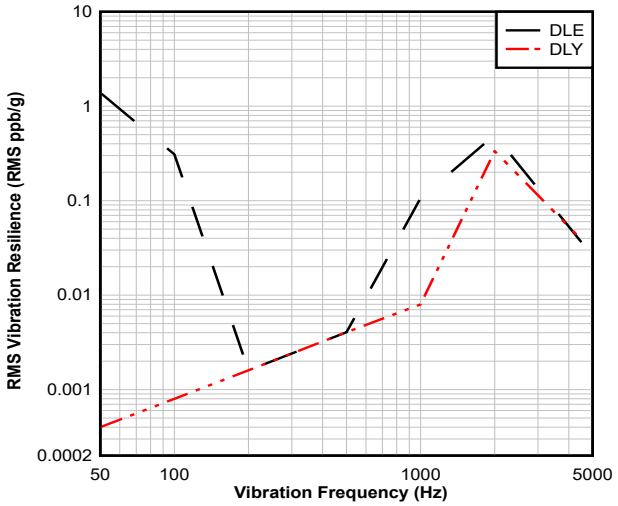


Figure 8-3. Vibration Resilience vs. Vibration Frequency at 25MHz, 25°C, Supply 1.8V - X-axis

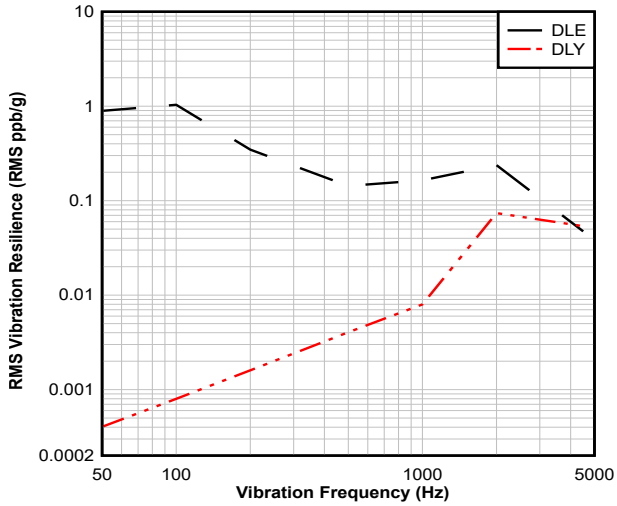


Figure 8-4. Vibration Resilience vs. Vibration Frequency at 25MHz, 25°C, Supply 1.8V - Y-axis

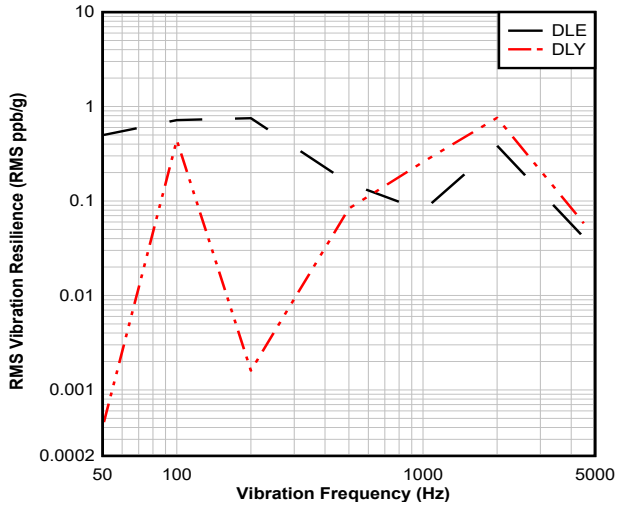


Figure 8-5. Vibration Resilience vs. Vibration Frequency at 25MHz, 25°C, Supply 1.8V - Z-axis

For the mechanical shock test, TI followed MIL-STD-883F Method 2002 Condition A (1500g) for testing. For more information on BAW technology mechanical robustness, please refer to Standalone BAW Oscillators Advantages Over Quartz Oscillators.

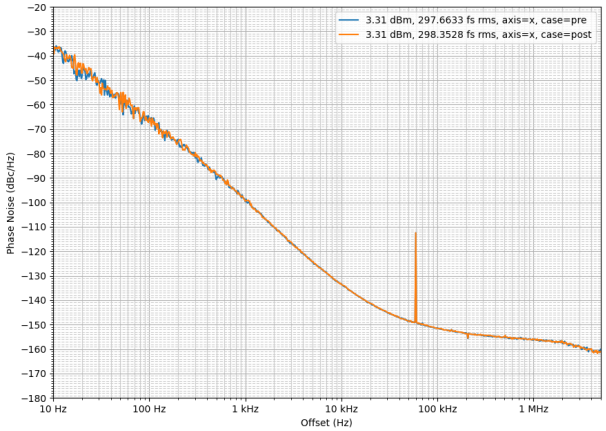


Figure 8-6. Pre and Post 1500g Mechanical Shock at 25MHz and 25°C, X-axis

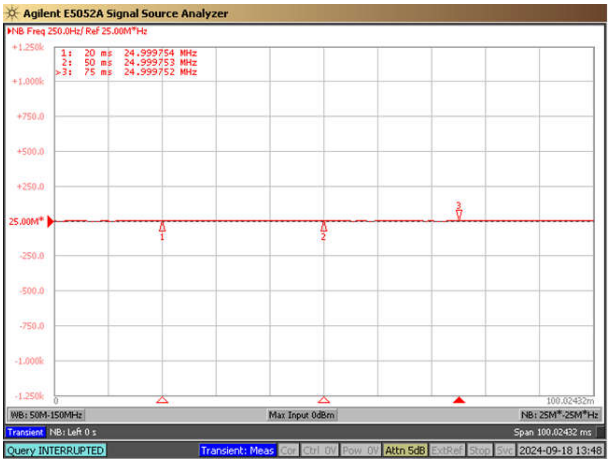


Figure 8-7. During 1500g Mechanical Shock at 25MHz and 25°C, X-axis

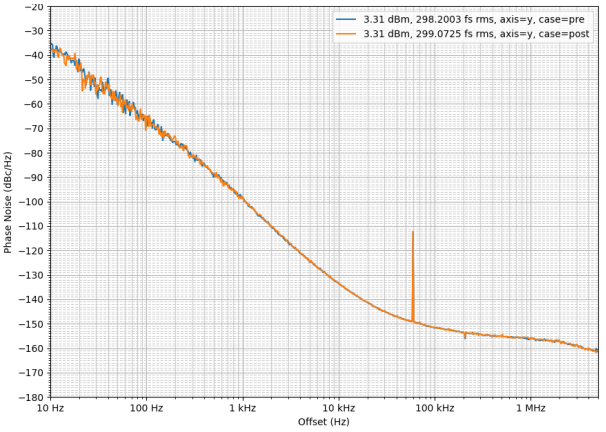


Figure 8-8. Pre and Post 1500g Mechanical Shock at 25MHz and 25°C, Y-axis

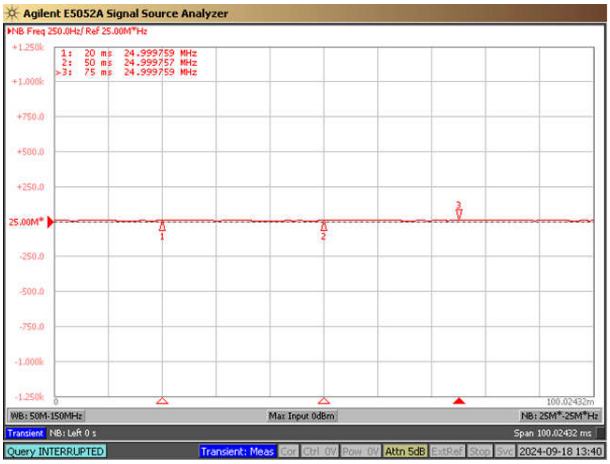


Figure 8-9. During 1500g Mechanical Shock at 25MHz and 25°C, Y-axis

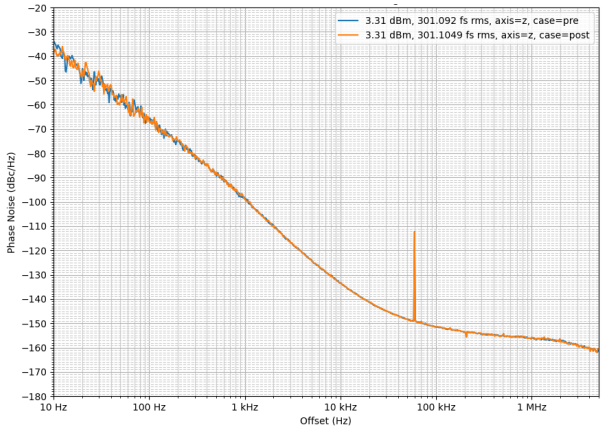


Figure 8-10. Pre and Post 1500g Mechanical Shock at 25MHz and 25°C, Z-axis

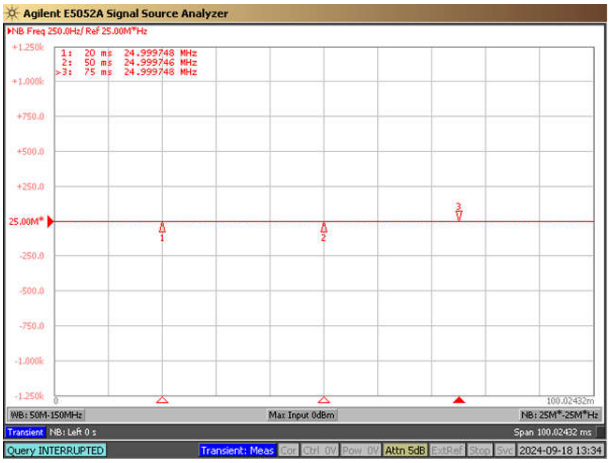


Figure 8-11. During 1500g Mechanical Shock at 25MHz and 25°C, Z-axis

8.4 Device Functional Modes

The CDC6Cx BAW Oscillator is a fixed frequency device and does not require any programming. The device pin 1 has different functions. See the Function Pin section for more information on the function pins.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The CDC6Cx is a low power, fixed frequency oscillator that can be used as a reference clock. The device supports any output frequency between 250kHz to 200MHz, single-ended output type, and 1.8V to 3.3V supply rails.

9.1.1 Driving Multiple Loads With a Single CDC6Cx

The CDC6Cx oscillator can be used to drive multiple loads to achieve cost reduction and BOM simplification. Be aware that using this technique degrades signal integrity and decreases performance. A good set of guidelines to follow when driving multiple loads include aiming to drive only 2 loads, maximizing common trace lengths across loads, and limiting total receiver capacitance to maximize fast rise and fall times. For more information on the effects of this technique and an implementation guide, please refer to Driving Multiple Loads With a Single LVCMOS Oscillator.

9.2 Typical Application

For a reference schematic implementation for CDC6Cx oscillator, refer to the Section 9.4.2 for bypass capacitor and AC-coupling capacitor value recommendations. Refer to the Clock Output Interfacing and Termination section for output clock required termination and biasing.

Application Example shows a typical application example. The CDC6Cx oscillator is used as a reference clock for a microcontroller or an FPGA in this example.

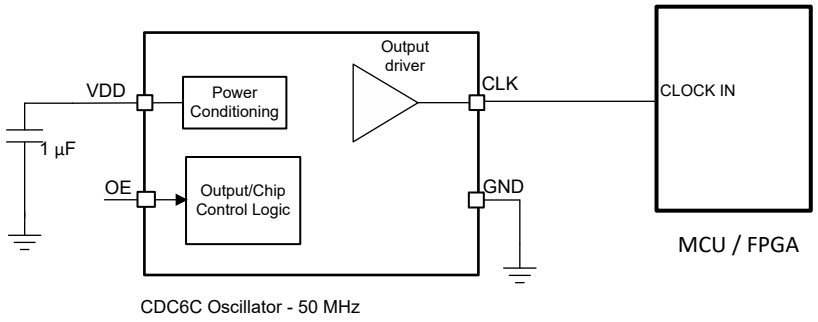


Figure 9-1. CDC6Cx Application Example

9.2.1 Design Requirements

The CDC6Cx is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in the Clock output Interfacing and termination section closely. Refer to the Function Pin section to understand the pin 1 function, and order the part number as per your requirements for Output Enable (OE), Standby (ST) options.

9.2.2 Detailed Design Procedure

The CDC6Cx has an integrated LDO and has excellent PSRR performance as shown in the **Electrical Characteristics** table. Refer to the CDC6CEVM User's Guide for the reference layout recommendation while designing with the CDC6Cx BAW oscillator.

For the Function Pin 1 of CDC6Cx, connect typical 10kΩ or smaller resistor to VDD for driving the OE pin High. Note that this pin can be left open if you do not want to use pullup resistor as the device has > 100kΩ internal pullup resistor. For driving the OE pin to Low, use the typical 10kΩ or smaller resistor as a pulldown resistor.

For EMI reduction, CDC6Cx has orderable options for reducing Rise / Fall time options. For applications requiring lesser EMI, select the appropriate Rise / Fall Time options.

CDC6Cx has four slow mode options other than the normal mode. Based on the desired rise/fall times, you can select the right slow mode option and load capacitance value which include 2pF, 5pF, 10pF and 15pF. The following table Rise / Fall options has recommended slow mode options for various load capacitance. For example, with load capacitance 15 pF, Slow Mode 4 option results in the slowest rise and fall times. You can also select Slow Mode 1, Slow Mode 2, or Slow Mode 3 with 15pF but the rise and fall times are faster.

Table 9-1. Rise / Fall time options

Slow Mode option	Load capacitance	Rise / Fall time (ns) with Slow Mode (Typical / Max)	Rise / Fall time (ns) with Normal Mode (Typical / Max)
Slow Mode 1	2pF	0.37 / 0.75	0.28 / 0.65
Slow Mode 2	5pF	0.9 / 2.0	0.3 / 0.8
Slow Mode 3	10pF	1.2 / 2.95	0.3 / 1.0
Slow Mode 4	15pF	1.95 / 4.0	0.57 / 2.2

9.2.3 Application Curves

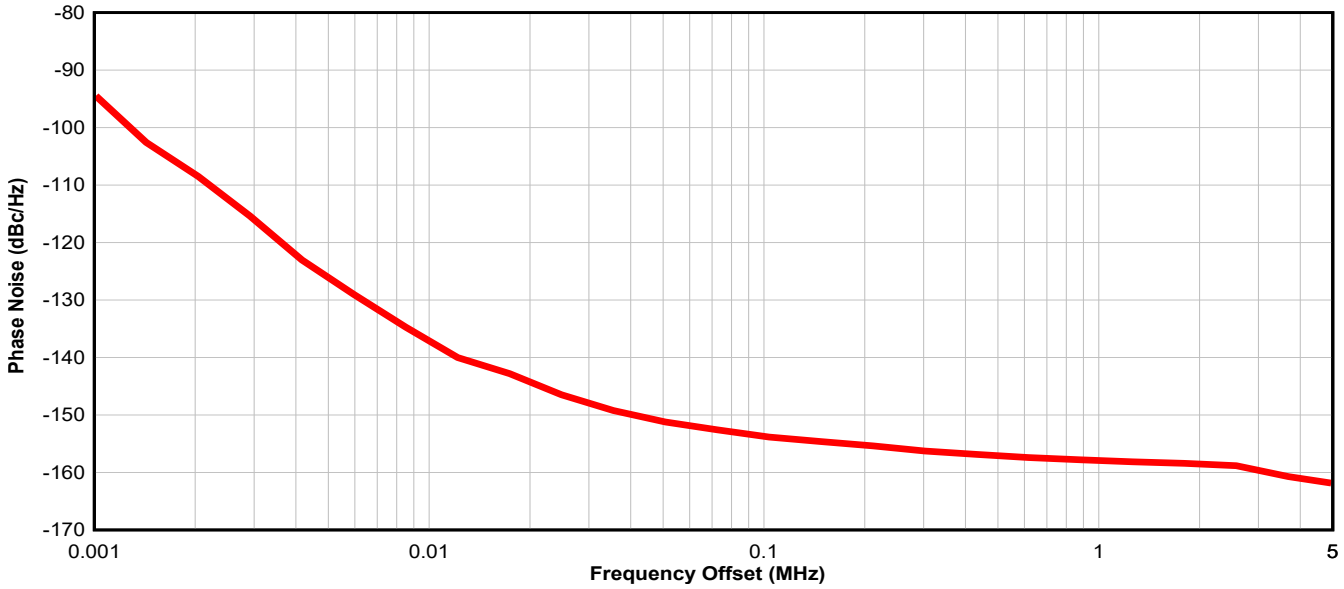


Figure 9-2. 19.2MHz LVCMOS, 25°C, 3.3V Supply

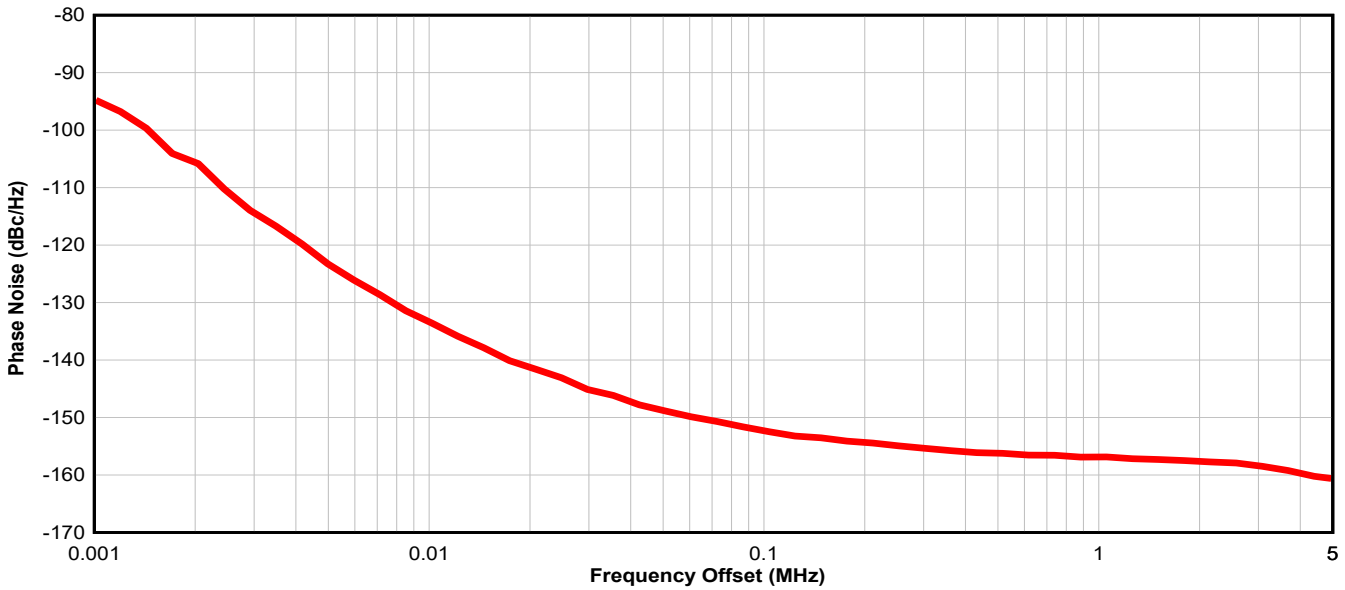


Figure 9-3. 25MHz LVCMOS, 25°C, 3.3V Supply

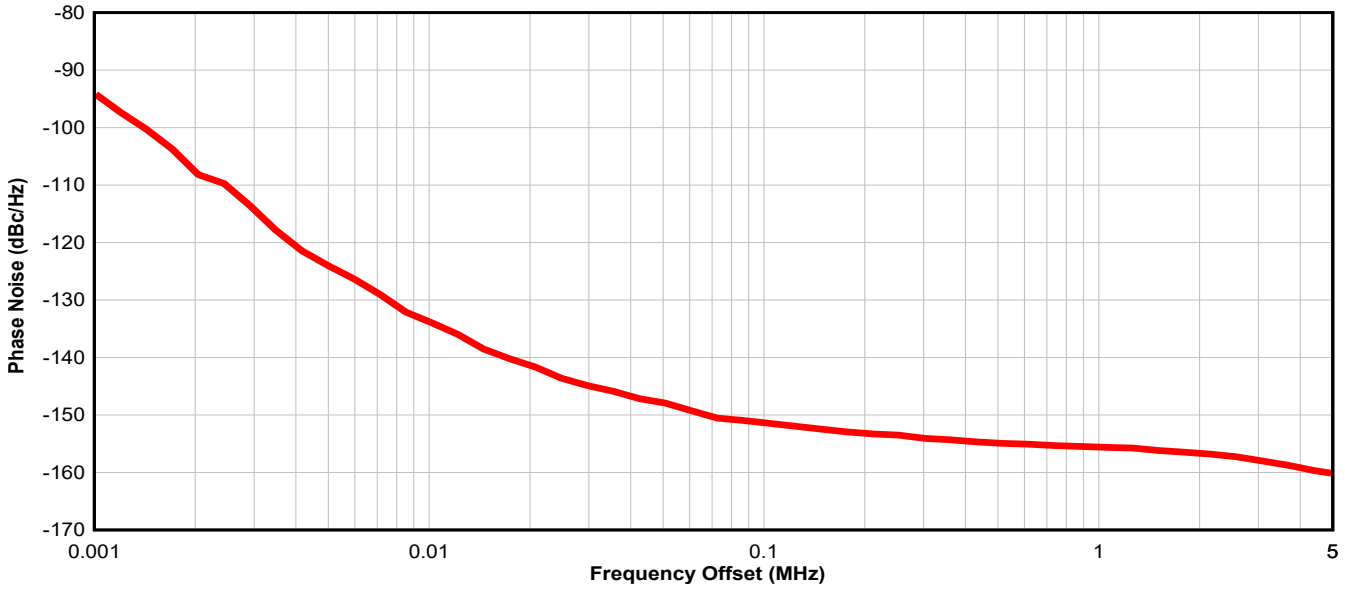


Figure 9-4. 27MHz LVCMOS, 25°C, 3.3V Supply

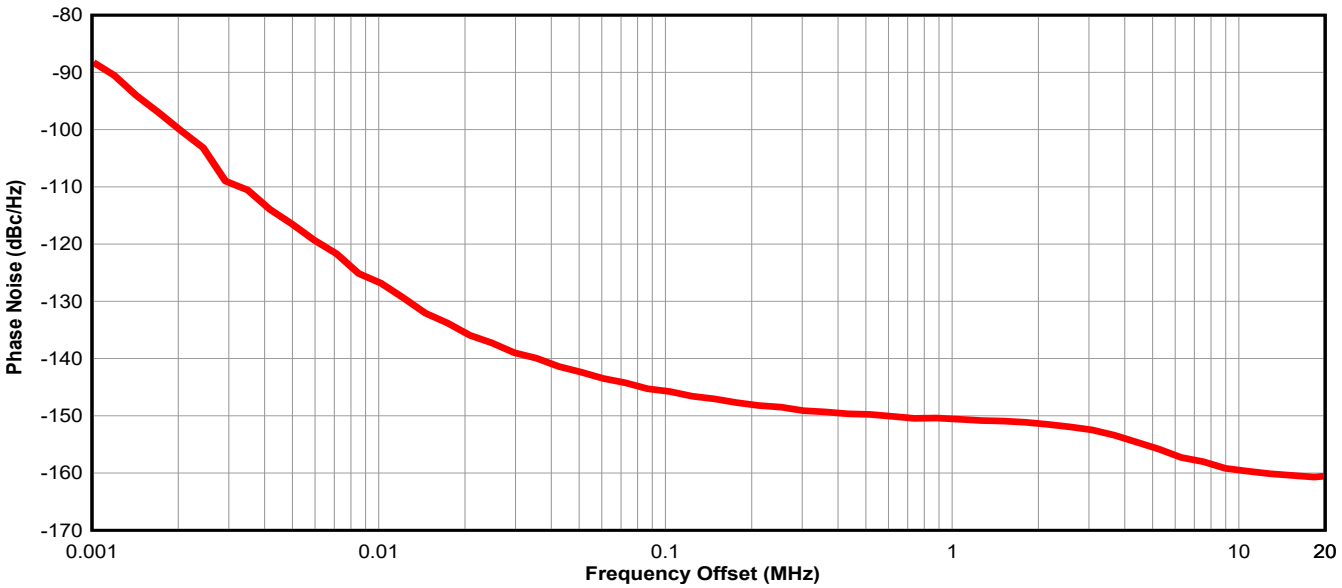


Figure 9-5. 50MHz LVCMOS, 25°C, 3.3V Supply

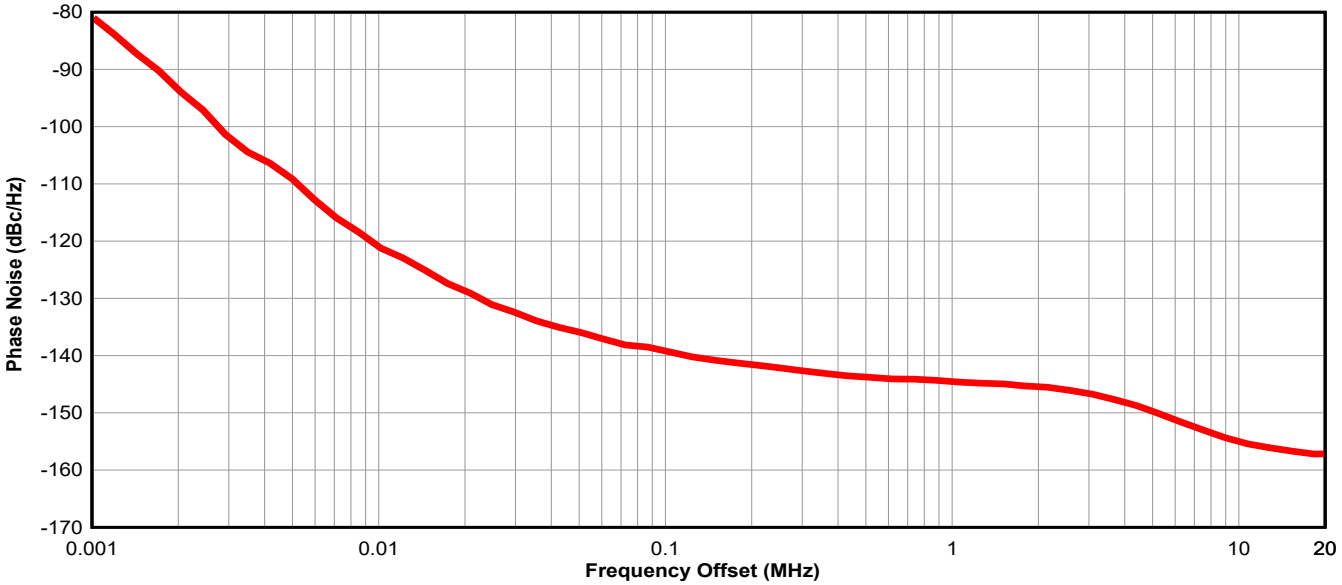


Figure 9-6. 100MHz LVCMOS, 25°C, 3.3V Supply

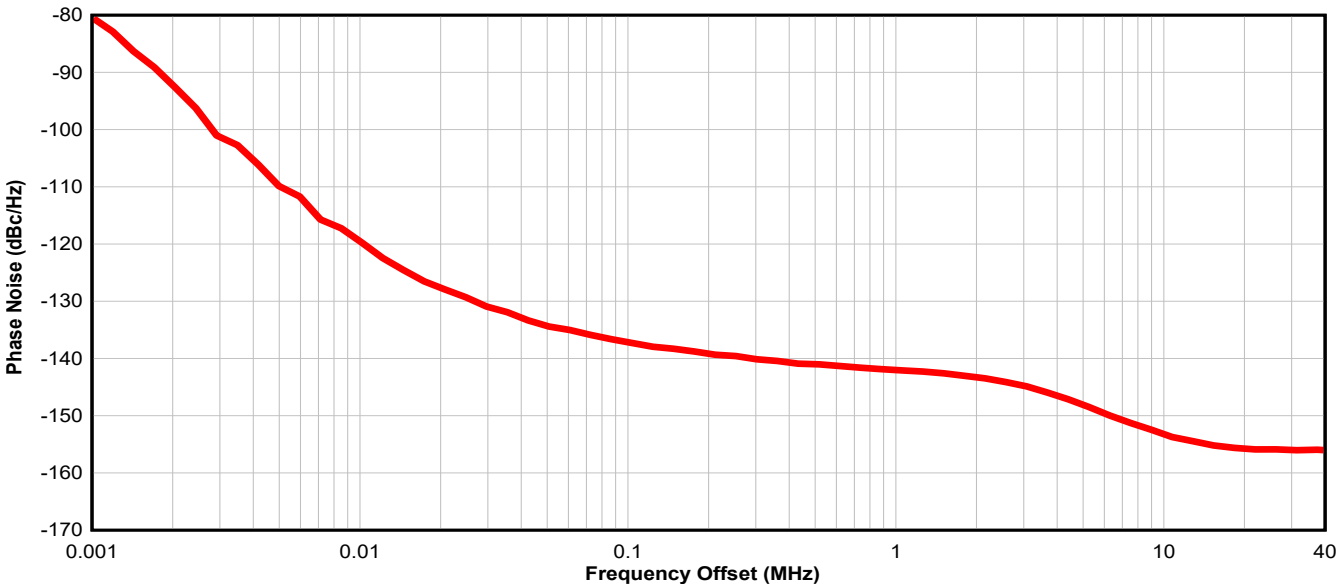


Figure 9-7. 125MHz LVCMOS, 25°C, 3.3V Supply

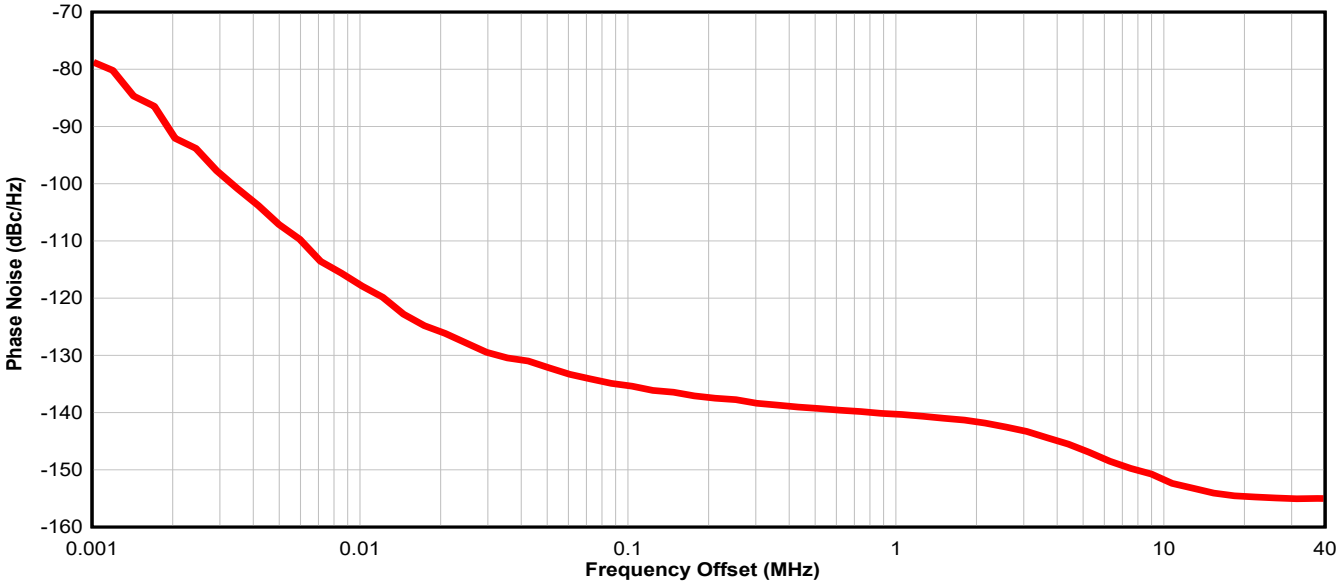


Figure 9-8. 156.25MHz LVCMOS, 25°C, 3.3V Supply

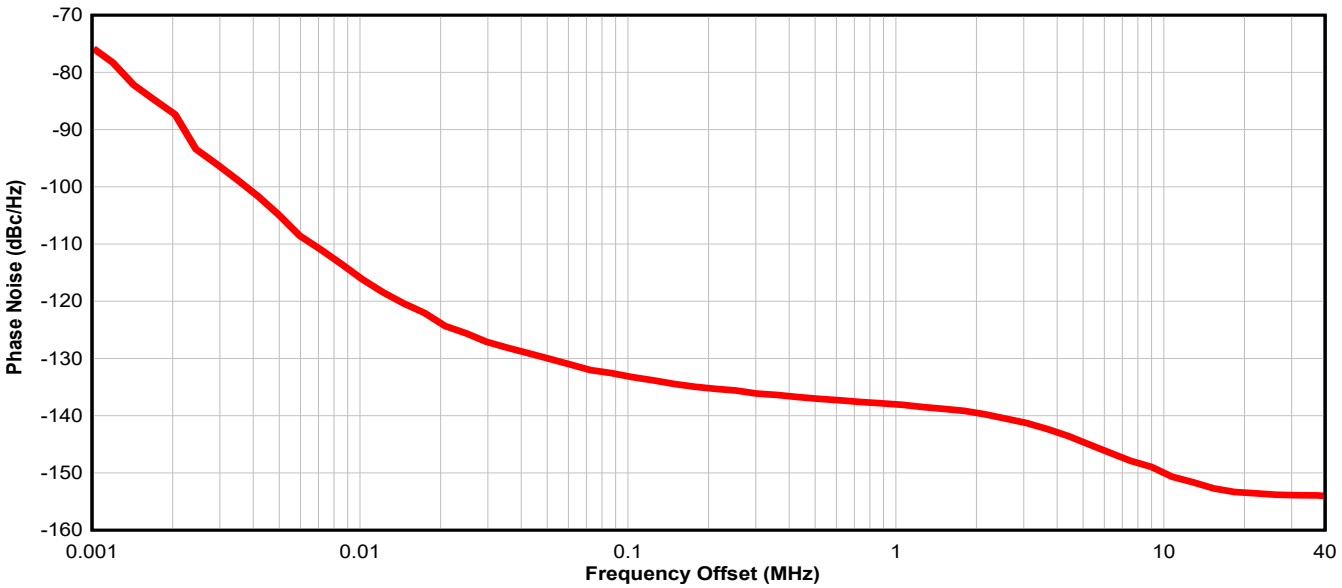


Figure 9-9. 200MHz LVCMOS, 25°C, 3.3V Supply

9.3 Power Supply Recommendations

For the best electrical performance of the CDC6Cx, TI recommends using a single 1µF power supply bypass capacitor. TI also recommends using component side mounting of the power supply bypass capacitors. 0201 or 0402 body size capacitors facilitate best signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

VDD power-up ramp time is defined as minimum time taken for power supply to exceed 95% of nominal VDD. Monotonic power supply ramp is assumed. In case the power supply falls between 1V to 1.5V after the power supply already reached >1.5V, the output is muted after power supply ramps back to >1.5V. The output clock recovers, when VDD is lowered below 1V and ramped back to >1.5V.

9.4 Layout

9.4.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power-supply bypassing when using the CDC6Cx to provide good thermal and electrical performance and signal integrity of the entire system.

9.4.1.1 Providing Thermal Reliability

The CDC6Cx is a low power, high performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

The equation below describes the relationship between the PCB temperature around the CDC6Cx and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- T_B: PCB temperature around the CDC6Cx
- T_J: Junction temperature of CDC6Cx
- Ψ_{JB}: Junction-to-board thermal resistance parameter of CDC6Cx (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- P: On-chip power dissipation of CDC6Cx

9.4.1.2 Recommended Solder Reflow Profile

TI recommends following the recommendations from the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-020E. Processing the CDC6Cx with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferable. The exact temperature profile depends on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, solder manufactures recommended profile, and capability of the reflow equipment as confirmed by the SMT assembly operation.

9.4.2 Layout Examples

Figure 9-10 shows the printed circuit board (PCB) layout examples as done on the evaluation module (EVM) for the CDC6Cx.

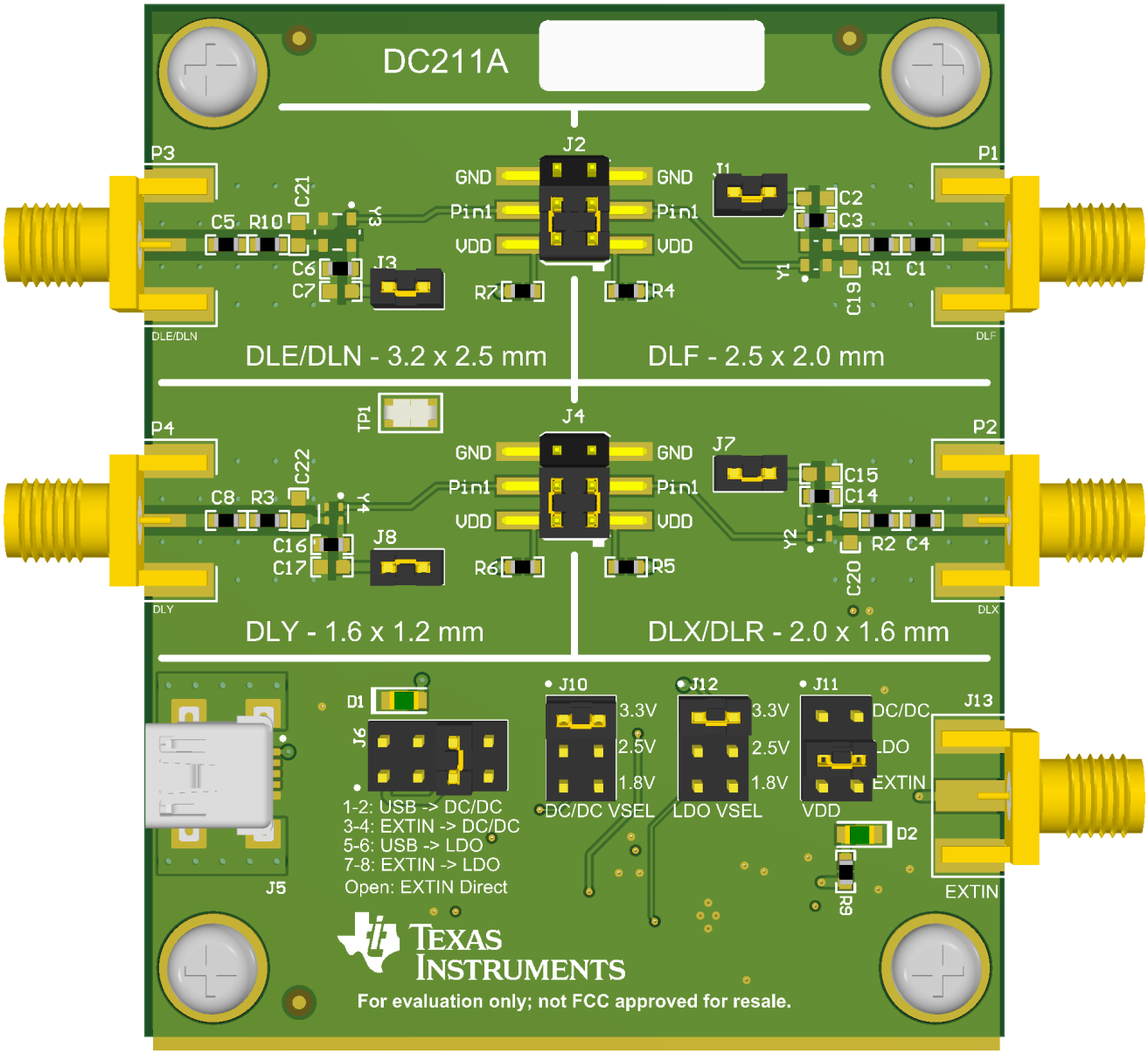


Figure 9-10. PCB Layout Example From CDC6 EVM

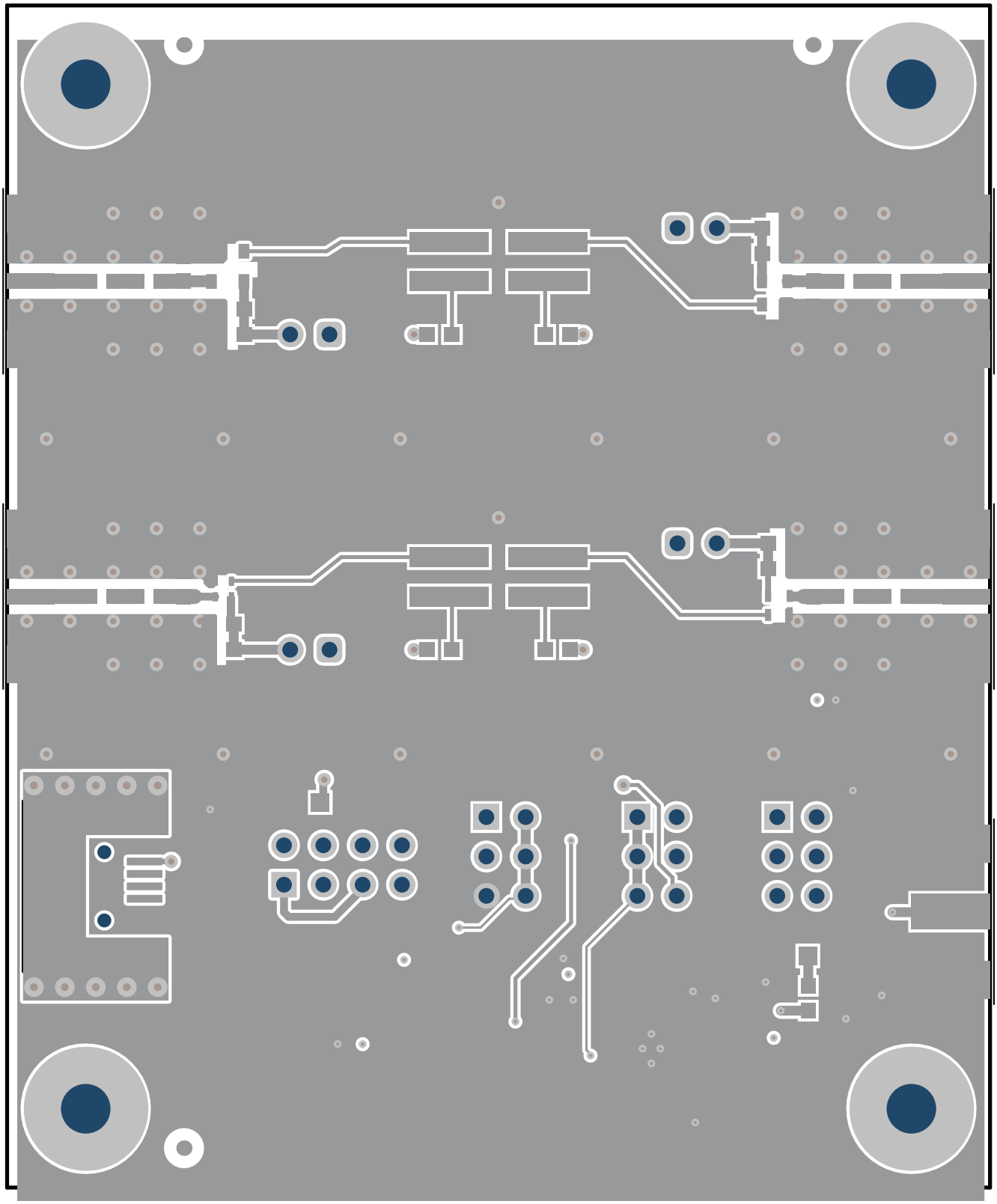


Figure 9-11. PCB Layout Example From CDC6 EVM - Top Layer

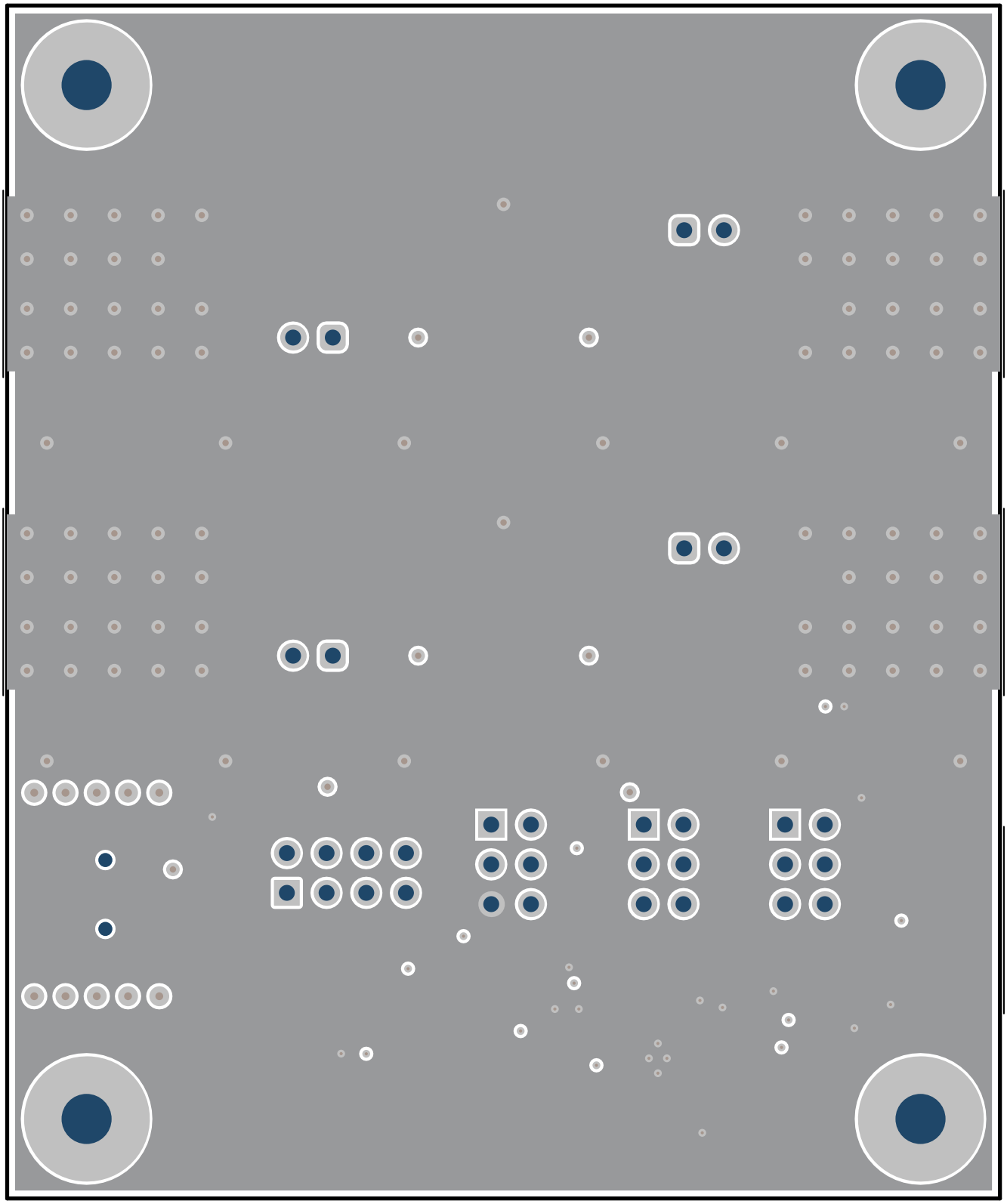


Figure 9-12. PCB Layout Example From CDC6 EVM - GND Layer

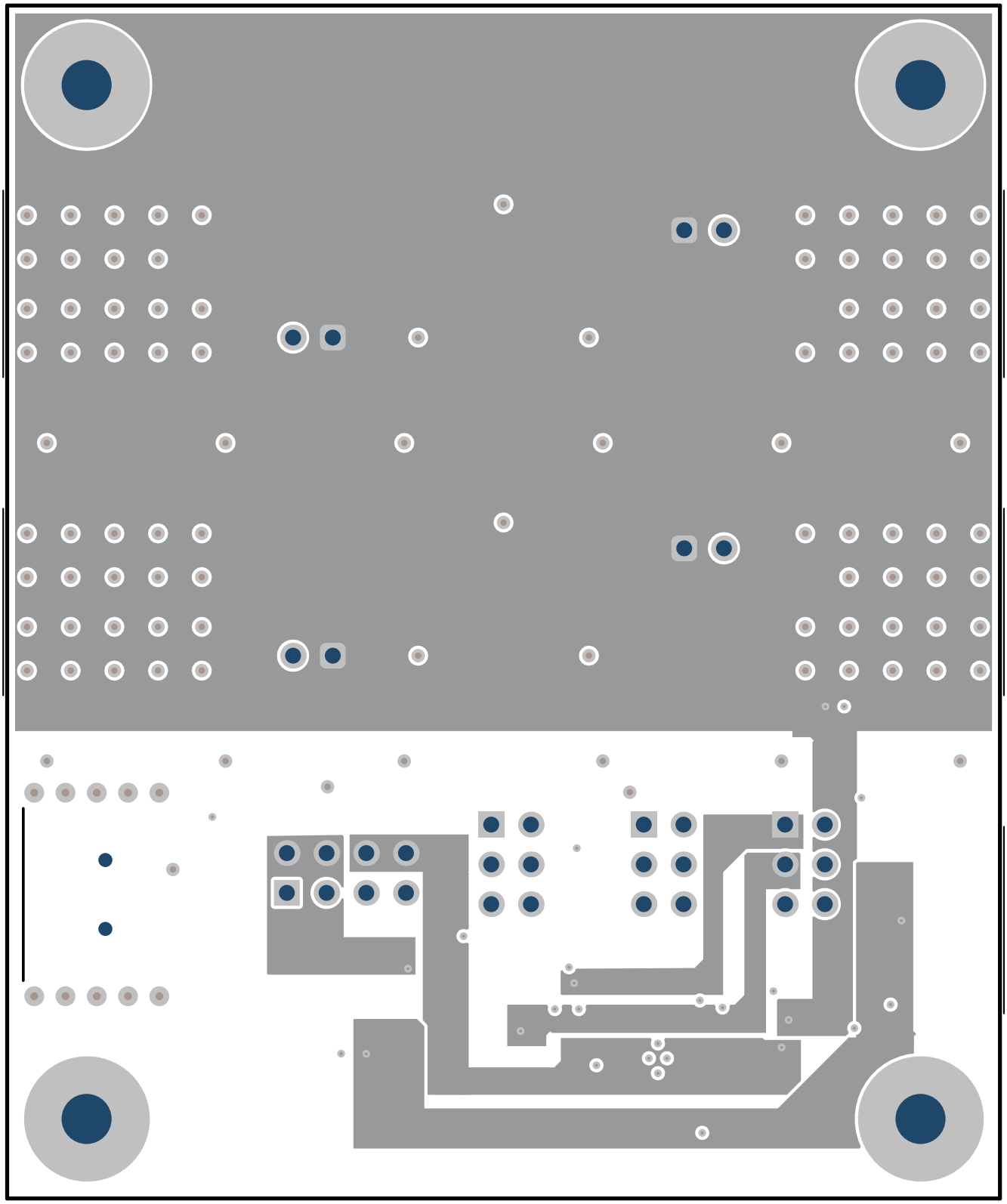


Figure 9-13. PCB Layout Example From CDC6 EVM - Power Layer

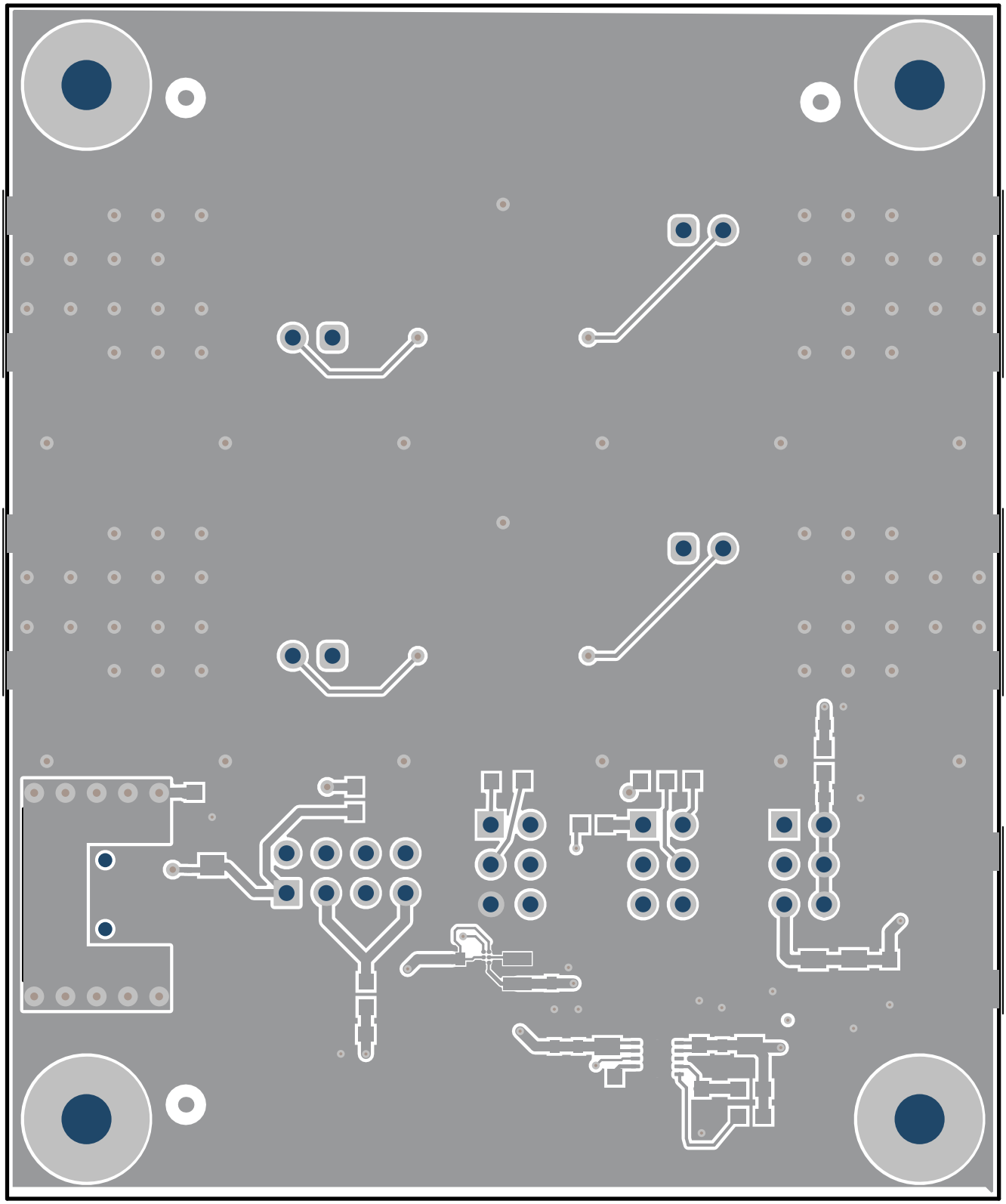


Figure 9-14. PCB Layout Example From CDC6 EVM - Bottom Layer

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CDC6CEVM User's Guide*
- Texas Instruments, *CDC6C OPN Decoder*, application note
- Texas Instruments, *Standalone BAW Oscillators Advantages Over Quartz Oscillators application note*, application note
- Texas Instruments, *BAW oscillator solutions for Building Automation*, application note
- Texas Instruments, *BAW oscillator solutions for Factory Automation*, application note
- Texas Instruments, *BAW oscillator solutions for Grid Infrastructure*, application note
- Texas Instruments, *BAW oscillator solutions for Optical Modules*, application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (January 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the device status from *Preview* to *Production*	1
• Updated the *Mechanical, Packaging, and Orderable Information* section	30

12 Mechanical, Packaging, and Orderable Information

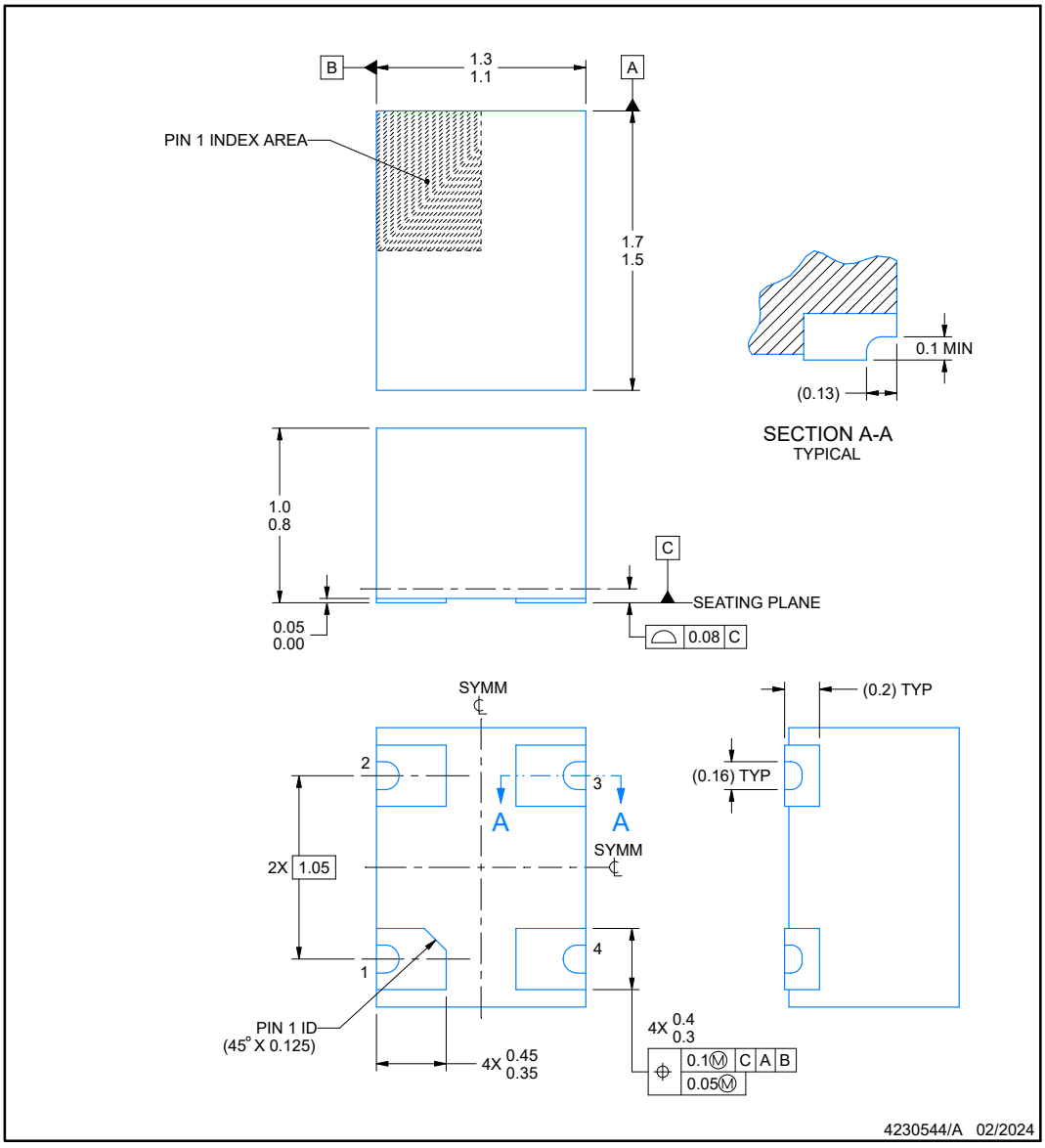
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DLY0004D

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

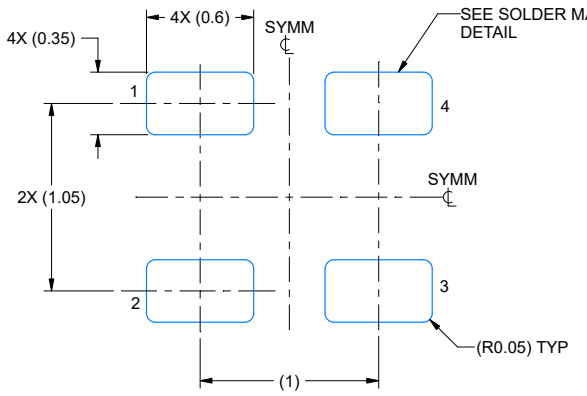
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

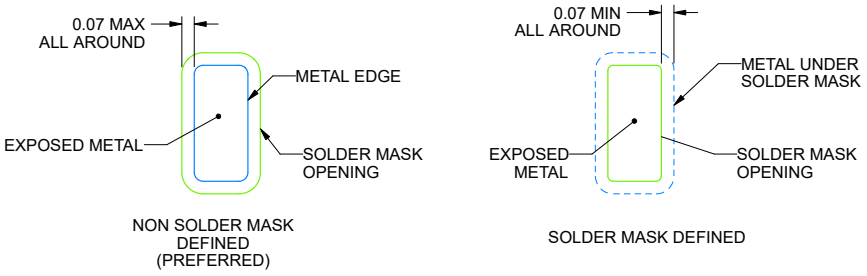
DLY0004D

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4230544/A 02/2024

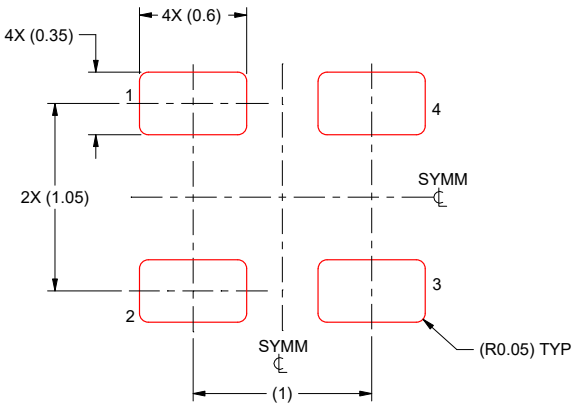
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DLY0004D — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4230544/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC6CE025000ADLER	ACTIVE	VSON	DLE	4	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	AA	Samples
CDC6CE025000ADLET	ACTIVE	VSON	DLE	4	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	AA	Samples
CDC6CE025000ADLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	AA	Samples
CDC6CE025000ADLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	AA	Samples
CDC6CE025000ADLYR	ACTIVE	VSON	DLY	4	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	AA	Samples
CDC6CE027000ADLXR	ACTIVE	VSON	DLX	4	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	JA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

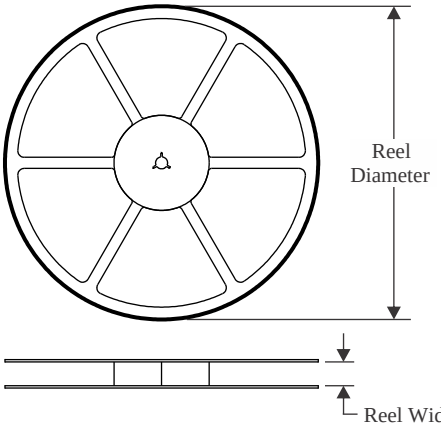
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

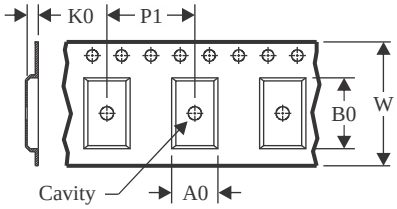
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

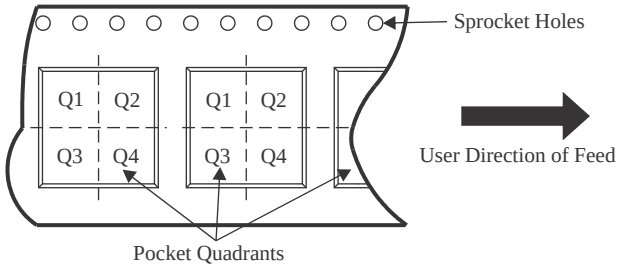


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

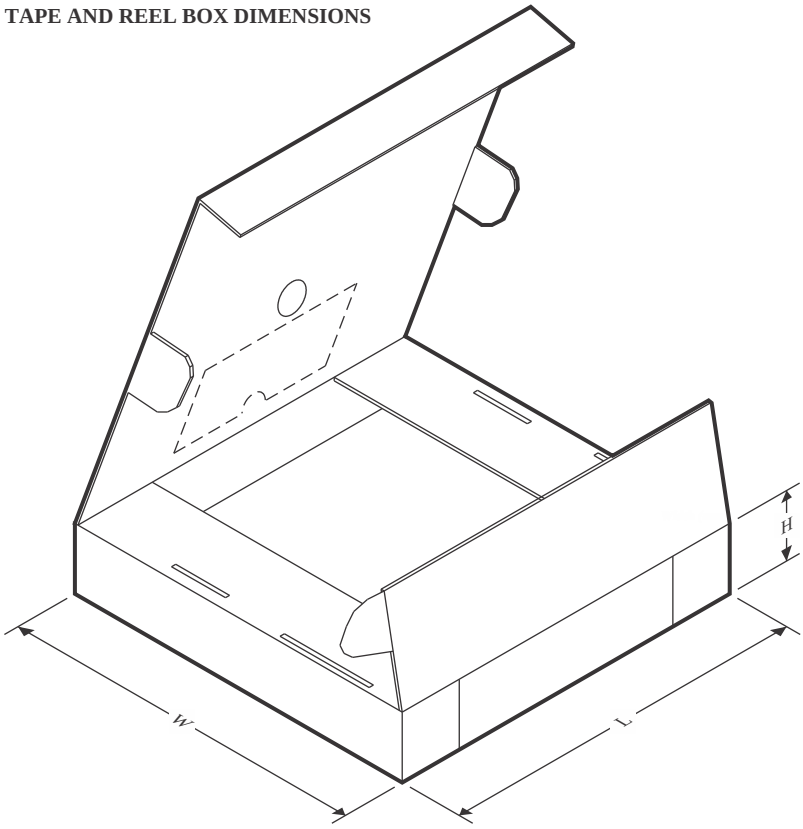
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC6CE025000ADLER	VSON	DLE	4	3000	330.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1
CDC6CE025000ADLET	VSON	DLE	4	250	180.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1
CDC6CE025000ADLFR	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6CE025000ADLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
CDC6CE025000ADLYR	VSON	DLY	4	3000	180.0	8.4	1.45	1.9	1.07	4.0	8.0	Q1
CDC6CE027000ADLXR	VSON	DLX	4	3000	180.0	8.4	1.85	2.3	1.16	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC6CE025000ADLER	VSON	DLE	4	3000	367.0	367.0	35.0
CDC6CE025000ADLET	VSON	DLE	4	250	182.0	182.0	20.0
CDC6CE025000ADLFR	VSON	DLF	4	3000	182.0	182.0	20.0
CDC6CE025000ADLFT	VSON	DLF	4	250	182.0	182.0	20.0
CDC6CE025000ADLYR	VSON	DLY	4	3000	182.0	182.0	20.0
CDC6CE027000ADLXR	VSON	DLX	4	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

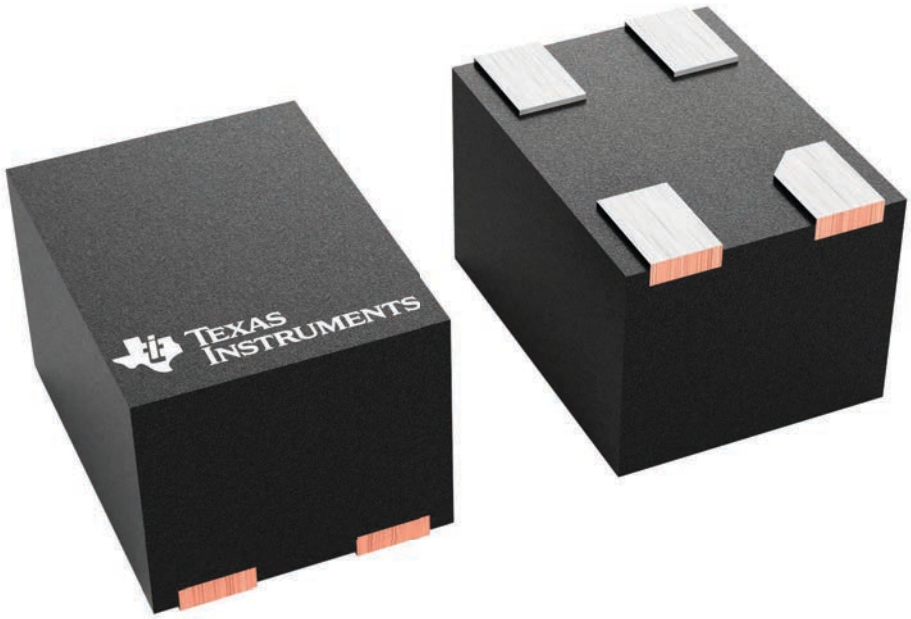
DLY 4

VSON - 1 mm max height

1.6 x 1.2, 0.7 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



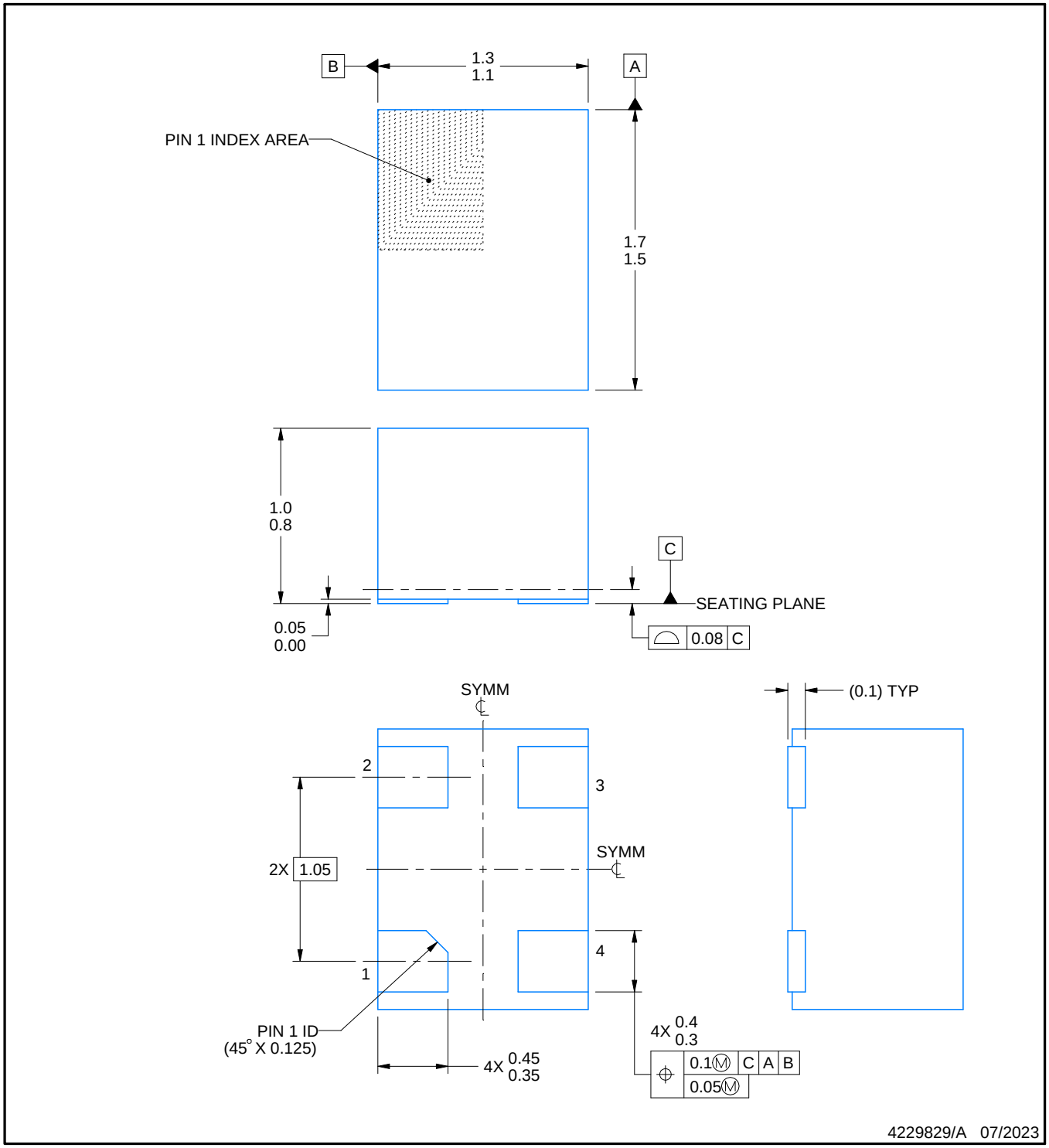
4229365/A

DLY0004C

PACKAGE OUTLINE

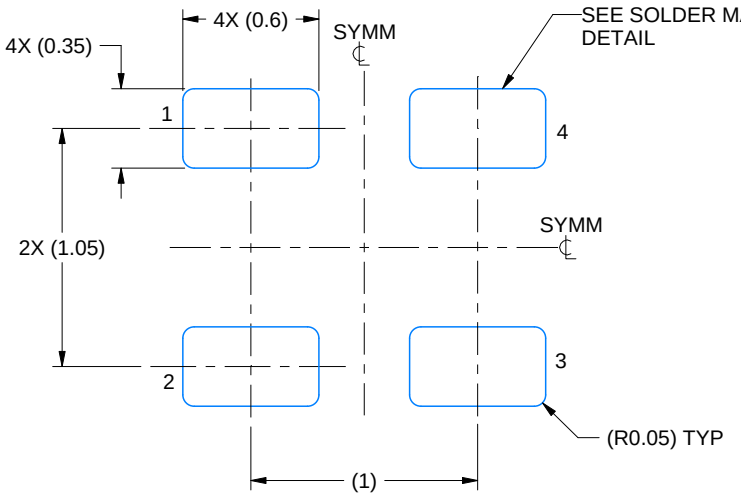
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

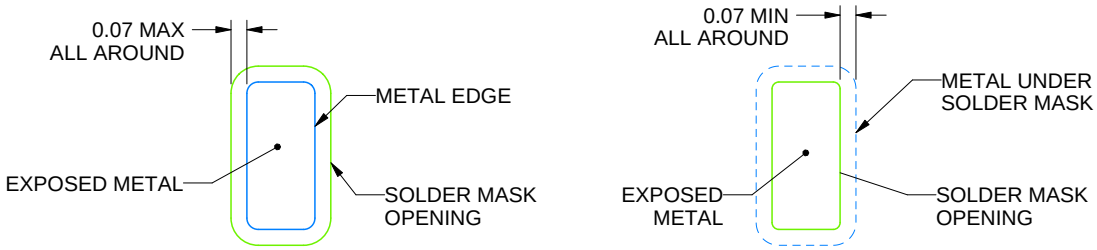


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

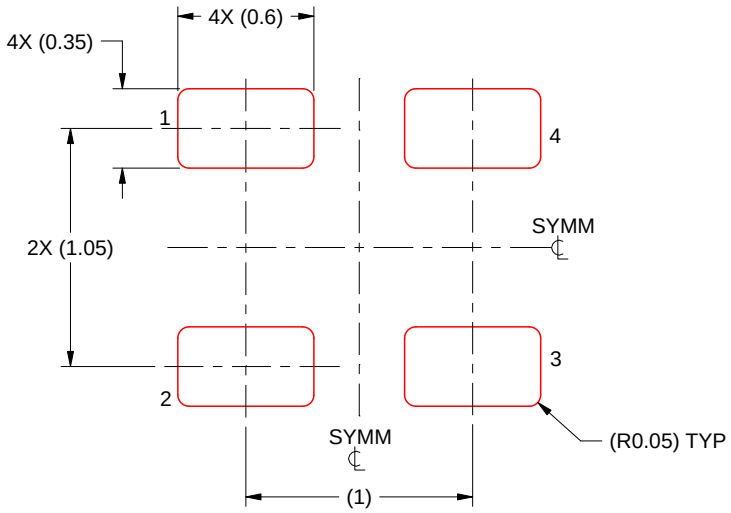


SOLDER MASK DETAILS

4229829/A 07/2023

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4229829/A 07/2023

NOTES: (continued)

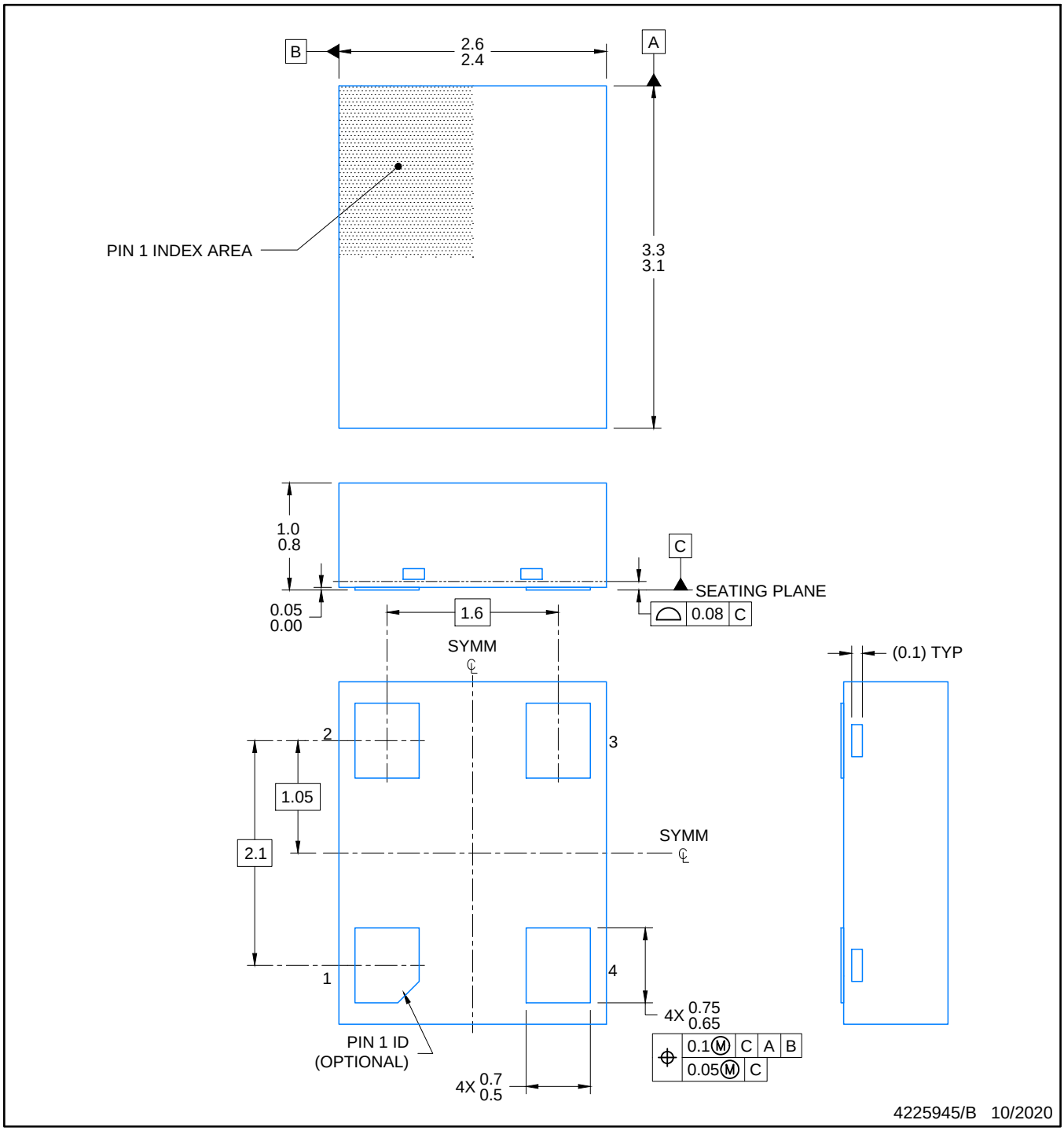
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLE0004A

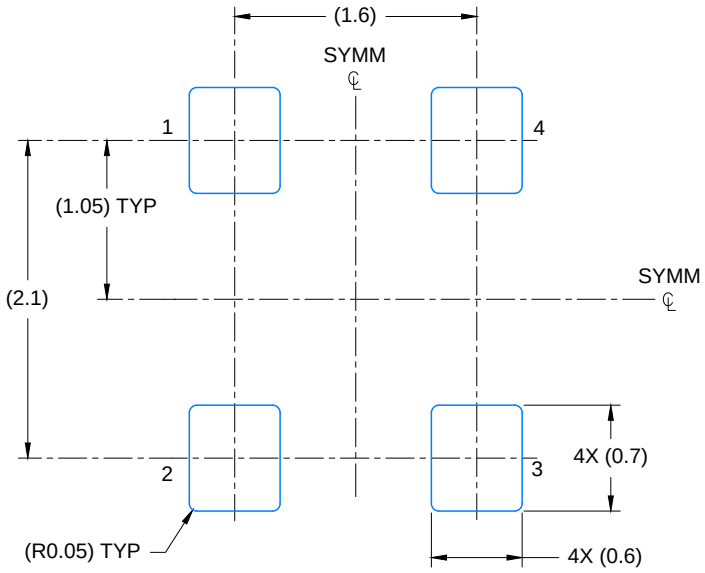
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

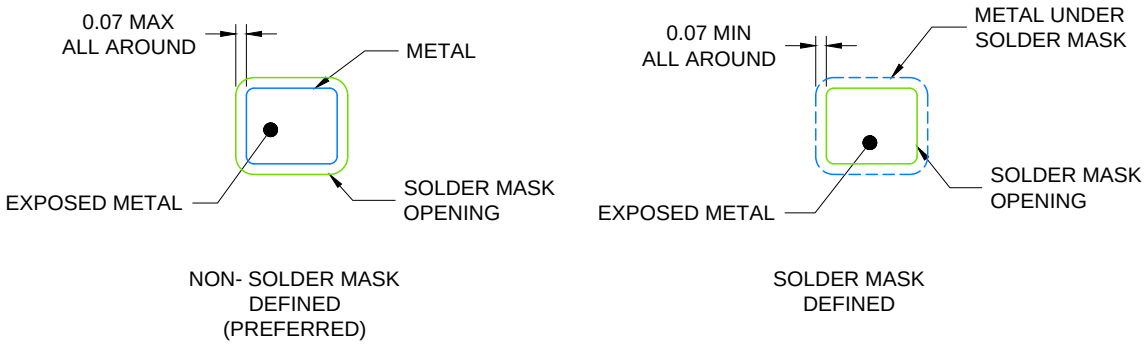


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

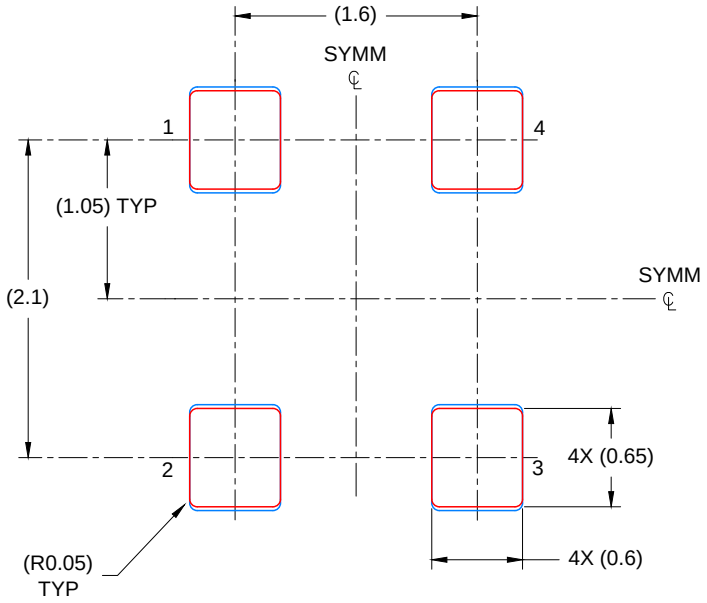


SOLDER MASK DETAILS

4225945/B 10/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 93%
SCALE: 20X

4225945/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DLF 4

VSON - 1 mm max height

2 x 2.5, 1.65 mm pitch

PLASTIC QUAD FLAT PACK-NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

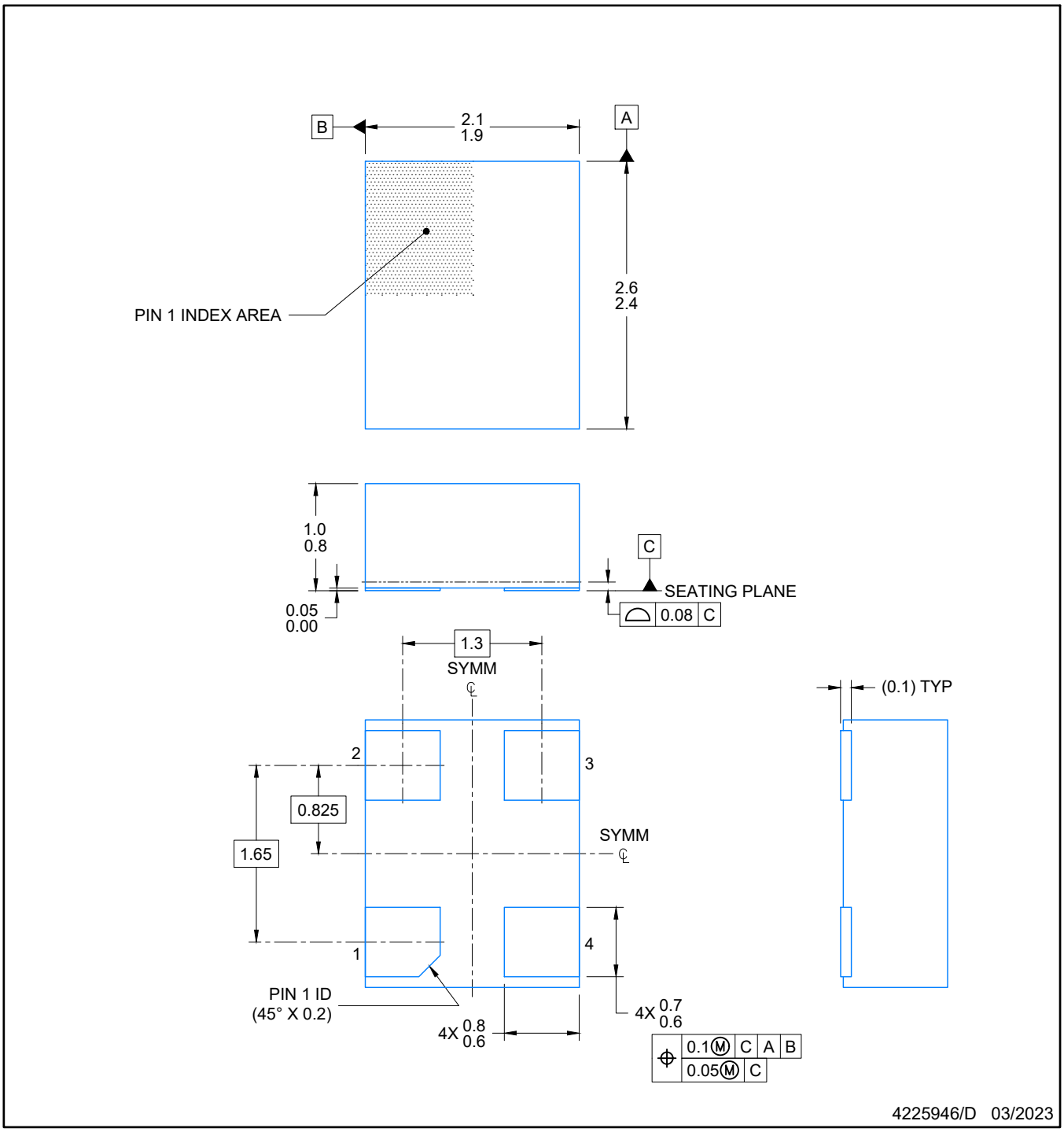
4231598/A

PACKAGE OUTLINE

DLF0004A

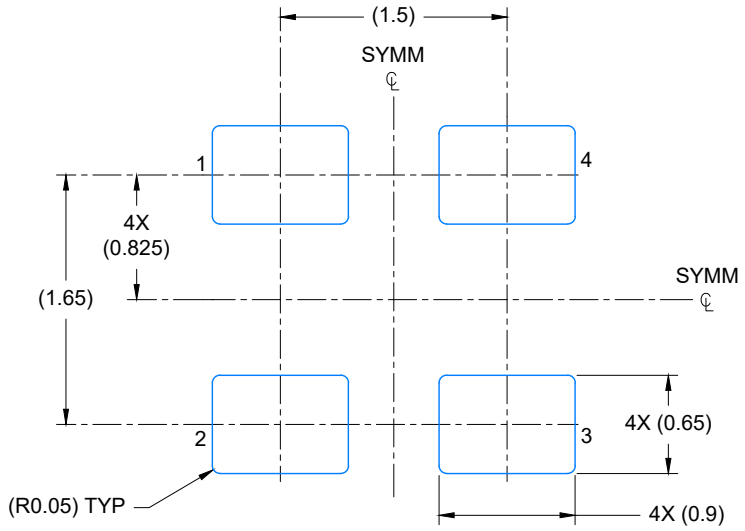
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

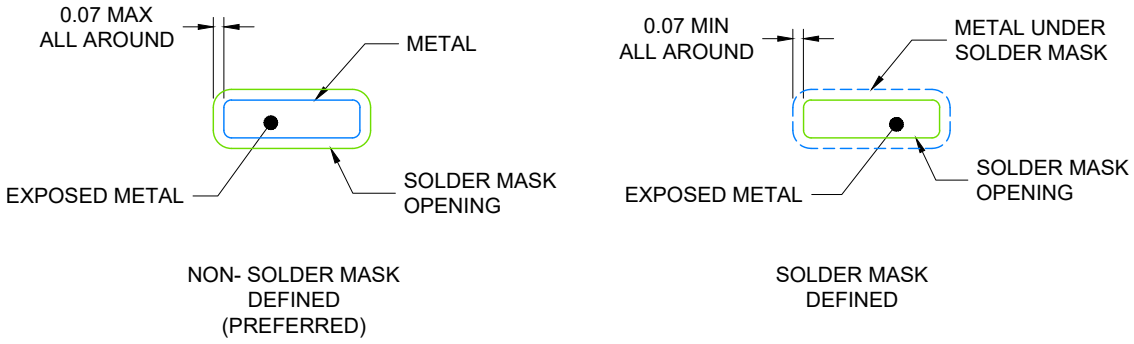


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

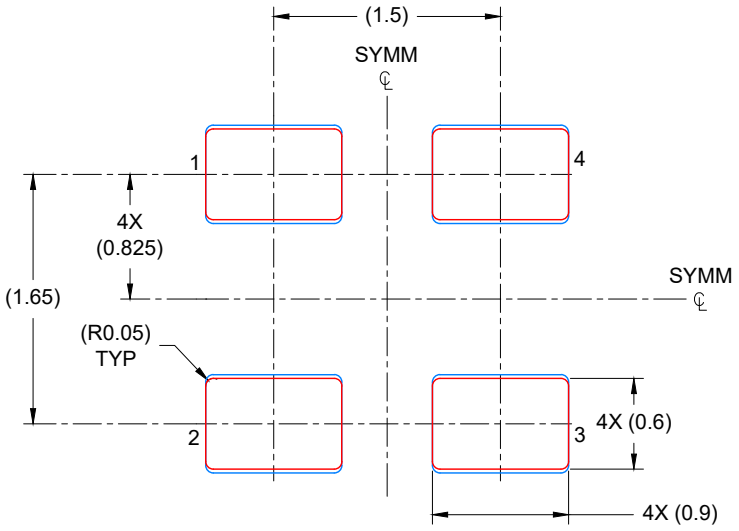


SOLDER MASK DETAILS

4225946/D 03/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4225946/D 03/2023

NOTES: (continued)

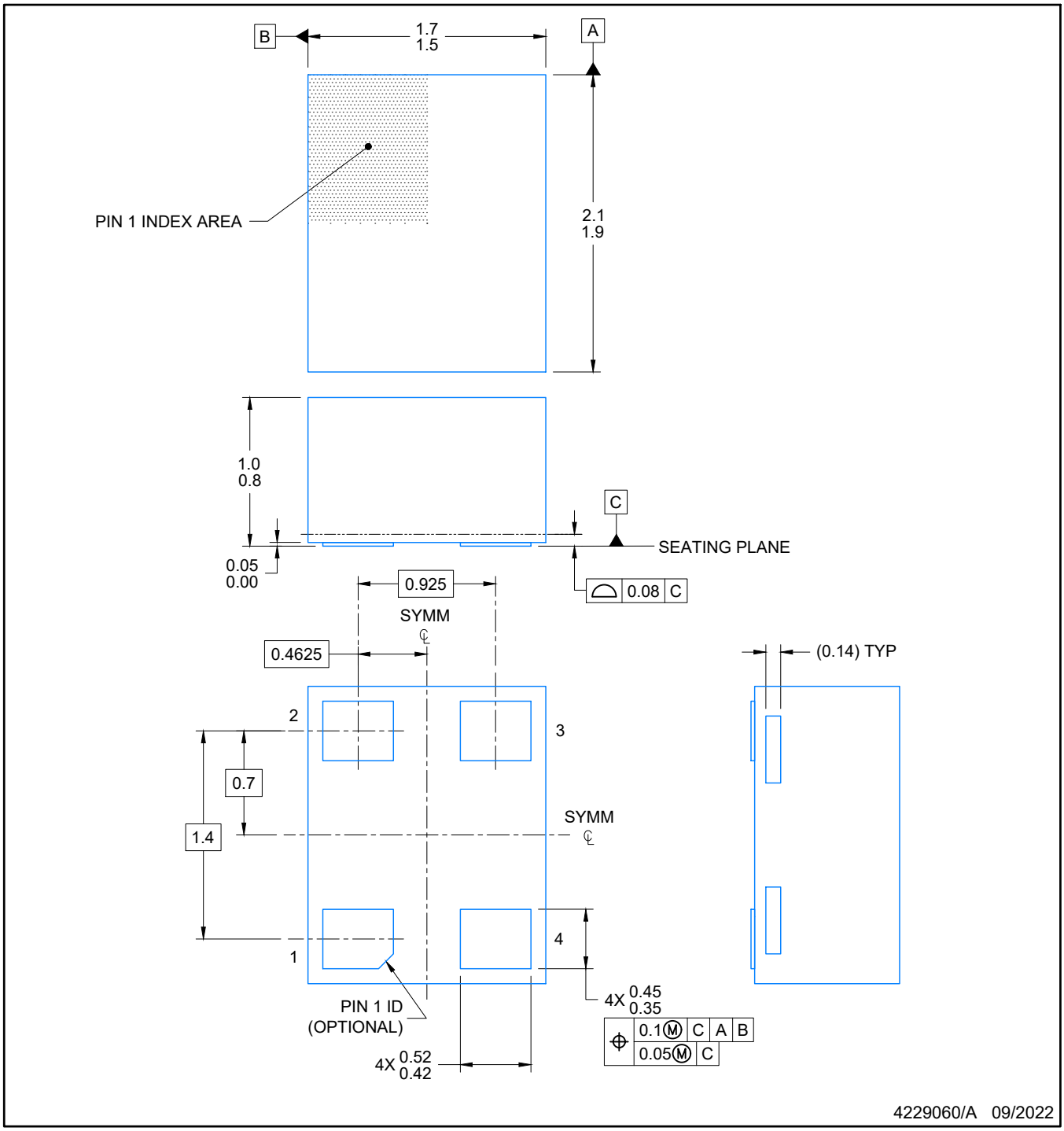
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLX0004A

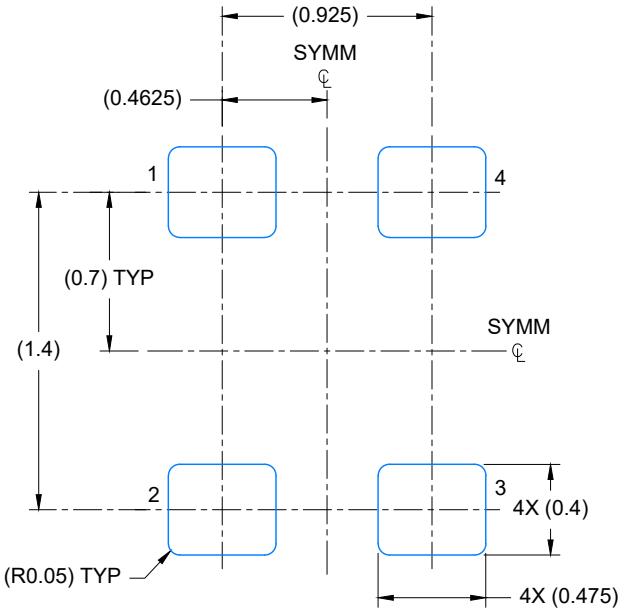
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

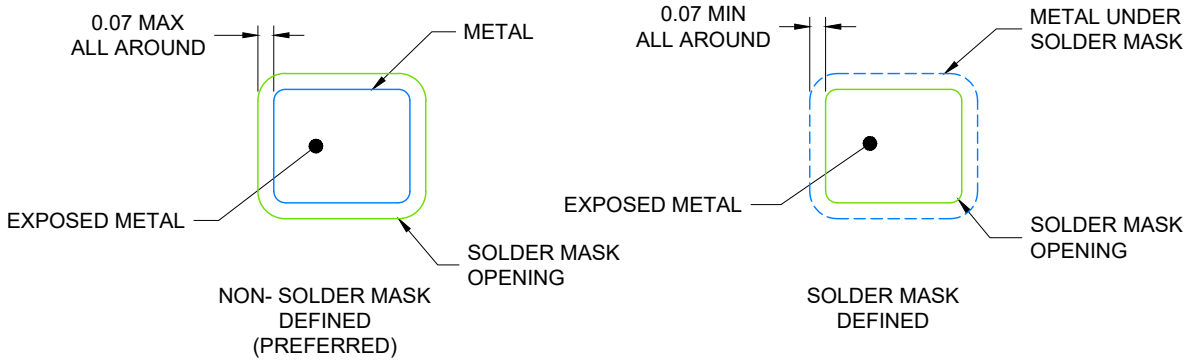


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

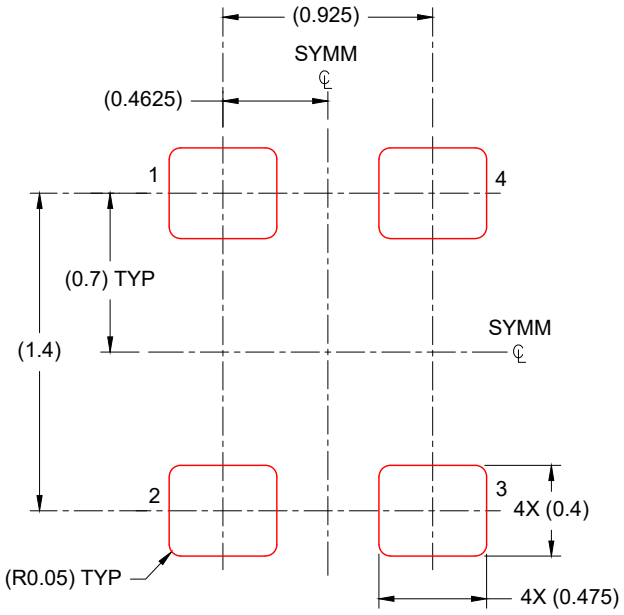


SOLDER MASK DETAILS

4229060/A 09/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4229060/A 09/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265