

## CC113L Value Line Receiver

### 1 Device Overview

#### 1.1 Features

- **RF Performance**
  - Receive Sensitivity Down to  $-116$  dBm at 0.6 kbps
  - Programmable Data Rate from 0.6 to 600 kbps
  - Frequency Bands: 300–348 MHz, 387–464 MHz, and 779–928 MHz
  - 2-FSK, 4-FSK, GFSK, MSK, and OOK Supported
- **Digital Features**
  - Flexible Support for Packet Oriented Systems
  - On-chip Support for Sync Word Detection, Flexible Packet Length, and Automatic CRC Calculation
- **Low-Power Features**
  - 200-nA Sleep Mode Current Consumption
  - Fast Startup Time; 240  $\mu$ s From Sleep to RX Mode
  - 64-Byte RX FIFO
- **General**
  - Few External Components; Completely On-chip Frequency Synthesizer, No External Filters or RF Switch Needed
  - Green Package: RoHS Compliant and No Antimony or Bromine
  - Small Size (QLP 4- x 4-mm Package, 20 Pins)
  - Suited for Systems Targeting Compliance with EN 300 220 (Europe) and FCC CFR Part 15 (US)
  - Support for Asynchronous and Synchronous Serial Transmit Mode for Backward Compatibility with Existing Radio Communication Protocols

#### 1.2 Applications

- Ultra Low-Power Wireless Applications Operating in the 315-, 433-, 868-, 915-MHz ISM or SRD Bands
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Remote Controls
- Toys
- Home and Building Automation

#### 1.3 Description

The CC113L is a cost optimized sub-1 GHz RF receiver for the 300–348 MHz, 387–464 MHz, and 779–928 MHz frequency bands. The circuit is based on the popular CC1101 RF transceiver, and RF performance characteristics are identical. The CC115L transmitter together with the CC113L receiver enable a low-cost RF link.

The RF receiver is integrated with a highly configurable baseband demodulator. The modem supports various modulation formats and has a configurable data rate up to 600 kbps.

The CC113L provides extensive hardware support for packet handling, data buffering, and burst transmissions.

The main operating parameters and the 64-byte receive FIFO of CC113L can be controlled through a serial peripheral interface (SPI). In a typical system, the CC113L will be used together with a microcontroller and a few additional passive components.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE
CC113LRGP	QFN (20)	4.00 mm x 4.00 mm

(1) For more information on these devices, see [Section 8](#), Mechanical Packaging and Orderable Information.



### 1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the device.

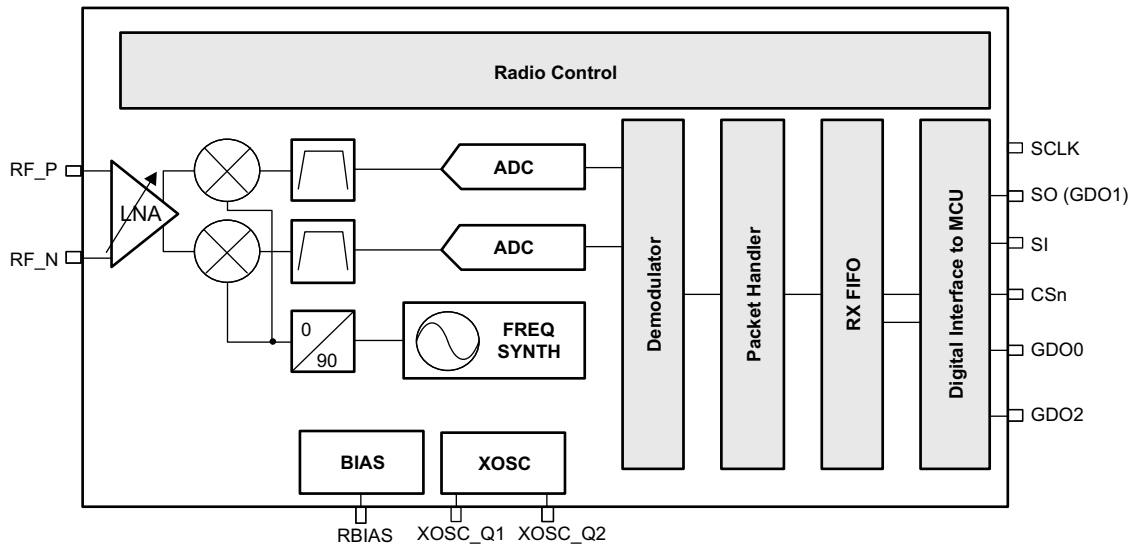


Figure 1-1. Functional Block Diagram

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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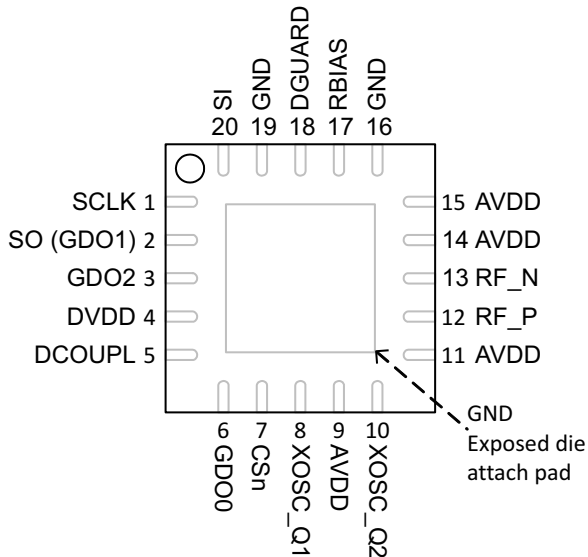
Changes from Revision A (February 2013) to Revision B	Page
• Changed format of data sheet to standard TI format. ....	<a href="#">1</a>
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### 3 Terminal Configuration and Functions

#### 3.1 Pin Diagram

The CC113L pinout is shown in [Figure 3-1](#) and [Table 3-1](#). See [Section 5.18](#) for details on the I/O configuration.



**Figure 3-1. Pinout Top View**

**NOTE**

The exposed die attach pad must be connected to a solid ground plane as this is the main ground connection for the chip

## 3.2 Signal Descriptions

**Table 3-1. Signal Descriptions**

Pin No.	Pin Name	Pin Type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: <ul style="list-style-type: none"> <li>• Test signals</li> <li>• FIFO status signals</li> <li>• Clock output, down-divided from XOSC</li> <li>• Serial output RX data</li> </ul>
4	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/Os and for the digital core voltage regulator
5	DCOUPPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling  NOTE: This pin is intended for use with the CC113L only. It can not be used to provide supply voltage to other devices
6	GDO0	Digital I/O	Digital output pin for general use: <ul style="list-style-type: none"> <li>• Test signals</li> <li>• FIFO status signals</li> <li>• Clock output, down-divided from XOSC</li> <li>• Serial output RX data</li> </ul>
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode
14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

## 4 Specifications

### 4.1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	-0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	-0.3	VDD + 0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N, DCOUPL, RBIAS	-0.3	2.0	V	
Voltage ramp-up rate		120	kV/ $\mu$ s	
Input RF level		+10	dBm	

### 4.2 Handling Ratings

Parameter		MIN	MAX	UNIT
Storage temperature range, T <sub>stg</sub>	(default)	-50	150	°C
ESD Stress Voltage, V <sub>ESD</sub>	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001 <sup>(1)</sup>		750	V
	Charged Device Model (CDM), per JESD22-C101 <sup>(2)</sup>		400	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

Parameter	Min	Max	Unit	Condition
Operating temperature	-40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

### 4.4 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency range	300		348	MHz	
	387		464	MHz	If using a 27 MHz crystal, the lower frequency limit for this band is 392 MHz
	779		928	MHz	
Data rate	0.6		500	kBaud	2-FSK
	0.6		250	kBaud	GFSK and OOK
	0.6		300	kBaud	4-FSK (the data rate in kbps will be twice the baud rate) Optional Manchester encoding (the data rate in kbps will be half the baud rate)

## 4.5 Current Consumption

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  if nothing else stated. All measurement results are obtained using [SWRR046](#) and [SWRR045](#). Reduced current settings, [MDMCFG2.DEM\\_DCFILT\\_OFF=1](#), gives a slightly lower current consumption at the cost of a reduction in sensitivity. See [Section 4.6](#) for additional details on current consumption and sensitivity.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		0.2	1	$\mu\text{A}$	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
		100		$\mu\text{A}$	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with <a href="#">MCSM0.OSC_FORCE_ON</a> set)
		165		$\mu\text{A}$	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		1.7		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		8.4		mA	The current consumption for the intermediate states when going from IDLE to RX, including the calibration state
Current consumption, 315 MHz		15.4		mA	Receive mode, 1.2 kBaud, reduced current, input at sensitivity limit
		14.4		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.2		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		14.3		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		16.5		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
Current consumption, 433 MHz		16.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.7		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		17.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.7		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
Current consumption, 868/915 MHz		15.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.
		14.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.
		14.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.
		16.9		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See <a href="#">Figure 4-1</a> through <a href="#">Figure 4-3</a> for current consumption with register settings optimized for sensitivity.

### 4.5.1 Typical RX Current Consumption over Temperature and Input Power Level, 868/915 MHz

See [Section 4.12.1](#).



## 4.6 RF Receive Section

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  if nothing else stated. All measurement results are obtained using [SWRR046](#) and [SWRR045](#).

Parameter	Min	Typ	Max	Unit	Condition
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
Spurious emissions		-68	-57	dBm	25 MHz - 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit)
		-66	-47	dBm	Above 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit) Typical radiated spurious emission is -49 dBm measured at the VCO frequency
RX latency		9		bit	Serial operation. Time from start of reception until data is available on the receiver data output pin is equal to 9 bit
<b>315 MHz</b>					
1.2 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (2-FSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-111		dBm	Sensitivity can be traded for current consumption by setting <a href="#">MDMCFG2.DEM_DCFILT_OFF=1</a> . The typical current consumption is then reduced from 17.2 mA to 15.4 mA at the sensitivity limit. The sensitivity is typically reduced to -109 dBm
<b>433 MHz</b>					
0.6 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 14.3 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-116		dBm	
1.2 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-112		dBm	Sensitivity can be traded for current consumption by setting <a href="#">MDMCFG2.DEM_DCFILT_OFF=1</a> . The typical current consumption is then reduced from 18.0 mA to 16.0 mA at the sensitivity limit. The sensitivity is typically reduced to -110 dBm
38.4 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		-104		dBm	
250 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		-95		dBm	
<b>868/915 MHz</b>					
1.2 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-112		dBm	Sensitivity can be traded for current consumption by setting <a href="#">MDMCFG2.DEM_DCFILT_OFF=1</a> . The typical current consumption is then reduced from 17.7 mA to 15.7 mA at sensitivity limit. The sensitivity is typically reduced to -109 dBm
Saturation		-14		dBm	<a href="#">FIFOTHR.CLOSE_IN_RX=0</a> . See more in DN010 <a href="#">SWRA147</a>
Adjacent channel rejection ±100 kHz offset		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing See <a href="#">Figure 4-4</a> and <a href="#">Figure 4-5</a> for selectivity performance at other offset frequencies
Image channel rejection		31		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset		-50		dBm	Desired channel 3 dB above the sensitivity limit See <a href="#">Figure 4-4</a> and <a href="#">Figure 4-5</a> for blocking performance at other offset frequencies
±10 MHz offset		-40		dBm	

Parameter	Min	Typ	Max	Unit	Condition
38.4 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		-104		dBm	Sensitivity can be traded for current consumption by setting <a href="#">MDMCFG2.DEM_DCFILT_OFF=1</a> . The typical current consumption is then reduced from 17.7 mA to 15.6 mA at the sensitivity limit. The sensitivity is typically reduced to -102 dBm
Saturation		-16		dBm	<a href="#">FIFOTHR.CLOSE_IN_RX=0</a> . See more in DN010 <a href="#">SWRA147</a>
Adjacent channel rejection -200 kHz offset +200 kHz offset		12 25		dB dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing See <a href="#">Figure 4-6</a> and <a href="#">Figure 4-7</a> for blocking performance at other offset frequencies
Image channel rejection		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking $\pm 2$ MHz offset $\pm 10$ MHz offset		-50 -40		dBm dBm	Desired channel 3 dB above the sensitivity limit See <a href="#">Figure 4-6</a> and <a href="#">Figure 4-7</a> for blocking performance at other offset frequencies
250 kBaud data rate, sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		-95		dBm	Sensitivity can be traded for current consumption by setting <a href="#">MDMCFG2.DEM_DCFILT_OFF=1</a> . The typical current consumption is then reduced from 18.9 mA to 16.9 mA at the sensitivity limit. The sensitivity is typically reduced to -91 dBm
Saturation		-17		dBm	<a href="#">FIFOTHR.CLOSE_IN_RX=0</a> . See more in DN010 <a href="#">SWRA147</a>
Adjacent channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 750-kHz channel spacing See <a href="#">Figure 4-8</a> and <a href="#">Figure 4-9</a> for blocking performance at other offset frequencies
Image channel rejection		14		dB	IF frequency 304 kHz Desired channel 3 dB above the sensitivity limit
Blocking $\pm 2$ MHz offset $\pm 10$ MHz offset		-50 -40		dBm dBm	Desired channel 3 dB above the sensitivity limit See <a href="#">Figure 4-8</a> and <a href="#">Figure 4-9</a> for blocking performance at other offset frequencies
4-FSK, 125 kBaud data rate (250 kbps), sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (1% packet error rate, 20 bytes packet length, 127 kHz deviation, 406 kHz digital channel filter bandwidth)					
Receiver sensitivity		-96		dBm	
4-FSK, 250 kBaud data rate (500 kbps), sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (1% packet error rate, 20 bytes packet length, 254 kHz deviation, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-91		dBm	
4-FSK, 300 kBaud data rate (600 kbps), sensitivity optimized, <a href="#">MDMCFG2.DEM_DCFILT_OFF=0</a> (1% packet error rate, 20 bytes packet length, 228 kHz deviation, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-89		dBm	

#### 4.6.1 Typical Sensitivity over Temperature and Supply Voltage, 868 MHz, Sensitivity Optimized Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
	–40	25	85	–40	25	85	–40	25	85
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–105	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–96	–92	–97	–95	–92	–97	–94	–92
Sensitivity [dBm] 500 kBaud	–91	–90	–86	–91	–90	–86	–91	–90	–86

#### 4.6.2 Typical Sensitivity over Temperature and Supply Voltage, 915 MHz, Sensitivity Optimized Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
	–40	25	85	–40	25	85	–40	25	85
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–104	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–94	–92	–97	–95	–92	–97	–95	–92
Sensitivity [dBm] 500 kBaud	–91	–89	–86	–91	–90	–86	–91	–89	–86

#### 4.6.3 Blocking and Selectivity

See [Section 4.12.2](#).

#### 4.7 Crystal Oscillator

T<sub>A</sub> = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using [SWRR046](#) and [SWRR045](#).

Parameter	Min	Typ	Max	Unit	Condition
Crystal frequency	26	26	27	MHz	For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26-MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		μs	This parameter is to a large degree crystal dependent. Measured on <a href="#">SWRR046</a> and <a href="#">SWRR045</a> using crystal AT-41CD2 from NDK

## 4.8 Frequency Synthesizer Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  if nothing else is stated. All measurement results are obtained using [SWRR046](#) and [SWRR045](#). Min figures are given using a 27-MHz crystal. Typ and max figures are given using a 26-MHz crystal.

Parameter	Min	Typ	Max	Unit	Condition
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26- to 27-MHz crystal. The resolution (in Hz) is equal for all frequency bands
Synthesizer frequency tolerance		$\pm 40$		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing
RF carrier phase noise		-92		dBc/Hz	at 50 kHz offset from carrier
RF carrier phase noise		-92		dBc/Hz	at 100 kHz offset from carrier
RF carrier phase noise		-92		dBc/Hz	at 200 kHz offset from carrier
RF carrier phase noise		-98		dBc/Hz	at 500 kHz offset from carrier
RF carrier phase noise		-107		dBc/Hz	at 1 MHz offset from carrier
RF carrier phase noise		-113		dBc/Hz	at 2 MHz offset from carrier
RF carrier phase noise		-119		dBc/Hz	at 5 MHz offset from carrier
RF carrier phase noise		-129		dBc/Hz	at 10 MHz offset from carrier
PLL turn-on or hop time (See <a href="#">Table 5-12</a> )	72	75	75	$\mu\text{s}$	Time from leaving the IDLE state until arriving in the RX state, when not performing calibration. Crystal oscillator running.
PLL calibration time (See <a href="#">Table 5-13</a> )	685	712	724	$\mu\text{s}$	Calibration can be initiated manually or automatically before entering or after leaving RX

## 4.9 DC Characteristics

$T_A = 25^\circ\text{C}$  if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	$V_{DD} - 0.7$	$V_{DD}$	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	$V_{DD} - 0.3$	$V_{DD}$	V	For up to 4 mA output current
Logic "0" input current	N/A	-50	nA	Input equals 0 V
Logic "1" input current	N/A	50	nA	Input equals $V_{DD}$

## 4.10 Power-On Reset

For proper Power-On-Reset functionality the power supply should comply with the requirements in [Section 4.10](#). Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See [Section 5.13.1, Power-On Start-Up Sequence](#), for further details.

Parameter	Min	Typ	Max	Unit	Condition
Power-up ramp-up time			5	ms	From 0 V until reaching 1.8 V
Power off time	1			ms	Minimum time between power-on and power-off

## 4.11 Thermal Characteristics<sup>(1)</sup>

NAME	DESCRIPTION	QFN ( $^\circ\text{C/W}$ )
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.12

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 4.12 Typical Characteristics

### 4.12.1 Typical Characteristics, RX Current Consumption

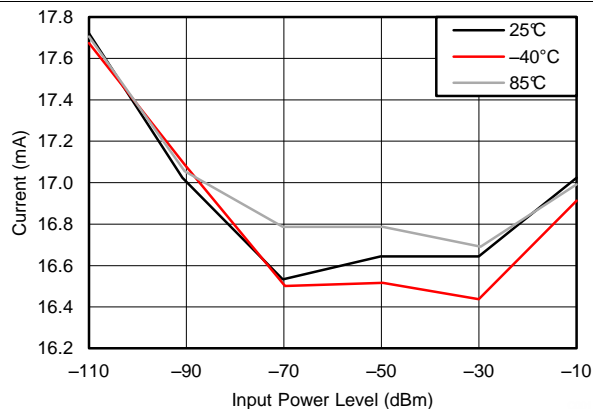


Figure 4-1. Typical RX Current Consumption Over Temperature and Input Power Level, 868 or 915 MHz, Sensitivity Optimized Setting – 1.2 kBaud GFSK

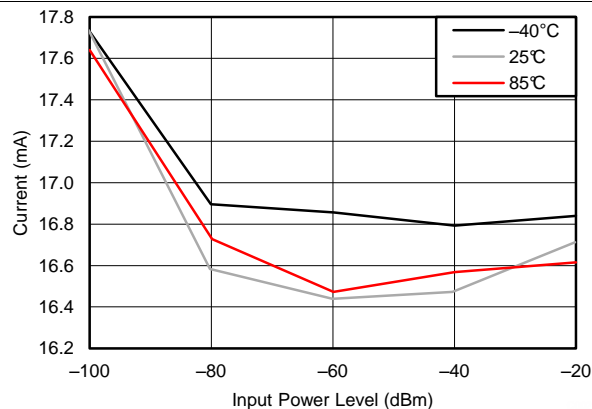


Figure 4-2. Typical RX Current Consumption Over Temperature and Input Power Level, 868 or 915 MHz, Sensitivity Optimized Setting – 38.4 kBaud GFSK

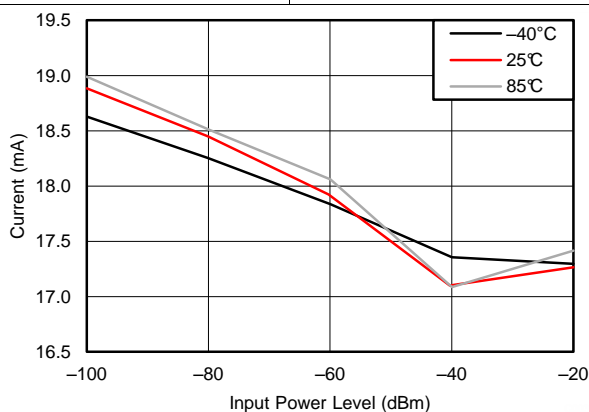


Figure 4-3. Typical RX Current Consumption Over Temperature and Input Power Level, 868 or 915 MHz, Sensitivity Optimized Setting – 250 kBaud GFSK

### 4.12.2 Typical Characteristics, Blocking and Selectivity

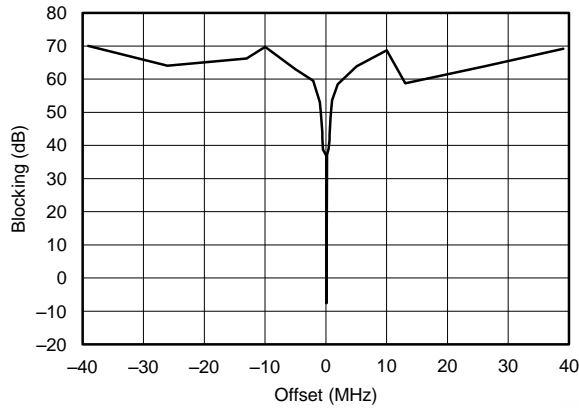


Figure 4-4. Typical Blocking at 1.2 kBaud Data Rate, 868.3 MHz, GFSK, 5.2 kHz Deviation. IF is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 kHz

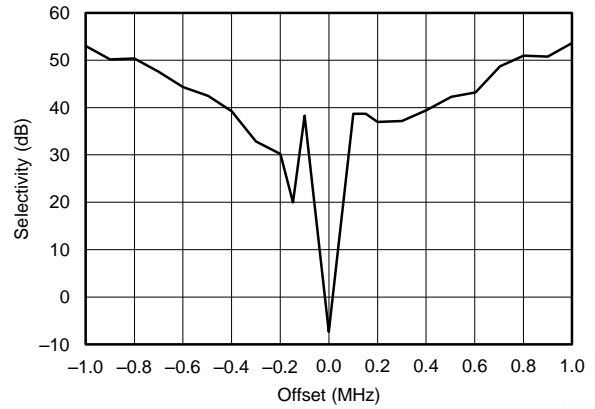


Figure 4-5. Typical Selectivity at 1.2 kBaud Data Rate, 868.3 MHz, GFSK, 5.2 kHz Deviation. IF is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 kHz

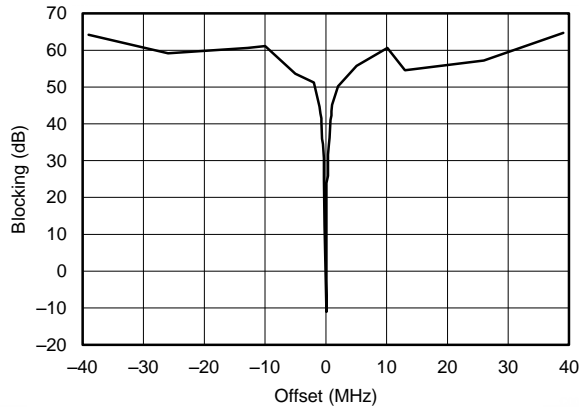


Figure 4-6. Typical Blocking at 38.4 kBaud Data Rate, 868 MHz, GFSK, 20 kHz Deviation. IF is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

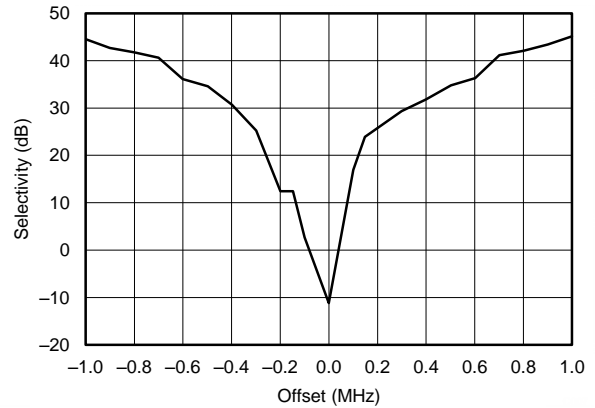


Figure 4-7. Typical Selectivity at 38.4 kBaud Data Rate, 868 MHz, GFSK, 20 kHz Deviation. IF is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

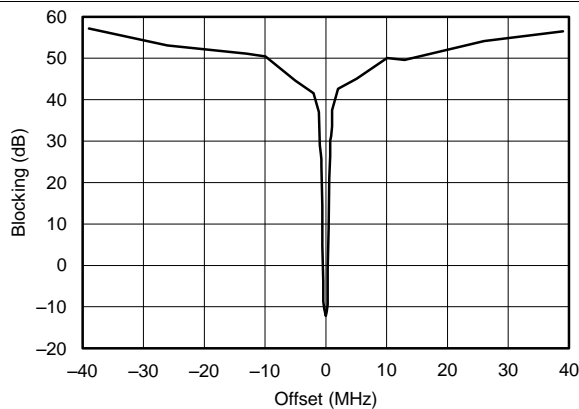


Figure 4-8. Typical Blocking at 250 kBaud Data Rate, 868 MHz, GFSK, IF is 304 kHz and the Digital Channel Filter Bandwidth is 540 kHz

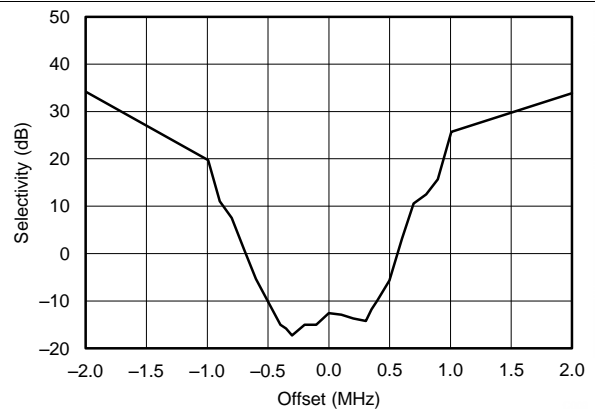


Figure 4-9. Typical Selectivity at 250 kBaud Data Rate, 868 MHz, GFSK, IF is 304 kHz and the Digital Channel Filter Bandwidth is 540 kHz

## 5 Detailed Description

### 5.1 Overview

CC113L features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation, and bit/packet synchronization are performed digitally.

The frequency synthesizer includes a completely on-chip LC VCO and a 90-degree phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC\_Q1 and XOSC\_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

### 5.2 Functional Block Diagram

A simplified block diagram of CC113L is shown in [Figure 5-1](#).

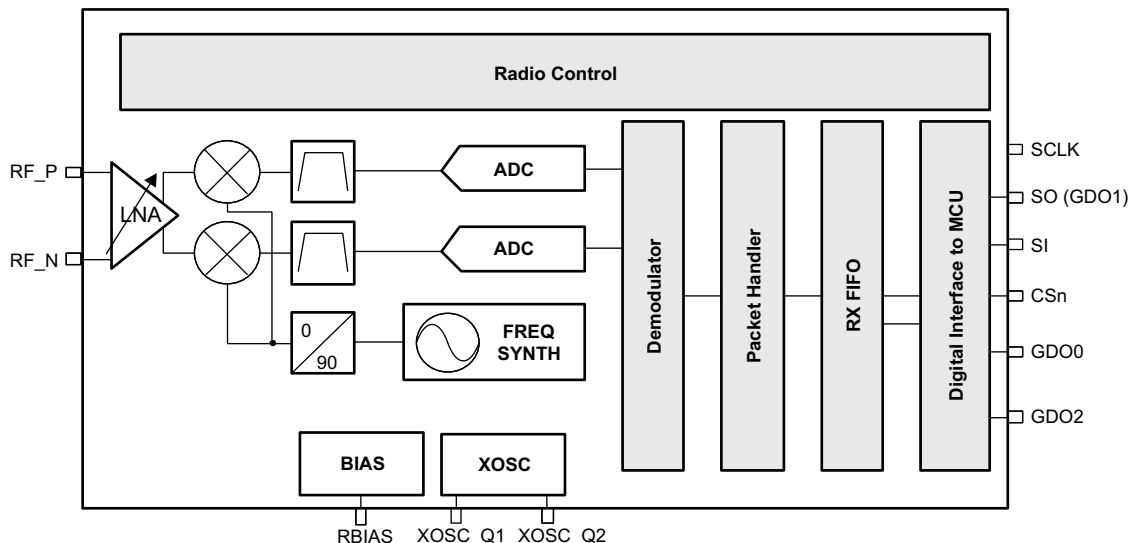


Figure 5-1. CC113L Simplified Block Diagram

### 5.3 Configuration Overview

CC113L can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. See [Section 5.5](#) for more description of the SPI interface. The following key parameters can be programmed:

- Power-down / power-up mode
- Crystal oscillator power-up / power-down
- Receive
- Carrier frequency / RF channel
- Data rate
- Modulation format
- RX channel filter bandwidth
- Data buffering with separate 64-byte RX FIFO
- Packet radio hardware support

Details of each configuration register can be found in [Section 5.21](#).

[Figure 5-2](#) shows a simplified state diagram that explains the main CC113L states together with typical usage and current consumption. For detailed information on controlling the CC113L state machine, and a complete state diagram, see [Section 5.13](#).



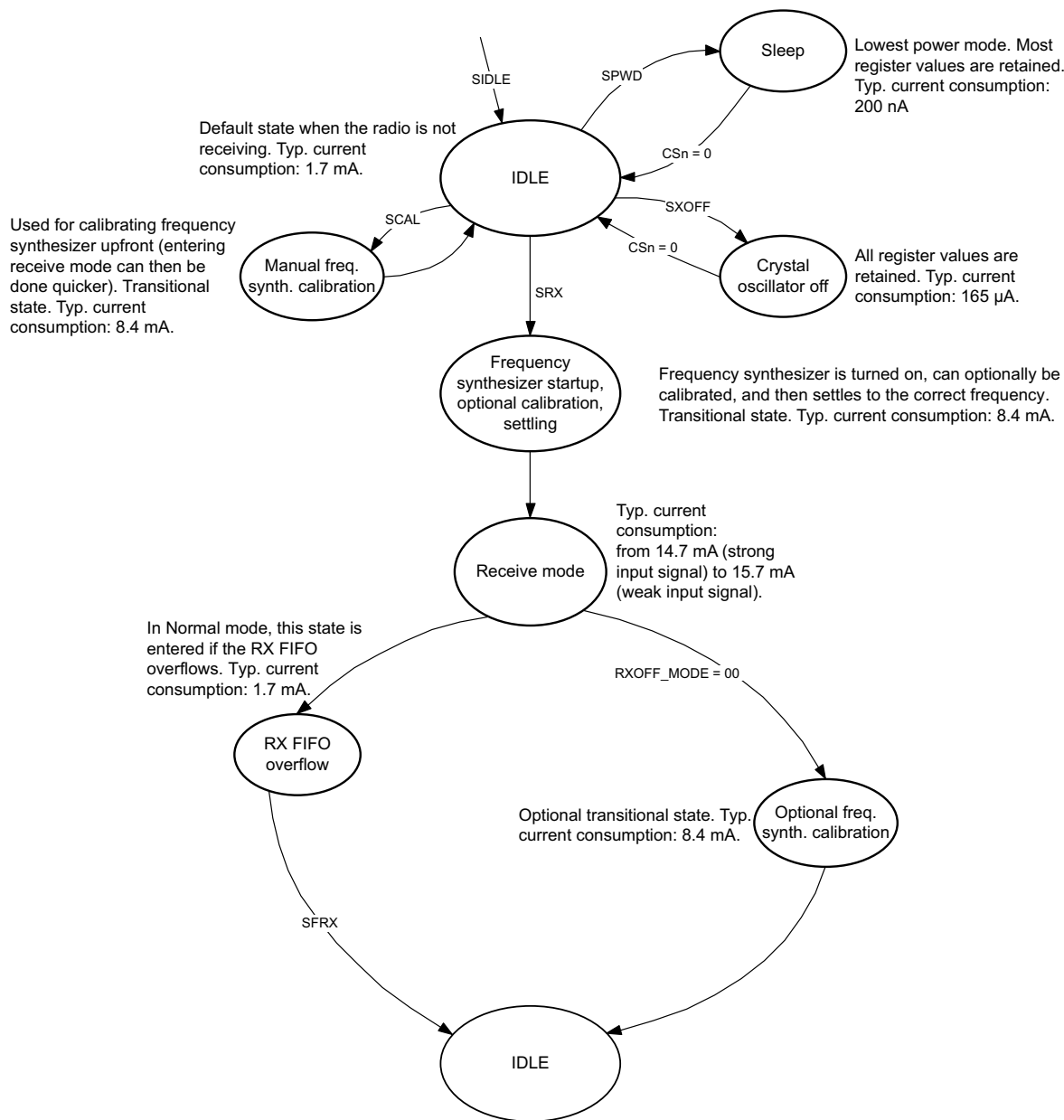


Figure 5-2. Simplified Radio Control State Diagram, with Typical Current Consumption at 1.2 kBaud Data Rate and `MDMCFG2.DEM_DCFILT_OFF=1` (current optimized) – Frequency Band = 868 MHz

## 5.4 Configuration Software

CC113L can be configured using the SmartRF™ Studio software [SWRC176](#). The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

After chip reset, all the registers have default values as shown [Section 5.21](#).

The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

### 5.5 4-wire Serial Configuration and Data Interface

CC113L is configured through a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where CC113L is the slave. This interface is also used to read and write buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R $\overline{W}$  bit, a burst access bit (B), and a 6-bit address (A<sub>5</sub>–A<sub>0</sub>).

The CSn pin must be kept low during transfers on the SPI bus. If CSn goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 5-3 with reference to Table 5-1.

When CSn is pulled low, the MCU must wait until CC113L SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

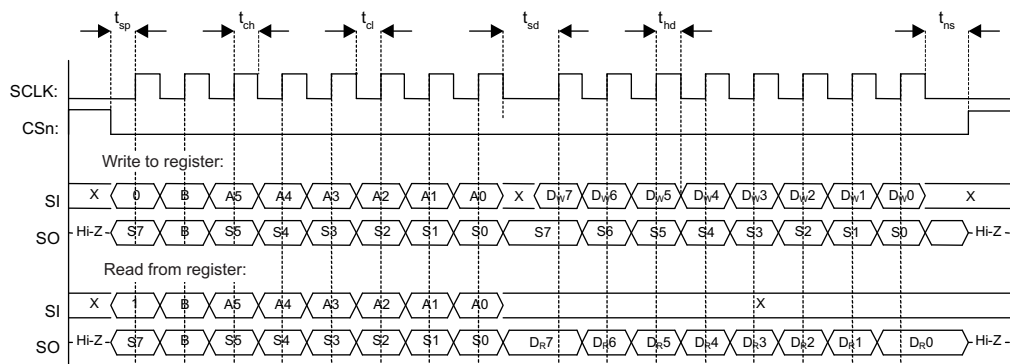


Figure 5-3. Configuration Registers Write and Read Operations

Table 5-1. SPI Interface Timing Requirements

Parameter	Description	Min	Max	Units	
f <sub>SCLK</sub>	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).	–	10	MHz	
	SCLK frequency, single access No delay between address and data byte	–	9		
	SCLK frequency, burst access No delay between address and data byte, or between data bytes	–	6.5		
t <sub>sp,pd</sub>	CSn low to positive edge on SCLK, in power-down mode	150	–	μs	
t <sub>sp</sub>	CSn low to positive edge on SCLK, in active mode	20	–	ns	
t <sub>ch</sub>	Clock high	50	–	ns	
t <sub>cl</sub>	Clock low	50	–	ns	
t <sub>rise</sub>	Clock rise time	–	40	ns	
t <sub>fall</sub>	Clock fall time	–	40	ns	
t <sub>sd</sub>	Setup data (negative SCLK edge) to positive edge on SCLK (tsd applies between address and data bytes, and between data bytes)	Single access	55	–	ns
		Burst access	76	–	
t <sub>hd</sub>	Hold data after positive edge on SCLK	20	–	ns	
t <sub>ns</sub>	Negative edge on SCLK to CSn high.	20	–	ns	

**NOTE**

The minimum  $t_{sp,pd}$  figure in [Table 5-1](#) can be used in cases where the user does not read the CHIP\_RDYn signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150  $\mu$ s in [Table 5-1](#) is the crystal oscillator start-up time measured on [SWRR046](#) and [SWRR045](#) using crystal AT-41CD2 from NDK.

**5.5.1 Chip Status Byte**

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the CC 113L113L113L on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP\_RDYn signal and this signal must go low before the first positive edge of SCLK. The CHIP\_RDYn signal indicates that the crystal is running.

Bits 6, 5, and 4 comprise the STATE value. This value reflects the state of the chip. The XOSC and power to the digital core are on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state.

The last four bits (3:0) in the status byte contains FIFO\_BYTES\_AVAILABLE. For these bits to give any valid information, the  $R/\overline{W}$  bit in the header byte must be set to 1. The FIFO\_BYTES\_AVAILABLE field will then contain the number of bytes that can be read from the RX FIFO. When FIFO\_BYTES\_AVAILABLE=15, 15 or more bytes can be read. The RX FIFO should not be emptied before the complete packet has been received (see the CC113L Errata Notes [SWRZ038](#) for more details).

[Table 5-2](#) gives a status byte summary.

**Table 5-2. Status Byte Summary**

Bits	Name	Description		
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.		
6:4	STATE[2:0]	Indicates the current main state machine mode		
		Value	State	Description
		000	IDLE	IDLE state (Also reported for some transitional states instead of SETTling or CALIBRATE)
		001	RX	Receive mode
		010	Reserved	
		011	Reserved	
		100	CALIBRATE	Frequency synthesizer calibration is running
		101	SETTLING	PLL is settling
		110	RXFIFO_OVERFLOW	RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX
111	Reserved			
3:0	FIFO_BYTES_AVAILABLE[3:0]	The number of bytes available in the RX FIFO		

## 5.5.2 Register Access

The configuration registers on the CC113L are located on SPI addresses from 0x00 to 0x2E. [Table 5-17](#) lists all configuration registers. It is highly recommended to use SmartRF Studio [SWRC176](#) to generate optimum register settings. The detailed description of each register is found in [Section 5.21.1](#) and [Section 5.21.2](#). All configuration registers can be both written to and read. The  $R/\overline{W}$  bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit (B) in the header byte. The address bits ( $A_5 - A_0$ ) set the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30 – 0x3D, the burst bit is used to select between status registers when burst bit is one, and command strobes when burst bit is zero (see [Section 5.5.3](#)). Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

## 5.5.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (that is, MARCSTATE or RXBYTES), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from RXBYTES being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the CC113L Errata Notes [SWRZ038](#) for more details.

## 5.5.4 Command Strokes

Command Strokes may be viewed as single byte instructions to CC113L. By addressing a command strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable receive mode, enable calibration etc. The 8 command strobes are listed in [Table 5-16](#).

### NOTE

An SIDLE strobe will clear all pending command strobes until IDLE state is reached. This means that if for example an SIDLE strobe is issued while the radio is in RX state, any other command strobes issued before the radio reaches IDLE state will be ignored.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the  $R/\overline{W}$  bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written. The  $R/\overline{W}$  bit can be either one or zero and will determine how the FIFO\_BYTES\_AVAILABLE field in the status byte should be interpreted.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an SRES strobe is being issued, one will have to wait for SO to go low again before the next header byte can be issued as shown in [Figure 5-4](#). The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes, which are executed when CSn goes high.

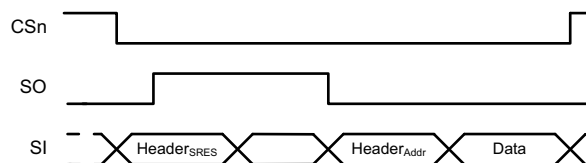


Figure 5-4. SRES Command Strobe

### 5.5.5 RX FIFO Access

The 64-byte RX FIFO is accessed through the 0x3F address. The RX FIFO is write-only and the  $R/\overline{W}$  bit should therefore be one.

The burst bit is used to determine if the RX FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte, a new header byte is expected; hence, CSn can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the RX FIFO:

- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

The RX FIFO may be flushed by issuing a SFRX command strobe. A SFRX command strobe can only be issued in the IDLE, or RXFIFO\_OVERFLOW states. The RX FIFO is flushed when going to the SLEEP state.

Figure 5-5 gives a brief overview of different register access types possible.

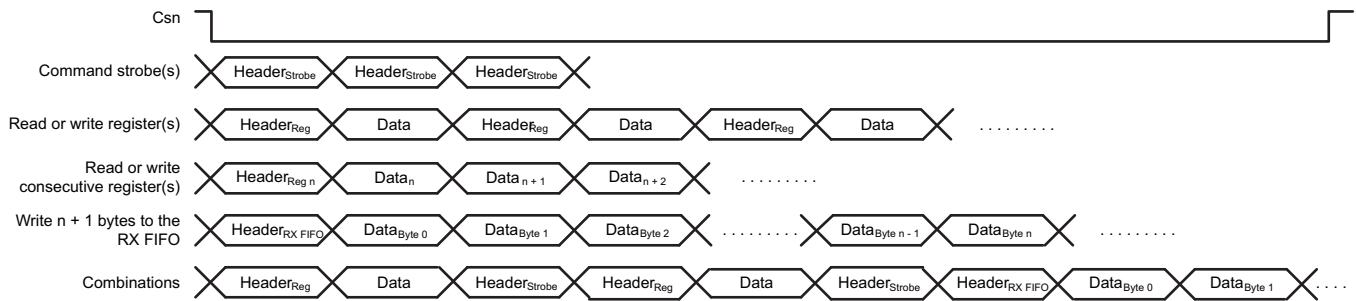


Figure 5-5. Register Access Types

## 5.6 Microcontroller Interface and Pin Configuration

In a typical system, CC113L will interface to a microcontroller. This microcontroller must be able to:

- Program CC113L into different modes
- Read buffered data
- Read back status information through the 4-wire SPI-bus configuration interface (SI, SO, SCLK, and CSn)

### 5.6.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK, and CSn). The SPI is described in [Section 5.5](#).

### 5.6.2 General Control and Status Pins

The CC113L has two dedicated configurable pins (GDO0 and GDO2) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See [Section 5.18](#) for more details on the signals that can be programmed.

GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options, the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

## 5.7 Data Rate Programming

The data rate expected in receive mode is programmed by the [MDMCFG3.DRATE\\_M](#) and the [MDMCFG4.DRATE\\_E](#) configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{\text{DATA}} = \frac{(256 + \text{DRATE\_M}) \cdot 2^{\text{DRATE\_E}}}{2^{28}} \cdot f_{\text{XOSC}} \quad (1)$$

The following approach can be used to find suitable values for a given data rate:

$$\text{DRATE\_E} = \log_2 \left( \frac{R_{\text{DATA}} \cdot 2^{20}}{f_{\text{XOSC}}} \right) \quad (2)$$

$$\text{DRATE\_M} = \frac{R_{\text{DATA}} \cdot 2^{28}}{f_{\text{XOSC}} \cdot 2^{\text{DRATE\_E}}} - 256 \quad (3)$$

If [DRATE\\_M](#) is rounded to the nearest integer and becomes 256, increment [DRATE\\_E](#) and use [DRATE\\_M](#) = 0.

The data rate can be set from 0.6 kBaud to 500 kBaud with the minimum step size according to [Table 5-3](#). See [Section 4.4](#) for the minimum and maximum data rates for the different modulation formats.

**Table 5-3. Data Rate Step Size (Assuming a 26-MHz crystal)**

Min Data Rate [kBaud]	Typical Data Rate [kBaud]	Max Data Rate [kBaud]	Data rate Step Size [kBaud]
0.6	1.0	0.79	0.0015
0.79	1.2	1.58	0.0031
1.59	2.4	3.17	0.0062
3.17	4.8	6.33	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.3	0.0496
25.4	38.4	50.7	0.0992
50.8	76.8	101.4	0.1984
101.6	153.6	202.8	0.3967
203.1	250	405.5	0.7935
406.3	500	500	1.5869



## 5.8 Receiver Channel Filter Bandwidth

In order to meet different channel width requirements, the receiver channel filter is programmable. The [MDMCFG4.CHANBW\\_E](#) and [MDMCFG4.CHANBW\\_M](#) configuration registers control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency.

The following formula gives the relation between the register settings and the channel filter bandwidth:

$$BW_{\text{channel}} = \frac{f_{\text{XOSC}}}{8 \cdot (4 + \text{CHANBW\_M}) \cdot 2^{\text{CHANBW\_E}}} \quad (4)$$

[Table 5-4](#) lists the channel filter bandwidths supported by the CC113L.

**Table 5-4. Channel Filter Bandwidths [kHz] (Assuming a 26-MHz Crystal)**

MDMCFG4.CHANBW_M	MDMCFG4.CHANBW_E			
	00	01	10	11
00	812	406	203	102
01	650	325	162	81
10	541	270	135	68
11	464	232	116	58

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel center tolerance due to crystal inaccuracy should also be subtracted from the channel filter bandwidth. The following example illustrates this:

With the channel filter bandwidth set to 500 kHz, the signal should stay within 80% of 500 kHz, which is 400 kHz. Assuming 915 MHz frequency and  $\pm 20$  ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is  $\pm 40$  ppm of 915 MHz, which is  $\pm 37$  kHz. If the whole transmitted signal bandwidth is to be received within 400 kHz, the transmitted signal bandwidth should be maximum 400 kHz –  $2 \times 37$  kHz, which is 326 kHz. By compensating for a frequency offset between the transmitter and the receiver, the filter bandwidth can be reduced and the sensitivity can be improved, see more in DN005 [SWRA122](#) and in [Section 5.9.1](#).

## 5.9 Demodulator, Symbol Synchronizer, and Data Decision

CC113L contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation is performed digitally. To generate the RSSI level (see [Section 5.12.2](#) for more information), the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

### 5.9.1 Frequency Offset Compensation

The CC113L has a very fine frequency resolution (see [Section 4.8](#)). This feature can be used to compensate for frequency offset and drift.

When using 2-FSK, GFSK, or 4-FSK modulation, the demodulator will compensate for the offset between the transmitter and receiver frequency within certain limits, by estimating the center of the received data. The frequency offset compensation configuration is controlled from the [FOCCFG](#) register. By compensating for a large frequency offset between the transmitter and the receiver, the sensitivity can be improved, see DN005 [SWRA122](#).

The tracking range of the algorithm is selectable as fractions of the channel bandwidth with the [FOCCFG.FOC\\_LIMIT](#) configuration register.

If the [FOCCFG.FOC\\_BS\\_CS\\_GATE](#) bit is set, the offset compensator will freeze until carrier sense asserts. This may be useful when the radio is in RX for long periods with no traffic, since the algorithm may drift to the boundaries when trying to track noise.

The tracking loop has two gain factors, which affects the settling time and noise sensitivity of the algorithm. [FOCCFG.FOC\\_PRE\\_K](#) sets the gain before the sync word is detected, and [FOCCFG.FOC\\_POST\\_K](#) selects the gain after the sync word has been found.

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#### NOTE

Frequency offset compensation is not supported for OOK modulation.

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The estimated frequency offset value is available in the [FREQEST](#) status register. This can be used for permanent frequency offset compensation. By writing the value from [FREQEST](#) into [FSCTRL0.FREQOFF](#), the frequency synthesizer will automatically be adjusted according to the estimated frequency offset. More details regarding this permanent frequency compensation algorithm can be found in DN015 [SWRA159](#).

### 5.9.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in [Section 5.7](#). Re-synchronization is performed continuously to adjust for error in the incoming symbol rate.

### 5.9.3 Byte Synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16 bit configurable field (can be repeated to get a 32 bit) that must be inserted at the start of the packet by the transmitter (for example the CC115L, CC110L, or CC1101). The MSB in the sync word must be transmitted first. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word will also function as a system identifier, since only packets with the correct predefined sync word will be received if the sync word detection in RX is enabled in register [MDMCFG2](#) (see [Section 5.12.1](#)). The sync word detector correlates against the user-configured 16 or 32 bit sync word. The correlation threshold can be set to 15/16, 16/16, or 30/32 bits match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is configured through the [SYNC1](#) and [SYNC0](#) registers.

### 5.10 Packet Handling Hardware Support

The CC113L has built-in hardware support for packet oriented radio protocols and the packet handler can be configured to implement the following (if enabled):

- Preamble detection
- Sync word detection
- CRC computation and CRC check
- One byte address check
- Packet length check (length byte checked against a programmable maximum length)

Optionally, two status bytes (see [Table 5-5](#) and [Table 5-6](#)) with RSSI value and CRC status can be appended in the RX FIFO.

**Table 5-5. Received Packet Status Byte 1 (First Byte Appended After the Data)**

Bit	Field Name	Description
7:0	RSSI	RSSI value

**Table 5-6. Received Packet Status Byte 2 (Second Byte Appended After the Data)**

Bit	Field Name	Description
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	Reserved	

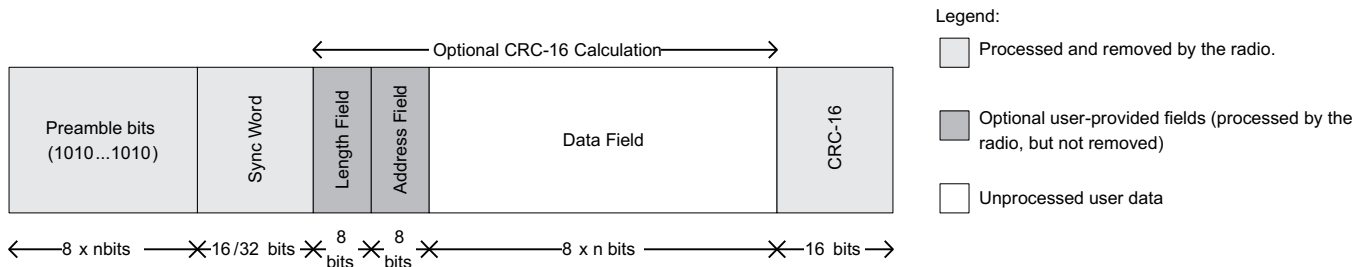
**NOTE**

Register fields that control the packet handling features should only be altered when CC113L is in the IDLE state.

#### 5.10.1 Packet Format

The format of the data packet can be configured and consists of the following items (see [Figure 5-6](#)):

- Preamble
- Synchronization word
- Optional length byte
- Optional address byte
- Payload
- Optional 2 byte CRC



**Figure 5-6. Packet Format**

The preamble pattern is an alternating sequence of ones and zeros that the receiver uses for bit synchronisation.

The synchronization word is a two-byte value set in the [SYNC1](#) and [SYNC0](#) registers. The sync word provides byte synchronization of the incoming packet. A one-byte sync word can be emulated by setting the [SYNC1](#) value to the preamble pattern. It is also possible to emulate a 32 bit sync word by setting [MDMCFG2.SYNC\\_MODE](#) to 3 or 7. The sync word will then be repeated twice.

CC113L supports both constant packet length protocols and variable length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting [PKTCTRL0.LENGTH\\_CONFIG=0](#). The desired packet length is set by the [PKTLEN](#) register. This value must be different from 0.

In variable packet length mode, [PKTCTRL0.LENGTH\\_CONFIG=1](#), the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional CRC. The [PKTLEN](#) register is used to set the maximum packet length allowed in RX. Any packet received with a length byte with a value greater than [PKTLEN](#) will be discarded. The [PKTLEN](#) value must be different from 0.

With [PKTCTRL0.LENGTH\\_CONFIG=2](#), the packet length is set to infinite and transmission and reception will continue until turned off manually. As described in [Section 5.10.1.1](#), this can be used to support packet formats with different length configuration than natively supported by CC113L.

---

#### NOTE

The minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

---

#### 5.10.1.1 Arbitrary Length Field Configuration

The packet length register, [PKTLEN](#), can be reprogrammed during RX. In combination with fixed packet length mode ( [PKTCTRL0.LENGTH\\_CONFIG=0](#)), this opens the possibility to have a different length field configuration than supported for variable length packets (in variable packet length mode the length byte is the first byte after the sync word). At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the [PKTLEN](#) value is set according to this value. The end of packet will occur when the byte counter in the packet handler is equal to the [PKTLEN](#) register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

#### 5.10.1.2 Packet Length > 255

The packet automation control register, [PKTCTRL0](#), can be reprogrammed during RX. This opens the possibility to receive packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode ( [PKTCTRL0.LENGTH\\_CONFIG=2](#)) must be active. When receiving, the MCU reads out enough bytes to interpret the length field in the packet and sets the [PKTLEN](#) register to  $\text{mod}(\text{length}, 256)$ . When less than 256 bytes remains of the packet, the MCU disables infinite packet length mode and activates fixed packet length mode ( [PKTCTRL0.LENGTH\\_CONFIG=0](#)). When the internal byte counter reaches the [PKTLEN](#) value, the transmission or reception ends (the radio enters the state determined by [RXOFF\\_MODE](#)). Automatic CRC appending/checking can also be used (by setting [PKTCTRL0.CRC\\_EN=1](#)).

When for example a 600-byte packet is to be received, the MCU should do the following (see Figure 5-7).

- Set `PKTCTRL0.LENGTH_CONFIG=2`.
- Receive enough bytes to interpret the length field
- Program the `PKTLEN` register to  $\text{mod}(600, 256) = 88$ .
- Receive at least 345 bytes ( $600 - 255$ )
- Set `PKTCTRL0.LENGTH_CONFIG=0`.
- The reception ends when the packet counter reaches 88. A total of 600 bytes have been received.

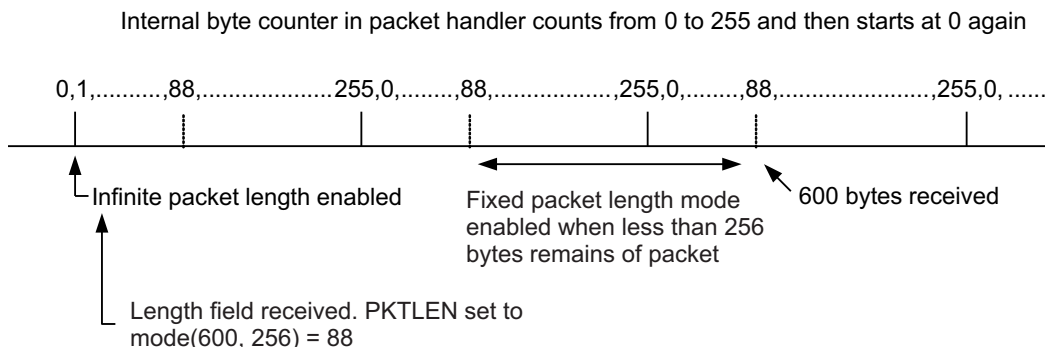


Figure 5-7. Packet Length > 255

## 5.10.2 Packet Filtering

CC113L supports three different types of packet-filtering; address filtering, maximum length filtering, and CRC filtering.

### 5.10.2.1 Address Filtering

Setting `PKTLEN.ADR_CHK` to any other value than zero enables the packet address filter. The packet handler engine will compare the destination address byte in the packet with the programmed node address in the `PKTCTRL0` register and the 0x00 broadcast address when `PKTLEN.ADR_CHK=10` or both the 0x00 and 0xFF broadcast addresses when `PKTLEN.ADR_CHK=11`. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded and receive mode restarted (regardless of the `MCSM1.RXOFF_MODE` setting).

If the received address matches a valid address when using infinite packet length mode and address filtering is enabled, 0xFF will be written into the RX FIFO followed by the address byte and then the payload data.

### 5.10.2.2 Maximum Length Filtering

In variable packet length mode, `PKTCTRL0.LENGTH_CONFIG=1`, the `PKTLEN.PACKET_LENGTH` register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded and receive mode restarted (regardless of the `MCSM1.RXOFF_MODE` setting).

### 5.10.2.3 CRC Filtering

The filtering of a packet when CRC check fails is enabled by setting `PKTLEN.CRC_AUTOFLUSH=1`. The CRC auto flush function will flush the entire RX FIFO if the CRC check fails. After auto flushing the RX FIFO, the next state depends on the `MCSM1.RXOFF_MODE` setting.

When using the auto flush function, the maximum packet length is 63 bytes in variable packet length mode and 64 bytes in fixed packet length mode. Note that when `PKTLEN.APPEND_STATUS` is enabled, the maximum allowed packet length is reduced by two bytes in order to make room in the RX FIFO for the two status bytes appended at the end of the packet. Since the entire RX FIFO is flushed when the CRC check fails, the previously received packet must be read out of the FIFO before receiving the current packet. The MCU must not read from the current packet until the CRC has been checked as OK.

### 5.10.3 Packet Handling in Receive Mode

In receive mode, the demodulator and packet handler will search for a valid preamble and the sync word. When found, the demodulator has obtained both bit and byte synchronization and will receive the first payload byte.

When variable packet length mode is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length mode is used, the packet handler will accept the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

At the end of the payload, the packet handler will optionally write two extra packet status bytes (see [Table 5-5](#) and [Table 5-6](#)) that contain CRC status, link quality indication, and RSSI value.

### 5.10.4 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been received. Additionally, for packets longer than 64 bytes, the RX FIFO needs to be read while in RX. There are two possible solutions to get the necessary status information:

#### a. Interrupt Driven Solution

The GDO pins can be used to give an interrupt when a sync word has been received or when a complete packet has been received by setting `IOCFGx.GDOx_CFG=0x06`. In addition, there are two configurations for the `IOCFGx.GDOx_CFG` register that can be used as an interrupt source to provide information on how many bytes that are in the RX FIFO (`IOCFGx.GDOx_CFG=0x00` and `IOCFGx.GDOx_CFG=0x01`). See [Table 5-15](#) for more information.

#### b. SPI Polling

The `PKTSTATUS` register can be polled at a given rate to get information about the current `GDO2` and `GDO0` values respectively. The `RXBYTES` register can be polled at a given rate to get information about the number of bytes in the RX FIFO. Alternatively, the number of bytes in the RX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

It is recommended to employ an interrupt driven solution since high rate SPI polling reduces the RX sensitivity. Furthermore, as explained in [Section 5.5.3](#) and the CC113L Errata Notes [SWRZ038](#), when using SPI polling, there is a small, but finite, probability that a single read from registers `PKTSTATUS`, and `RXBYTES` is being corrupt. The same is the case when reading the chip status byte.

## 5.11 Modulation Formats

CC113L supports amplitude, frequency, and phase shift modulation formats. The desired modulation format is set in the [MDMCFG2.MOD\\_FORMAT](#) register.

Optionally, if the data has been Manchester coded on the transmitter side it can be decoded by the demodulator. This option is enabled by setting [MDMCFG2.MANCHESTER\\_EN](#)=1.

### NOTE

Manchester encoding is not supported at the same time as using 4-FSK modulation.

### 5.11.1 Frequency Shift Keying

CC113L supports 2-(G)FSK and 4-FSK modulation. When selecting 4-FSK, the preamble and sync word to be received needs to be 2-FSK (see [Figure 5-8](#)).

When 2-FSK/GFSK/4-FSK modulation is used, the [DEVIATN](#) register specifies the expected frequency deviation of incoming signals in RX and should be the same as the deviation of the transmitted signal for demodulation to be performed reliably and robustly.

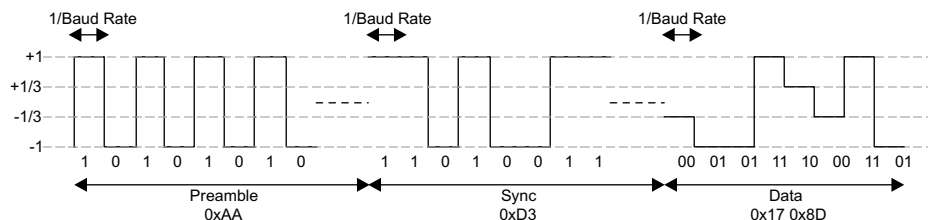
The frequency deviation is programmed with the [DEVIATION\\_M](#) and [DEVIATION\\_E](#) values in the [DEVIATN](#) register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{XOSC}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E} \quad (5)$$

The symbol encoding is shown in [Table 5-7](#).

**Table 5-7. Symbol Encoding for 2-FSK/GFSK and 4-FSK Modulation**

Format	Symbol	Coding
2-FSK/GFSK	0	– Deviation
	1	+ Deviation
4-FSK	01	– Deviation
	00	– 1/3xDeviation
	10	+ 1/3xDeviation
	11	+ Deviation



**Figure 5-8. Data Sent Over the Air ( [MDMCFG2.MOD\\_FORMAT](#)=100)**

### 5.11.2 Amplitude Modulation

The amplitude modulation supported by CC113L is On-Off Keying (OOK).

OOK modulation simply turns the PA on or off to modulate ones and zeros respectively.

When using OOK, the AGC settings from the SmartRF Studio [SWRC176](#) preferred FSK settings are not optimum. DN022 [SWRA215](#) gives guidelines on how to find optimum OOK settings from the preferred settings in SmartRF Studio [SWRC176](#). The [DEVIATN](#) register setting has no effect when using OOK.

## 5.12 Received Signal Qualifiers and RSSI

CC113L has several qualifiers that can be used to increase the likelihood that a valid sync word is detected:

- Sync Word Qualifier
- RSSI
- Carrier Sense

### 5.12.1 Sync Word Qualifier

If sync word detection is enabled in the [MDMCFG2](#) register, the CC113L will not start filling the RX FIFO and perform the packet filtering described in [Section 5.10.2](#) before a valid sync word has been detected. The sync word qualifier mode is set by [MDMCFG2.SYNC\\_MODE](#) and is summarized in [Table 5-8](#). Carrier sense described in [Section 5.12.3](#).

**Table 5-8. Sync Word Qualifier Mode**

<a href="#">MDMCFG2.SYNC_MODE</a>	Sync Word Qualifier Mode
000	No preamble/sync
001	15/16 sync word bits detected
010	16/16 sync word bits detected
011	30/32 sync word bits detected
100	No preamble/sync + carrier sense above threshold
101	15/16 + carrier sense above threshold
110	16/16 + carrier sense above threshold
111	30/32 + carrier sense above threshold

### 5.12.2 RSSI

The RSSI value is an estimate of the signal power level in the chosen channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the RSSI status register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters the RX state.

#### NOTE

It takes some time from the radio enters RX mode until a valid RSSI value is present in the RSSI register. See DN505 [SWRA114](#) for details on how the RSSI response time can be estimated.

The RSSI value is given in dBm with a ½-dB resolution. The RSSI update rate,  $f_{\text{RSSI}}$ , depends on the receiver filter bandwidth ( $BW_{\text{channel}}$  is defined in [Section 5.8](#)) and [AGCCTRL0.FILTER\\_LENGTH](#).

$$f_{\text{RSSI}} = \frac{2 \cdot BW_{\text{channel}}}{8 \cdot 2^{\text{FILTER\_LENGTH}}} \quad (6)$$

If [PKTLEN.APPEND\\_STATUS](#) is enabled, the last RSSI value of the packet is automatically added to the first byte appended after the payload.



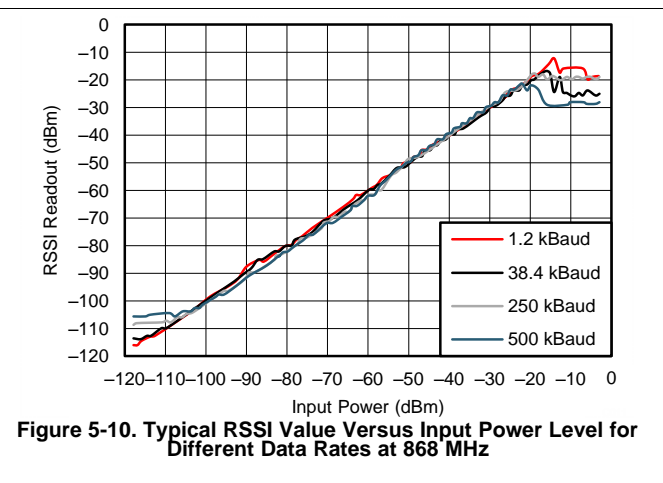
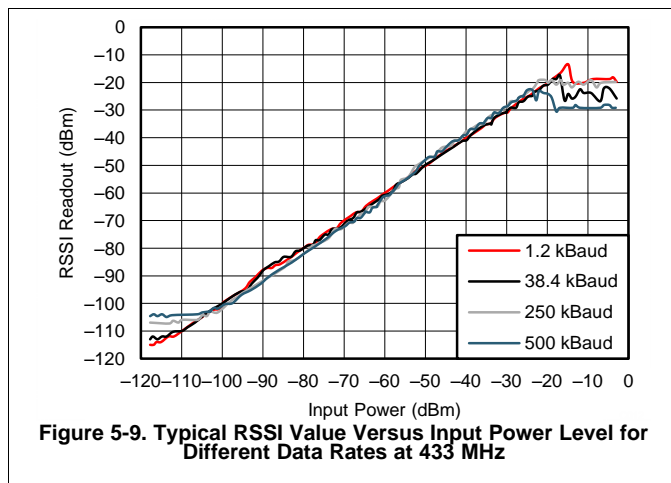
The RSSI value read from the RSSI status register is a 2s complement number. The following procedure can be used to convert the RSSI reading to an absolute power level (RSSI\_dBm).

1. Read the RSSI status register
2. Convert the reading from a hexadecimal number to a decimal number (RSSI\_dec)
3. If  $RSSI\_dec \geq 128$  then  $RSSI\_dBm = (RSSI\_dec - 256)/2 - RSSI\_offset$
4. Else if  $RSSI\_dec < 128$  then  $RSSI\_dBm = (RSSI\_dec)/2 - RSSI\_offset$

Table 5-9 gives typical values for the RSSI\_offset. Figure 5-9 and Figure 5-10 show typical plots of RSSI readings as a function of input power level for different data rates.

**Table 5-9. Typical RSSI\_offset Values**

Data rate [kBaud]	RSSI_offset [dB], 433 MHz	RSSI_offset [dB], 868 MHz
1.2	74	74
38.4	74	74
250	74	74
500	74	74



### 5.12.3 Carrier Sense (CS)

Carrier sense (CS) is used as a sync word qualifier and can be asserted based on two conditions which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold, and deasserted when RSSI is below the same threshold (with hysteresis). See more in [Section 5.12.3.1](#).
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next, and de-asserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with time varying noise floor. See more in [Section 5.12.3.2](#).

Carrier sense can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed and is set by setting [MDMCFG2](#). The carrier sense signal can be observed on one of the GDO pins by setting `IOCFGx.GDOx_CFG=14` and in the status register bit `PKTSTATUS.CS`.

### 5.12.3.1 CS Absolute Threshold

The absolute threshold related to the RSSI value depends on the following register fields:

- [AGCCTRL2.MAX\\_LNA\\_GAIN](#)
- [AGCCTRL2.MAX\\_DVGA\\_GAIN](#)
- [AGCCTRL1.CARRIER\\_SENSE\\_ABS\\_THR](#)
- [AGCCTRL2.MAGN\\_TARGET](#)

For given [AGCCTRL2.MAX\\_LNA\\_GAIN](#) and [AGCCTRL2.MAX\\_DVGA\\_GAIN](#) settings, the absolute threshold can be adjusted  $\pm 7$  dB in steps of 1 dB using [CARRIER\\_SENSE\\_ABS\\_THR](#).

The [MAGN\\_TARGET](#) setting is a compromise between blocker tolerance/selectivity and sensitivity. The value sets the desired signal level in the channel into the demodulator. Increasing this value reduces the headroom for blockers, and therefore close-in selectivity. It is strongly recommended to use SmartRF Studio [SWRC176](#) to generate the correct [MAGN\\_TARGET](#) setting. [Table 5-11](#) show the typical RSSI readout values at the CS threshold at 2.4 kBaud and 250 kBaud data rate respectively. The default reset value for [CARRIER\\_SENSE\\_ABS\\_THR](#) = 0 (0 dB) has been used. [MAGN\\_TARGET](#) = 3 (33 dB) and 7 (42 dB) have been used for 2.4 kBaud and 250 kBaud data rate respectively. For other data rates, the user must generate similar tables to find the CS absolute threshold.

**Table 5-10. Typical RSSI Value in dBm at CS Threshold with [MAGN\\_TARGET](#) = 3 (33 dB) at 2.4 kBaud, 868 MHz**

		<a href="#">MAX_DVGA_GAIN[1:0]</a>			
		00	01	10	11
<a href="#">MAX_LNA_GAIN[2:0]</a>	000	-97.5	-91.5	-85.5	-79.5
	001	-94	-88	-82.5	-76
	010	-90.5	-84.5	-78.5	-72.5
	011	-88	-82.5	-76.5	-70.5
	100	-85.5	-80	-73.5	-68
	101	-84	-78	-72	-66
	110	-82	-76	-70	-64
	111	-79	-73.5	-67	-61

**Table 5-11. Typical RSSI Value in dBm at CS Threshold with [MAGN\\_TARGET](#) = 7 (42 dB) at 250 kBaud, 868 MHz**

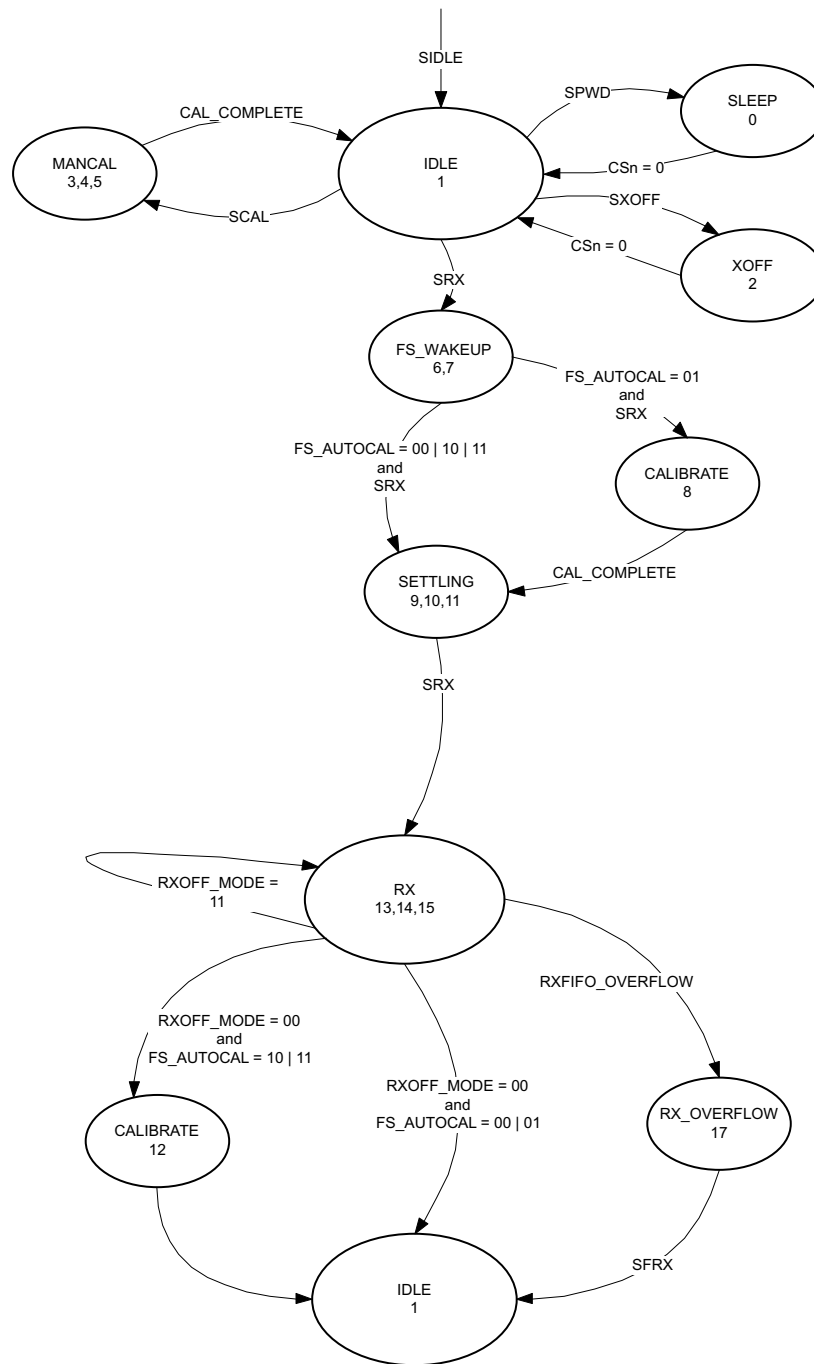
		<a href="#">MAX_DVGA_GAIN[1:0]</a>			
		00	01	10	11
<a href="#">MAX_LNA_GAIN[2:0]</a>	000	-90.5	-84.5	-78.5	-72.5
	001	-88	-82	-76	-70
	010	-84.5	-78.5	-72	-66
	011	-82.5	-76.5	-70	-64
	100	-80.5	-74.5	-68	-62
	101	-78	-72	-66	-60
	110	-76.5	-70	-64	-58
	111	-74.5	-68	-62	-56

If the threshold is set high, that is, only strong signals are wanted, the threshold should be adjusted upwards by first reducing the MAX\_LNA\_GAIN value and then the MAX\_DVGA\_GAIN value. This will reduce power consumption in the receiver front end, since the highest gain settings are avoided.

#### 5.12.3.2 CS Relative Threshold

The relative threshold detects sudden changes in the measured signal level. This setting does not depend on the absolute signal level and is thus useful to detect signals in environments with a time varying noise floor. The register field [AGCCTRL1.CARRIER\\_SENSE\\_REL\\_THR](#) is used to enable/disable relative CS, and to select threshold of 6 dB, 10 dB, or 14 dB RSSI change.

### 5.13 Radio Control



**Figure 5-11. Complete Radio Control State Diagram**

CC113L has a built-in state machine that is used to switch between different operational states (modes). The change of state is done either by using command strobes or by internal events such as RX FIFO overflow.

A simplified state diagram, together with typical usage and current consumption, is shown in [Figure 5-2](#). The complete radio control state diagram is shown in [Figure 5-11](#). The numbers refer to the state number readable in the MARCSTATE status register. This register is primarily for test purposes.

### 5.13.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, that is, automatic power-on reset (POR) or manual reset. After the automatic power-on reset or manual reset, it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK\_XOSC/192. However, to optimize performance in RX, an alternative GDO setting from the settings found in [Table 5-15](#) should be selected.

#### 5.13.1.1 Automatic POR

A power-on reset circuit is included in the CC113L. The minimum requirements stated in [Section 4.10](#) must be followed for the power-on reset to function properly. The internal power-up sequence is completed when CHIP\_RDYn goes low. CHIP\_RDYn is observed on the SO pin after CSn is pulled low. See [Section 5.5.1](#) for more details on CHIP\_RDYn.

When the CC113L reset is completed, the chip will be in the IDLE state and the crystal oscillator will be running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed, the SO pin will first go high, indicating that the crystal oscillator is not stabilized, before going low as shown in [Figure 5-12](#).

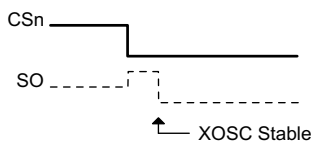


Figure 5-12. Power-On Reset with SRES

#### 5.13.1.2 Manual Reset

The other global reset possibility on CC113L uses the SRES command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see [Figure 5-13](#)):

- Set SCLK = 1 and SI = 0.
- Strobe CSn low / high.
- Hold CSn low and then high for at least 40  $\mu$ s relative to pulling CSn low
- Pull CSn low and wait for SO to go low (CHIP\_RDYn).
- Issue the SRES strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

XOSC and voltage regulator switched on

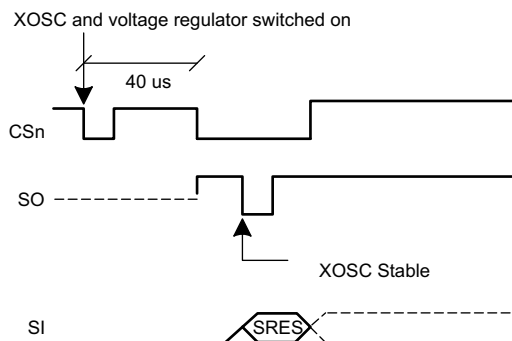


Figure 5-13. Power-On Reset with SRES

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**NOTE**

The above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the CC113L after this, it is only necessary to issue an SRES command strobe.

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### 5.13.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if [MCSM0.XOSC\\_FORCE\\_ON](#) is set.

In the automatic mode, the XOSC will be turned off if the SXOFF or SPWD command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from the IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used as described in [Section 5.5.1](#).

If the XOSC is forced on, the crystal will always stay on even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in [Section 4.7](#).

### 5.13.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a SPWD command strobe has been sent on the SPI interface. The chip is then in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

### 5.13.4 Receive Mode (RX)

Receive mode is activated directly by the MCU by using the SRX command strobe.

The frequency synthesizer must be calibrated regularly. CC113L has one manual calibration option (using the SCAL strobe), and three automatic calibration options that are controlled by the [MCSM0.FS\\_AUTOCAL](#) setting:

- Calibrate when going from IDLE to RX
- Calibrate when going from RX to IDLE automatically (not forced in IDLE by issuing an SIDLE strobe)
- Calibrate every fourth time when going from RX to IDLE automatically (not forced in IDLE by issuing an SIDLE strobe)

If the radio goes from RX to IDLE by issuing an SIDLE strobe, calibration will not be performed. The calibration takes a constant number of XOSC cycles; see [Table 5-12](#) for timing details regarding calibration.

When RX is activated, the chip will remain in receive mode until a packet is successfully received or until RX mode terminated due to lack of carrier sense (see [Section 18.5](#)). The probability that a false sync word is detected can be reduced by using CS together with maximum sync word length as described in [Section 17](#). After a packet is successfully received, the radio controller goes to the state indicated by the [MCSM1.RXOFF\\_MODE](#) setting. The possible destinations are:

- IDLE
- RX: Start search for a new packet

### NOTE

When `MCSM1.RXOFF_MODE=11` and a packet has been received, it will take some time before a valid RSSI value is present in the RSSI register again even if the radio has never exited RX mode. This time is the same as the RSSI response time discussed in DN505 [SWRA114](#).

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state.

### 5.13.5 RX Termination

If the system expects the transmission to have started when entering RX mode, the `MCSM2.RX_TIME_RSSI` function can be used. The radio controller will then terminate RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold). See [Section 5.12.3](#) for details on Carrier Sense.

For OOK modulation, lack of carrier sense is only considered valid after eight symbol periods. Thus, the `MCSM2.RX_TIME_RSSI` function can be used in OOK mode when the distance between two “1” symbols is eight or less.

If RX terminates due to no carrier sense when the `MCSM2.RX_TIME_RSSI` function is used, the radio will always go back to IDLE, regardless of the `MCSM1.RXOFF_MODE` setting.

### 5.13.6 Timing

#### 5.13.6.1 Overall State Transition Times

The main radio controller needs to wait in certain states in order to make sure that the internal analog/digital parts have settled down and are ready to operate in the new states. A number of factors are important for the state transition times:

- The crystal oscillator frequency,  $f_{xosc}$
- The value of the TEST0, TEST1, and `FSCAL3` registers

[Table 5-12](#) shows timing in crystal clock cycles for key state transitions.

**Table 5-12. Overall State Transition Times [Example for 26-MHz Crystal Oscillator, 250 kBaud Data Rate, and TEST0 = 0x0B (Maximum Calibration Time)].**

Description	Transition Time (FREND0.PA_POWER=0)	Transition Time [μs]
IDLE to RX, no calibration	$1953/f_{xosc}$	75.1
IDLE to RX, with calibration	$1953/f_{xosc} + \text{FS calibration Time}$	799
RX to IDLE, no calibration	$2/f_{xosc}$	~0.1
RX to IDLE, with calibration	$2/f_{xosc} + \text{FS calibration Time}$	724
Manual calibration	$283/f_{xosc} + \text{FS calibration Time}$	735

#### 5.13.6.2 Frequency Synthesizer Calibration Time

[Table 5-13](#) summarizes the frequency synthesizer (FS) calibration times for possible settings of TEST0 and `FSCAL3.CHP_CURR_CAL_EN`. Setting `FSCAL3.CHP_CURR_CAL_EN` to 00b disables the charge pump calibration stage. TEST0 is set to the values recommended by SmartRF Studio software. The possible values for TEST0 when operating with different frequency bands are 0x09 and 0x0B. SmartRF Studio software always sets `FSCAL3.CHP_CURR_CAL_EN` to 10b.

The calibration time can be reduced from 712/724 μs to 145/157 μs. See for more details.

**Table 5-13. Frequency Synthesizer Calibration Times (26- and 27-MHz Crystal)**

TEST0	FSCAL3.CHP_CURR_CAL_EN	FS Calibration Time $f_{\text{xosc}} = 26 \text{ MHz}$	FS Calibration Time $f_{\text{xosc}} = 27 \text{ MHz}$
0x09	00b	$3764/f_{\text{xosc}} = 145 \mu\text{s}$	$3764/f_{\text{xosc}} = 139 \mu\text{s}$
0x09	10b	$18506/f_{\text{xosc}} = 712 \mu\text{s}$	$18506/f_{\text{xosc}} = 685 \mu\text{s}$
0x0B	00b	$4073/f_{\text{xosc}} = 157 \mu\text{s}$	$4073/f_{\text{xosc}} = 151 \mu\text{s}$
0x0B	10b	$18815/f_{\text{xosc}} = 724 \mu\text{s}$	$18815/f_{\text{xosc}} = 697 \mu\text{s}$



## 5.14 RX FIFO

The CC113L contains a 64-byte RX FIFO for received data and the SPI interface is used to read the RX FIFO (see [Section 5.5.5](#) for more details). The FIFO controller will detect overflow in the RX FIFO.

When reading the RX FIFO the MCU must avoid reading it past its empty value since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

Likewise, when reading the RX FIFO the MCU must avoid reading the RX FIFO past its empty value since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

The chip status byte that is available on the SO pin while transferring the SPI header contains the fill grade of the RX FIFO ( $R/\overline{W} = 1$ ). [Section 5.5.1](#) contains more details on this.

The number of bytes in the RX FIFO can also be read from the status register RXBYTES.NUM\_RXBYTES. If a received data byte is written to the RX FIFO at the exact same time as the last byte in the RX FIFO is read over the SPI interface, the RX FIFO pointer is not properly updated and the last read byte will be duplicated. To avoid this problem, the RX FIFO should never be emptied before the last byte of the packet is received.

For packet lengths less than 64 bytes it is recommended to wait until the complete packet has been received before reading it out of the RX FIFO.

If the packet length is larger than 64 bytes, the MCU must determine how many bytes can be read from the RX FIFO (RXBYTES.NUM\_RXBYTES-1). The following software routine can be used:

1. Read RXBYTES.NUM\_RXBYTES repeatedly at a rate specified to be at least twice that of which RF bytes are received until the same value is returned twice; store value in n.
2. If  $n < \#$  of bytes remaining in packet, read n-1 bytes from the RX FIFO.
3. Repeat steps 1 and 2 until  $n =$  number of bytes remaining in packet.
4. Read the remaining bytes from the RX FIFO.

The 4-bit [FIFOTH.R.FIFO\\_THR](#) setting is used to program threshold points in the FIFOs.

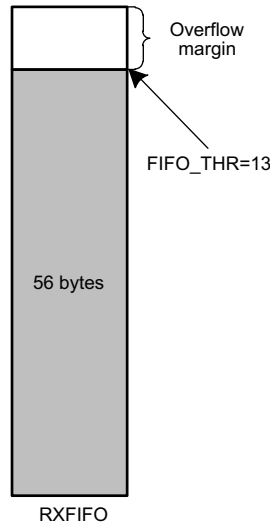
[Table 5-14](#) lists the 16 FIFO\_THR settings and the corresponding thresholds for the RX FIFO.

**Table 5-14. FIFO\_THR Settings and the Corresponding FIFO Thresholds**

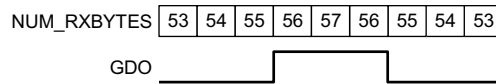
FIFO_THR	Bytes in RX FIFO
0 (0000)	4
1 (0001)	8
2 (0010)	12
3 (0011)	16
4 (0100)	20
5 (0101)	24
6 (0110)	28
7 (0111)	32
8 (1000)	36
9 (1001)	40
10 (1010)	44
11 (1011)	48
12 (1100)	52
13 (1101)	56
14 (1110)	60
15 (1111)	64

A signal will assert when the number of bytes in the RX FIFO is equal to or higher than the programmed threshold. This signal can be viewed on the GDO pins (see [Table 5-15](#)).

[Figure 5-14](#) shows the number of bytes in the RX FIFO when the threshold signal toggles in the case of FIFO\_THR=13. [Figure 5-15](#) shows the signal on the GDO pin as the RX FIFO is filled above the threshold, and then drained below in the case of FIFO\_THR=13.



**Figure 5-14. Example of RX FIFO at Threshold**



**Figure 5-15. Number of Bytes in RX FIFO vs. the GDO Signal (GDOx\_CFG=0x00 and FIFO\_THR=13)**

## 5.15 Frequency Programming

The frequency programming in CC113L is designed to minimize the programming needed when changing frequency.

To set up a system with channel numbers, the desired channel spacing is programmed with the [MDMCFG0.CHANSPC\\_M](#) and [MDMCFG1.CHANSPC\\_E](#) registers. The channel spacing registers are mantissa and exponent respectively. The base or start frequency is set by the 24 bit frequency word located in the [FREQ2](#), [FREQ1](#), and [FREQ0](#) registers. This word will typically be set to the center of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, [CHANNR.CHAN](#), which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{\text{carrier}} = \frac{f_{\text{XOSC}}}{2^{16}} \cdot (\text{FREQ} + \text{CHAN} \cdot ((256 + \text{CHANSPC\_M}) \cdot 2^{\text{CHANSPC\_E}-2})) \quad (7)$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get that is, 1-MHz channel spacing, one solution is to use 333 kHz channel spacing and select each third channel in [CHANNR.CHAN](#).

The preferred IF frequency is programmed with the [FSCTRL1.FREQ\\_IF](#) register. The IF frequency is given by:

$$f_{\text{IF}} = \frac{f_{\text{XOSC}}}{2^{10}} \cdot \text{FREQ\_IF} \quad (8)$$

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency should only be updated when the radio is in the IDLE state.

## 5.16 VCO

The VCO is completely integrated on-chip.

### 5.16.1 VCO and PLL Self-Calibration

The VCO characteristics vary with temperature and supply voltage changes as well as the desired operating frequency. In order to ensure reliable operation, CC113L includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in [Table 5-12](#).

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the [MCSM0.FS\\_AUTOCAL](#) register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

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#### NOTE

The calibration values are maintained in SLEEP mode, so the calibration is still valid after waking up from SLEEP mode unless supply voltage or temperature has changed significantly.

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To check that the PLL is in lock, the user can program register [IOCFGx.GDOx\\_CFG](#) to 0x0A, and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1, or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register [FSCAL1](#). The PLL is in lock if the register content is different from 0x3F. Refer also to the CC113L Errata Notes [SWRZ038](#).

For more robust operation, the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

## 5.17 Voltage Regulators

CC113L contains several on-chip linear voltage regulators that generate the supply voltages needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in [Table 3-1](#) and [Table 5-1](#) are not exceeded.

By setting the CSn pin low, the voltage regulator to the digital core turns on and the crystal oscillator starts. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in [Table 5-1](#)).

If the chip is programmed to enter power-down mode (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator for the digital core requires one external decoupling capacitor.

The voltage regulator output should only be used for driving the CC113L.

## 5.18 General Purpose and Test Output Control Pins

The three digital output pins GDO0, GDO1, and GDO2 are general control pins configured with [IOCFG0.GDO0\\_CFG](#), [IOCFG1.GDO1\\_CFG](#), and [IOCFG2.GDO2\\_CFG](#) respectively. [Table 5-15](#) shows the different signals that can be monitored on the GDO pins. These signals can be used as inputs to the MCU.

GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CS<sub>n</sub> is high. The default value for GDO1 is 3-stated which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 135 - 141 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to [IOCFG0.GDO0\\_CFG](#).

If the [IOCFGx.GDOx\\_CFG](#) setting is less than 0x20 and [IOCFGx\\_GDOx\\_INV](#) is 0 (1), the GDO0 and GDO2 pins will be hardwired to 0 (1), and the GDO1 pin will be hardwired to 1 (0) in the SLEEP state. These signals will be hardwired until the CHIP\_RDY<sub>n</sub> signal goes low.

If the [IOCFGx.GDOx\\_CFG](#) setting is 0x20 or higher, the GDO pins will work as programmed also in SLEEP state. As an example, GDO1 is high impedance in all states if [IOCFG1.GDO1\\_CFG=0x2E](#).

**Table 5-15. GDOx Signal Selection (x = 0, 1, or 2)**

GDOx_CFG[5:0]	Description <sup>(1)</sup>
0 (0x00)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold. Deasserts when RX FIFO is drained below the same threshold.
1 (0x01)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold or the end of packet is reached. Deasserts when the RX FIFO is empty.
2 (0x02) – 3 (0x03)	Reserved - used for test.
4 (0x04)	Asserts when the RX FIFO has overflowed. Deasserts when the FIFO has been flushed.
5 (0x05)	Reserved - used for test.
6 (0x06)	Asserts when sync word has been received, and de-asserts at the end of the packet. The pin will also de-assert when a packet is discarded due to address or maximum length filtering or when the radio enters RXFIFO_OVERFLOW state.
7 (0x07)	Asserts when a packet has been received with CRC OK. Deasserts when the first byte is read from the RX FIFO.
8 (0x08)	Reserved - used for test.
9 (0x09)	Clear channel assessment. High when RSSI level is below threshold (dependent on the current CCA_MODE setting).
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. Data is set up on the falling edge by CC113L when <a href="#">GDOx_INV=0</a> .
12 (0x0C)	Serial Synchronous Data Output. Used for synchronous serial mode.
13 (0x0D)	Serial Data Output. Used for asynchronous serial mode.
14 (0x0E)	Carrier sense. High if RSSI level is above threshold. Cleared when entering IDLE mode.
15 (0x0F)	CRC_OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.
16 (0x10) – 27 (0x1B)	Reserved - used for test.
28 (0x1C)	LNA_PD. Note: LNA_PD will have the same signal level in SLEEP and RX states. To control an external LNA in applications where the SLEEP state is used it is recommended to use <a href="#">GDOx_CFGx=0x2F</a> instead.
29 (0x1D) – 38 (0x26)	Reserved - used for test.
39 (0x27)	CLK_32k.
40 (0x28)	Reserved - used for test.

(1) There are 3 GDO pins, but only one CLK\_XOSC/n can be selected as an output at any time. If CLK\_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK\_XOSC/192. To optimize RF performance, these signals should not be used while the radio is in RX.

**Table 5-15. GDOx Signal Selection (x = 0, 1, or 2) (continued)**

GDOx_CFG[5:0]	Description <sup>(1)</sup>
41 (0x29)	CHIP_RDYn.
42 (0x2A)	Reserved - used for test.
43 (0x2B)	XOSC_STABLE.
44 (0x2C) – 45 (0x2D)	Reserved - used for test.
46 (0x2E)	High impedance (3-state).
47 (0x2F)	HW to 0 (HW1 achieved by setting GDOx_INV=1). Can be used to control an external LNA
48 (0x30)	CLK_XOSC/1
49 (0x31)	CLK_XOSC/1.5
50 (0x32)	CLK_XOSC/2
51 (0x33)	CLK_XOSC/3
52 (0x34)	CLK_XOSC/4
53 (0x35)	CLK_XOSC/6
54 (0x36)	CLK_XOSC/8
55 (0x37)	CLK_XOSC/12
56 (0x38)	CLK_XOSC/16
57 (0x39)	CLK_XOSC/24
58 (0x3A)	CLK_XOSC/32
59 (0x3B)	CLK_XOSC/48
60 (0x3C)	CLK_XOSC/64
61 (0x3D)	CLK_XOSC/96
62 (0x3E)	CLK_XOSC/128
63 (0x3F)	CLK_XOSC/192

Note: There are 3 GDO pins, but only one CLK\_XOSC/n can be selected as an output at any time. If CLK\_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK\_XOSC/192.  
To optimize RF performance, these signals should not be used while the radio is in RX mode.

## 5.19 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the CC113L to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller, and simplify software development.

### 5.19.1 Asynchronous Serial Operation

Asynchronous transfer is included in the CC113L for backward compatibility with systems that are already using the asynchronous data transfer.

When asynchronous transfer is enabled, all packet handling support is disabled and it is not possible to use Manchester encoding.

Asynchronous serial mode is enabled by setting `PKTCTRL0.PKT_FORMAT` to 3. Data output can be on GDO0, GDO1, or GDO2. This is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG` and `IOCFG2.GDO2_CFG` fields.

In asynchronous serial mode no data decision is done on-chip and the raw data is put on the data output line. When using asynchronous serial mode make sure the interfacing MCU does proper oversampling and that it can handle the jitter on the data output line. The MCU should tolerate a jitter of  $\pm 1/8$  of a bit period as the data stream is time-discrete using 8 samples per bit.

In asynchronous serial mode there will be glitches of 37 - 38.5 ns duration ( $1/XOSC$ ) occurring infrequently and with random periods. A simple RC filter can be added to the data output line between CC113L and the MCU to get rid of the 37 - 38.5 ns glitches if considered a problem. The filter 3 dB cut-off frequency needs to be high enough so that the data is not filtered and at the same time low enough to remove the glitch. As an example, for 2.4 kBaud data rate a 1 k $\Omega$  resistor and 2.7 nF capacitor can be used. This gives a 3 dB cut-off frequency of 59 kHz.

### 5.19.2 Synchronous Serial Operation

Setting `PKTCTRL0.PKT_FORMAT` to 1 enables synchronous serial mode. When using this mode, sync detection should be disabled together with CRC calculation ( `MDMCFG2.SYNC_MODE=000` and `PKTCTRL0.CRC_EN=0`). Infinite packet length mode should be used ( `PKTCTRL0.LENGTH_CONFIG=10b`).

In synchronous serial mode, data is transferred on a two-wire serial interface. The CC113L provides a clock that is used to sample data on the data output line. The data output pin can be any of the GDO pins. This is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG`, and `IOCFG2.GDO2_CFG` fields. The RX latency is 9 bits.

The MCU must handle preamble and sync word detection in software, together with CRC calculation.

## 5.20 System Consideration and Guidelines

### 5.20.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. Short Range Devices (SRDs) for license free operation below 1 GHz are usually operated in the 315 MHz, 433 MHz, 868 MHz or 915 MHz frequency bands. The CC113L is specifically designed for such use with its 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz operating ranges. The most important regulations when using the CC113L in the 315 MHz, 433 MHz, 868 MHz, or 915 MHz frequency bands are EN 300 220 V2.3.1 (Europe) and FCC CFR47 part 15 (USA).

For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.

Please note that compliance with regulations is dependent on the complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

### 5.20.2 Calibration in Multi-Channel Systems

CC113L is highly suited for multi-channel systems due to its agile frequency synthesizer and effective communication interface.

Charge pump current, VCO current, and VCO capacitance array calibration data is required for each frequency when implementing a multi-channel system. There are 3 ways of obtaining the calibration data from the chip:

1. Calibration for every frequency change. The PLL calibration time is 712/724  $\mu$ s (26 MHz crystal and TEST0 = 0x09/0B, see [Table 5-13](#)). The blanking interval between each frequency is then 787/799  $\mu$ s.
2. Perform all necessary calibration at startup and store the resulting FSCAL3, FSCAL2, and FSCAL1 register values in MCU memory. The VCO capacitance calibration FSCAL1 register value must be found for each RF frequency to be used. The VCO current calibration value and the charge pump current calibration value available in FSCAL2 and FSCAL3 respectively are not dependent on the RF frequency, so the same value can therefore be used for all RF frequencies for these two registers. Between each frequency change, the calibration process can then be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values that corresponds to the next RF frequency. The PLL turn on time is approximately 75  $\mu$ s ([Table 5-12](#)). The blanking interval between each frequency hop is then approximately 75  $\mu$ s.
3. Run calibration on a single frequency at startup. Next write 0 to FSCAL3[5:4] to disable the charge pump calibration. After writing to FSCAL3[5:4], strobe SRX with MCSM0.FS\_AUTOCAL=1 for each new frequency. That is, VCO current and VCO capacitance calibration is done, but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from 712/724  $\mu$ s to 145/157  $\mu$ s (26 MHz crystal and TEST0 = 0x09/0B, see [Table 5-13](#)). The blanking interval between each frequency hop is then 220/232  $\mu$ s.

There is a trade-off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. This solution also requires that the supply voltage and temperature do not vary much in order to have a robust solution. Solution 3) gives 567  $\mu$ s smaller blanking interval than solution 1).

The recommended settings for TEST0.VCO\_SEL\_CAL\_EN change with frequency. This means that one should always use SmartRF Studio [4] to get the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is being used.

#### NOTE

The content in the TEST0 register is not retained in SLEEP state, thus it is necessary to re-write this register when returning from the SLEEP state.



## 5.21 Configuration Registers

The configuration of CC113L is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF Studio software [SWRC176](#). Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 8 command strobe registers, listed in [Table 5-16](#). Accessing these registers will initiate the change of an internal state or mode. There are 43 normal 8-bit configuration registers listed in [Table 5-17](#) and SmartRF Studio will provide recommended settings for these registers (Addresses marked as “Not Used” can be part of a burst access and one can write a dummy value to them. Addresses marked as “Reserved” must be configured according to SmartRF Studio ).

There are also 8 status registers that are listed in [Table 5-18](#). These registers, which are read-only, contain information about the status of CC113L.

The RX FIFO is accessed through one 8-bit register. During the header byte transfer and while writing data to a register, a status byte is returned on the SO line. This status byte is described in [Table 5-2](#)

[Table 5-19](#) summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

**Table 5-16. Command Strobes**

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	Reserved	
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode ( <a href="#">MCSM0.FS_AUTOCAL=0</a> )
0x34	SRX	In IDLE state: Enable RX. Perform calibration first if <a href="#">MCSM0.FS_AUTOCAL=1</a> .
0x35	Reserved	
0x36	SIDLE	Enter IDLE state
0x37 - 0x38	Reserved	
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B - 0x3C	Reserved	
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

**Table 5-17. Configuration Registers Overview**

Address	Register	Description	Preserved in SLEEP State	Section
0x00	IOCFG2	GDO2 output pin configuration	Yes	<a href="#">Table 5-20</a>
0x01	IOCFG1	GDO1 output pin configuration	Yes	<a href="#">Table 5-21</a>
0x02	IOCFG0	GDO0 output pin configuration	Yes	<a href="#">Table 5-22</a>
0x03	FIFOTHR	RX FIFO thresholds	Yes	<a href="#">Table 5-23</a>
0x04	SYNC1	Sync word, high byte	Yes	<a href="#">Table 5-24</a>
0x05	SYNC0	Sync word, low byte	Yes	<a href="#">Table 5-25</a>
0x06	PKTLEN	Packet length	Yes	<a href="#">Table 5-26</a>
0x07	PKTCTRL1	Packet automation control	Yes	<a href="#">Table 5-27</a>
0x08	PKTCTRL0	Packet automation control	Yes	<a href="#">Table 5-28</a>
0x09	ADDR	Device address	Yes	<a href="#">Table 5-29</a>
0x0A	CHANNR	Channel number	Yes	<a href="#">Table 5-30</a>
0x0B	FSCTRL1	Frequency synthesizer control	Yes	<a href="#">Table 5-31</a>
0x0C	FSCTRL0	Frequency synthesizer control	Yes	<a href="#">Table 5-32</a>
0x0D	FREQ2	Frequency control word, high byte	Yes	<a href="#">Table 5-33</a>
0x0E	FREQ1	Frequency control word, middle byte	Yes	<a href="#">Table 5-34</a>
0x0F	FREQ0	Frequency control word, low byte	Yes	<a href="#">Table 5-35</a>
0x10	MDMCFG4	Modem configuration	Yes	<a href="#">Table 5-36</a>
0x11	MDMCFG3	Modem configuration	Yes	<a href="#">Table 5-37</a>
0x12	MDMCFG2	Modem configuration	Yes	<a href="#">Table 5-38</a>
0x13	MDMCFG1	Modem configuration	Yes	<a href="#">Table 5-39</a>
0x14	MDMCFG0	Modem configuration	Yes	<a href="#">Table 5-40</a>
0x15	DEVIATN	Modem deviation setting	Yes	<a href="#">Table 5-41</a>
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	<a href="#">Table 5-42</a>
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	<a href="#">Table 5-43</a>
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	<a href="#">Table 5-44</a>
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	<a href="#">Table 5-45</a>
0x1A	BSCFG	Bit Synchronization configuration	Yes	<a href="#">Table 5-46</a>
0x1B	AGCCTRL2	AGC control	Yes	<a href="#">Table 5-47</a>
0x1C	AGCCTRL1	AGC control	Yes	<a href="#">Table 5-48</a>
0x1D	AGCCTRL0	AGC control	Yes	<a href="#">Table 5-49</a>
0x1E - 0x1F	Not Used			
0x20	RESERVED		Yes	<a href="#">Table 5-50</a>
0x21	FREND1	Front end RX configuration	Yes	<a href="#">Table 5-51</a>
0x22	Not Used			
0x23	FSCAL3	Frequency synthesizer calibration	Yes	<a href="#">Table 5-52</a>
0x24	FSCAL2	Frequency synthesizer calibration	Yes	<a href="#">Table 5-53</a>
0x25	FSCAL1	Frequency synthesizer calibration	Yes	<a href="#">Table 5-54</a>
0x26	FSCAL0	Frequency synthesizer calibration	Yes	<a href="#">Table 5-55</a>
0x27 - 0x28	Not Used			
0x29 - 0x2B	RESERVED		No	<a href="#">Table 5-56</a>
0x2C	TEST2	Various test settings	No	<a href="#">Table 5-59</a>
0x2D	TEST1	Various test settings	No	<a href="#">Table 5-60</a>
0x2E	TEST0	Various test settings	No	<a href="#">Table 5-61</a>

**Table 5-18. Status Registers Overview**

Address	Register	Description	Section
0x30 (0xF0)	PARTNUM	Part number for CC113L	<a href="#">Table 5-62</a>
0x31 (0xF1)	VERSION	Current version number	<a href="#">Table 5-63</a>
0x32 (0xF2)	FREQEST	Frequency Offset Estimate	<a href="#">Table 5-64</a>
0x33 (0xF3)	CRC_REG	CRC OK	<a href="#">Table 5-65</a>
0x34 (0xF4)	RSSI	Received signal strength indication	<a href="#">Table 5-66</a>
0x35 (0xF5)	MARCSTATE	Control state machine state	<a href="#">Table 5-67</a>
0x36 - 0x37 (0xF6 – 0xF7)	Reserved		
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	<a href="#">Table 5-68</a>
0x39 – 0x3A (0xF9 – 0xFA)	Reserved		
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	<a href="#">Table 5-69</a>
0x3C – 0x3D (0xFC – 0xFD)	Reserved		

**Table 5-19. SPI Address Space**

	Write		Read		
	Single Byte	Burst	Single Byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00					IOCFG2
0x01					IOCFG1
0x02					IOCFG0
0x03					FIFOTHR
0x04					SYNC1
0x05					SYNC0
0x06					PKTLEN
0x07					PKTCTRL1
0x08					PKTCTRL0
0x09					ADDR
0x0A					CHANNR
0x0B					FSCTRL1
0x0C					FSCTRL0
0x0D					FREQ2
0x0E					FREQ1
0x0F					FREQ0
0x10					MDMCFG4
0x11					MDMCFG3
0x12					MDMCFG2
0x13					MDMCFG1
0x14					MDMCFG0
0x15					DEVIATN
0x16					MCSM2
0x17					MCSM1
0x18					MCSM0
0x19					FOCCFG
0x1A					BSCFG
0x1B					AGCCTRL2
0x1C					AGCCTRL1
0x1D					AGCCTRL0
0x1E					Not Used
0x1F					Not Used
0x20					RESERVED
0x21					FREND1
0x22					Not Used
0x23					FSCAL3
0x24					FSCAL2
0x25					FSCAL1
0x26					FSCAL0
0x27					Not Used
0x28					Not Used
0x29					RESERVED
0x2A					RESERVED
0x2B					RESERVED
0x2C					TEST2
0x2D					TEST1
0x2E					TEST0
0x2F					Not Used

RW configuration registers, burst access possible

**Table 5-19. SPI Address Space (continued)**

	Write		Read		
	Single Byte	Burst	Single Byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers
0x31	Reserved		Reserved	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	CRC_REG	
0x34	SRX		SRX	RSSI	
0x35	Reserved		Reserved	MARCSTATE	
0x36	SIDLE		SIDLE	Reserved	
0x37	Reserved		Reserved	Reserved	
0x38	Reserved		Reserved	PKTSTATUS	
0x39	SPWD		SPWD	Reserved	
0x3A	SFRX		SFRX	Reserved	
0x3B	Reserved		Reserved	RXBYTES	
0x3C	Reserved		Reserved	Reserved	
0x3D	SNOP		SNOP	Reserved	
0x3E	Reserved		Reserved	Reserved	
0x3F	Reserved		RX FIFO	RX FIFO	

### 5.21.1 Configuration Register Details - Registers with preserved values in SLEEP state

**Table 5-20. 0x00: IOCFG2 - GDO2 Output Pin Configuration**

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	GDO2_INV	0	R/W	Invert output, that is, select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (101001)	R/W	Default is CHP_RDYn (see <a href="#">Table 5-15</a> ).

**Table 5-21. 0x01: IOCFG1 - GDO1 Output Pin Configuration**

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, that is, select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (101110)	R/W	Default is 3-state (see <a href="#">Table 5-15</a> ).

**Table 5-22. 0x02: IOCFG0 - GDO0 Output Pin Configuration**

Bit	Field Name	Reset	R/W	Description
7		0	R/W	Use setting from SmartRF Studio
6	GDO0_INV	0	R/W	Invert output, that is, select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (see <a href="#">Table 5-15</a> ). It is recommended to disable the clock output in initialization, in order to optimize RF performance.

**Table 5-23. 0x03: FIFOTHR - RX FIFO Thresholds**

Bit	Field Name	Reset	R/W	Description																																		
7		0	R/W	Use setting from SmartRF Studio																																		
6	ADC_RETENTION	0	R/W	<p>0: TEST1 = 0x31 and TEST2= 0x88 when waking up from SLEEP</p> <p>1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP</p> <p>Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode will always be the reset value.</p> <p>The ADC_RETENTION bit should be set to 1 before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.</p>																																		
5:4	CLOSE_IN_RX[1:0]	0 (00)	R/W	<p>For more details, see DN010 <a href="#">SWRA147</a></p> <table border="1"> <thead> <tr> <th>Setting</th> <th>RX Attenuation, Typical Values</th> </tr> </thead> <tbody> <tr> <td>0 (00)</td> <td>0 dB</td> </tr> <tr> <td>1 (01)</td> <td>6 dB</td> </tr> <tr> <td>2 (10)</td> <td>12 dB</td> </tr> <tr> <td>3 (11)</td> <td>18 dB</td> </tr> </tbody> </table>	Setting	RX Attenuation, Typical Values	0 (00)	0 dB	1 (01)	6 dB	2 (10)	12 dB	3 (11)	18 dB																								
Setting	RX Attenuation, Typical Values																																					
0 (00)	0 dB																																					
1 (01)	6 dB																																					
2 (10)	12 dB																																					
3 (11)	18 dB																																					
3:0	FIFO_THR[3:0]	7 (0111)	R/W	<p>Set the threshold for the RX FIFO. The threshold is exceeded when the number of bytes in the RX FIFO is equal to or higher than the threshold value.</p> <table border="1"> <thead> <tr> <th>Setting</th> <th>Bytes in RX FIFO</th> </tr> </thead> <tbody> <tr><td>0 (0000)</td><td>4</td></tr> <tr><td>1 (0001)</td><td>8</td></tr> <tr><td>2 (0010)</td><td>12</td></tr> <tr><td>3 (0011)</td><td>16</td></tr> <tr><td>4 (0100)</td><td>20</td></tr> <tr><td>5 (0101)</td><td>24</td></tr> <tr><td>6 (0110)</td><td>28</td></tr> <tr><td>7 (0111)</td><td>32</td></tr> <tr><td>8 (1000)</td><td>36</td></tr> <tr><td>9 (1001)</td><td>40</td></tr> <tr><td>10 (1010)</td><td>44</td></tr> <tr><td>11 (1011)</td><td>48</td></tr> <tr><td>12 (1100)</td><td>52</td></tr> <tr><td>13 (1101)</td><td>56</td></tr> <tr><td>14 (1110)</td><td>60</td></tr> <tr><td>15 (1111)</td><td>64</td></tr> </tbody> </table>	Setting	Bytes in RX FIFO	0 (0000)	4	1 (0001)	8	2 (0010)	12	3 (0011)	16	4 (0100)	20	5 (0101)	24	6 (0110)	28	7 (0111)	32	8 (1000)	36	9 (1001)	40	10 (1010)	44	11 (1011)	48	12 (1100)	52	13 (1101)	56	14 (1110)	60	15 (1111)	64
Setting	Bytes in RX FIFO																																					
0 (0000)	4																																					
1 (0001)	8																																					
2 (0010)	12																																					
3 (0011)	16																																					
4 (0100)	20																																					
5 (0101)	24																																					
6 (0110)	28																																					
7 (0111)	32																																					
8 (1000)	36																																					
9 (1001)	40																																					
10 (1010)	44																																					
11 (1011)	48																																					
12 (1100)	52																																					
13 (1101)	56																																					
14 (1110)	60																																					
15 (1111)	64																																					

**Table 5-24. 0x04: SYNC1 - Sync Word, High Byte**

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

**Table 5-25. 0x05: SYNC0 - Sync Word, Low Byte**

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

**Table 5-26. 0x06: PKTLEN - Packet Length**

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed. This value must be different from 0.

**Table 5-27. 0x07: PKTCTRL1 - Packet Automation Control**

Bit	Field Name	Reset	R/W	Description	
7:5		0 (000)	R/W	Use setting from SmartRF Studio	
4		0	R0	Not Used.	
3	CRC_AUTOFLUSH	0	R/W	Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RX FIFO and that packet length is limited to the RX FIFO size.	
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain the RSSI value, as well as CRC OK.	
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages.	
				Setting	Address check configuration
				0 (00)	No address check
				1 (01)	Address check, no broadcast
				2 (10)	Address check and 0 (0x00) broadcast
3 (11)	Address check and 0 (0x00) and 255 (0xFF) broadcast				

**Table 5-28. 0x08: PKTCTRL0 - Packet Automation Control**

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used	
6		1	R/W	Use setting from SmartRF Studio	
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX data	
				Setting	Packet format
				0 (00)	Normal mode, use RX FIFO
				1 (01)	Synchronous serial mode. Data in on GDO0 and data out on either of the GDOx pins
				2 (10)	Reserved
3 (11)	Asynchronous serial mode. Data in on GDO0 and data out on either of the GDOx pins				
3		0	R0	Not used	
2	CRC_EN	1	R/W	1: CRC calculation enabled 0: CRC calculation disabled	
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length	
				Setting	Packet length configuration
				0 (00)	Fixed packet length mode. Length configured in PKTLEN register
				1 (01)	Variable packet length mode. Packet length configured by the first byte after sync word
				2 (10)	Infinite packet length mode
3 (11)	Reserved				

**Table 5-29. 0x09: ADDR - Device Address**

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

**Table 5-30. 0x0A: CHANNR - Channel Number**

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

**Table 5-31. 0x0B: FSCTRL1 - Frequency Synthesizer Control**

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5		0	R/W	Use setting from SmartRF Studio
4:0	FREQ_IF[4:0]	15 (01111)	R/W	<p>The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator.</p> $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ <p>The default value gives an IF frequency of 381kHz, assuming a 26.0 MHz crystal.</p>

**Table 5-32. 0x0C: FSCTRL0 - Frequency Synthesizer Control**

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer. (2s-complement). Resolution is $FXTAL/2^{14}$ (1.59 kHz-1.65 kHz); range is $\pm 202$ kHz to $\pm 210$ kHz, dependent of XTAL frequency.

**Table 5-33. 0x0D: FREQ2 - Frequency Control Word, High Byte**

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0 (00)	R	FREQ[23:22] is always 0 (the FREQ2 register is less than 36 with 26 - 27 MHz crystal)
5:0	FREQ[21:16]	30 (011110)	R/W	<p>FREQ[23:0] is the base frequency for the frequency synthesizer in increments of <math>f_{XOSC}/2^{16}</math>.</p> $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23 : 0]$

**Table 5-34. 0x0E: FREQ1 - Frequency Control Word, Middle Byte**

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	See <a href="#">Table 5-33</a> .

**Table 5-35. 0x0F: FREQ0 - Frequency Control Word, Low Byte**

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	See <a href="#">Table 5-33</a> .



**Table 5-36. 0x10: MDMCFG4 - Modem Configuration**

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (10)	R/W	
5:4	CHANBW_M[1:0]	0 (00)	R/W	<p>Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth.</p> $BW_{\text{channel}} = \frac{f_{\text{XOSC}}}{8 \cdot (4 + \text{CHANBW\_M}) \cdot 2^{\text{CHANBW\_E}}}$ <p>The default values give 203 kHz channel filter bandwidth, assuming a 26.0 MHz crystal.</p>
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

**Table 5-37. 0x11: MDMCFG3 - Modem Configuration**

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	<p>The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is:</p> $R_{\text{DATA}} = \frac{(256 + \text{DRATE\_M}) \cdot 2^{\text{DRATE\_E}}}{2^{28}} \cdot f_{\text{XOSC}}$ <p>The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.</p>

**Table 5-38. 0x12: MDMCFG2 - Modem Configuration**

Bit	Field Name	Reset	R/W	Description	
7	DEM_DCFILT_OFF	0	R/W	<p>Disable digital DC blocking filter before demodulator.</p> <p>0 = Enable (better sensitivity)</p> <p>1 = Disable (current optimized). Only for data rates ≤ 250 kBaud</p> <p>The recommended IF frequency changes when the DC blocking is disabled. Use SmartRF Studio to calculate correct register setting.</p>	
6:4	MOD_FORMAT[2:0]	0 (000)	R/W	The modulation format of the radio signal	
				Setting	Modulation format
				0 (000)	2-FSK
				1 (001)	GFSK
				2 (010)	Reserved
				3 (011)	OOK
				4 (100)	4-FSK
				5 (101)	Reserved
				6 (110)	Reserved
7 (111)	Reserved				
				4-FSK modulation cannot be used together with Manchester encoding	
3	MANCHESTER_EN	0	R/W	<p>Enables Manchester decoding.</p> <p>0 = Disable</p> <p>1 = Enable</p> <p>Manchester encoding cannot be used when using asynchronous serial mode or 4-FSK modulation</p>	
2:0	SYNC_MODE[2:0]	2 (010)	R/W	Combined sync-word qualifier mode.	
				The values 0 and 4 disables preamble and sync word detection	
				The values 1, 2, 5, and 6 enables 16-bit sync word detection. Only 15 of 16 bits need to match when using setting 1 or 5. The values 3 and 7 enables 32-bits sync word detection (only 30 of 32 bits need to match).	
				Setting	Sync-word qualifier mode
				0 (000)	No preamble/sync
				1 (001)	15/16 sync word bits detected
				2 (010)	16/16 sync word bits detected
				3 (011)	30/32 sync word bits detected
				4 (100)	No preamble/sync, carrier-sense above threshold
5 (101)	15/16 + carrier-sense above threshold				
6 (110)	16/16 + carrier-sense above threshold				
7 (111)	30/32 + carrier-sense above threshold				

**Table 5-39. 0x13: MDMCFG1 - Modem Configuration**

Bit	Field Name	Reset	R/W	Description
7		0	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>
6:2			R0	Not used
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

**Table 5-40. 0x14: MDMCFG0 - Modem Configuration**

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	<p>8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format:</p> $\Delta f_{\text{CHANNEL}} = \frac{f_{\text{XOSC}}}{2^{18}} \cdot (256 + \text{CHANSPC\_M}) \cdot 2^{\text{CHANSPC\_E}}$ <p>The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.</p>

**Table 5-41. 0x15: DEVIATN - Modem Deviation Setting**

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used.	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent.	
3			R0	Not used.	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	2-FSK/GFSK/4-FSK	Specifies the expected frequency deviation of incoming signal, must be approximately right for demodulation to be performed reliably and robustly.
				OOK	This setting has no effect.

**Table 5-42. 0x16: MCSM2 - Main Radio Control State Machine Configuration**

Bit	Field Name	Reset	R/W	Description
7:5			R0	Not used
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3:0		7 (0111)	R/W	Use setting from SmartRF Studio

**Table 5-43. 0x17: MCSM1 - Main Radio Control State Machine Configuration**

Bit	Field Name	Reset	R/W	Description	
7:6			R0	Not used	
5:4		3 (11)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>	
3:2	RXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been received.	
				Setting	Next state after finishing packet reception
				0 (00)	IDLE
				1 (01)	Reserved
				2 (10)	Reserved
3 (11)	Stay in RX				
1:0		0 (00)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>	

**Table 5-44. 0x18: MCSM0 - Main Radio Control State Machine Configuration**

Bit	Field Name	Reset	R/W	Description		
7:6			R0	Not used		
5:4	FS_AUTOCAL[1:0]	0 (00)	R/W	Automatically calibrate when going to or from RX mode		
				Setting	When to perform automatic calibration	
				0 (00)	Never (manually calibrate using SCAL strobe)	
				1 (01)	When going from IDLE to RX	
				2 (10)	When going from RX back to IDLE automatically	
3 (11)	Every 4th time when going from RX to IDLE automatically					
3:2	PO_TIMEOUT	1 (01)	R/W	Programs the number of times the six-bit ripple counter must expire after the XOSC has settled before CHP_RDYn goes low. <sup>(1)</sup> If XOSC is on (stable) during power-down, PO_TIMEOUT shall be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 $\mu$ s. For robust operation it is recommended to use PO_TIMEOUT = 2 or 3 when XOSC is off during power-down.		
				Setting	Expire count	Timeout after XOSC start
				0 (00)	1	Approximately 2.3 - 2.4 $\mu$ s
				1 (01)	16	Approximately 37 - 39 $\mu$ s
				2 (10)	64	Approximately 149 - 155 $\mu$ s
				3 (11)	256	Approximately 597 - 620 $\mu$ s
Exact timeout depends on crystal frequency.						
1		0	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>		
0	XOSC_FORCE_ON	0	R/W	Force the XOSC to stay on in the SLEEP state.		

(1) Note that the XOSC\_STABLE signal will be asserted at the same time as the CHIP\_RDYn signal; that is, the PO\_TIMEOUT delays both signals and does not insert a delay between the signals.

**Table 5-45. 0x19: FOCCFG - Frequency Offset Compensation Configuration**

Bit	Field Name	Reset	R/W	Description	
7:6			R0	Not used	
5	FOC_BS_CS_GATE	1	R/W	If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CS signal goes high.	
4:3	FOC_PRE_K[1:0]	2 (10)	R/W	The frequency compensation loop gain to be used before a sync word is detected.	
				Setting	Freq. compensation loop gain before sync word
				0 (00)	K
				1 (01)	2K
				2 (10)	3K
3 (11)	4K				
2	FOC_POST_K	1	R/W	The frequency compensation loop gain to be used after a sync word is detected.	
				Setting	Freq. compensation loop gain after sync word
				0	Same as FOC_PRE_K
1	K/2				

**Table 5-45. 0x19: FOCCFG - Frequency Offset Compensation Configuration (continued)**

Bit	Field Name	Reset	R/W	Description	
1:0	FOC_LIMIT[1:0]	2 (10)	R/W	The saturation point for the frequency offset compensation algorithm:	
				Setting	Saturation point (max compensated offset)
				0 (00)	±0 (no frequency offset compensation)
				1 (01)	±BW <sub>CHAN</sub> /8
				2 (10)	±BW <sub>CHAN</sub> /4
				3 (11)	±BW <sub>CHAN</sub> /2
Frequency offset compensation is not supported for OOK. Always use FOC_LIMIT=0 with this modulation format.					

**Table 5-46. 0x1A: BSCFG - Bit Synchronization Configuration**

Bit	Field Name	Reset	R/W	Description	
7:6	BS_PRE_KI[1:0]	1 (01)	R/W	The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):	
				Setting	Clock recovery loop integral gain before sync word
				0 (00)	K <sub>I</sub>
				1 (01)	2K <sub>I</sub>
				2 (10)	3K <sub>I</sub>
5:4	BS_PRE_KP[1:0]	2 (10)	R/W	The clock recovery feedback loop proportional gain to be used before a sync word is detected.	
				Setting	Clock recovery loop proportional gain before sync word
				0 (00)	K <sub>P</sub>
				1 (01)	2K <sub>P</sub>
				2 (10)	3K <sub>P</sub>
3	BS_POST_KI	1	R/W	The clock recovery feedback loop integral gain to be used after a sync word is detected.	
				Setting	Clock recovery loop integral gain after sync word
				0	Same as BS_PRE_KI
2	BS_POST_KP	1	R/W	The clock recovery feedback loop proportional gain to be used after a sync word is detected.	
				Setting	Clock recovery loop proportional gain after sync word
				0	Same as BS_PRE_KP
1:0	BS_LIMIT[1:0]	0 (00)	R/W	The saturation point for the data rate offset compensation algorithm:	
				Setting	Data rate offset saturation (max data rate difference)
				0 (00)	±0 (No data rate offset compensation performed)
				1 (01)	±3.125 % data rate offset
				2 (10)	±6.25 % data rate offset
3 (11)	±12.5 % data rate offset				

**Table 5-47. 0x1B: AGCTRL2 - AGC Control**

Bit	Field Name	Reset	R/W	Description	
7:6	MAX_DVGA_GAIN[1:0]	0 (00)	R/W	Reduces the maximum allowable DVGA gain.	
				Setting	Allowable DVGA settings
				0 (00)	All gain settings can be used
				1 (01)	The highest gain setting cannot be used
				2 (10)	The 2 highest gain settings cannot be used
				3 (11)	The 3 highest gain settings cannot be used
5:3	MAX_LNA_GAIN[2:0]	0 (000)	R/W	Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.	
				Setting	Maximum allowable LNA + LNA 2 gain
				0 (000)	Maximum possible LNA + LNA 2 gain
				1 (001)	Approximately 2.6 dB below maximum possible gain
				2 (010)	Approximately 6.1 dB below maximum possible gain
				3 (011)	Approximately 7.4 dB below maximum possible gain
				4 (100)	Approximately 9.2 dB below maximum possible gain
				5 (101)	Approximately 11.5 dB below maximum possible gain
				6 (110)	Approximately 14.6 dB below maximum possible gain
7 (111)	Approximately 17.1 dB below maximum possible gain				
2:0	MAGN_TARGET[2:0]	3 (011)	R/W	These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).	
				Setting	Target amplitude from channel filter
				0 (000)	24 dB
				1 (001)	27 dB
				2 (010)	30 dB
				3 (011)	33 dB
				4 (100)	36 dB
				5 (101)	38 dB
				6 (110)	40 dB
7 (111)	42 dB				

**Table 5-48. 0x1C: AGCTRL1 - AGC Control**

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used	
6	AGC_LNA_PRIORITY	1	R/W	Selects between two different strategies for LNA and LNA 2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA 2 gain is decreased to minimum before decreasing LNA gain.	
5:4	CARRIER_SENSE_REL_THR[1:0]	0 (00)	R/W	Sets the relative change threshold for asserting carrier sense	
				Setting	Carrier sense relative threshold
				0 (00)	Relative carrier sense threshold disabled
				1 (01)	6 dB increase in RSSI value
				2 (10)	10 dB increase in RSSI value
3 (11)	14 dB increase in RSSI value				

**Table 5-48. 0x1C: AGCCTRL1 - AGC Control (continued)**

Bit	Field Name	Reset	R/W	Description	
3:0	CARRIER_SENSE_ABS_THR[3:0]	0 (0000)	R/W	Sets the absolute RSSI threshold for asserting carrier sense. The 2-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.	
				Setting	Carrier sense absolute threshold (Equal to channel filter amplitude when AGC has not decreased gain)
				-8 (1000)	Absolute carrier sense threshold disabled
				-7 (1001)	7 dB below MAGN_TARGET setting
				...	...
				-1 (1111)	1 dB below MAGN_TARGET setting
				0 (0000)	At MAGN_TARGET setting
				1 (0001)	1 dB above MAGN_TARGET setting
				...	...
				7 (0111)	7 dB above MAGN_TARGET setting

**Table 5-49. 0x1D: AGCCTRL0 - AGC Control**

Bit	Field Name	Reset	R/W	Description	
7:6	HYST_LEVEL[1:0]	2 (10)	R/W	Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determine gain changes).	
				Setting	Description
				0 (00)	No hysteresis, small symmetric dead zone, high gain
				1 (01)	Low hysteresis, small asymmetric dead zone, medium gain
				2 (10)	Medium hysteresis, medium asymmetric dead zone, medium gain
3 (11)	Large hysteresis, large asymmetric dead zone, low gain				
5:4	WAIT_TIME[1:0]	1 (01)	R/W	Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.	
				Setting	Channel filter samples
				0 (00)	8
				1 (01)	16
				2 (10)	24
3 (11)	32				
3:2	AGC_FREEZE[1:0]	0 (00)	R/W	Control when the AGC gain should be frozen.	
				Setting	Function
				0 (00)	Normal operation. Always adjust gain when required.
				1 (01)	The gain setting is frozen when a sync word has been found.
2 (10)	Manually freeze the analogue gain setting and continue to adjust the digital gain.				
3 (11)	Manually freezes both the analogue and the digital gain setting. Used for manually overriding the gain.				

**Table 5-49. 0x1D: AGCTRL0 - AGC Control (continued)**

Bit	Field Name	Reset	R/W	Description		
1:0	FILTER_LENGTH[1:0]	1(01)	R/W	2-FSK and 4-FSK: Sets the averaging length for the amplitude from the channel filter. OOK: Sets the OOK decision boundary for OOK reception.		
				Setting	Channel filter samples	OOK decision boundary
				0 (00)	8	4 dB
				1 (01)	16	8 dB
				2 (10)	32	12 dB
				3 (11)	64	16 dB

**Table 5-50. 0x20: RESERVED**

Bit	Field Name	Reset	R/W	Description
7:3		31 (11111)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>
2			R0	Not used
1:0		0 (00)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>

**Table 5-51. 0x21: FRENDD1 - FrontEnd RX Configuration**

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

**Table 5-52. 0x23: FSCAL3 - Frequency Synthesizer Calibration**

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (10)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF Studio software <a href="#">SWRC176</a> .
5:4	CHP_CURR_CAL_EN[1:0]	2 (10)	R/W	Disable charge pump calibration stage when 0.
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $I_{OUT} = I_0 \times 2^{FSCAL3[3:0]/4}$ . See <a href="#">Section 5.20.2</a> for more details.

**Table 5-53. 0x24: FSCAL2 - Frequency Synthesizer Calibration**

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (01010)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value. See <a href="#">Section 5.20.2</a> for more details.

**Table 5-54. 0x25: FSCAL1 - Frequency Synthesizer Calibration**

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. See <a href="#">Section 5.20.2</a> for more details.



**Table 5-55. 0x26: FSCAL0 - Frequency Synthesizer Calibration**

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF Studio software <a href="#">SWRC176</a>

### 5.21.2 Configuration Register Details - Registers that Loose Programming in SLEEP State

**Table 5-56. 0x29: RESERVED**

Bit	Field Name	Reset	R/W	Description
7:0		89 (0x59)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>

**Table 5-57. 0x2A: RESERVED**

Bit	Field Name	Reset	R/W	Description
7:0		127 (0x7F)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>

**Table 5-58. 0x2B: RESERVED**

Bit	Field Name	Reset	R/W	Description
7:0		63 (0x3F)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>

**Table 5-59. 0x2C: TEST2 - Various Test Settings**

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	136 (0x88)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a> This register will be forced to 0x88 or 0x81 when it wakes up from SLEEP mode, depending on the configuration of <a href="#">FIFOTHR.ADC_RETENTION</a> . The value read from this register when waking up from SLEEP always is the reset value (0x88) regardless of the <a href="#">ADC_RETENTION</a> setting. The inverting of some of the bits due to the <a href="#">ADC_RETENTION</a> setting is only seen INTERNALLY in the analog part.

**Table 5-60. 0x2D: TEST1 - Various Test Settings**

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a> This register will be forced to 0x31 or 0x35 when it wakes up from SLEEP mode, depending on the configuration of <a href="#">FIFOTHR.ADC_RETENTION</a> . The value read from this register when waking up from SLEEP always is the reset value (0x31) regardless of the <a href="#">ADC_RETENTION</a> setting. The inverting of some of the bits due to the <a href="#">ADC_RETENTION</a> setting is only seen INTERNALLY in the analog part.

**Table 5-61. 0x2E: TEST0 - Various Test Settings**

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (000010)	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	Use setting from SmartRF Studio <a href="#">SWRC176</a>

### 5.21.3 Status Register Details

**Table 5-62. 0x30 (0xF0): PARTNUM - Chip ID**

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	0 (0x00)	R	Chip part number

**Table 5-63. 0x31 (0xF1): VERSION - Chip ID**

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	24 (0x18)	R	Chip version number. Subject to change without notice.

**Table 5-64. 0x32 (0xF2): FREQEST - Frequency Offset Estimate from Demodulator**

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (2s complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is $\pm 202$ kHz to $\pm 210$ kHz, depending on XTAL frequency. Frequency offset compensation is only supported for 2-FSK, GFSK, and 4-FSK modulation. This register will read 0 when using OOK modulation.

**Table 5-65. 0x33 (0xF3): CRC\_REG - CRC OK**

Bit	Field Name	Reset	R/W	Description
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0			R	Reserved

**Table 5-66. 0x34 (0xF4): RSSI - Received Signal Strength Indication**

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

**Table 5-67. 0x35 (0xF5): MARCSTATE - Main Radio Control State Machine State**

Bit	Field Name	Reset	R/W	Description		
7:5			R0	Not used		
4:0	MARC_STATE[4:0]		R	Main Radio Control FSM State		
				Value	State name	State (see <a href="#">Figure 5-11</a> )
				0 (0x00)	SLEEP	SLEEP
				1 (0x01)	IDLE	IDLE
				2 (0x02)	XOFF	XOFF
				3 (0x03)	VCOON_MC	MANCAL
				4 (0x04)	REGON_MC	MANCAL
				5 (0x05)	MANCAL	MANCAL
				6 (0x06)	VCOON	FS_WAKEUP
				7 (0x07)	REGON	FS_WAKEUP
				8 (0x08)	STARTCAL	CALIBRATE
				9 (0x09)	BWBOOST	SETTLING
				10 (0x0A)	FS_LOCK	SETTLING
				11 (0x0B)	IFADCON	SETTLING
				12 (0x0C)	ENDCAL	CALIBRATE
				13 (0x0D)	RX	RX
				14 (0x0E)	RX_END	RX
				15 (0x0F)	RX_RST	RX
				16 (0x10)	Reserved	
				17 (0x11)	RXFIFO_OVERFLOW	RXFIFO_OVERFLOW
				18 (0x12)	Reserved	
				...		
22 (0x16)						
				Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.		

**Table 5-68. 0x38 (0xF8): PKTSTATUS - Current GDOx Status and Packet Status**

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense. Cleared when entering IDLE mode.
5			R	Reserved
4			R	Reserved
3	SFD		R	Start of Frame Delimiter. This bit is asserted when sync word has been received and deasserted at the end of the packet. It will also de-assert when a packet is discarded due to address or maximum length filtering or the radio enters RXFIFO_OVERFLOW state.
2	GDO2		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective of what <a href="#">IOCFG2.GDO2_INV</a> is programmed to. It is not recommended to check for PLL lock by reading <a href="#">PKTSTATUS[2]</a> with <a href="#">GDO2_CFG=0x0A</a> .
1			R0	Not used
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective of what <a href="#">IOCFG0.GDO0_INV</a> is programmed to. It is not recommended to check for PLL lock by reading <a href="#">PKTSTATUS[0]</a> with <a href="#">GDO0_CFG=0x0A</a> .

**Table 5-69. 0x3B (0xFB): RXBYTES - Overflow and Number of Bytes**

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

## 5.22 Development Kit Ordering Information

Orderable Evaluation Module	Description	Minimum Order Quantity
CC11xLDK-868-915	CC11xL Development Kit, 868/915 MHz	1
CC11xLEMK-433	CC11xL Evaluation Module Kit, 433 MHz	1

## 6 Applications, Implementation, and Layout

Figure 5-1 shows the low cost CC113LEM application circuit (see [SWRR083](#) and [SWRR084](#)) (see Table 6-1 for component values).

The designs in [SWRR046](#) and [SWRR045](#) were used for CC113L characterization. The application circuits are shown in Figure 6-2 and Figure 6-3 (see Table 6-1 for component values).

### 6.1 Bias Resistor

The 56-k $\Omega$  bias resistor R171 is used to set an accurate bias current.

### 6.2 Balun and RF Matching

The balun component values and their placement are important to keep the performance optimized. Gerber files and schematics for the reference designs are available for download from the TI website.

#### 6.2.1 Balun and RF Matching (Low-Cost Application Circuit)

The components between the RF\_N/RF\_P pins and the point where the two signals are joined together (C131, C122, L122, and L132, see Figure 6-1) form a balun that converts singleended RF signal at the antenna to a differential RF signal on CC113L. C124 is needed for DC blocking.

The balun components also matches the CC113L input impedance to a 50- $\Omega$  source. C126 provides DC blocking and is only needed if there is a DC path in the antenna.

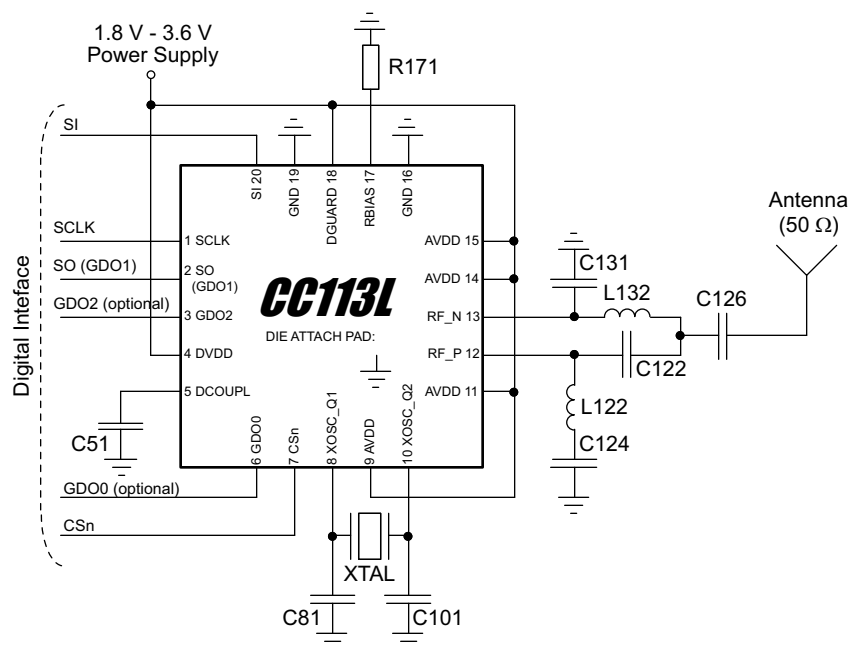


Figure 6-1. Low Cost Application Circuit and Evaluation Circuit 315, 433, 868, or 915 MHz (Excluding Supply Decoupling Capacitors)

**Table 6-1. External Components (Low-Cost Application Circuit)**

Component	Value at 315 MHz	Value at 433 MHz	Value at 868/915 MHz
C124	220 pF	220 pF	100 pF
C122	6.8 pF	3.9 pF	2.2 pF
C126	220 pF	220 pF	100 pF
C131	6.8 pF	3.9 pF	2.2 pF
L122	33 nH	27 nH	12 nH
L132	33 nH	27 nH	12 nH

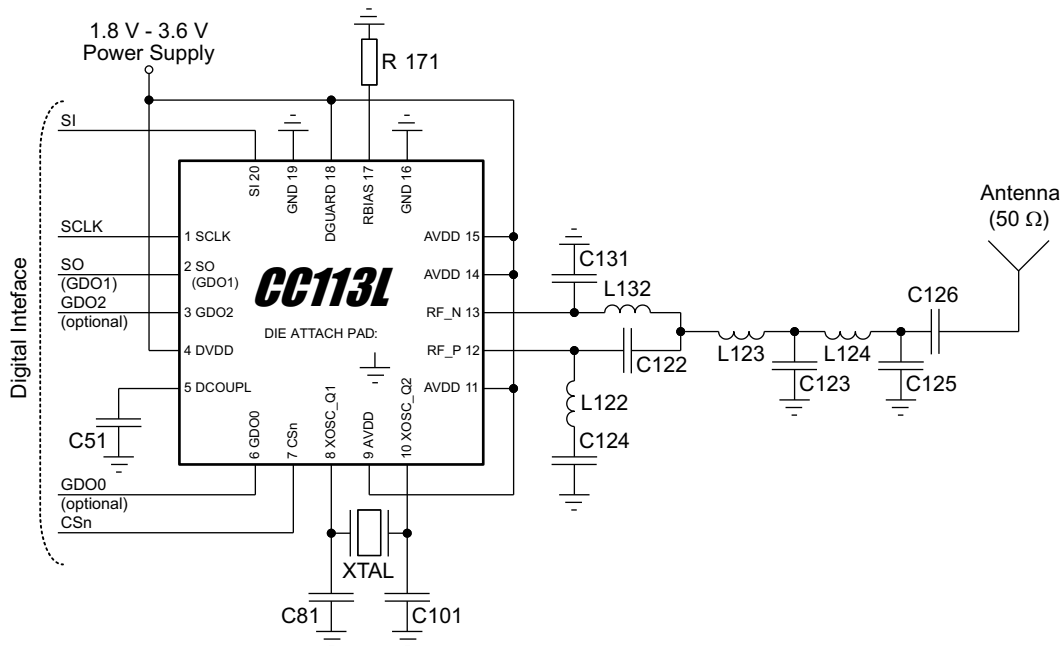
**6.2.2 Balun and RF Matching (Characterization Circuit)**

The components between the RF\_N/RF\_P pins and the point where the two signals are joined together (C131, C122, L122, and L132 in Figure 6-2 and L121, L131, C121, L122, C131, C122, and L132 in Figure 6-3) form a balun that converts single-ended RF signal at the antenna to a differential RF signal on CC113L. C124 is needed for DC blocking.

The balun components also matches the CC113L input impedance to a 50-Ω source. C126 provides DC blocking and is only needed if there is a DC path in the antenna.

Note that the 315/433 MHz design [SWRR046](#) uses Murata LQG15 multi-layer inductors while the 868/915 MHz design [SWRR045](#) uses Murata LQW15 wire-wound inductors.

L123, L124, and C123 (plus C125 in Figure 6-2) form an LC low-pass filter. This filter is not required for an RX-only design and can be omitted.



**Figure 6-2. Characterization Circuit 315 and 433 MHz (Excluding Supply Decoupling Capacitors)**

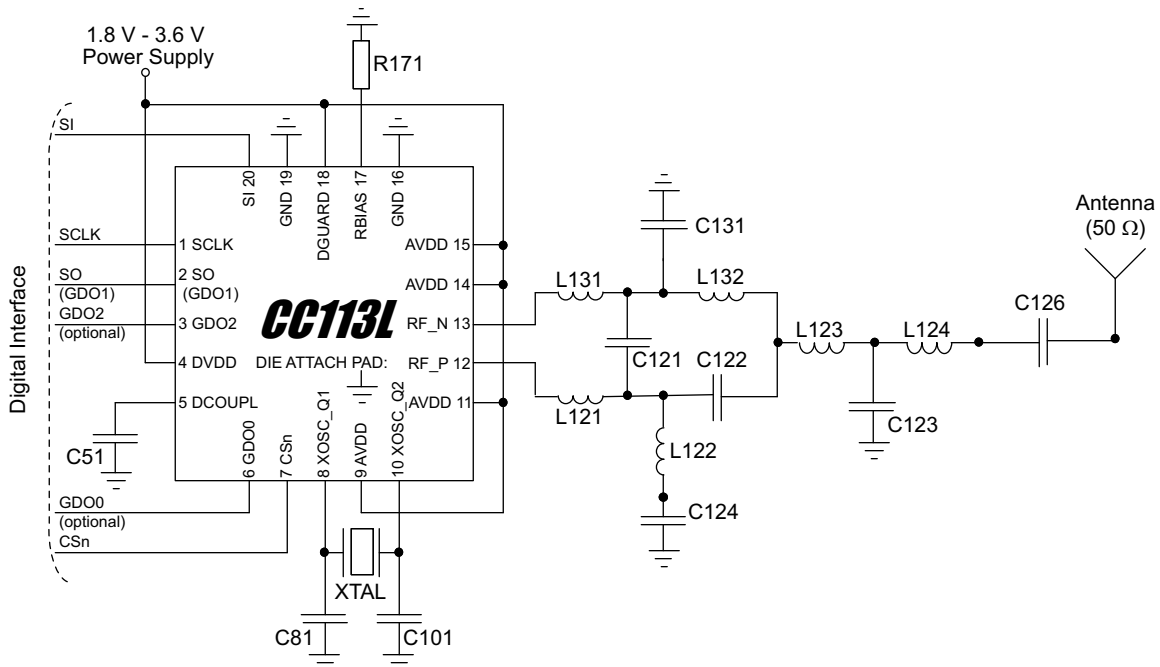


Figure 6-3. Characterization Circuit 868 and 915 MHz (Excluding Supply Decoupling Capacitors)

Table 6-2. External Components

Component	Value at 315 MHz	Value at 433 MHz	Value at 868/915 MHz
C121			1 pF
C122	6.8 pF	3.9 pF	1.5 pF
C123	12 pF	8.2 pF	3.3 pF
C124	220 pF	220 pF	100 pF
C125	6.8 pF	5.6 pF	
C126	220 pF	220 pF	100 pF
C131	6.8 pF	3.9 pF	1.5 pF
L121			12 nH
L122	33 nH	27 nH	18 nH
L123	18 nH	22 nH	12 nH
L124	33 nH	27 nH	12 nH
L131			12 nH
L132	33 nH	27 nH	18 nH



### 6.3 Crystal

A crystal in the frequency range 26 - 27 MHz must be connected between the XOSC\_Q1 and XOSC\_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance,  $C_L$ , specified for the crystal. The total load capacitance seen between the crystal terminals should equal  $C_L$  for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{\text{parasitic}} \quad (9)$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 V<sub>pp</sub> signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see [Section 4.7](#)).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

Avoid routing digital signals with sharp edges close to XOSC\_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

### 6.4 Reference Signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC\_Q1 input. The sine wave must be connected to XOSC\_Q1 using a serial capacitor. When using a full-swing digital signal, this capacitor can be omitted. The XOSC\_Q2 line must be left un-connected. C81 and C101 can be omitted when using a reference signal.

### 6.5 Power Supply Decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. The CC113LEM reference designs [SWRR081](#) and [SWRR082](#) should be followed closely.

### 6.6 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground.

In the CC113LEM reference designs, [SWRR081](#) and [SWRR082](#), 5 vias are placed inside the exposed die attached pad. These vias should be “tented” (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using “tented” vias reduces the solder paste coverage below 100%. See [Figure 6-4](#) for top solder resist and top paste masks.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the CC113L supply pin. Supply power filtering is very important.

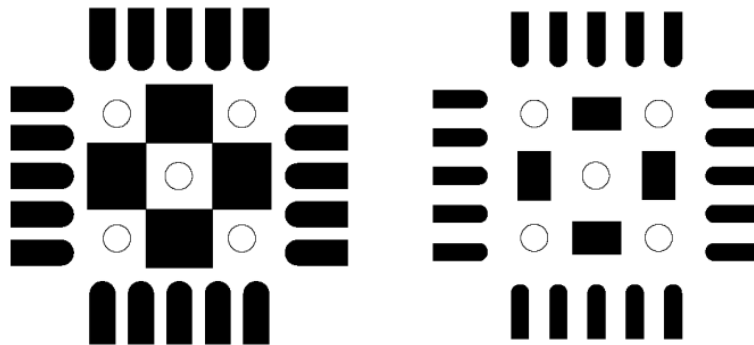
Each decoupling capacitor ground pad should be connected to the ground plane by separate vias. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary. Routing in the ground plane underneath the chip or the balun/RF matching circuit, or between the chip's ground vias and the decoupling capacitor's ground vias should be avoided. This improves the grounding and ensures the shortest possible current return path.

Avoid routing digital signals with sharp edges close to XOSC\_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Components with different sizes than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC11xL Development Kit with a fully assembled CC113L Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The schematic, BOM and layout Gerber files are all available from the TI website ([SWRR081](#) and [SWRR082](#)).



**Figure 6-4. Left: Top Solder Resist Mask (Negative) – Right: Top Paste Mask. Circles are Vias**

## 7 Device and Documentation Support

### 7.1 Device Support

#### 7.1.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *CC113L*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGP*) and the temperature range (for example, blank is the default commercial temperature range).

For orderable part numbers of *CC113L* devices in the *QFN* package types, see the Package Option Addendum of this document, the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

## 7.2 Documentation Support

### 7.2.1 Related Documentation from Texas Instruments

The following documents describe the CC113L receiver. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

- [SWRR046](#) Characterization Design 315 - 433 MHz (Identical to the CC1101EM 315 - 433 MHz Reference Design)
- [SWRR045](#) Characterization Design 868 - 915 MHz (Identical to the CC1101EM 868 - 915 MHz Reference Design)
- [SWRZ038](#) CC113L Errata Notes
- [SWRC176](#) SmartRF Studio
- [SWRA147](#) DN010 Close-in Reception with CC1101
- [SWRA159](#) DN015 Permanent Frequency Offset Compensation
- [SWRA114](#) DN505 RSSI Interpretation and Timing
- [SWRA215](#) DN022 CC11xx OOK/ASK register settings
- [SWRA122](#) DN005 CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy
- [SWRR083](#) CC113LEM 433 MHz Reference Design
- [SWRR084](#) CC113LEM 868 - 915 MHz Reference Design

### 7.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 7.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 7.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 7.7 Additional Acronyms

Additional acronyms used in this data sheet are described below.

<b>2-FSK</b>	Binary Frequency Shift Keying
<b>4-FSK</b>	Quaternary Frequency Shift Keying
<b>ADC</b>	Analog to Digital Converter
<b>AFC</b>	Automatic Frequency Compensation
<b>AGC</b>	Automatic Gain Control
<b>AMR</b>	Automatic Meter Reading
<b>BER</b>	Bit Error Rate
<b>BT</b>	Bandwidth-Time product
<b>CFR</b>	Code of Federal Regulations
<b>CRC</b>	Cyclic Redundancy Check
<b>CS</b>	Carrier Sense
<b>DC</b>	Direct Current
<b>DVGA</b>	Digital Variable Gain Amplifier
<b>ESR</b>	Equivalent Series Resistance
<b>FCC</b>	Federal Communications Commission
<b>FIFO</b>	First-In-First-Out
<b>FS</b>	Frequency Synthesizer
<b>GFSK</b>	Gaussian shaped Frequency Shift Keying
<b>IF</b>	Intermediate Frequency
<b>I/Q</b>	In-Phase/Quadrature
<b>ISM</b>	Industrial, Scientific, Medical
<b>LC</b>	Inductor-Capacitor

<b>LNA</b>	Low Noise Amplifier
<b>LO</b>	Local Oscillator
<b>LSB</b>	Least Significant Bit
<b>MCU</b>	Microcontroller Unit
<b>MSB</b>	Most Significant Bit
<b>N/A</b>	Not Applicable
<b>NRZ</b>	Non Return to Zero (Coding)
<b>OOK</b>	On-Off Keying
<b>PA</b>	Power Amplifier
<b>PCB</b>	Printed Circuit Board
<b>PD</b>	Power Down
<b>PER</b>	Packet Error Rate
<b>PLL</b>	Phase Locked Loop
<b>POR</b>	Power-On Reset
<b>PTAT</b>	Proportional To Absolute Temperature
<b>QLP</b>	Quad Leadless Package
<b>QPSK</b>	Quadrature Phase Shift Keying
<b>RC</b>	Resistor-Capacitor
<b>RF</b>	Radio Frequency
<b>RSSI</b>	Received Signal Strength Indicator
<b>RX</b>	Receive, Receive Mode
<b>SMD</b>	Surface Mount Device
<b>SPI</b>	Serial Peripheral Interface
<b>SRD</b>	Short Range Devices
<b>VCO</b>	Voltage Controlled Oscillator
<b>XOSC</b>	Crystal Oscillator
<b>XTAL</b>	Crystal

## 8 Mechanical Packaging and Orderable Information

### 8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC113LRGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC113L	<a href="#">Samples</a>
CC113LRGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC113L	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC113LRGPR	QFN	RGP	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC113LRGPR	QFN	RGP	20	3000	350.0	350.0	43.0

**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC113LRGPR	RGP	VQFN	20	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

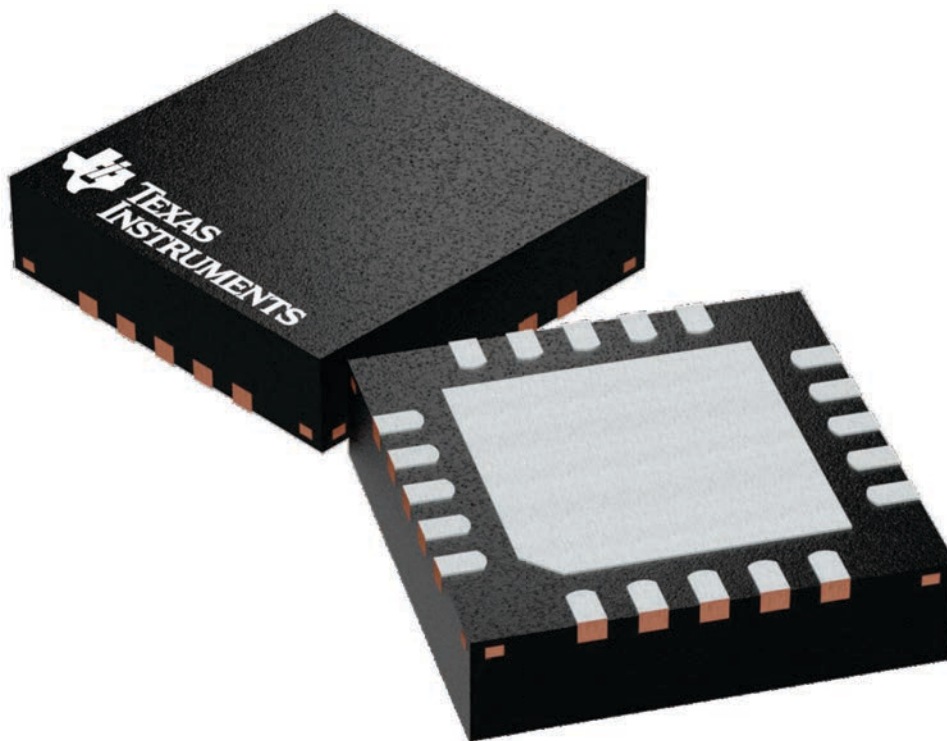
## GENERIC PACKAGE VIEW

**RGP 20**

**VQFN - 1 mm max height**

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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