BQ41Z90 Highly Integrated 3–16 Cell Battery Fuel Gauge with IT-DZT Algorithm and ECC Authentication

ADVANCE INFORMATION

1 Features

- Highly integrated battery pack manager for 3 to 16 cells in series applications
  - Ultra-low power 32-bit RISC processor
  - ADC measurements for up to 16 cells in series with 80V tolerance
  - High Accuracy SoC and SoH with Dynamic Z Track™ gauging algorithm
  - Certificate-based security protected flash memory
- Precision analog front end with two independent ADCs:
  - High-accuracy 18-bit integrating delta-sigma coulomb counter
  - High-accuracy 16-bit delta-sigma with input translation and multiplexer
  - Support for simultaneous current and voltage sampling
  - Supports up to eight external thermistor measurements and an internal temperature sensor
- Strong High-side NMOS FET drive with fast turn-on and turn-off time
- Charge pump support for pre-charge and pre-discharge NMOS FET drivers
- Parallel configuration support for removable battery with separate charger and system ports
- Cell balancing support up to 50mA bypass per cell
- Diagnostic lifetime data monitor and recorder
- Multiple host communication support:
  - I^2C (up to 1MHz)
  - SMBus 3.2 (up to 1MHz)
- Multiple power modes for low quiescent current operation
- SHA-1, SHA-2, or EC-KCDSA authentication for robust battery pack security

2 Applications

- Battery backup unit (BBU)
- E-bike, e-scooter, and LEV
- Handheld vacuum cleaners and vacuum robots
- Gardening robots and power tools
- Drones
- Medical and test equipment
- Other industrial battery pack

3 Description

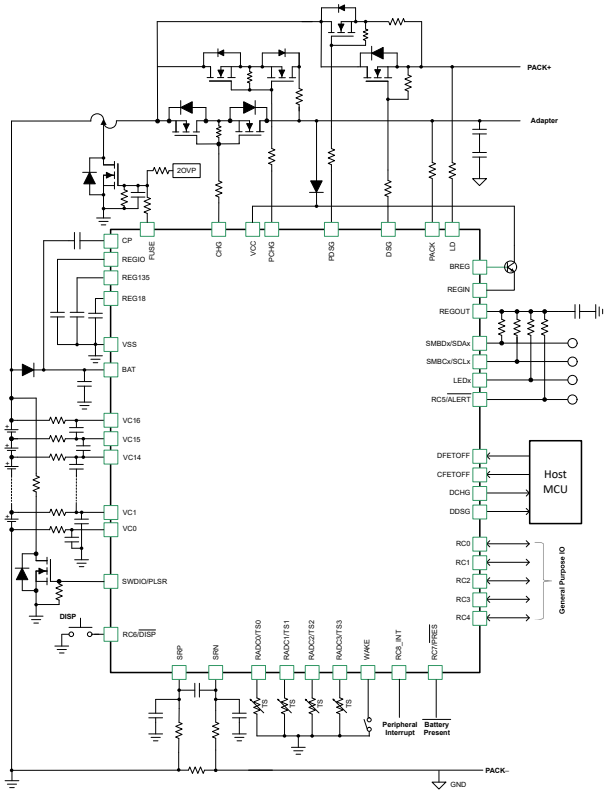
The Texas Instruments BQ41Z90 is a fully integrated pack-based battery pack manager solution, that provides a flash programmable CPU, safety protection, and elliptical curve cryptography (ECC) authentication for 3 to 16 cells in series Li-ion, LiFeP4, NiMH, and Li-polymer battery packs.

The BQ41Z90 battery pack manager communicates through SMBus v3.2 or I^2C-compatible interfaces, and combines an ultra-low-power, high-speed 32-bit processor, high-accuracy analog measurement capabilities, integrated flash memory, an array of peripheral IO, an NMOS protection FET drive, and a SHA-1, SHA-2, or EC-KCDSA authentication responder into a complete, high-performance battery management solution.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
BQ41Z90 RSN	PVP (64)	7.00mm × 7.00mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.



Simplified Schematic

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4 Pin Configuration and Functions:

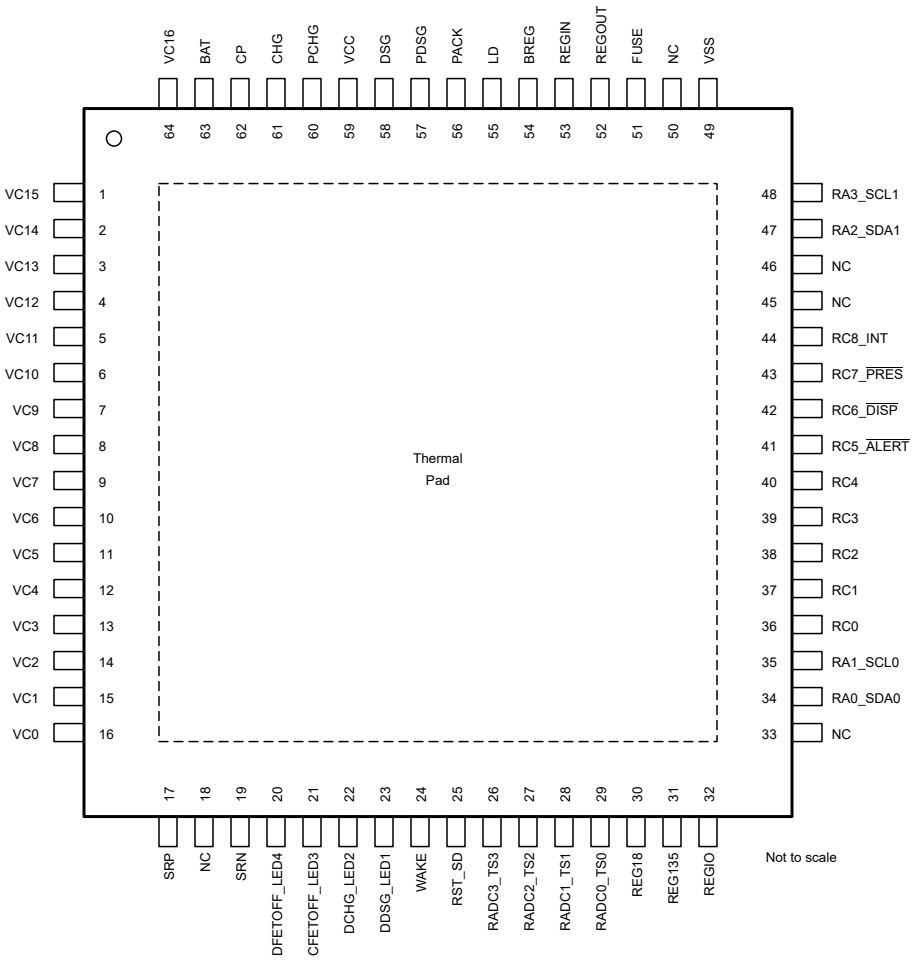

Figure 4-1. Pin Diagram

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VC15	1	AI	Sense voltage input pin for the fifteenth cell from the bottom of the stack, balance current input for the fifteenth cell from the bottom of the stack, and return balance current for the sixteenth cell from the bottom of the stack
VC14	2	AI	Sense voltage input pin for the fourteenth cell from the bottom of the stack, balance current input for the fourteenth cell from the bottom of the stack, and return balance current for the fifteenth cell from the bottom of the stack
VC13	3	AI	Sense voltage input pin for the thirteenth cell from the bottom of the stack, balance current input for the thirteenth cell from the bottom of the stack, and return balance current for the fourteenth cell from the bottom of the stack
VC12	4	AI	Sense voltage input pin for the twelveth cell from the bottom of the stack, balance current input for the twelveth cell from the bottom of the stack, and return balance current for the thirteenth cell from the bottom of the stack
VC11	5	AI	Sense voltage input pin for the eleventh cell from the bottom of the stack, balance current input for the eleventh cell from the bottom of the stack, and return balance current for the twelfth cell from the bottom of the stack

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VC10	6	AI	Sense voltage input pin for the tenth cell from the bottom of the stack, balance current input for the tenth cell from the bottom of the stack, and return balance current for the eleventh cell from the bottom of the stack
VC9	7	AI	Sense voltage input pin for the ninth cell from the bottom of the stack, balance current input for the ninth cell from the bottom of the stack, and return balance current for the tenth cell from the bottom of the stack
VC8	8	AI	Sense voltage input pin for the eighth cell from the bottom of the stack, balance current input for the eighth cell from the bottom of the stack, and return balance current for the ninth cell from the bottom of the stack
VC7	9	AI	Sense voltage input pin for the seventh cell from the bottom of the stack, balance current input for the seventh cell from the bottom of the stack, and return balance current for the eighth cell from the bottom of the stack
VC6	10	AI	Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack, and return balance current for the seventh cell from the bottom of the stack
VC5	11	AI	Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack
VC4	12	AI	Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack
VC3	13	AI	Sense voltage input pin for the third cell from the bottom of the stack, balance current input for the third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack
VC2	14	AI	Sense voltage input pin for the second cell from the bottom of the stack, balance current input for the second cell from the bottom of the stack, and return balance current for the third cell from the bottom of the stack
VC1	15	AI	Sense voltage input pin for the first cell from the bottom of the stack, balance current input for the first cell from the bottom of the stack, and return balance current for the second cell from the bottom of the stack
VC0	16	AI	Sense voltage input pin for the negative terminal of the first cell from the bottom of the stack, and return balance current for the first cell from the bottom of the stack
SRP	17	AI	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN
NC	18	NC	This pin is not connected to silicon
SRN	19	AI	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN
DFETOFF_LED4	20	I/O	DFETOFF input to keep the DFET off as long as this pin is asserted, or LED4 open drain output pin with current sink.
CFETOFF_LED3	21	I/O	CFETOFF input to keep the CFET off as long as this pin is asserted, or LED3 open drain output pin with current sink,
DCHG_LED2	22	O	DCHG output to indicate protection faults which should cause CFET to be off, or LED2 open drain output pin with current sink.
DDSG_LED1	23	O	DDSG output to indicate protection faults which should cause DFET to be off, or LED1 open drain output pin with current sink.
WAKE	24	AI	Push-down button input to wake up the device from Shutdown or Hibernate mode.
RST_SD	25	AI	Input pin for reset or shutdown
RADC3_TS3	26	AI	General-purpose ADC or thermistor input
RADC2_TS2	27	AI	General-purpose ADC or thermistor input
RADC1_TS1	28	AI	General-purpose ADC or thermistor input
RADC0_TS0	29	AI	General-purpose ADC or thermistor input

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
REG18	30	PO	Internal 1.8V LDO Output Cap Connection (only for internal use)
REG135	31	PO	Internal 1.35V LDO Output Cap Connection (only for internal use)
REGIO	32	PI	Internal 3.3V/1.8V LDO Output Cap Connection (only for internal use)
NC	33	NC	This pin is not connected to silicon
RA0_SDA0	34	I/O	General-purpose input with or without INT, or multifunction open-drain output, can be configured as SDA, SCL, SMBD, or SMBC
RA1_SCL0	35	I/O	General-purpose input with or without INT, or multifunction open-drain output, can be configured as SDA, SCL, SMBD, or SMBC
RC0	36	I/O	General-purpose digital input with or without INT, or multifunction push-pull output.
RC1	37	I/O	General-purpose digital input with or without INT, or multifunction push-pull output.
RC2	38	I/O	General-purpose digital input with or without INT, or multifunction push-pull output.
RC3	39	I/O	General-purpose digital input with or without INT, or multifunction push-pull output.
RC4	40	I/O	General-purpose digital input with or without INT, or multifunction push-pull output.
RC5_$\overline{\text{ALERT}}$	41	I/O	General-purpose digital input with or without INT, or multifunction push-pull output. Defaults to $\overline{\text{ALERT}}$ output to signal general fault detection.
RC6_$\overline{\text{DISP}}$	42	I/O	General-purpose digital input with or without INT, or multifunction push-pull output. Defaults to $\overline{\text{DISP}}$bottom control output signal.
RC7_$\overline{\text{PRES}}$	43	I/O	General-purpose digital input with or without INT, or multifunction push-pull output. Defaults to $\overline{\text{PRES}}$ for battery presence input signal.
RC8_INT	44	I/O	General-purpose digital input with or without INT, or multifunction push-pull output
NC	45	NC	This pin is not connected to silicon
NC	46	NC	This pin is not connected to silicon
RA2_SDA1	47	IO	General-purpose input or multifunction open-drain output, can be configured as SDA, SCL, SMBD, or SMBC
RA3_SCL1	48	IO	General-purpose input or multifunction open-drain output, can be configured as SDA, SCL, SMBD, or SMBC
VSS	49	P	Device ground
NC	50	NC	This pin is not connected to silicon
FUSE	51	IO,A	Fuse sense and drive
REGOUT	52	AO	External LDO output, which can be programmed for 2 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V
REGIN	53	AI	Input pin for external LDO REGOUT
BREG	54	AO	Base control signal for external regulatory transistor
LD	55	AI	Load detect pin
PACK	56	AI	Pack sense input pin
PDSG	57	AO	Pre-discharge control pin
DSG	58	AO	Discharge control pin
VCC	59	P	Secondary power supply input
PCHG	60	AO	Pre-charge control pin
CHG	61	AO	Charge control pin
CP	62	AO	Charge pump capacitor
BAT	63	P	Primary power supply input from battery
VC16	64	AI	Sense voltage input pin for the sixteenth cell from the bottom of the stack, and balance current input for the sixteenth cell from the bottom of the stack

(1) I = Input, O = Output, I/O = Input or Output, AI = Analog Input, AO = Analog Output, G = Ground, P = Power.

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5 Pin Equivalent Diagrams

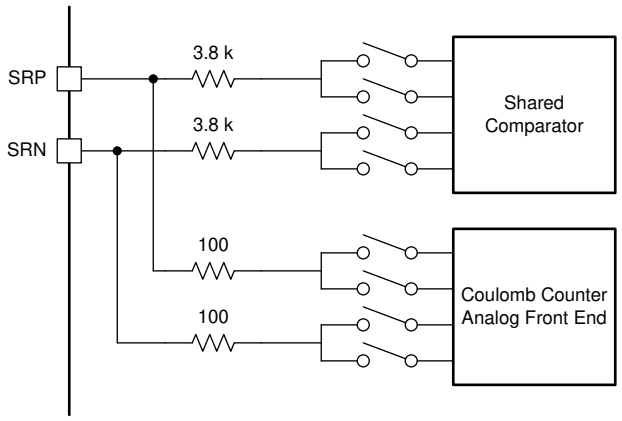

Figure 5-1. SRx Pins

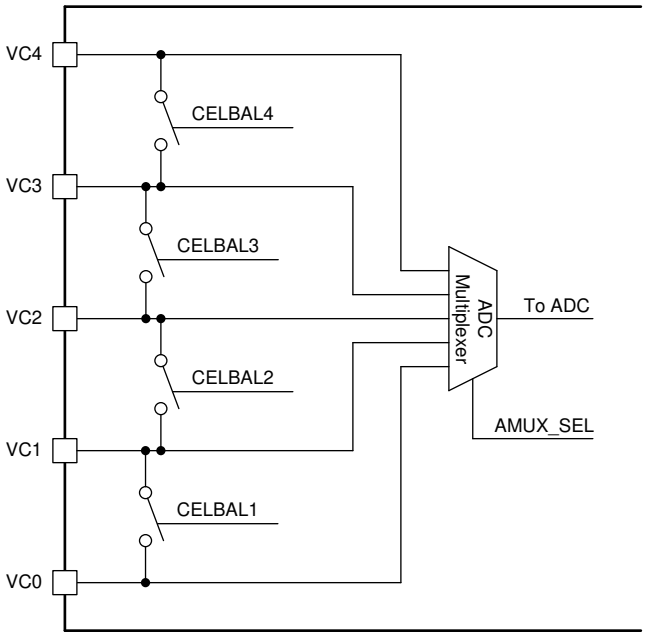

Figure 5-2. VCx Pins

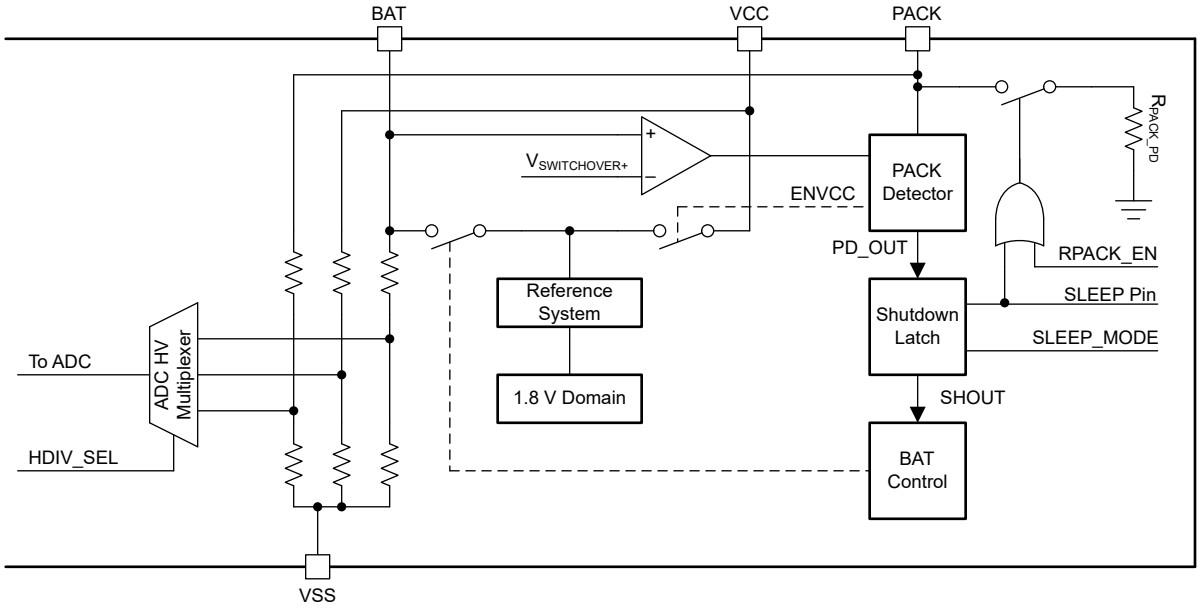

Figure 5-3. Power Supply Pins

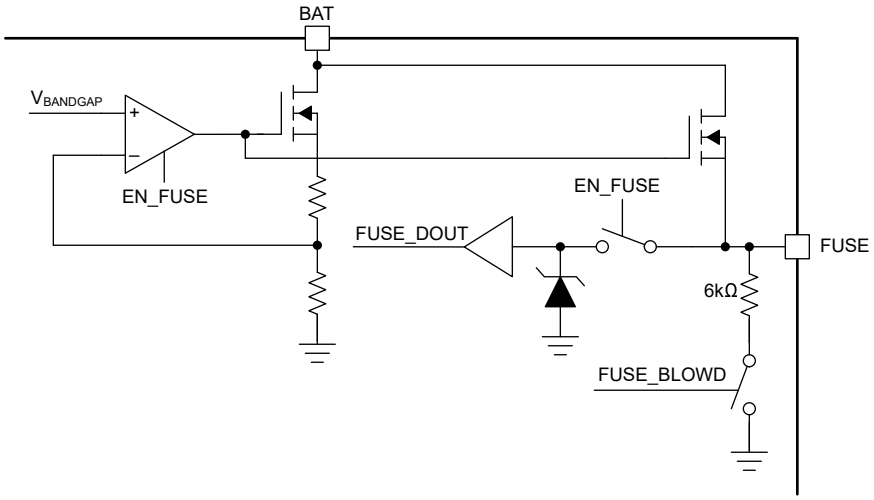

Figure 5-4. Fuse Pin

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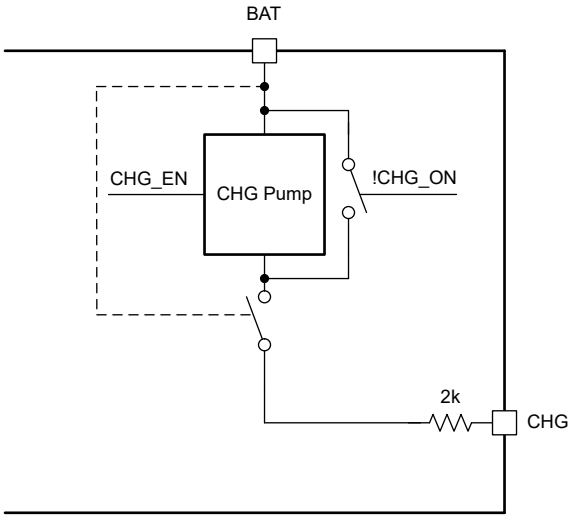

Figure 5-5. CHG Pin

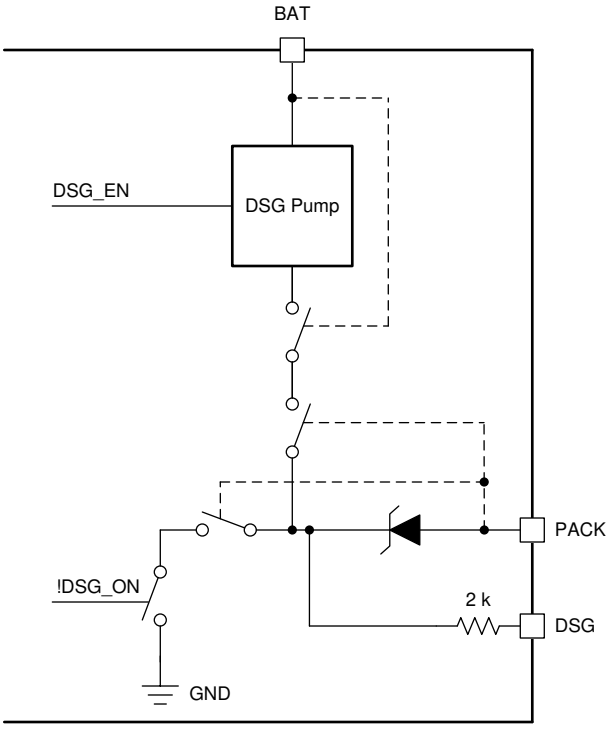

Figure 5-6. DSG Pin

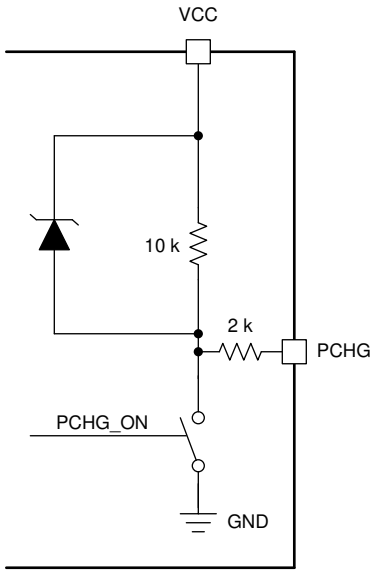

Figure 5-7. PCHG Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		PINS	MIN	MAX	UNIT
V_{DD}	Supply voltage range	BAT, VCC	VSS–0.3	VSS+85	V
V_{IN}	Voltage on Input pins	PACK, LD	VSS–0.3	VSS+85	V
		FUSE(2)	VSS–0.3	minimum of VSS+20 or V_{BAT}+0.3	V
		REGIN	VSS–0.3	minimum of VSS+6 or V_{BREG}+0.3	V
		RAx (SDL0, SCLK0, SDL1, SCLK1)	VSS–0.3	VSS+6	V
		RADCx, TSx, LEDx, DFETOFF, CFETOFF, WAKE, RST_SD	VSS–0.3	VSS+3.6	V
		RCx	VSS–0.3	VSS+3.6	V
		SRP, SRN	VSS–0.3	V_{REG18} + 0.3	V
		VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12, VC13, VC14, VC15, VC16	maximum of VSS–0.3 and VC0–0.3	VSS+85	V
		VC0	VSS–0.3	VSS+6	V
V_{OUT}	Voltage on Output pins	CP	V_{BAT}–0.3	minimum of VSS+85 or VBAT+15	V
		CHG, DSG	VSS–0.3	VSS+85	V
		PCHG, PDSG	maximum of V_{BAT}–10 or V_{LD}–10	VSS+85	V
		REG135	VSS–0.3	VSS+1.45	V
		REG18	VSS–0.3	VSS+2	V
		REGIO	VSS–0.3	VSS+3.5	V
		REGOUT	VSS–0.3	VSS+5.5	V
$I_{BALANCE}$	Maximum cell balancing current through a single cell	VC0 – VC16		100	mA
I_{SS}	Maximum VSS current			75	mA
T_J	Junction temperature (operational)		–40	125	°C
T_{STG}	Storage temperature		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The current allowed to flow into the FUSE pin must be limited (such as by using external series resistance) to 2 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	BAT pin, I_{REG18} ≤ 22mA	$V_{SWITCHOVER}$		80	V
		VCC pin	5		80	V
V_{IN}	Input voltage range	PACK, LD	0		80	V
		RAx (SDL0, SCLK0, SDL1, SCLK1)	0		5.5	V
		RCx	0		V_{REGIO}	V
		RADCx, TSx, LEDx, DFETOFF, CFETOFF, RST_SD	0		V_{REG18} + 0.3	V
		SRP, SRN pins	–0.25		0.5	V
		VC16	VC_{15}–0.2		VC_{15}+5	V
		VC15	VC_{14}–0.2		VC_{14}+5	V
		VC14	VC_{13}–0.2		VC_{13}+5	V
		VC13	VC_{12}–0.2		VC_{12}+5	V
		VC12	VC_{11}–0.2		VC_{11}+5	V
		VC11	VC_{10}–.02		VC_{10}+5	V
		VC10	VC_{9}–.02		VC_{9}+5	V
		VC9	VC_{8}–0.2		VC_{8}+5	V
		VC8	VC_{7}–0.2		VC_{7}+5	V
		VC7	VC_{6}–0.2		VC_{6}+5	V
		VC6	VC_{5}–0.2		VC_{5} +5	V
		VC5	VC_{4}–0.2		VC_{4}+5	V
		VC4	VC_{3}–0.2		VC_{3}+5	V
		VC3	VC_{2}–0.2		VC_{2}+5	V
		VC2	VC_{1}–0.2		VC_{1}+5	V
		VC1	VC_{0}–.02		VC_{0}+5	V
		VC0	–0.2		0.5	V
V_{OUT}	Output voltage range	CHG, DSG, PCHG, PDSG	0		80	V
V_{OUT}	Output voltage range	FUSE	0		28	V
C_{BAT} (1)	BAT external capacitor	Derated to 2.2V, 100V capacitor	0.47	1		µF
C_{VCC} (1)	VCC external capacitor	Derated to 2.2V, 100V capacitor	0.1	0.47		µF
C_{REGIO} (1)	REGIO exteranl capacitor	Derated to 3.3 V, 10V capacitor	0.47	1	2.2	µF
C_{REG18} (1)	REG18 external capacitor	Derated to 1.8 V, 10V capacitor	0.47	1	2.2	µF
C_{REG135} (1)	REG135 external capacitor	Derated to 1.35 V, 10V capacitor	0.47	1	2.2	µF
Cp	Charge pump capacitor	Derated to 2.2V, 100V capacitor	100	470	2200	nF
CC	External cell input capacitor	Derated to 2.2V, 100V capacitor		100		nF

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Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
R_C	External cell measurement input resistor		20		100	Ω
R_{PACK} (1)	PACK series external resistor	For lowest Startup voltage	2	10	12	kΩ
I_{SS} (1)	Maximum current through Vss pin	Includes LDOs, GPIO and Cell balancing			200	mA
T_A (2)	Operating free-air temperature		–40		105	°C

(1) Specified by design. Not production tested.
(2) Additional cooling strategies may be necessary to keep junction temperature at recommended limits.

6.4 Thermal Information

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

THERMAL METRIC(1)		PVP (QFP)	UNIT
		64 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	0.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Supply Current

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ACTIVE} (1)	ACTIVE mode	CPU active, ADC and CC On, Protections On, CHG and DSG FETs On, No Communication		500		µA
I_{SLEEP} (2)	SLEEP mode	CPU halted, ADC and CC On, Protections On, CHG and DSG FETs On, RAM in retension, No Flash read/write/erase, No Communication		250		µA
$I_{DEEPSLEEP}$	DEEP SLEEP mode	CPU halted, ADC and CC Off, Protections Off, CHG and DSG FETs Off, RAM in retension, No Flash read/write/erase, No Communication		80		µA
$I_{HIBERNATE}$	HIBERNATE mode	Everything powered OFF execpt PACK and WAKE detection functions		30		µA
I_{SHELF}	SHELF mode	Everything powered OFF except PACK detection function and Low Power Timer		3	5	µA
I_{SHUT}	SHUTDOWN mode	Everything powered OFF except PACK detection function. External Pullup on GPIO pins not powered		0.6	2	µA

(1) Assuming device is running typical firmware settings under ACTIVE mode, which manages CPU and ADC/CC duty cycle to <4%
(2) Assuming device is running typical firmware settings under SLEEP mode, which manages CPU and CC duty cycle to <1%

6.6 Power Selector

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Selector					

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Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{STARTUP}$	Startup Voltage at PACK	V_{PACK} > $V_{STARTUP}$ for 1 ms	3.5	4.5	5.5	V
$V_{SWITCHOVER-}$	BAT to VCC switchover voltage	V_{BAT} < $V_{SWITCHOVER-}$	4.9	4.95	5.05	V
$V_{SWITCHOVER+}$	VCC to BAT switchover voltage	V_{BAT} > $V_{SWITCHOVER-}$ + V_{HYS}	5.85	6.1	6.5	V
V_{HYS}	Switchover hysteresis voltage	$V_{SWITCHOVER+}$ - $V_{SWITCHOVER-}$		1.02		V
T_{SD_ALERT+}	Thermal shutdown alert temperature rising			120	135	°C
T_{SD_ALERT-}	Thermal shutdown alert temperature falling	Exit from RESET, REG135 enabled	100	102		°C
T_{SD+}	Thermal shutdown temperature rising			140	148	°C
T_{SD-}	Thermal shutdown temperature falling	REG18 Enabled	122	130		°C
I_{LKG}	Input leakage current	BAT pin, BAT = 0 V, VCC = 60 V, PACK = 60 V			1	µA
		PACK pin, BAT = 60V, VCC = 0 V, PACK = 0 V			1	µA
R_{PACK_PD}	Internal pulldown resistance	PACK pin	30	40	50	kΩ
Power On Reset						
t_{RST_POR} (1)	Power on reset time: From application of valid input voltage to release of POR for the MCU			2.5	4.0	ms
t_{RST_ROM} (1)	Power on reset time: From application of valid input voltage to CPU ready to execute ROM code			5	10	ms
t_{RST_EXE} (1)	Power on reset time: From application of valid input voltage to CPU ready to execute flash code	Not including CRC of flash array performed by ROM		5	10	ms

(1) Specified by design. Not production tested.

6.7 Current Wake Detector

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE_THR}	Wakeup voltage threshold	Nominal settings, threshold based on V_{SRP} - V_{SRN}		±0.5 to ±7.5 in 0.5 steps		mV
$V_{WAKE\_THR\_ERR}$ (1)	Wakeup voltage threshold error	T_A = 25°C, V_{WAKE} = V_{SRP} – V_{SRN}	–350		350	µV

(1) Specified by design. Not production tested.

6.8 General Purpose Input-Outputs

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low Voltage GPIO (RA and RC Ports)						
V_{IN}	Input voltage range	RA0..3 (SDA0, SCL0, SDA1, SCL1)	–0.2		5.5	V
V_{IN}	Input voltage range	RC0..8	–0.2		$V_{REG3.3}$	V
V_{IH} (2)	High-level input voltage	RA0..3 (SDA0, SCL0, SDA1, SCL1)	0.7 x V_{REGIO}			V
V_{IH} (2)	High-level input voltage	RC0..8	0.7 x V_{REGIO}			V

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL} (2)	Low-level input voltage	RA0..3 (SDA0, SCL0, SDA1, SCL1)			0.3 x V_{REGIO}	V
V_{IL} (2)	Low-level input voltage	RC0..8			0.3 x V_{REGIO}	V
V_{IOHYS} (1)	Hysteresis of Input	RA0..3, RC0..8	75			mV
V_{OH} (2)	Output voltage high	RC0..8 : I_{OH} = -450 µA	0.7*V_{REGIO}			V
V_{OL}	Output voltage low	RA0..3 (SDA0, SCL0, SDA1, SCL1): I_{OH} = 3mA			0.35	V
V_{OL}	Output voltage low	RC0..8 : I_{OH} = 1mA			0.35	V
$t_{PWMRISE}$	PWM Output Rise Time	RC0, RC1: C_L = 100 pF, Q_{tot} = 1 nC, 0% to 90% of Gate Drive, PWM_SYNC = 1			6	µs
$t_{PWMFALL}$	PWM Output Fall Time	RC0, RC1: C_L = 100 pF, Q_{tot} = 1 nC, 100% to 10% of Gate Drive, PWM_SYNC = 1			6	µs
R_{BUSPD}	Internal weak pull down resistance	RA0...3, Always ON	3.2	4	4.8	MΩ
R_{WKPD}	Internal pull down resistance	RA0...3 (SDA0, SCL0, SDA1, SCL1)	35	40	50	kΩ
R_{WKPD}	Internal pull down resistance	RC0...8	15	20	30	kΩ
R_{WKPU}	Internal pull up resistance	RC0...8	180	100	120	kΩ
C_I (1)	Input capacitance	RA0...3 (SDA0, SCL0, SDA1, SCL1)		1.8		pF
C_I (1)	Input capacitance	RC0...8		1.5		pF
I_{lkg} (1)	Input leakage current	RA0...3, including always on R_{BUSPD} pulldown		0.5	2	µA
I_{lkg} (1)	Input leakage current	RC0...8		1	2	µA
GPIO with ADC Inputs (RADC Port)						
V_{IN}	Input voltage range	RADCx/TS: When used as ADC input, Internal Reference (V_{REF1})	–0.2		1	V
		RADCx/TS: When used as ADC input, External Reference (V_{REG18})	–0.2		0.8 x V_{REG18}	V
		RADCx/TS without weak pull-up, where n = 0 to 8	–0.2		5.5	V
		RADCx/TS with weak pull-up where n = 0 to 8	–0.2		V_{REGIO}	V
V_{IH} (2)	High-level input voltage	RADCx/TS	0.7 x V_{REGIO}			V
V_{IL} (2)	Low-level input voltage	RADCx/TS0			0.3 x V_{REGIO}	V
V_{IOHYS} (1)	Hysteresis of Input	RADCx/TS	75			mV
V_{OH} (2)	Output voltage high	RADCx/TS: I_{OH} = -1 mA	0.7*V_{REGIO}			V
V_{OL} (2)	Output voltage low	RADCx/TS: I_{OL} = 3mA			0.3 x V_{REGIO}	V
R_{WKPD}	Internal weak pull down resistance	RADC0...8	0.8	1	1.2	MΩ
R_{WKPU}	Internal weak pull up resistance	RADC0...8	0.8	1	1.2	MΩ
C_I (1)	Input capacitance	RADC0...8		2		pF
I_{lkg} (1)	Input leakage current	RADC0...8		1	5	µA
Low Voltage GPIO with Current Sinks (RL/LED Ports)						
V_{IN}	Input voltage range	Without weak pull up	–0.2		5.5	V
V_{IN} (2)	Input voltage range	With weak pull up	–0.2		V_{REGIO}	V

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 85°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} (2)	High-level input voltage		0.7*V_{REGIO}			V
V_{IL} (2)	Low-level input voltage				0.3 x V_{REGIO}	V
V_{IOHYS} (1)	Hysteresis of Input		75			mV
V_{OH} (2)	Output voltage high	I_{OH} = -1 mA	0.7*V_{REGIO}			V
I_{OL}	Sink current	V_{OL} = 1 V	3.5	5	6.5	mA
R_{WKPD}	Internal weak pull down resistance		0.8	1	1.2	MΩ
R_{WKPU}	Internal weak pull up resistance		0.8	1	1.2	MΩ
C_I (1)	Input capacitance			5		pF
I_{lkg} (1)	Input leakage current			1	2	µA

(1) Specified by design. Not production tested.
(2) V_{REGIO} can be 1.8V or 3.3V depending on OTP configuration.

6.9 Aux REGOUT LDO

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_REGOUT}	Minimum V_{BAT} voltage for V_{REGOUT} operation(1)	V_{BAT} ≥ 7.5 V		7.5	8.5	V
$V_{REGOUT\_3.3}$	Regulator voltage (programmed to 3.3V setting)	VREGIN≥ 4.2 V, I_{REG} = 0 mA to 100 mA	3	3.3	3.6	V
$V_{REGOUT\_5.0}$	Regulator voltage (programmed to 5.0V setting)	V_{BREG} ≥5.8V, I_{REG} = 0 mA to 100 mA	4.5	5	5.5	V
Δ $V_{REGOUT(TEMP)}$	Temp regulation	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, I_{REGOUT} = 20 mA, V_{REGIN} = 5.5 V, V_{REGOUT}set to nominal 3.3 V setting)	–1.5	±0.25	1.5	%
Δ $V_{REGOUT(LINE)}$	Line regulation	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, V_{REGIN}= 5.5 V, I_{REGOUT} = 20 mA, as V_{REGIN} varies from 5 V to 6 V, V_{REGOUT} set to nominal 3.3 V setting)	–1		1	%
Δ $V_{REGOUTLOAD}$	Load regulation	I_{REGOUT} = 1 to 5 mA	–2.6		2.6	%
Δ $V_{REGOUTLOAD}$	Load regulation	I_{REGOUT} = 1 to 100 mA	–5		5	%
I_{SC}	Regulator short-circuit current limit with external BJT	V_{REGOUT}= 0 V	101		230	mA
C_{EXT_REGIN}	External capacitor REGIN to VSS(1)			0.02		µF
C_{EXT}	External capacitor REGOUT to VSS(1)		1			µF
$ΔV_{O(TEMP)}$	Regulator output over temperature	ΔV_{REGIN} vs V_{REGIN} at 25°C, I_{REGIN} = 50 mA, V_{BAT} > 8.5 V		±1		%
I_{Max}	Maximum current driven out from BREG without external BJT(1)	Under short circuit conditions (V_{BREG} = 0 V)	2	3	4	mA

(1) Specified by design

ADVANCE INFORMATION

6.10 LD Pin

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
RLD	LD pin serial resistor resistance		2	10		kΩ
$I_{(PULLUP)}$	Internal pullup current from BAT pin to LD pin, used for load detect functionality	V_{BAT} ≥ 8 V, V_{LD} = VSS	1.75	3	4.05	mA

6.11 Shelf Timer

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low Frequency Oscillator						
$F_{OSC\_SHUTDOWN}$	Oscilator Operating Frequency in Shutdown Mode			2		kHz
T_{WAKEUP_DELAY}	Preloaded Wake up Delay Time (Selectable options: 33s, 66s, 131s, 262s, 524s, 1048s, 2097s and 4194s)		33		4194	s
F_{LOSC_DRIFT} (1) (2)	Frequency Drift after Trim at Room Temp	25°C	-5		5	%
F_{LOSC_DRIFT} (1) (2)	Frequency Drift after Trim Across Temp	-25°C to 65°C	–8		8	%
		-40°C to 85°C	–10		10	%

(1) Specified by Design. Not production tested.
(2) The frequency drift is included and measured from the trimmed frequency at T_A = 25°C, with the minimum and maximum based on characterization, actual value stored in OTP.

6.12 Cell Balancing

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(CB)}$	Internal cell balancing resistance(1) (2)	$R_{DS(ON)}$ for internal FET switch at $V_{VC(n)}$ - $V_{VC(n-1)}$ = 1.5V, 1 ≤ n ≥ 16, V_{BAT} ≥ 4.7 V	15	28	46	Ω

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) Cell balancing must be controlled to limit the current based on the absolute maximum allowed current, and to avoid exceeding the recommended device operating temperature. This can be accomplished by appropriate sizing of the offchip cell input resistors and limiting the number of cells that can be balanced simultaneously.

6.13 Comparator-Based Detections (SCOMP)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OT} (1)	Overtemperature detection resistance threshold	OT_SEL = 0x07 to 0x7F		893 to 108000		Ω
		OT_SEL = 0x15 (35°C)		7200		Ω
		OT_SEL = 0x18 (40°C)		6000		Ω
		OT_SEL = 0x1c (45°C)		4909		Ω
		OT_SEL = 0x20 (50°C)		4154		Ω
		OT_SEL = 0x24 (55°C)		3600		Ω
		OT_SEL = 0x2a (60°C)		3000		Ω
		OT_SEL = 0x30 (65°C)		2571		Ω
		OT_SEL = 0x36 (70°C)		2250		Ω
		OT_SEL = 0x3e (75°C)		1929		Ω
		OT_SEL = 0x47 (80°C)		1662		Ω
		OT_SEL = 0x50 (85°C)		1459		Ω
		OT_SEL = 0x5c (90°C)		1256		Ω
		OT_SEL = 0x68 (95°C)		1102		Ω
		OT_SEL = 0x75 (100°C)		973		Ω
		OT_SEL = 0x7f (105°C)		893		Ω
R_{OT_ACC}	Overtemperature detection resistance threshold accuracy	T_A = -25°C to 65°C	–2.5		2.5	%
R_{OT_ACC}	Overtemperature detection resistance threshold accuracy	T_A = -40°C to 85°C	–5		5	%
V_{OCC}	Overcurrent in charge (OCC) voltage threshold range	Nominal settings, programmable in 2mV steps, threshold based on V_{SRP} - V_{SRN}	2		254	mV
V_{OCD}	Overcurrent in discharge (OCD1, OCD2) voltage threshold ranges	Nominal settings, programmable in 2mV steps, thresholds based on V_{SRP} - V_{SRN}	–2		–254	mV
V_{OC_ACC}	Overcurrent (OCC, OCD1, OCD2) detection voltage threshold accuracy	|Setting| < 20 mV	–1.5		1.5	mV
		|Setting| = 20 mV ~ 56 mV	–4		4	mV
		|Setting| = 56 mV ~ 100 mV	–5		5	mV
		|Setting| > 100 mV	–5		5	mV

(1) Expected temperature threshold using a 103AT NTC thermistor

6.14 SCOMP Timing Requirements

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SCOMP}	SCOMP Detection Clock Frequency			32768		Hz
F_{SCOMP_ERR}	SCOMP Detection Clock Frequency Error		–3		3	%
t_{SCD} (1) (2)	Short Circuit Fault Detection Delay	Programmable in 15.625µs interval after minimum delay	5		3970	µs
t_{OCC} (1) (2)	Over Current in Charge Fault Detection Delay	Programmable in 0.0625ms interval after minimum delay	0.187		1531	ms
t_{OCD1} (1) (2)	Over Current in Disharge 1 Fault Detection Delay	Programmable in 0.0625ms interval after minimum delay	0.187		1531	ms
t_{OCD2} (1) (2)	Over Current in Disharge Fault 2 Detection Delay	Programmable in 0.0625ms interval after minimum delay	0.187		1531	ms

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OT} (1) (2)	Over Temperature Fault Detection Delay	Programmable in 0.55ms interval after minimum delay	1		31	s
t_{WAKE_CD} (1) (2)	Current Wake in Discharge Detection Delay	Programmable in 0.187ms interval after minimum delay	0.187		383	ms
t_{WAKE_CC} (1) (2)	Current Wake in Charge Detection Delay	Programmable in 0.187ms interval after minimum delay	0.187		383	ms

(1) Specified by design. Not production tested.
(2) Not including LFO frequency error

6.15 SCD Comparator

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCD)}$	Short circuit in discharge voltage threshold range	Nominal settings, threshold based on V_{SRP} - V_{SRN}, programmable.	–500		–10	mV
$V_{(SCD\_ACC)}$	Short circuit in discharge voltage threshold detection accuracy(1)	T_A = -40°C to +85°C, $V_{(SCD)}$ settings < 20 mV	–15		15	% of nominal threshold
		T_A = -40°C to +85°C, $V_{(SCD)}$ settings ≥20 mV	–35		35	% of nominal threshold
$V_{(SCD\_DLY)}$	Short circuit in discharge detection delay	Fastest setting (with 3 mV on V_{SRN} - V_{SRP})		8		µs
		Fastest setting (with 25 mV on V_{SRN} - V_{SRP})		600		ns
		Nominal setting, programmable in 15.2 µs steps between min and max delay	19.2		3900	µs

(1) Specified by a combination of characterization and production test

6.16 High-side NFET Drivers (CHG and DSG and PCHG and PDSG)

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to LD/PACK, 6 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (1) (2)	V_{BAT} ≥ 6V, CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, charge pump normal operation setting	9	10	12	V
$V_{(FETON\_LP)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to LD/PACK, 6 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (1) (2)	V_{BAT} ≥ 6V, CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, charge pump low power mode setting	6	7	8.5	
$V_{(FET\_UVLO)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to LD/PACK, 6 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (1) (2)	V_{BAT} ≥ 6V, CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, charge pump in normal mode setting	4.5	5	6.5	V
$V_{(FET\_UVLO\_LP)}$	CHG pin voltage with respect to BAT, DSG pin voltage with respect to LD/PACK, 6 V ≤ V_{BAT} ≤ 80 V, V_{LD} ≤ V_{DSG} (1) (2)	V_{BAT} ≥ 6V, CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, charge pump UVLO at low power mode setting	2.5	3	3.5	

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SRCFOL\_FETON)}$	DSG on voltage with respect to BAT	CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, source follower mode		0		V
$V_{(CHGFETOFF)}$	CHG off voltage with respect to BAT	CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, steady state value			0.7	V
$V_{(DSGFETOFF)}$	DSG off voltage with respect to LD/PACK	CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, steady state value			0.1	V
$t_{(CHG/DSG\_FET\_ON)}$	CHG and DSG rise time	CHG/DSG C_L = 20nF, R_{GS} = 10MΩ, R_{GATE} = 100 Ω, 0.5 V to 4 V gate-source overdrive, charge pump high overdrive setting(4) (5)		21	40	µs
$t_{(CHGFETOFF)}$	CHG fall time to BAT	CHG C_L = 20nF, R_{GS} = 10MΩ, R_{GATE} = 100 Ω, 90% to 10% of $V_{(FETON)}$ (5)		46	65	µs
$t_{(DSGFETOFF)}$	DSG fall time to LD/PACK	DSG C_L = 20nF, R_{GATE} = 100Ω, R_{GS} = 10MΩ, 90% to 10% of $V_{(FETON)}$ (5)		2	20	µs
$t_{(PCHG/PDSG\_FET\_ON)}$	PCHG and PDSG rise time	PCHG/PDSG C_L = 5nF, R_{GS} = 10MΩ, R_{GATE} = 100Ω, 0.5V to 4V gate-source overdrive, charge pump high overdrive setting(4) (5)		21	40	µs
$t_{(PCHGFETOFF)}$	PCHG fall time to BAT	PCHG C_L = 5nF, R_{GS} = 10MΩ, R_{GATE} = 100Ω, 90% to 10% of $V_{(FETON)}$ (5)		150	250	µs
$t_{(PDSGFETOFF)}$	PDSG fall time to LD/PACK	PDSG C_L = 5nF, R_{GS} = 10MΩ, R_{GATE} = 100Ω, 90% to 10% of $V_{(FETON)}$ (5)		150	250	µs
$t_{(CP\_START)}$	Charge pump start up time	C_L = 20nF, $C_{(CP1)}$ = 470nF, 10% to 90% of $V_{(FETON)}$			20	ms
$C_{(CP1)}$	Charge pump capacitor(3)		100	470	2200	nF

(1) Operation with V_{BAT} up to 80 V is supported when the charge pump is not in operation. Whenever the charge pump is in operation (in 5.5 V or 11 V mode), the maximum voltage on V_{BAT} should be reduced to ensure the voltage on CP1, CHG, and DSG does not exceed their maximum specified voltage.
(2) When the DSG driver is enabled, the CHG driver is disabled, and a voltage is applied at the LD pin such that $V_{LD} > V_{DSG}$, the voltage at DSG will rise to ≈ V_{LD} - 0.7 V
(3) Specified by design
(4) Specified by characterization
(5) R_{GATE} can be optimized during design and system evaluation for best performance. A larger value may be desired to avoid an overly fast FET turn on/off, which can result in a large voltage transient due to cell and harness inductance.

6.17 FUSE Pin

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage high (when driving fuse)	V_{BAT} [char_not_recognized] 8 V, C_L = 10 nF, 5 kΩ load.	6	6.5	7	V
V_{OH}	Output voltage high relative to V_{BAT} (when driving fuse)	2.7 V [char_not_recognized] V_{BAT} < 8 V, C_L = 10 nF, 5 kΩ load.	–1.5		0	V
V_{IH}	High-level input (for fuse detection)	Current into device pin must be limited to maximum 2 mA	2			V
V_{IL}	Low-level input (for fuse detection)				0.9	V
C_{IN} (1)	Input capacitance			1.8		pF

(1) Specified by Design. Not Production Tested

6.18 Flash Memory

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR} (1)	Data retention		10	100		Years

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Flash programming write-cycles(1)		20000			Cycles
t_{FPWRUP} (2)	Flash Power Up Time	From PM_CONFIG_ACTIVE change to PM_CONFIG_ST update		150	200	µs
$t_{FPWRDOWN}$ (1)	Flash Power Down	From PM_CONFIG_ACTIVE change to PM_CONFIG_ST update		6	15	µs
$t_{ROWPROG}$ (1)	Word (128 bits) programming time	Including High Level API (ROM API) use		100		µs
$t_{MASSERASE}$ (1)	Mass-erase time	Including High Level API (ROM API) use		34	500	ms
$t_{SECTORERASE}$ (1)	Sector-erase time	Including High Level API (ROM API) use		14	500	ms

(1) Specified by design. Not production tested.
(2) Confirmed by Characterization. Not production tested.

6.19 Interface I/O

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C						
V_{IH} (2)	Input voltage high	SDA,SCL	0.7*V_{REG18}			V
V_{IL} (2)	Input voltage low	SDA,SCL	–0.5		0.3*V_{REG18}	V
V_{OL}	Output low voltage	SDA,SCL, I_{OL} = -3mA			0.4	V
t_{SP} (1)	Pulse width of spikes that must be suppressed by the input filter	SDA,SCL, AGFSEL = 0x3			50	ns
C_{IN} (1)	Input capacitance	SDA,SCL		1.8		pF
C_B (1)	Bus capacitance per line	SDA, SCL			100	pF
I_{LKG} (1)	Input leakage current	SDA,SCL, including always on R_{BUSPD} pull down		0.5	2	µA
SMBus						
V_{BUS}	Nominal Bus Voltage	SMBD, SMBC	1.8		5	V
	Operating Bus Voltage	SMBD, SMBC	1.62		5.5	V
V_{IH}	Input voltage high	SMBD, SMBC	1.35		V_{BUS}	V
V_{IL}	Input voltage low	SMBD, SMBC			0.8	V
V_{OL}	Output low voltage	SMBD, SMBC, I_{OL} = -3mA			0.4	V
t_{SP} (1)	Pulse width of spikes that must be suppressed by the input filter	SMBD, SMBC, AGFSEL = 0x3			50	ns
C_{IN} (1)	Input capacitance	SMBD, SMBC		1.8		pF
C_B (1)	Bus capacitance per line	SMBD, SMBC			100	pF
I_{LKG} (1)	Input leakage current	SMBD, SMBC, , including always R_{BUSPD}on pull down		0.5	2	µA

(1) Specified by design. Not prodcution Tested
(2) When used with pull up voltages greater than V_{REG18} the voltage and timing thresholds are still based on V_{REG18}.

6.20 I²C Interface Timing

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
I2C 100 kHz					

ADVANCE INFORMATION

Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SCL}	Clock Frequency				100	kHz
$t_{HD:STA}$	START Condition Hold Time		4			µs
t_{LOW}	LowPeriod of SCL Clock		4.7			µs
t_{HIGH}	HighPeriod of SCL Clock		4			µs
$t_{SU:STA}$	Setup Time for repeated START		4.7			µs
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:DAT}$	Data in Setup Time		250			ns
	Data out Setup Time		250			ns
t_r (2)	SDA and SCL Rise Time	30% to 70% of V_{REGIO}			1000	ns
t_F (2)	SDA and SCL Fall Time	30% to 70% of V_{REGIO}			300	ns
$t_{SU:STO}$	STOP Condition Setup Time		4			µs
t_{BUF}	Bus Free Time between STOP and START		4.7			µs
$t_{VD:DAT}$ (1) (3) (4)	Data Valid Time				3.45	µs
$t_{VD:ACK}$ (1) (3) (4)	Data Valid Acknowledge Time				3.45	µs
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x1		0.5		s
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x2		1		s
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x4		2		s
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x7		3.5		s
C_D	Capacitive load for each bus line				400	pF
I2C 400 kHz						
f_{SCL}	Clock Frequency				400	kHz
$t_{HD:STA}$	START Condition Hold Time		0.6			µs
t_{LOW}	LowPeriod of SCL Clock		1.3			µs
t_{HIGH}	HighPeriod of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for repeated START		0.6			µs
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:DAT}$	Data in Setup Time		100			ns
	Data out Setup Time		100			ns
t_r (2)	SDA and SCL Rise Time	30% to 70% of V_{REGIO}	20		300	ns
t_F (2)	SDA and SCL Fall Time	30% to 70% of V_{REGIO}	20 * (V_{REGIO}/ 5.5)		300	ns
$t_{SU:STO}$	STOP Condition Setup Time		0.6			µs
t_{BUF}	Bus Free Time between STOP and START		1.3			µs
$t_{VD:DAT}$ (1) (2) (3)	Data Valid Time				0.9	µs
$t_{VD:ACK}$ (1) (2) (3)	Data Valid Acknowledge Time				0.9	µs

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Typical values stated where T_A = 25°C and V_{BAT} = 59.2 V, min/max values stated where T_A = -40°C to 105°C and V_{BAT} = 5 V to 80 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x1		0.5		s
		BUSLOWCNT = 0x2		1		s
		BUSLOWCNT = 0x4		2		s
		BUSLOWCNT = 0x7		3.5		s
C_D	Capacitive load for each bus line				400	pF
I2C 1 MHz						
f_{SCL}	Clock Frequency				1000	kHz
$t_{HD:STA}$	START Condition Hold Time		0.26			µs
t_{LOW}	LowPeriod of SCL Clock		0.5			µs
t_{HIGH}	HighPeriod of SCL Clock		0.26			µs
$t_{SU:STA}$	Setup Time for repeated START		0.26			µs
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:DAT}$	Data in Setup Time		50			ns
	Data out Setup Time		50			ns
t_r (2)	SDA and SCL Rise Time	30% to 70% of V_{REGIO}			120	ns
t_F (2)	SDA and SCL Fall Time	30% to 70% of V_{REGIO}	20 * (V_{REGIO}/ 5.5)		120	ns
$t_{SU:STO}$	STOP Condition Setup Time		0.26			µs
t_{BUF}	Bus Free Time between STOP and START		0.5			µs
$t_{VD:DAT}$ (1) (2) (3)	Data Valid Time				0.45	µs
$t_{VD:ACK}$ (1) (2) (3)	Data Valid Acknowledge Time				0.45	µs
t_{BUSLOW}	Max SCL/SDA Low (BUSLOW) Signal Detect Time by device	BUSLOWCNT = 0x1		0.5		s
		BUSLOWCNT = 0x2		1		s
		BUSLOWCNT = 0x4		2		s
		BUSLOWCNT = 0x7		3.5		s
C_D	Capacitive load for each bus line				100	pF

(1) This maximum is only met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(2) V_{REGIO} can be 1.8V or 3.3V depending on OTP selection.
(3) $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(4) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

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7 Detailed Description

7.1 Overview

The BQ41Z90 battery pack manager is a highly integrated device that employs flash-based firmware and integrated hardware protection to provide a complete solution for battery stack architectures with 3 to 16 series cells in series. The BQ41Z90 device utilizes Dynamic Z-Track™ technology to report highly accurate state of charge even under dynamic loading conditions. This technology is the extension of TI's renowned Impedance Track™ gauging algorithm which tracks the changing impedance over the lifetime of the battery to provide accurate full charge capacity (FCC), state of charge (SoC), and state of health (SoH) estimations.

The BQ41Z90 device supports systems with FETs in a series configuration as well as systems with parallel charging and discharging paths to accommodate different magnitudes of charging current vs. discharging current. In parallel configuration the device can connect to the charger connector while discharging through the load connection. The device also support systems that only use one FET or no FETs, replacing the FETs with external protectors.

The BQ41Z90 device provides Elliptic Curve Cryptographic (ECC) authentication capability to boost the battery pack security in addition to the SHA-1 and SHA-2 authentication options. The ECC authentication uses unique asymmetrical private/public key cryptography, eliminating the requirement of sharing the same secret in the host system.

The BQ41Z90 device provides hardware comparators to detect fault conditions due to over-voltage, over-temperature, short circuit detection, and over-current under charge and discharge, as well as the hardware drivers to turn off the FETs to protect the device from these fault conditions. The device firmware provides software-based 1st- and 2nd-level safety alerts and protection against over-voltage, under-voltage, over-current, short circuit current, and over-temperature conditions, as well as other fault conditions such as hardware watchdog timed-out or cell charge/voltage imbalance.

The BQ41Z90 battery pack manager interfaces with a host system through an SBS v3.2 compliant SMBus interface or an I^2C-compliant interface, and processes instructions and data using a state-of-the-art, ultra-low-power 32-bit RISC processor. High-performance integrated peripherals enable support for a sense resistor down to 0.25mΩ, with simultaneous current/voltage data conversion for instant power calculations.

The following sections detail all of the major component blocks included as part of the BQ41Z90 Battery Manager.

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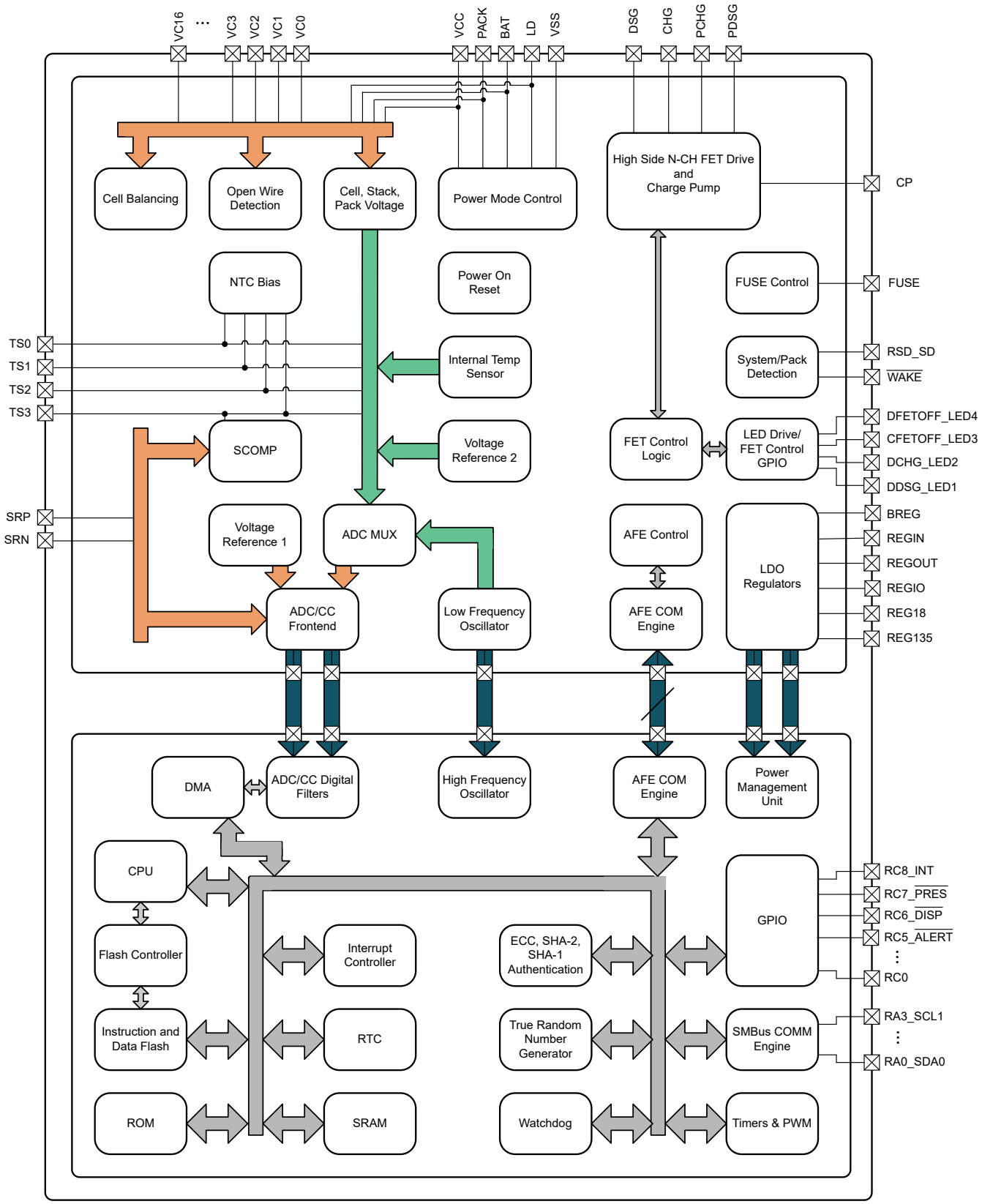
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Functional Modes

7.3.1.1 Analog Front End (AFE)

The Analog Front End (AFE) includes most of the analog features of the device including the following:

- Analog to Digital Converters (ADCs) used for measuring cell voltages, temperatures and other signals.
- Coulomb Conter (CC) used for measuring coulombs and current flow.
- High-Side NFET Drivers for Charge, Precharge, Discharge and Predischarge control and protection.
- Low Drop Out Regulators (LDOs) to power the AFE and source the power to the MCU.
- Low Frequency Oscillator (LFO) which is the main clock for the AFE.
- Array of protection features through Hardware Fault Detection (SCOMP and SCD).
  - Over Current in Discharge (OCD)
  - Over Current in Charge (OCC)
  - Over Temperature (OT)
  - Short Circuit Detection (SCD)
- Cell bypass control to support Section 6.12 and Open Wire Detection (OWD)
- Constant Current Sink I/O support for LED drive

Each of the features have a range of configurable options which are detailed in the AFE Registers section.

7.3.1.2 Power Management

The BQ41Z90 includes three LDOs and many configuration options that need to be managed to support correct operation of the device and ensure the device power consumption is optimal for a given usage case.

7.3.1.2.1 Power Mode Block Configuration

The BQ41Z90 has many features that can be enabled and disabled through firmware control.

Transitioning between the various power mode configurations, except SHUTDOWN, is primarily under the control of firmware and features that can be enabled to create an interrupt such as GPIO, communications, current detections, charger detection, ADC state machine, RTC, and timers.

Table 7-1. Power Mode Transition

	Next State					
Current State	Normal	Sleep	DeepSleep	Hibernate	Shelf	Shutdown
Normal	--	Firmware	Firmware	Firmware	Firmware	Firmware/ Low voltage
					RST_SD Pushbutton	
Sleep	IO, comms,protection, current flow above threshold, charger detect	--			RST_SD Pushbutton	Low voltage
DeepSleep	IO, comms, charger detect, RTC timer		--		RST_SD Pushbutton	Low voltage
Hibernate	IO, comms, charger detect, RTC timer			--	RST_SD Pushbutton	Low voltage
Shelf	charger detect, shelf timer, WAKE button				--	Low voltage
Shutdown	charger detect, WAKE button					--

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7.3.1.2.2 Power Supply Control

The BQ41Z90 device manages it's supply voltage dynamically according to operating conditions.

To initiate the exit from SHUTDOWN mode, the WAKE push button must be detected if $V_{BAT} > V_{SWITCHOVER–} + V_{HYS}$, or the PACK pin must be connected to a voltage above $V_{STARTUP,}$ for example, a charger is attached. The device will then connect an internal switch to VCC and uses this pin to supply power to its internal 1.8-V LDO, which subsequently powers all device logic and flash operations. The device continues to be powered from VCC until $V_{BAT} > V_{SWITCHOVER–} + V_{HYS}$ at this time the AFE connects an internal switch to BAT to power the device and disconnects the switch from VCC.

It is expected that the DSG FET is connected where its body diode allows current to flow from the PACK+ node to the VCC pin of the device so no direct power supply connection to VCC is needed.

If BAT decreases to $V_{BAT} < V_{SWITCHOVER–}$, the AFE will connect an internal switch to VCC to power the device and disconnects the switch from BAT, allowing sourcing of power from a charger. If there is no valid power source on the VCC pin then the device will power down.

An external diode and capacitor connected to BAT provide a momentary supply voltage to help guard against system brownouts due to transient short-circuit or overload events that would otherwise pull V_{BAT} below $V_{SWITCHOVER–}$.

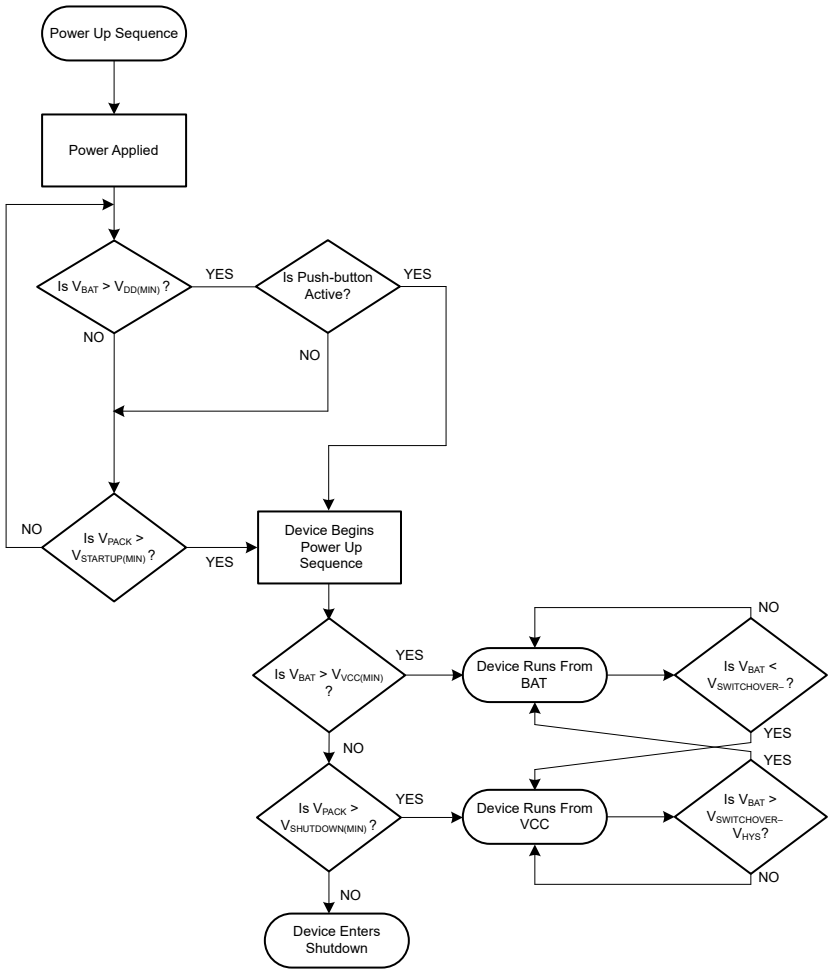

Figure 7-1. Power-Up Sequence

7.3.1.2.2.1 HIBERNATE Mode

HIBERNATE mode is a low power mode where major blocks within the device are completely powered down to minimize power consumption while still allowing the device to exit HIBERNATE without the connection of a charger. Entry to HIBERNATE is through firmware command. The main method for exiting HIBERNATE is through charger detection, a WAKE pin assertion, or using the real time clock alarm function.

When entering HIBERNATE mode, the MCU can configure the device to keep RAM enabled and to enable the real time clock. If the FETs are required to be OFF in HIBERNATE mode, then the firmware must turn them off before HIBERNATE is entered. The device cannot exit HIBERNATE through I2C/SMBus communications, which are disabled by firmware control to conserve power. If it is not disabled and an I2C/SMBus START is received the device will clock stretch until the 25ms SCL low timeout while waiting for the HFO to startup, even though the HFO will not start up in HIBERNATE mode.

7.3.1.2.2.2 SHUTDOWN Mode

SHUTDOWN mode is an ultra-low power mode where the device is completely powered down except for support circuits enabling the device to be able to exit SHUTDOWN. The primary exit circuit is a small voltage detection circuit that uses the internal R_{PACK_PD} and the external R_{PACK} to detect the $V_{STARTUP}$ threshold at the PACK pin. R_{PACK_PD} is automatically enabled upon entry to SHUTDOWN but can also be enabled and disabled under FW control.

The device can be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. If the top-of-stack voltage falls below a programmed stack voltage threshold, or if the minimum cell voltage falls below a programmed cell voltage threshold, the SHUTDOWN mode sequence is automatically initiated. The shutdown based on cell voltage does not apply to cell input pins being used to measure interconnect.

While the BQ41Z90 device is in NORMAL mode or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds a programmed temperature threshold for a programmed delay if this functionality is enabled through configuration.

See Power Supply Control for more details on powering up from SHUTDOWN mode.

7.3.1.2.2.3 SHELF Mode

SHELF mode is when the device is in shutdown mode but with an activated low power timer that can be used to log the time and periodically wake up for cell measurement as needed. This mode can be used for shipping or long-term storage.

When the SHELF mode sequence has been initiated by subcommand in the firmware or the RST_SD pin driven high for 5-sec, the device will wait for a delay then disable the protection FETs before entering SHELF mode. However, if the voltage on the PACK or LD pin is still above the $V_{STARTUP}$ level, shutdown will be delayed until the voltage on PACK or LD falls below that level.

The device can be configured to perform periodic memory integrity checks and will force a watchdog reset if any corruption is detected. To avoid a cycle of resets in the case of a memory fault, the device will enter SHUTDOWN mode rather than resetting if a memory error is detected within a programmed number of seconds after a watchdog reset has occurred.

SHUTDOWN mode has priority over SHELF mode and will override and reset all analog registers associated with SHELF mode. In SHELF mode, when the battery voltage drops below the preprogrammed threshold, the gauge will enter SHUTDOWN mode for power saving. Prior entering the SHUTDOWN or SHELF mode, the Wake pin needs to pull up high to be able to wake up the device from shutdown.

7.3.1.2.2.4 Wake Functionality

The device can be waken up by interrupt from GPIO or Communications, or by RTC Timer during Sleep or Hibernate. While the device is in SHUTDOWN or SHELF mode, the device can be waken up by the Wake pin or a voltage applied at the PACK pin above $V_{STARTUP}$ (such as when a charger is attached in series FET configuration).

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A ≈5 V voltage is provided at the RADC4_Wakep pin with high source impedance. If the RADC4 pin is pulled low, such as by a switch to VSS, the device will exit SHUTDOWN or SHELF mode.

Note

RADC4 can't be used to connect to a thermistor for temperature measurement.

When the device is wakened from SHUTDOWN, internal circuitry including the LDOs will start power up and MCU will perform initiation, load settings from memories, perform initial measurements, evaluate those relative to enabled protections, then to enable FETs if conditions allow. This can be configured for a faster power-up depending on settings.

As a countermeasure to avoid an unintentional wake from SHELF mode when putting the BQ41Z90 device into long-term storage, the device can be configured to automatically reenter SHELF mode after a programmed number of minutes.

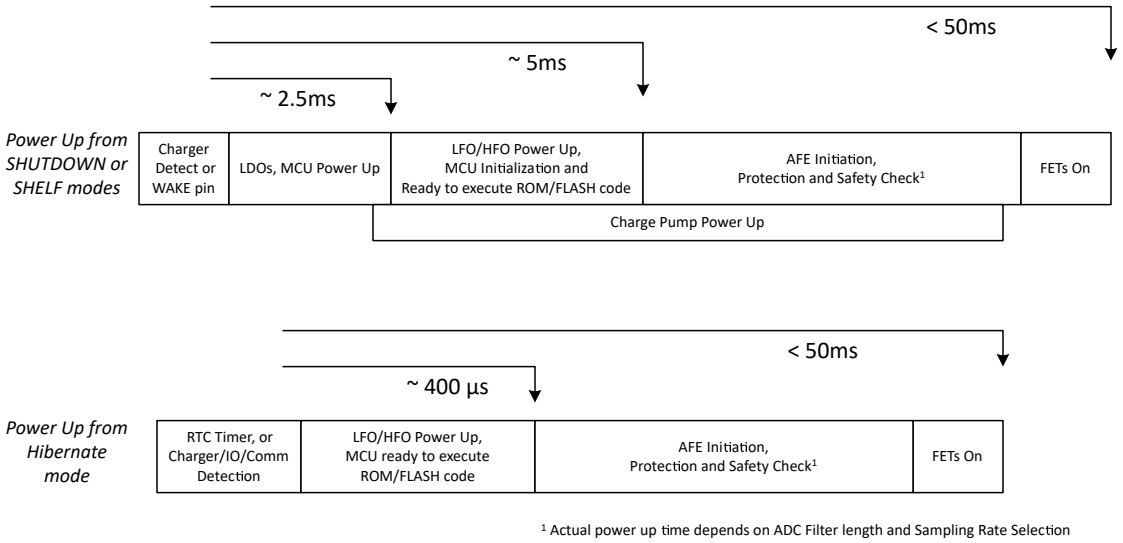

Figure 7-2. Device Wake-Up Timing

7.3.1.2.3 Power Management Unit

7.3.1.2.3.1 PMU Overview

The MCU digital die has three hardware power modes: RUN, STOP, and STANDBY managed by a state machine.

RUN is the active power mode. All functions can be operating including the FLASH memory in read, erase, or program mode. The RAM and ROM can be on, the processor can run at full clock frequency and all peripherals can be active. RUN mode also allows the firmware to turn off FLASH, RAM, or ROM if not used to save power.

STOP is a low power mode. In this mode, the FLASH and ROM can be turned off and the RAM can be put in retention to save power. The processor is halted in this mode, but other peripherals can continue to run.

STANDBY is a low power mode. In this mode, the sleep signal to the AFE is asserted, changing the state of the VDD core voltage regulator (REG135) from normal to low power mode. In this mode, the HFO is off and only select peripherals are running. Since the LDO is in low power mode, this mode disables the FLASH and ROM and puts the RAM in retention mode. Logic runs at 32 kHz once this mode is entered.

The typical mapping from PMU modes to system power modes is:

- RUN: NORMAL
- STOP: SLEEP and DEEPSLEEP
- STANDBY: HIBERNATE and entry to SHUTDOWN; exit from SHUTDOWN is through reset.

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7.3.1.2.4 Thermal Shutdown

The BQ41Z90 uses an integrated temperature sensor local to the LDOs to determine if the device is overheating. If the internal temperature sensor reaches t_{SD_ALERT+}, then the MCU is placed in RESET and disables REG135 although REG18 and the AFE remain enabled. If the temperature then falls and reaches t_{SD_ALERT-}, the device enables the REG135 and allows the MCU powerup sequence to begin.

However, if the temperature continues to rise and the internal temperature sensor reaches t_{SD+}, then the device is placed in RESET with both REG135 and REG18 disabled. When the internal device temperature falls below $t_{SD–}$, then the REG18 is allowed to power up, but the device power-up sequence is not allowed to begin until the temperature falls below $t_{SD\_ALERT–}$.

7.3.1.2.5 Low Drop Out Regulators (LDOs)

The BQ41Z90 includes four low dropout regulators to support the device, a 1.8-V nominal output LDO (REG18), a 1.35-V nominal output LDO (REG135), REGIO (1.8 V / 3.3 V), and REGOUT (programmable 2.5 V, 3 V, 3.3 V, and 5 V).

7.3.1.2.5.1 REG18

This regulator resides on the AFE is used to provide power to the AFE, REG135, flash charge pump, GPIO, and analog circuits of the MCU die. A 1-µF capacitor (C_{REG18}) is required to be connected as close to the REG18 pin as possible for optimal operation.

There is output short protection of the LDO, although this protection limit is reduced in HIBERNATE mode.

The REG18 output is available to be used external to the device to power other circuits but is limited to the maximum current of $I_{REG18EXT}$.

Note

The maximum load current available from the REG18 LDO includes both the REG135 LDO current and any external load currents on the REG18 pin.

7.3.1.2.5.2 REG135

This regulator resides on the AFE is used to provide power to the MCU digital core including the CPU, RAM, ROM, and flash. A 1-µF capacitor (C_{REG135}) is required to be connected as close to the REG135 pin as possible for optimal operation.

There is output short protection of the LDO although this protection limit is reduced in HIBERNATE mode.

The REG135 output is not available to be used by external circuits.

7.3.1.2.5.3 REGIO

BQ41Z90 has a dedicated LDO to provide the VDDIO for the communications IOs. The output voltage of REGIO can be programmed to 3.3V or 1.8V through OTP bit control. If the OTP bit is programmed to let the firmware control the default voltage level, the default voltage is determined by flash configuration bit. Otherwise the OTP sets the REGIO voltage to 3.3V by default.

7.3.1.2.5.4 REGOUT

The REGOUT LDO in the BQ41Z90 device is for external use, and its output voltage can be programmed to 2.5 V, 3.0 V, 3.3 V, or 5.0 V. It needs to be used with an external BJT to carry the large current when used to drive pheriperal devices. When BQ41Z90 is powered off, REGOUT can be ORed with external power supply to continue to drive the external devices.

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7.3.1.3 Reset Management

The BQ41Z90 device can be reset through several hardware methods including a Power-On-Reset (POR), Windowed Watchdog timer (WWDT) initiated reset, optional FLASH DED initiated reset, security violation initiated reset and CPU initiated reset. The device can also be triggered to MCU reset or Power-On-Reset through an external pin assertion (see the description in the next section). Through communications from the host the device can also be configured into reset if the application firmware on the device is programmed to allow this and is operational, for example: the use of a ManufacturerAccess( ) command to trigger an MCU power cycle.

Table 7-2. Reset sources and the block they reset

Reset Type	Blocks Reset						
	CPU	MCU DieDigital	RAM	Communications	Diagnostics Registers on MCU (2)	Diagnostics Registers on AFE(3)	AFE
POR	X	X	X	X	X	X	X
MCU	X	X	X	X			
WWDT	X						
Communications(1)	X	X	X	X		X	X

(1) Based on implemented firmware functionality
(2) Diagnostic Regs on MCU are: FAULT_LOG and USER_DATA
(3) Diagnostic Regs on AFE are: AIF_CTRL1 [MCU_RESET_REASON]

- **Power-On-Reset (POR)**

  The AFE enters power-on reset when the voltage at V_{REG18} falls below $V_{REG18POR–}$ which is typically triggered by voltage at both BAT and VCC pins being removed. The device exits reset when V_{REG18} rises above $V_{REG18POR–}$ + V_{HYS} for t_{RST} time.

  In the event of a power-cycle, the BQ41Z90 AFE will hold its internal RESET output pin high for t_{RST_POR} duration to allow its on-chip trim to load and the integrated 1.8 V LDO, 1.35 V LDO and LFO to stabilize before releasing the MCU die from its reset.

  When the MCU die is released from reset it will power up and perform some limited trim loading and then enable the CPU. The time from when power is applied until this stage is t_{RST_ROM}.

  Once the CPU boots up and the ROM initialization code has run then the flash code can begin to execute. The time from when power is applied until this stage is t_{RST_EXE}.
- **MCU Reset**

  The MCU Reset can be triggered by the WWDT, CPU, Security violation or optional Flash DED

  – CPU initiated reset.

    This is on the MCU and doesn't influence the AFE. This resets everything related to the CPU.
- **Windowed Watchdog timer initiated reset**

  This is on the MCU and doesn't influence the AFE. This resets everything in the MCU other than the RESET_REASON register which indicates that the WWDT triggered the RESET and the USER_DATA register.
- **MCU Power Recycle Reset**

  The MCU of the BQ41Z90 can be reset through a command to the AFE. If activated then the AFE will cycle power to the MCU by disabling and then enabling the REG135 regulator output of the AFE.

7.3.1.3.1 RST_SD Pin Operation

The RST_SD pin provides a simple way to reset or shutdown the BQ41Z90 device without needing to use serial bus communication. During normal operation, the RST_SD pin should be driven low. When the RSD_SD pin is driven high, we debounce and take one of the following actions:

- An alert can be sent to the MCU to notify the firmware to reset the serial communication bus
- Hold the MCU in reset until RST_SD pin is released
- Rest MCU and shuts down REG135 until RST_SD is released. REG135 is restored after RST_SD is released

RST_SD does not reset the logic that holds the state of the protection FETs and FUSE.They remain as they were before the pin was driven high until the programmable AFE timer expires.

If the pin continues to be driven high for 5 second, the device will then transition into SHUTDOWN mode 1, which disables external protection FETs and powers off the internal oscillators and the LDOs. The shutdown timer can be used to with the pre-programmed time to periodically wake up for measurement and data logging.

7.3.1.3.2 AFE Watchdog

BQ41Z90 has an AFE Watchdog feature to ensure that if the MCU is no longer responsive for any reason, the FETs are not left ON indefinitely.

The Watchdog timer is only enabled when the FETs are on.

Note

The WDT Alert cannot be used to wake the MCU unless the FETs are left on

There are 3 programmable timers.

- The first provides an Alert timer with 0.25 seconds increments, up to 32 seconds
- The second provides the time that follows the Alert before the MCU is reset in 0.25 seconds increments, up to 8 seconds
- The third provides the time after the MCU reset before the FETs are turned off, in 0.25 seconds increments, up to 8 seconds

The MCU periodically acknowleges the AFE watchdog to reset all timers and to allow the FETs to be turned on.

7.3.1.4 Diagnostics Features

The BQ41Z90 device includes a suite of diagnostic features that the system can use to improve operation robustness. These include self-checking the voltage references integrated within the device, self-checking the LDO output, a hardware monitor of the LFO frequency, an internal watchdog on the MCU, memory checks at power-up or reset, and more. The integrated flash and SRAM also come with ECC features. The BQ41Z90 Technical Reference Manual describes these in detail.

7.3.1.5 Internal Oscillators

The BQ41Z90 has two integrated oscillators to support different functions of the device. Each clock source supports a variety of internal clock frequencies that are managed automatically to ensure that the individual frequencies and the oscillator source is enabled and disabled when needed. The low frequency oscillator is always on.

7.3.1.5.1 Low Frequency Oscillator (LFO)

The low frequency oscillator, which is typically 262.144 kHz, is on the AFE die and is powered from REG18. The LFO is used to manage the AFE and is also provided to the MCU through an internal die to die connection.

The device includes an LFO watchdog that can trigger faults and actions to turn off the protection FETs (if configured).

7.3.1.5.2 High Frequency Oscillator (HFO)

The high frequency oscillator, which is typically 32.768 MHz, is on the MCU die and is powered from REG18.

The HFO is used for the CPU and digital peripherals on the MCU and a divided down 524.288-kHz output is provided for the ADC modulator when that mode is enabled.

7.3.1.5.3 Low Power Oscillator (LPO)

The LPO is a dedicated oscillator circuit that runs at 2 kHz typical to create the Shelf Timer. An AFE register can configured to indicate whether or not the device has awaken from SHELF mode after a POR event.

The timer counts down a delay time after the device enters SHELF Mode. The delay time to wake up can be configured prior to entering the SHELF mode. Preloaded Wake-up delay time can be selected between 33s, 66s, 131s, 262s, 524s, 1048s, 2097s and 4194s. Once in SHELF mode BQ41Z90 can wake up peirodically to do safety check and log the measurement data.

7.3.2 Temperature Measurement

The BQ41Z90 can measure an integrated temperature sensor and also up to four external negative temperature coefficient (NTC) thermistors.

7.3.2.1 External Temperature Measurement Support

The BQ41Z90 device can support up to four external thermistors on the RADCx port pins. The device includes two 18-kΩ (typ) internal pullup resistors to bias a thermistor during measurement. The first is used for RADC0, RADC1, and RADC2 while the second is used for RADC3. RADC3 is also used as the temperature input to the hardware fault detection (SCOMP) block. The RADC3 resistor is trimmed and that trim is shared with the RADC0..2 resistor.

The two resistor values and RADCx pad resistance are measured during factory production and stored within the device for use during temperature calculations. Any additional internal interconnect resistance is < 1 Ω.

To provide a high precision temperature result, the device uses the same 1.8-V LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level.

When the RADCx pin is not used it should be enabled with its internal weak pulldown.

7.3.2.2 Internal Temperature Sensor

The integrated temperature sensor is located near the REG18 LDO in the AFE die and is used to determine the thermal shutdown of the device if the device becomes too hot and can also be measured via the ADC through selection in the ADC multiplexer.

7.3.3 Random Cell Connection Support

The BQ41Z90 device supports a random connection sequence of cells to the device during pack manufacturing. When the cells are connected to the BQ41Z90 they can be connected in any order although it is recommended to connect VSS and VC0 first. For example, cell-10 in a 16-cell stack might be first connected at the input terminals leading to pins VC10 and VC9, then cell-4 may next be connected at the input terminals leading to pins VC4 and VC3, and so on. It is not necessary to connect the negative terminal of cell-1 first at VC0. As another example, consider a cell stack that is already assembled and cells already interconnected to each other, then the stack is connected to the PCB through a connector, which is plugged or soldered to the PCB. In this case, the sequence order in which the connections are made to the PCB can be random in time, they do not need to be controlled in a certain sequence.

There are, however, some restrictions to how the cells are connected during manufacturing:

- To avoid misunderstanding, note that the cells in a stack ***cannot*** be randomly connected to ***any*** VC pin on the device, such as the lowest cell (cell-1) connected to VC15, while the top cell (cell-16) is connected to VC4, and so on. It is important that the cells in the stack be connected in ascending pin order, with the lowest cell (cell-1) connected between VC1 and VC0, the next higher voltage cell (cell-2) connected between VC2 and VC1, and so on.
- The random cell connection support is possible due to high voltage tolerance on pins VC1–VC16.

Note

VC0 has a lower voltage tolerance. This is because VC0 should be connected through the series-cell input resistor to the VSS pin on the PCB, before any cells are attached to the PCB. Thus, the VC0 pin voltage is expected to remain close to the VSS pin voltage during cell attach. If VC0 is not connected through the series resistor to VSS on the PCB, then cells cannot be connected in random sequence.

- Each of the VC1–VC16 pins includes a diode between the pin and the adjacent lower cell input pin (that is, between VC16 and VC15, between VC9 and VC8, and so on), which is reverse biased in normal operation. This means an upper cell input pin should not be driven to a low voltage while a lower cell input pin is driven to a higher voltage, since this would forward bias these diodes. During cell attach, the cell input terminals should generally be floating before they are connected to the appropriate cell. It is expected that transient current will flow briefly when each cell is attached, but the cell voltages will quickly stabilize to a state without DC current flowing through the diodes. However, if a large capacitance is included between a cell input pin and another terminal (such as VSS or another cell input pin), the transient current may become excessive and lead to device heating. Therefore, it is recommended to limit capacitances applied at each cell input pin to the values recommended in the specifications.

Note

After the cells are first connected, the WAKE pin can be used to power up the device only after the device power supply is stablizied to pull up the pin.

See Power Supply Control for further details on the device powering up.

7.3.3.1 Usage of VC Pins for Cells Versus Interconnect

If the BQ41Z90 device is used in a system with fewer than 16-series cells, the additional cell inputs can be utilized to improve measurement performance. For example, a long connection may exist between two cells in a pack, such that there may be significant interconnect resistance between the cells, such as shown in Figure 7-3 between CELL-A and CELL-B. By connecting VC12 close to the positive terminal of CELL-B, and connecting VC13 close to the negative terminal of CELL-A, more accurate cell voltage measurements are obtained for CELL-A and CELL-B, since the I·R voltage across the interconnect resistance between the cells is not included in either cell voltage measurement. Since the device reports the voltage across the interconnect resistance and the synchronized current, the resistance of the interconnect between CELL-A and CELL-B can also be calculated and monitored during operation. It is recommended to include the series resistance and bypass capacitor on cell inputs connected in this manner, as shown below.

Note

It is important that the differential input for each cell input not fall below –0.3V (the Absolute Maximum data sheet limit), with the recommended minimum voltage of –0.2V. Therefore, it is important that the I·R voltage drop across the interconnect resistance does not cause a violation of this requirement.

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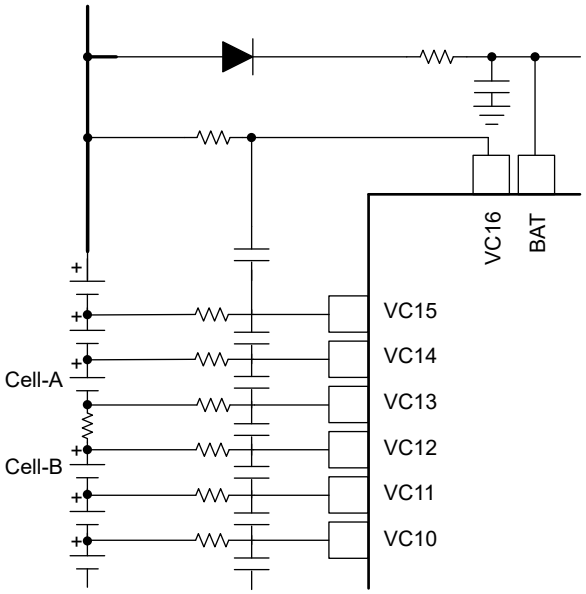

Figure 7-3. Using Cell Input Pins for Interconnect Measurement

If this connection across an interconnect is not needed (or it is preferred to avoid the extra resistor and capacitor), then the unused cell input pins should be shorted to adjacent cell input pins, as shown in Figure 7-4 for VC13.

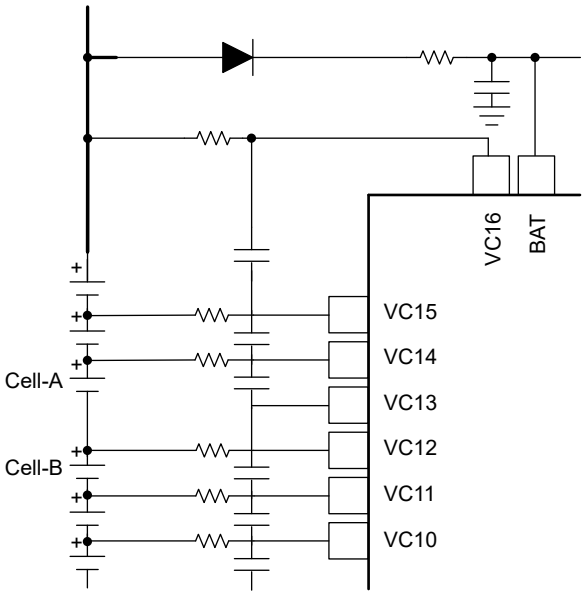

Figure 7-4. Terminating an Unused Cell Input Pin

Figure 7-5 shows the standard cell to VC pin connection for different series cell count configurations. The device uses this information to disable cell voltage protections associated with inputs which are used to measure interconnect or are not used at all. Voltage measurements for all inputs are reported in 16-bit format (in units of mV) as well as 32-bit format (in units of raw ADC counts), irrespective of whether they are used for cells or not.

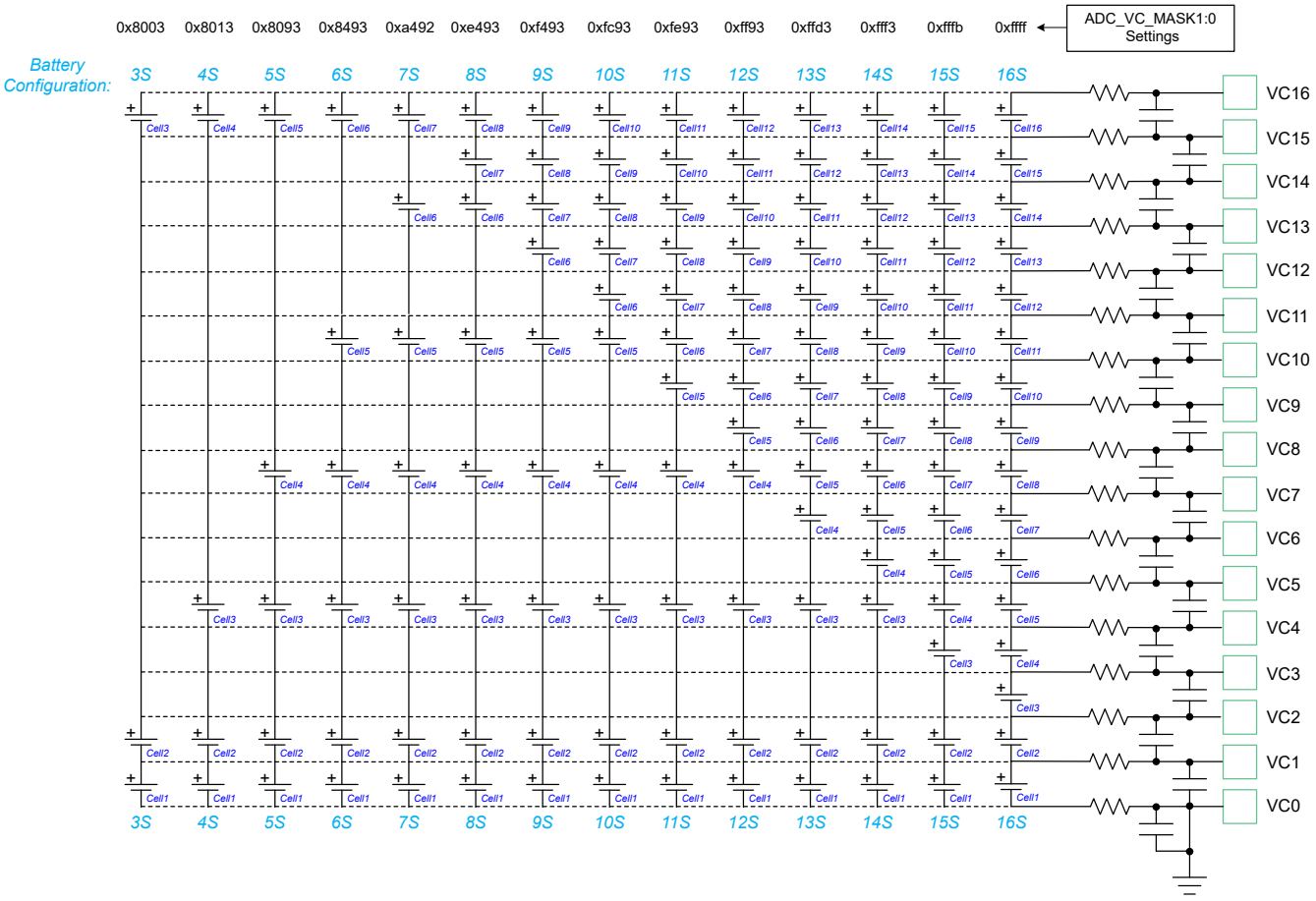

Figure 7-5. Standard Cell to VC pin Connections for Different Cell Count

7.3.3.2 Unused Pins

Some device pins may not be needed in a particular application. The manner in which each should be terminated in this case is described below.

Table 7-3. Terminating Unused Pins

Pin	Name	Recommendation
1–16, 64	VC0–VC16	Cell inputs 1, 2, and 16 should always be connected to actual cells, with cells connected between VC1 and VC0, VC2 and VC1, and VC16 and VC15. VC0 should be connected through a resistor and capacitor on the pcb to pin 49 (VSS). Pins related to unused cells (which may be cell 3–cell 15, pins 1–13) can be connected to the cell stack to measure interconnect resistance or provide a Kelvin-connection to actual cells, in which case they should include a series resistor and parallel capacitor, in similar fashion to pins connected to actual cells (see Section 7.3.3.1). Another option is to short unused VC pins directly to an adjacent VC pin. All VC pins should be connected to either an adjacent VC pin, an actual cell (through R and C) or stack interconnect resistance (through R and C).
17, 19	SRP, SRN	If not used, these pins should be connected to pin 49 (VSS).
18, 33, 45, 46	NC	These pins are not connected to silicon. They can be left floating or connected to an adjacent pin or connected to VSS.
20-23, 26-29, 34-44, 47-48	RADCx (0...8, except for RAD4) RAx, RCx,	If not used, these pins (except for RADC4 _Wake) can be left floating or connected to pin 49 (VSS). Any of these pins (except for RADC4 _Wake) may be configured with the internal weak pulldown resistance enabled during operation, although this is not necessary.
24	RADC-Wake	If the device is intended to enter SHUTDOWN mode, this pin should be left floating. If SHUTDOWN mode will not be used in the application,this pin can be left floating or connected to pin 17 (VSS).
25	RST_SD	If not used, this pin should be connected to pin 49 (VSS).
52	REGOUT	If not used, these pins can be left floating or connected to pin 49 (VSS).

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Table 7-3. Terminating Unused Pins (continued)

Pin	Name	Recommendation
53	REGIN	If not used, this pin should be connected to pin 49 (VSS).
54	BREG	If this pin is not used and pin 53 (REGIN) is also not used, both pins should be connected to pin 49 (VSS). If this pin is not used but pin 53 is used (such as driven from an external source), then this pin should be connected to pin 53 (REGIN).
51	FUSE	If not used, this pin can be left floating or connected to pin 49 (VSS).
57	PDSG	If not used, this pin should be left floating.
60	PCHG	If not used, this pin should be left floating.
55	LD	If the DSG driver will not be used, this pin can be connected through a series resistor to the PACK+ connector, or can be connected to pin 49 (VSS).
58	DSG	If not used, this pin should be left floating.
61	CHG	If not used, this pin should be left floating.
62	CP	If not used, this pin should be connected to pin 63 (BAT). **Note** If the charge pump is enabled with CP1 connected to BAT, the device will consume an additional ≈200µA.

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7.3.4 Cell Balancing Support

The integrated cell balancing FETs included in BQ41Z90 device allow the AFE to bypass cell current around a given cell or numerous cells to effectively balance the entire battery stack. External series resistors placed between the cell connections and the VCx input pins set the balancing current magnitude, which should be restricted to a maximum of I_{CB}.

The cell balancing circuitry can be enabled or disabled through commands. Series input resistors between 20 Ω and 100 Ω and are recommended for effective cell balancing.

A normal VCELL measurement through the ADC using the state machine automatically disables the selected cell balancing FET and adjacent cell balancing FETs for the ADC Config Time and the ADC measurement time. This setting provides the most accurate VCELL measurement. Once the ADC measurement is finished, then the cell balancing FETs are immediately returned to the preconfigured condition.

7.3.4.1 Open Wire Detection

The BQ41Z90 has the ability to use the cell balancing FETs to support a firmware derived open VCx wire detection feature. Using the ADC multiplexer to measure cells 1 through 16, respectively. The device automatically enables the CB FET for that specific cell channel measurement.

The functionality and detection method are slightly different, depending on the connection to the PCB from the cell stack.

1. Using a single BAT-/VC0- connection to the PCB. In this case, each VCx input needs to have the same cell balancing limiting resistor. For VC1,2,3,4…,16 disconnect detection the firmware measures and determine if the voltage is very close to the normal cell voltage indicating the wire is connected or close to 0 V indicating the wire is disconnected. To detect if VC0 is open then the firmware measures VC0:VC1 and a result of 0 or negative indicates an open wire, whether using the cell balancing FET or not.
2. Using separate BAT- and VC0 connections to the PCB. In this configuration, the external resistor in series with VC0 is lowered to 20 ohms or less. For VC0, 1,2,3,4...,16 disconnect detection, the firmware measures and determines if the voltage is very close to the normal cell voltage, indicating the wire is connected or close to 0 V and the wire is disconnected.

7.3.5 Protection and Charge Control Outputs

The BQ41Z90 device includes two high side N-channel FET drivers for CHG and DSG control, as well two high side N-channel FET drivers for P-CHG (Precharge) and P-DSG (Predischarge) control, and a FUSE output

capability to provide different methods to disconnect the cells from the system and to control the flow of charge current.

7.3.5.1 High-Side NFET Drivers

The BQ41Z90 device includes an integrated charge pump and high-side NFET drivers for driving CHG, DSG, PCHG and PDSG protection FETs. The charge pump uses an external capacitor connected between the BAT and CP pin that is charged to an overdrive voltage when the charge pump is enabled.

The overdrive level of the charge pump voltage can be set to 7V or 10V, based on the configuration setting. In general, the 7V setting results in lower power dissipation when a FET is being driven, while the higher 10V overdrive reduces the on-resistance of the FET. If a FET exhibits significant gate leakage current when driven at the higher overdrive level, this can result in a higher device current for the charge pump to support this. In this case, using the lower overdrive level can reduce the leakage current and thus the device current.

A 10 MΩ resistor between the FET gate and source is required. The charge (CHG) and discharge (DSG) FETs are automatically disabled if a protection fault is detected. When the gate drive is disabled, an internal circuit discharges CHG to BAT and DSG to PACK.

The FET drivers in the BQ41Z90 device can be controlled in several different manner, depending on customer requirements:

Fully autonomous

The BQ41Z90 device can detect protection faults and autonomously disable the FETs, monitor for a recovery condition, and autonomously reenable the FETs, without requiring any host processor involvement. The device provides flexibility to configure the aumonomous protections per use cases.

Partially autonomous

The BQ41Z90 device can detect protection faults and autonomously disable the FETs. When the host receives an interrupt and recognizes the fault, the host can send commands across the digital communications interface to keep the FETs off until the host decides to release them.

Alternatively, the host can assert the CFETOFF or DFETOFF pins to keep the FETs off. As long as these pins are asserted, the FETs are blocked from being reenabled. When these pins are deasserted, the BQ41Z90 will reenable the FETs if nothing is blocking them being reenabled (such as fault conditions still present, or the CFETOFF or DFETOFF pins are asserted).

Manual control

The BQ41Z90 device can detect protection faults and provide an interrupt to a host processor over the interrupt pin. The host processor can read the status information of the fault over the communication bus (if desired) and can quickly force the CHG or DSG FETs off by driving the CFETOFF or DFETOFF pins from the host processor, or commands over the digital communications interface.

When the host decides to allow the FETs to turn on again, it writes the appropriate command or deasserts the CFETOFF and DFETOFF pins, and the BQ41Z90 device will reenable the FETs if nothing is blocking them being reenabled.

7.3.5.2 PRECHARGE and PREDISCHARGE Modes

The BQ41Z90 device includes precharge functionality, which can be used to reduce the charging current for an undervoltage battery by charging through a high-side PCHG NFET (driven from the PCHG pin). The precharge (PCHG) FET is placed in series with a high power resistor to set the current. When the minimum cell voltage is less than a programmable threshold, the PCHG FET will be used for charging until the battery reaches a programmable voltage level.The PCHG FET is automatically disabled if a protection fault is detected.

The device also supports predischarge functionality, which can be used to reduce inrush current when the load is initially powered, by first enabling a high-side PDSG NFET (driven from the PDSG pin) with series resistor, which enables the load to slowly charge. If PREDISCHARGE mode is enabled, whenever the DSG FET is turned on to power the load, the device will first enable the PDSG FET, then transition to turn on the DSG FET and turn off the PDSG FET.

The PCHG and PDSG drivers are limited in the current they can sink while enabled. As such, it is recommended to use 1 MΩ or larger resistance across the FET gate-source.

7.3.5.3 FET Configuration

The BQ41Z90 provides controls of CHG, DSG, PCHG and PDSG with flexibility of various configurations. The device supports a system with FETs in a series or parallel configuration, which includes a separate path for the charger connection into to the connector versus the discharge (load) connection , as well as a system that does not use one or both FETs. The FETs arrangement are different in the series configuration versus parallel configuration for the protection.

If the CHG FET is off, the DSG or PDSG FET is on, and a discharge current greater in magnitude than a programmable threshold (that is, a significant discharging current) is detected, the device will turn on the CHG FET, to avoid current flowing through the CHG FET body diode and damaging the FET. When the current rises above the threshold (that is, less discharge current flowing), the CHG FET will be turned off again if the reasons for its turn-off are still present.

If the DSG FET is off, the CHG or PCHG FET is on, and a current in excess of a programmable threshold (that is, a significant charging current) is detected, the device will turn on the DSG FET, to avoid current flowing through the DSG FET body diode and damaging the FET. When the current falls below the threshold (that is, less charging current flowing), the DSG FET will be turned off again if the reasons for its turn-off are still present.

When a series FET configuration is used, the BQ41Z90 device provides body diode protection for the case when one FET is off and one FET is on. When a parallel configuration is used, the body diode protection is disabled.

7.3.5.4 CFETOFF, DFETOFF Pin Functionality

The BQ41Z90 device includes two pins (CFETOFF and DFETOFF) which can be used to disable the protection FET drivers quickly, without going through the host serial communications interface. When the selected pin is asserted, the device disables the respective protection FET. Both the CFETOFF and DFETOFF pins can be used for other functions if the FET turnoff feature is not required.

Note

when the selected pin is deasserted, the respective FET will only be enabled if there are no other items blocking them being reenabled, such as if the host also sent a command to disable the FETs using the serial communications interface after setting the selected pin.

The FET drivers in BQ41Z90 device can be controlled in a couple of different manner, depending on customer requirements:

Fully autonomous mode: The BQ41Z90 device can detect protection faults and autonomously disable the FETs, monitor for a recovery condition, and autonomously re-enable the FETs, without requiring any host processor involvement.

Partially autonomous: The host can assert the CFETOFF or DFETOFF pins to keep the FETs off. As long as these pins are asserted, the FETs are blocked from being re-enabled. When these pins are de-asserted, BQ41Z90 will re-enable the FETs if nothing is blocking them being re-enabled (such as fault conditions still present, or the CFETOFF or DFETOFF pins are asserted).

Manual mode: The BQ41Z90 device can detect protection faults and provide an interrupt to a host processor over the ALERT pin. The host processor can read the status information of the fault over the communication bus (if desired) and can force the CHG or DSG FETs off by driving the CFETOFF or DFETOFF pins from the host processor.

The host inputs (CFETOFF/DFETOFF) when selected are “OR-ed” with the other reasons for BQ41Z90 to turn off FETs, such as upon detecting SCD/OCC/OCD conditions which requires various FETs (CHG/DSG/PCHG/PDSG) to be turned off.

7.3.5.5 DDSG and DCHG Pin Operation

The BQ41Z90 device includes two multifunction pins, DDSG and DCHG, which can be configured as logic-level outputs to provide a fault-related signal to a host processor or external circuitry (that is, DDSG and DCHG functionality), as a thermistor input, a general purpose ADC input, or for LED current sink.

When used as a digital output, the pins can be configured to drive an active high output, with the output voltage driven from the REG18 1.8-V LDO.

When the pins are configured for DDSG and DCHG functionality, they provide signals related to protection faults that (on the DCHG pin) would normally cause the CHG driver to be disabled, or (on the DDSG pin) would normally cause the DSG driver to be disabled. These signals can be used to control external protection circuitry, if the integrated high-side NFET drivers will not be used in the system. They can also be used as interrupts in manual FET control mode for the host processor to decide whether to disable the FETs through commands or using the CFETOFF and DFETOFF pins.

7.3.5.6 Hardware Fault Detection (SCOMP and SCD)

The BQ41Z90 includes a time divided comparator and configurable digital scheduler that is used for multiple voltage condition detections and is enabled when SCOMP_CTRL[SCOMP_EN] = 1. The detections included in this feature are Overcurrent in Discharge 1 and 2 Protection, Over current in Charge Protection and Over Temperature Protection

Table 7-4. SCOMP Feature FET Actions

Condition	DSG	CHG	PDSG	PCHG
Overcurrent in Discharge 1 & 2	OFF	Unchanged	OFF	Unchanged
Overcurrent in Charge	Unchanged	OFF	Unchanged	OFF
Over Temperature	Configurable	Configurable	Configurable	Configurable

The digital scheduler is responsible for meeting the timing requirements of the electrical functions. All measurements can be configured to have 1 to 9 consecutive detections.

BQ41Z90 also integrated a dedicated comparator for Short-Circuit Detection with fast response time. Short-Circuit Current in Charge Protection and Short-Circuit Current in Discharge Protection and each can turn OFF the CHG, DSG, PCHG and PDSG FETs and will stop them from being turned back ON till the Short-Circuit status is cleared but will not turn the FETs ON directly

Table 7-5. SCD FET Actions

Condition	DSG	CHG	PDSG	PCHG
Short-Circuit Detetion	OFF	OFF	OFF	OFF

7.3.5.7 FET UVLO Protection

The BQ41Z90 provides FET UVLO control to prevent the FETs underdrive and get over heated . It can be used to inform the digital when the pump voltage on the external capacitor is ready for use or too low. A signal based on the pump voltage will be generated in the charge pump block and sent to the digital to indicate whether the pump is above 5-V in the normal FET operation mode or whether it is above 3-V in the low-power operation mode The digital can be configured to hold off FET turn-on or alternatively turn-off the FETs should a UVLO condition be detected. This function could be turned off if this is not needed.

7.3.5.8 Fuse Drive

The BQ41Z90 AFE has the ability to blow an external fuse in the event of a permanent failure. The fuse drive itself is supplied from the BAT input pinand its state can be monitored using the AIF_ANA_DIN register. To drive

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the FUSE output set AIF_CTRL2 [FUSE_BLOWD] = 1. When the firmware is not intending to drive the FUSE pin then the fuse drive can be configured to monitor for activity on the FUSE pin from an external source such as a second level voltage protector.

If the FUSE output is not used, it should be connected to VSS. When FUSE is in the low state, it uses an internal weak pullup to detect disconnection between the FUSE pin and the fuse drive circuitry.

7.3.6 Load Detect Functionality

When a Short Circuit in Discharge Latch or Overcurrent in Discharge Latch protection fault has occurred and the DSG FET is off, the device can be configured to recover when load removal is detected. This feature is useful if the system has a removable pack, such that the user can remove the pack from the system when a fault occurs, or if the effective system load that remains on the battery pack is higher than a set threshold (minimum of 300 Ω) when the DSG FET is disabled. The device will periodically enable a 3mA current source out the LD pin and will recover the fault if a voltage is detected at the LD pin above a set threshold level. If a low-impedance load is still present on the pack, the voltage the device measures on the LD pin is lower than the threshold voltage, preventing recovery based on Load Detect. If the pack has been removed from the system and the effective load is high, then the device can recover from the fault. This feature can be also used to detect if the load impdeance is too low before turning on the CHG and DSG FETs in the power-up.

Note

Typically, an external resistor can be connected between the PACK+ terminal and the LD pin to reach the threshold voltage needed based on the calibration of the system. This resistance should be comprehended when considering the load impedance. The Load Detect current is enabled for a programmable time duration, then is disabled for another programmable time duration, with this sequence repeating until the load has been detected as removed or it times out.

7.3.7 MCU Peripherals

The device includes a number of peripherals in the MCU.

7.3.7.1 General Purpose and Special Function I/O

The BQ41Z90 device has 4 types of I/O, 13 on the MCU and 8 on the AFE.

I/O Port	Die Location	Rec Max Voltage	I/O Type	Internal Pull Up/ Down available	Special Function
RAx	MCU	5.5V	Open Drain	Pull Down only	Communications
RCx	MCU	V_{REG18}	Push Pull	Yes	Communications, Pulser and SWD port
RLx	AFE	5.5V	Open Drain	Yes	LED current sinks
RADCx	AFE	V_{REG18}	Open Drain	Yes	Temperature sensor inputs

Configuration options and descriptions for the GPIO pins are detailed in the IOMUX Registers and GPIO Registers sections.

7.3.7.1.1 Low Voltage RAx I/O

Four general-purpose, open-drain I/Os are available for use on the BQ41Z90 device and are on the MCU. There are pulldown and interrupt feature options available that are programmable.

The RA0 through RA3 pins are capable of 1-MHz operation are targeted as the SMBus or I2C with RA0–RA1 used for the I2C0 peripheral and RA2–RA3 used for the I2C1 peripheral. Either bus can be configured as a target or a host.

Each RAx pin requires a series external resistance of a minimum 250Ω to any node that could be exposed to electrostatic discharge (ESD).

7.3.7.1.2 Low Voltage RCx I/O

Two general-purpose, tristate I/Os are available for use on the BQ41Z90 device. These pins are tolerant up to V_{REG18} without causing damage to the MCU. Internal pullups and pull downs are included for each of the RCx pins and can be enabled using the RCWKPUP and registers.

RC0 RC1 also functions as the pulser output pin, which can be driven by the PWM module and synchronized with the ADC.

Through RC0/SWDIO and RC1/SWCLK the SWD interface is also available.

7.3.7.1.3 Constant Current Sink I/O

Five general-purpose, tri-state I/Os are available for use on the BQ41Z90 device. They can be used as GPIO or be configured as constant-current sinks for driving external LEDs. Internal pullups are included for each RLx pin and can be enabled through pin configuration regsiters.

CAUTION

When connecting any circuitry to an RL pin (for example, a pull-down, pullup, etc.) that interfaces outside of the pack, there must be a diode connected at the BAT pin. Without a diode on the BAT pin, there is a potential sneak path to charge the battery under a fault condition.

7.3.7.2 Communication Interfaces

The BQ41Z90 supports both SMBus 3.2 and I²C serial interfaces in Target and Controller Modes. The communication interfaces are available through the RA0 and RA1 by default or RA2 and RA3. The SMBus and I²C Controller can be enabled on RA0 and RA1 to be the Controller on the same bus or on RA2, and RA3 to be the Controller on a second bus.

Expected use combinations are:

1. SMBus Target only
2. SMBus Target with SMBus Controller of the same bus
3. SMBus Target with I²C Controller of a different bus
4. I²C Target only
5. I²C Target with I²C Controller of a separate bus
6. SMBus Target with SMBus Controller of a separate bus

The SMBus and I²C communication interfaces are simplified by using the communications APIs.

7.3.7.2.1 I²C Interface

The BQ41Z90 device provides an I²C interface (data SDA and clock SCL) to enable bidirectional data transfer.

The device includes the following I²C features:

- Devices on the I²C bus can be designated as either a controller or a target with 7-bit addressing.
- Support four I²C modes:
  - Controller transmit
  - Controller receive
  - Target transmit
  - Target receive
- Supported transmission speeds:
  - Standard-mode (Sm) with a bit rate up to 100 kbps
  - Fast-mode (Fm) with a bit rate up to 400 kbps
  - Fast-mode Plus (Fm+) with a bit rate up to 1 Mbps
- Independent 8-byte FIFOs for reception and transmission

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- Dual target address capability
- Glitch suppression
- Independent controller and target interrupt generation
- Controller operation with arbitration, clock synchronization
- Hardware support for SMBus
- Clock low timeout detection and interrupt
- Hardware support for DMA with separate channels for transmit and receive

7.3.7.2.2 SMBus Interface

The device provides an SMBus interface (SMBC and SMBD) that works with firmware to comply with the SBS v3.2 protocol supporting packet error checking (PEC). The SMBC and SMBD pins also include 1-MΩ pull down resistors to prevent potential noise due to floating SMBus nodes.

The SMBus interface uses the I^2C HW modules with some additional capabilities that can be configured using the I^2C registers.

7.3.7.3 Authentication Support

The BQ41Z90 supports ECC, SHA-1, and SHA-2 authentication algorithms between hardware peripherals and ROM functions, described in following sections.

7.3.7.3.1 ECC Authentication

For robust battery pack security, the BQ41Z90 offers Elliptic Curve Cryptographic (ECC) authentication. ECC authentication uses unique asymmetrical private/public key cryptography, eliminating the requirement of sharing the same secret in the host system.

The ECC authentication protocol in the BQ41Z90 device is the Elliptic Curve Korean Certificate-based Digital Signature Algorithm (EC-KCDSA), implemented based on the International Organization for Standardization (ISO) specification, 14888-3. The EC-KCDSA signature (that is, response from a challenge) is calculated based on the B-163 or B-233 pseudo-random elliptic curve that is standardized and freely available from the National Institute of Standards and Technology (NIST) in the publication FIPS 186-3. Elliptic curve parameters based on B-163 or B-233 will be hard coded into the Mask ROM since these need not be modified.

For reference, see http://csrc.nist.gov/publications/PubsFIPS.html.

The BQ41Z90 includes a hardware-based binary field accelerator peripheral for enhanced performance of the ROM-based EC-KCDSA library functions. The accelerator handles the computation of all binary field additions and multiplications directly in hardware, which allows computations to be done in parallel with other CPU tasks, significantly improving the overall speed of the EC-KCDSA implementation. The top-level EC-KCDSA signature generation protocol is handled in the Mask ROM and uses computation results acquired from the math accelerator to construct the final authentication signature that is provided to the host system via the device serial interface.

The private key and public key can be programmed and stored in physically secure memory that is isolated from Program FLASH, preventing attempts to access or read out its value over the serial interface.

The key pair generation occurs externally so the host system will need knowledge of the public key prior to requesting a signature from the BQ41Z90 device. Similar to SHA-1 authentication, a random challenge must be constructed by the system host and sent to the BQ41Z90 prior to initiating signature generation. From there, the Mask ROM handles execution of all tasks required to communicate with the integrated math accelerator and CPU before making the final result available to the Program FLASH via library function calls.

7.3.7.3.2 SHA-1 Support

The BQ41Z90 include SHA-1 support through the ROM and does not have any specific hardware support other than secure key storage.

7.3.7.3.3 SHA-2 Support

The BQ41Z90 include SHA-2 support through the ROM and does not have any specific hardware support other than secure key storage.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The BQ41Z90 is a gas gauge with primary protection support that can be used with a 3-S to 16-S Li-ion or LFP battery packs. To implement and design a comprehensive set of parameters for a specific battery pack, users need the Battery Management Studio (bqStudio) graphical user-interface tool installed on a PC during development. The firmware installed on the bqStudio tool has default values for this product. Using the bqStudio tool, these default values can be changed to cater to specific application requirements. During development, once the system parameters are known, such as fault trigger thresholds for protection, enabling or disabling certain features for operation, configuration of cells, chemistry that best matches the cell used, and more. This data is referred to as the "golden image."

8.2 Typical Applications

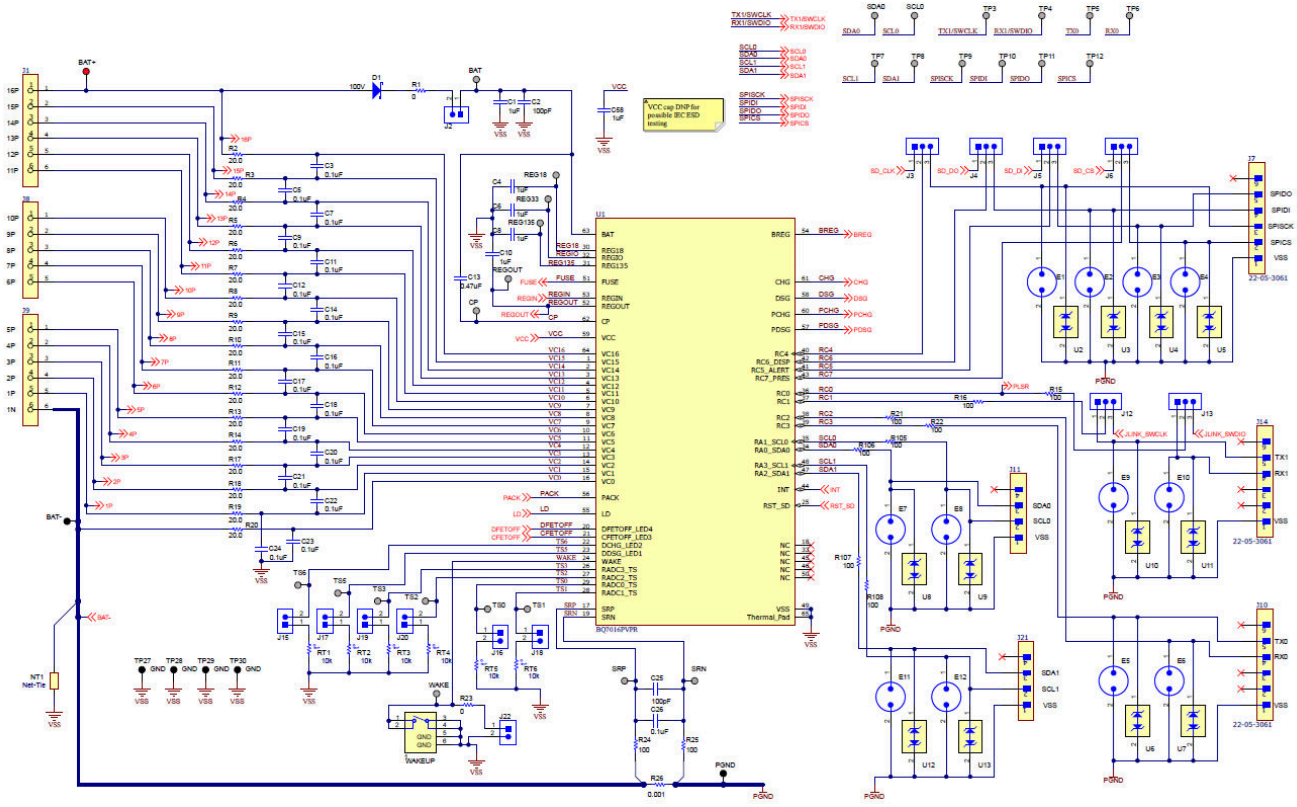

Figure 8-1. Typical Applications

ADVANCE INFORMATION

8.2.1 Design Requirements

Table 8-1 shows the default settings for the BQ41Z90 main parameters. Use the bqStudio tool to update the gauge settings to meet the specific application or battery pack configuration requirements.

The device should be calibrated before any gauging tests are ran. Follow the bqStudio Calibration page to calibrate the device, and use the bqStudio Chemistry page to update the ChemID configured on the device.

Table 8-1. Design Parameters

Design Parameters	Example
Cell Configuration	3S
Design Capacity	4400mAh
Device Chemistry	1210 (LiCoO2/graphitized carbon)
Cell Overvoltage at Standard Temperature	4300mV
Cell Undervoltage	2500mV
Shutdown Voltage	2300mV
Overcurrent in CHARGE Mode	6000mA
Overcurrent in DISCHARGE Mode	-6000mA
Short Circuit in DISCHARGE Mode	0.1V/R_{Sense} across SRP, SRN
Safety Overvoltage	4500mV
Cell Balancing	Disabled
Internal or External Temperature Sensor	External Temperature Sensor is used
Undertemperature Charging	0°C
Undertemperature Discharging	0°C
BROADCAST Mode	Disabled

ADVANCE INFORMATION

9 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 5 V to 80V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum VCC. This enables the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

The BAT input requires a 1-µF capacitor connected to VSS and placed as close to the BAT pin as possible. The BAT input also requires a diode between the top of the battery stack and the input capacitor so that the input capacitor is not discharged when PACK is shorted to VSS.

The VCC input does not require a capacitor, but if one is added, it should be connected as close to the VCC pin as possible.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

None available at this time.

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADVANCE INFORMATION

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (December 2024)	Page
• Updated *3 to 6 cells* to *3 to 16 cells*	1

DATE	REVISION	NOTES
December 2024	*	Initial Release

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PBQ41Z90PVPT	ACTIVE	HTQFP	PVP	64	3000	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

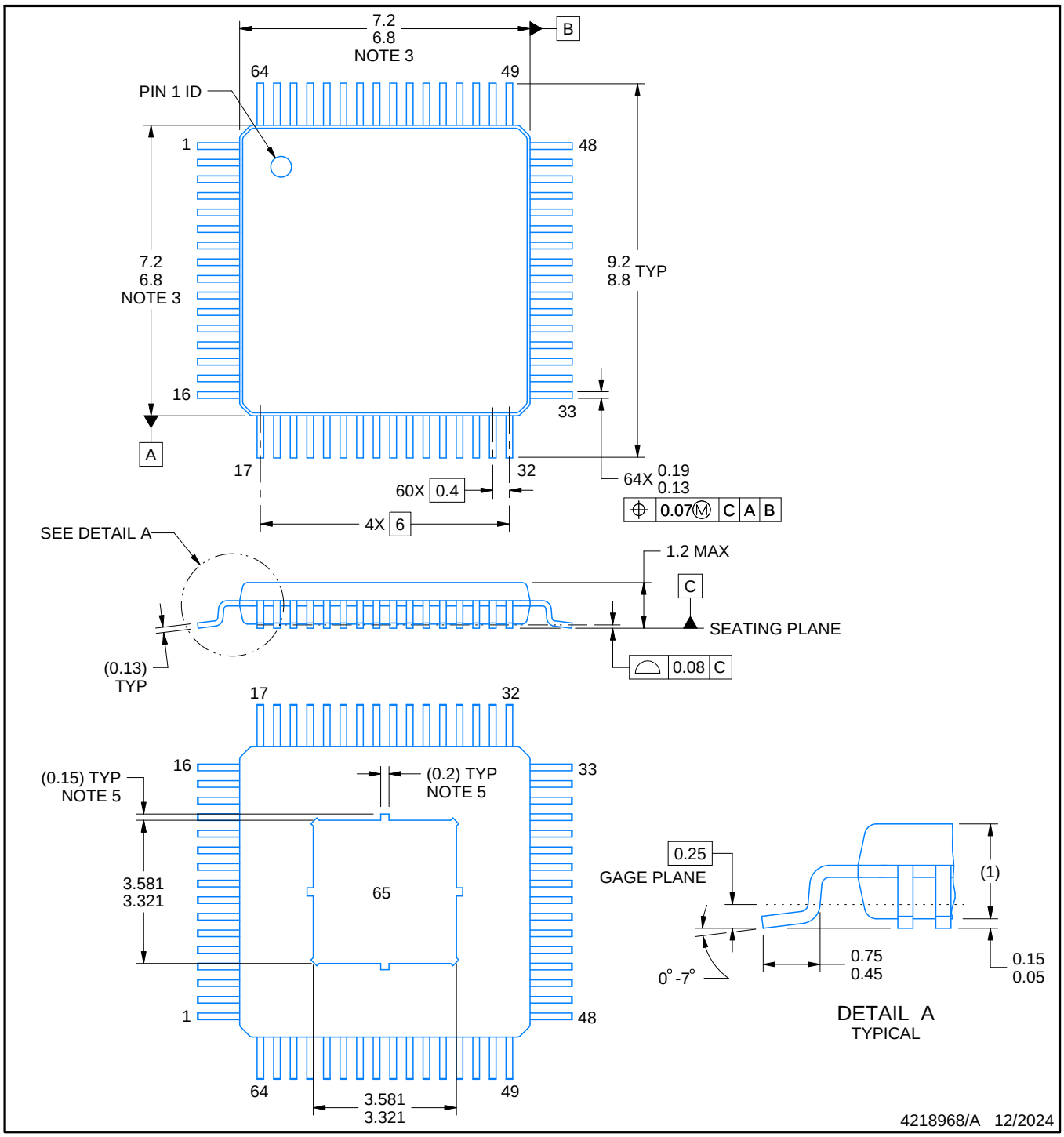
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PVP0064A

PowerPAD™ HTQFP - 1.2 mm max height

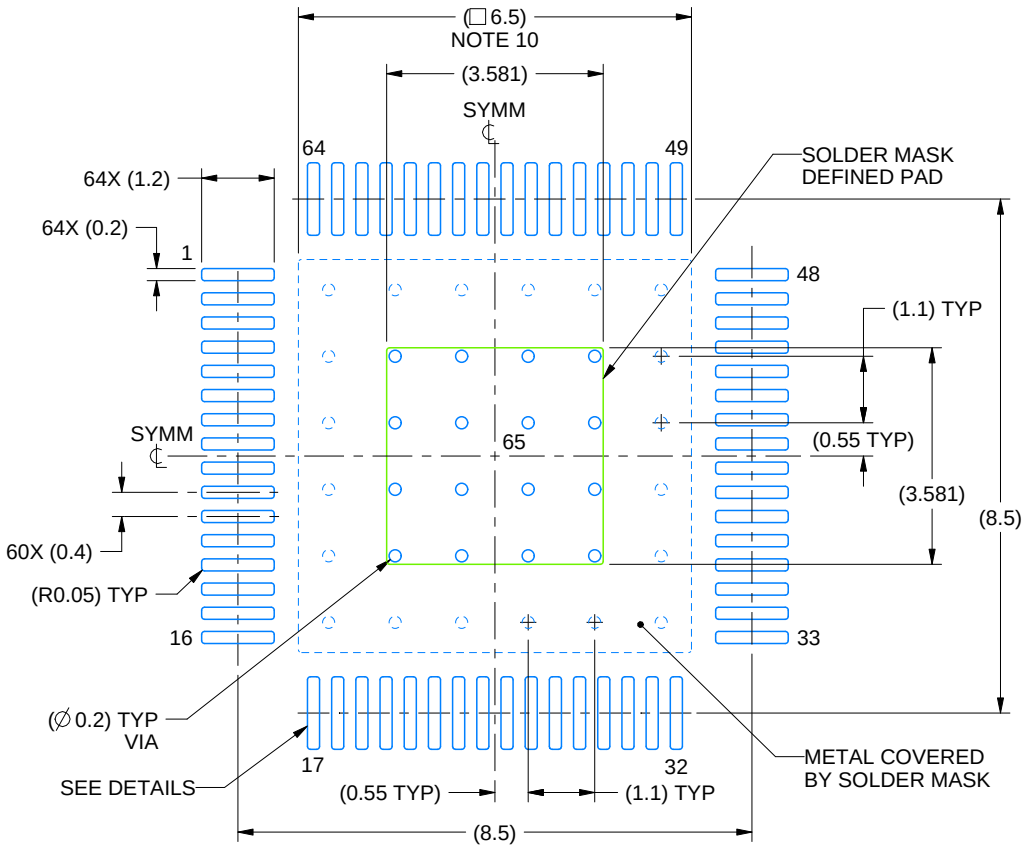
PLASTIC QUAD FLATPACK



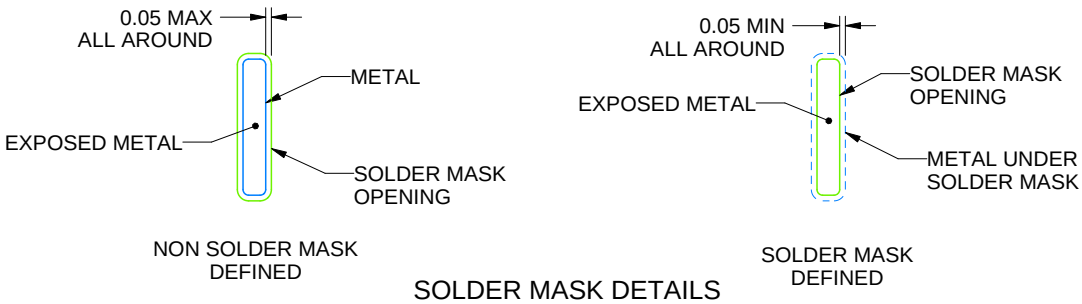
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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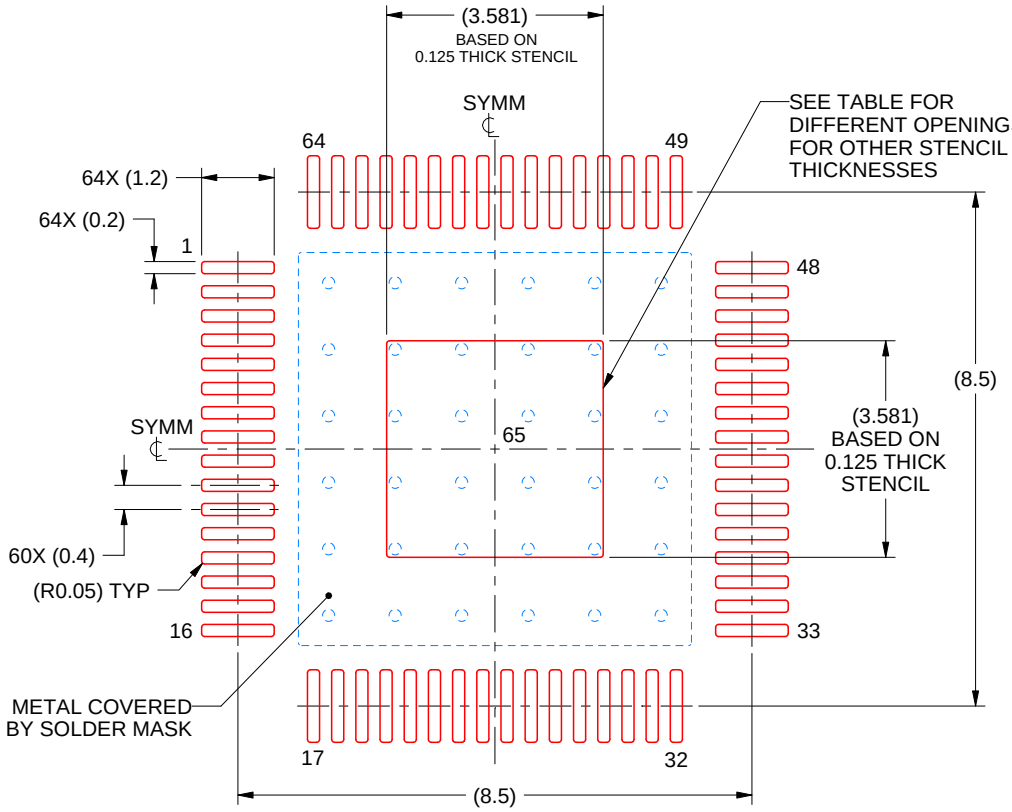
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.004 X 4.004
0.125	3.581 X 3.581 (SHOWN)
0.150	3.269 X 3.269
0.175	3.026 X 3.026

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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